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Random Telegraph Signal Noise in Tunneling Field-Effect Transistors with S below 60 mV/decade

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***Abstract*—Single gate oxide defects in strongly scaled Tunneling Field-Effect Transistors with an inverse subthreshold slope well below 60 mV/decade are investigated by Random Telegraph Signal (RTS) noise measurements. The cause for RTS noise are electrons being captured in and released from individual defects in the gate oxide. Under the assumption that elastic tunneling is the underlying capture and emission mechanism, the measured RTS time constants vary with the relative position of the channel Fermi level and the defect energy level while the amplitudes – independent of the capture and release mechanism – follow the inverse of the inverse subthreshold slope.**

Keywords—Tunneling Field-Effect Transistors, Nanowires, Below 60 mV/decade, Random Telegraph Signal Noise, Elastic Tunneling

I. Introduction

Transistor dimensions are an important scaling parameter to continue Moore's law. Also for devices beyond Moore's law, certain transistor dimensions remain important metrics for optimized device performance. For vertical nanowire transistors, one of the key dimensions is the diameter of the nanowires, strongly affecting the electrostatic control of the gate over the channel [1]. With excellent electrostatic control and a carefully designed III-V heterojunction, we demonstrated Tunneling Field-Effect Transistors (TFETs) with an inverse subthreshold slope (S) well below 60 mV/decade [2]. At the same time, while improving the electrostatic gate control, scaling down transistor dimensions to a few nanometers limits the number of gate oxide defects to a few individual locations. Capturing and releasing individual electrons in and from these defects changes the channel potential energy by a discrete amount and thus – specific for TFETs with a dominant defect close to the junction – also the reverse bias of the tunneling junction. This leads to discrete steps in the device current, so-called Random Telegraph Signal (RTS) noise, and results in degradation of transistor and circuit performance [3]. In TFETs, this effect has been simulated thoroughly [3, 4], but rarely been observed experimentally [5, 6] and explained in detail even less. Here, we study RTS noise in TFETs with S well below 60 mV/decade, which allows estimations of both the spatial as well as energetical position of the dominant defect and its electrostatic effect on the channel potential.

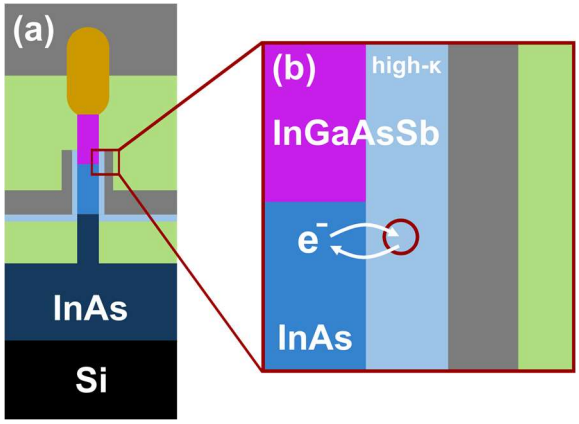

Fig. 1: (a) Schematic illustration of the studied devices. Dark blue indicates InAs, doped in the bottom, intrinsic in the channel region, purple indicates the InGaAsSb segment, yellow the GaSb segment, light blue indicates the gate oxide, grey are metals, green spacers. (b) Schematic of the tunneling process causing RTS noise. The red circle indicates a single defect in the gate oxide.

II. Device and Measurement Specifications

A. Device Fabrication

To clearly separate and identify all effects, only transistors made of one single nanowire were studied for this work. A schematic illustration is shown in Fig. 1. All nanowires were grown by metalorganic vapor phase epitaxy (MOVPE) from an Au seed particle defined by electron beam lithography (EBL). The substrate consisted of a MOVPE-grown InAs buffer layer on top of Si. The InAs bottom segment of the nanowire was n-doped with Sn to reduce series resistance. In order to achieve a gate control as good as possible, the channel segment on top was not intentionally doped. The tunneling junction was created

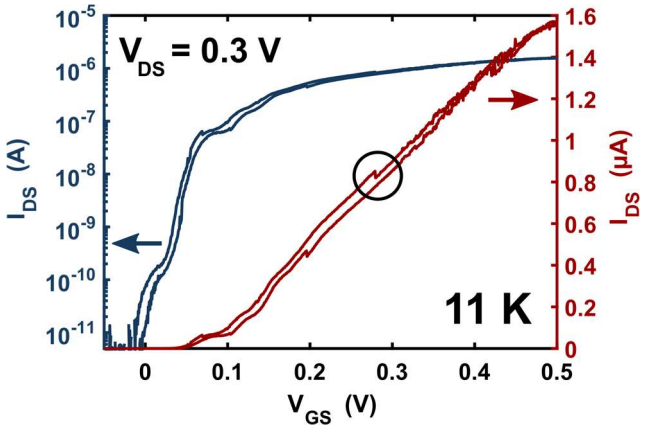

Fig. 2: Transfer characteristics for an example device at 11 K with V_{DS} = 0.3 V. Blue shows a logarithmic scale (left), red a linear scale (right). The circle indicates the RTS step more closely examined in this article. For the highest currents in the linear scale there are many more RTS steps.

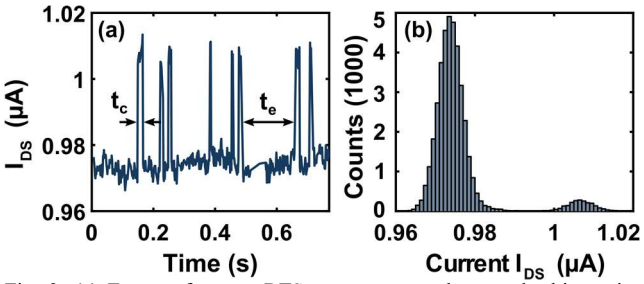

Fig. 3: (a) Excerpt from an RTS measurement close to the bias point indicated in Fig. 2. t_c and t_e denote the capture and the emission times, respectively. (b) Current histogram for the complete measurement in (a), clearly indicating two current levels.

by changing from the un-doped InAs channel segment to p-doped (using Zn) InGaAsSb. For good source contacts, the InGaAsSb segment was followed by a p-doped GaSb top segment. After growth, the InAs parts of the nanowire were thinned down to a final diameter of 20 nm by first oxidizing the surface with ozone plasma and then etching this oxide with citric acid. Immediately afterwards, a high-κ gate oxide consisting of approximately 1 nm of Al_2O_3 and 3.5 nm of HfO_2 was applied by atomic layer deposition (ALD). The estimated equivalent oxide thickness (EOT) is 1.4 nm. A SiO_x bottom spacer was deposited to separate the drain from the gate contact and a 60-nm-thick W gate metal was sputtered over the whole sample. To define the gate length from this coverage, another (temporary) spacer was applied and etched back so that all W beyond the intended gate contact could be removed from the nanowire. The gate pad in the lateral direction was defined by UV-lithography. After exchanging the temporary spacer for the final photoresist top spacer, the high-κ oxide was removed from the top of the nanowire and a 10 nm Ni/150 nm Au source metal contact was deposited. As a last step, drain and gate vias were etched and the top metal source, drain, and gate pads were defined, all by UV-lithography. The transfer characteristics of a representative device is shown in Fig. 2. For consistency, all data presented here are from this same device and the analysis is focused on the RTS step marked in Fig. 2. Further details on fabrication can be found in [2].

B. Measurement Setup and Technique

The measurement setup consisted of a Lake Shore Cryotronics CRX-4K probe station and an Agilent B2912A

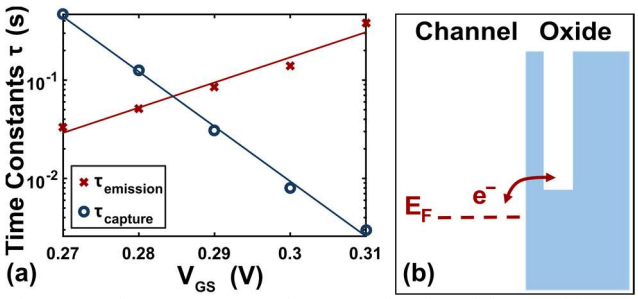

Fig. 5: (a) Time constants (markers) as a function of the gate bias V_{GS} together with exponential fits (lines). A decreasing capture time constant for an increasing emission time constant was observed for all TFETs. (b) Schematic illustration of the capture and emission process for a single oxide defect. The trends in (a) can be explained by the difference between the channel Fermi level and the defect energy level.

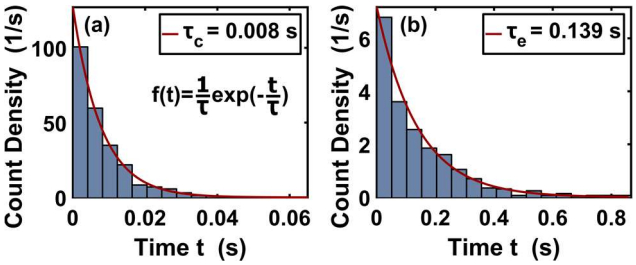

Fig. 4: Histograms of the capture (a) and emission (b) times for the measurement from Fig. 3. The red lines indicate the exponential distribution (equation in (a)) fitted to the data.

Source/Measure Unit. RTS noise measurements were carried out at room temperature, at 150 K, and at 11 K. However, due to the high sensitivity of the noise signal to even small changes in the device behavior and due to threshold voltage shifts at different temperatures, it was not possible to identify and measure with certainty the same defect at different temperatures. In each measurement like the one presented in Fig. 3, the drain current (InAs side) of a transistor was measured in sections of up to 200 seconds at constant gate and drain bias, while the source (GaSb top contact) was grounded. For each defect and each bias point, at least a hundred and up to 2200 transitions between current levels were recorded with measurement resolutions between 0.2 ms and 2 ms. The capture and emission time constants were determined by fitting an exponential distribution to the histograms of the times spent in the high current states (capture times) and the low current states (emission times), respectively (Fig. 4). The data presented here are from a measurement at 11 K, but are representative for measurements at all temperatures.

III. Results and Discussion

Both the measured capture and emission time constants τ_c and τ_e vary with varying gate bias (Fig. 5(a)), which can be qualitatively explained with the help of the process illustrated in Fig. 5(b) under the assumption that elastic tunneling is the capture and emission mechanism. If the channel Fermi level is increased towards the defect energy level from below, electron tunneling into the oxide defect exhibits a rather long time constant due to the energy difference between the two states. The emission time constant in this configuration is rather short since the electron can always tunnel out of the defect and relax to the energy corresponding to the channel Fermi level. Increasing the channel Fermi level above the trap energy level reverses this behavior. Since the effect of the defect considered here shows up in the on-state, the defect energy level must be located quite far below the channel conduction band in the unbiased state.

Besides the energy difference explained above, the tunneling time constant is determined by the depth z of the defect from the channel into the oxide. According to standard quantum-mechanical tunneling the probability of a state in a forbidden area – and thus the tunneling time constant τ – decays exponentially as

$$\tau_{c/e} = \tau_0 \exp(z/\lambda) \qquad (1)$$

where τ_0 is a constant, and λ the tunneling attenuation constant according to the Wentzel-Kramers-Brillouin approximation [7] given by

$$\lambda = \left(\frac{4\pi}{h}\sqrt{2m^*\phi_B}\right)^{-1} = 0.13\ \text{nm}, \qquad (2)$$

where h is the Planck constant, $m^* = 0.23 \cdot m_0$ the effective mass in the gate oxide (m_0 is the electron rest mass), and $\phi_B = 2.3$ eV the barrier height from the channel to the gate oxide [8]. With the assumptions made above, z can be determined from the biasing point where $\tau_c = \tau_e$ since in this configuration the channel Fermi level and the defect energy level are aligned and there is no energy difference, which distorts the time constants. With $\tau_{e/c} \approx 6 \cdot 10^{-2}$ s from Fig. 5(a), $\tau_0 = 4 \cdot 10^{-11}$ s from [9], and (1) rearranged to $z = \lambda \ln(\tau/\tau_0)$, the depth z amounts to approximately 2.7 nm from the channel interface into the gate oxide and thus to approximately halfway between the channel and the gate metal. From this calculation it is obvious that z depends on τ_0, for which different values can be found in literature, ranging from 10^{-10} s [7] to $6.6 \cdot 10^{-14}$ s [10]. Between these two extreme values, the position of the defect in the oxide would change by up to 1 nm, which does, however, not influence the underlying tunneling model. The value of $\tau_0 = 4 \cdot 10^{-11}$ s chosen here is taken from our own high-frequency characterizations of Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) similar to the presented TFET structures and corresponds to tunneling into defects which are very close to the channel/gate oxide interface.

Independent of the exact capture and emission mechanism, the RTS amplitude can be used to estimate the change in the channel potential energy that results from a single electron captured in a defect in the oxide. With the simplified expression

$$I_{1D} = a\,(V_R - V_T)\exp\left(-\frac{b}{\xi}\right) \qquad (3)$$

for a 1D TFET [11], it can be readily shown that the change in the TFET current from one single charge q_{ox} in the gate oxide amounts to

$$\frac{\partial I_{1D}}{\partial q_{ox}} = \frac{\partial V_R}{\partial q_{ox}} g_m, \qquad (4)$$

which also holds for a 3D expression of the current. In (3) and (4), a and b are constants summarizing elementary constants and material parameters, V_R is the reverse bias applied to the tunneling junction, V_T is the thermal voltage kT/q, ξ denotes the electrical field across the tunneling junction and g_m is the transconductance. From (4) it is clear that the change in the channel potential energy can be determined from the transfer characteristics. For this purpose, a more detailed illustration of the encircled RTS step in Fig. 2 is provided in Fig. 6.

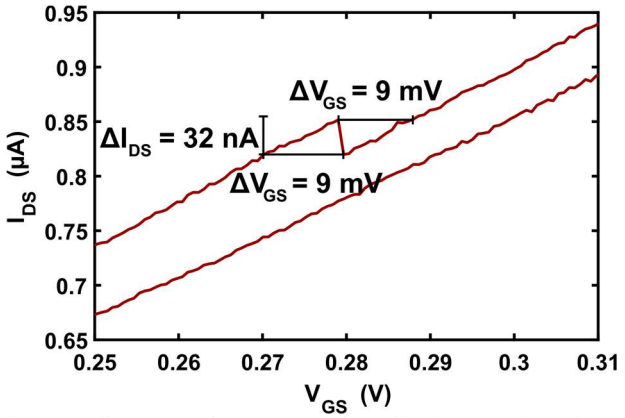

Fig. 6: Detailed view of the RTS step indicated in Fig. 2. As shown in (4), the change of the channel potential energy can be directly determined from the step.

According to a simple model of the surface potential Ψ_S, it depends on the gate voltage V_{GS} as

$$\Delta\Psi_S = \Delta V_{GS}\frac{C_{ox}}{C_{ox} + C_q + C_{it}}, \qquad (5)$$

where C_{ox} is the gate oxide capacitance, C_q is the semiconductor capacitance resulting from a finite density of states in the channel, and C_{it} represents interface defects between channel and gate oxide. The centroid capacitance C_c is neglected for the sake of simplicity, and furthermore it is masked by the small C_q. Since V_R denotes the change of Ψ_S due to the change in V_{GS}, (5) can be applied to V_R in exactly the same way as to Ψ_S.

The step ΔI_{DS} in the current indicated in Fig. 6 is caused by an abrupt change $\partial V_R/\partial q_{ox}$ in the tunnel junction reverse bias V_R due to a single captured charge q_{ox} in the gate oxide. To obtain the same ΔI_{DS} by changing the gate bias V_{GS}, a ΔV_{GS} of 9 mV would be required, as obtained from Fig. 6. To estimate the actual $\partial V_R/\partial q_{ox}$ from (5), we need to calculate C_{ox}, C_q, and C_{it}. C_{ox} can be simply calculated as a cylindrical capacitor, and C_q can be calculated as

$$C_q = \sqrt{\frac{2m^*}{E_F - E_1(0)}}\,\frac{q^2}{\pi\hbar} \qquad (6)$$

for the approximation of a 1D channel with a large C_{ox} [12], where $m^* = 0.023 \cdot m_0$ is the effective mass in the channel, $E_F - E_1(0)$ denotes the position of the Fermi level above the first subband, $\hbar$ the reduced Planck constant, and q the elementary charge. C_{it} can be calculated as $C_{it} = q^2 D_{it}$, where $D_{it} \approx 5 \cdot 10^{12}$ eV^{-1} cm^{-2} close to the conduction band edge [13]. With values of $C_{ox} \approx 0.033$ F/m^2, $C_q \approx 0.002$ F/m^2 ($E_F - E_1(0) \approx 0.15$ eV from Fig. 2 and (5) and C_q divided by the channel circumference for equal units), $C_{it} \approx 0.008$ F/m^2, and $\Delta V_{GS} = 9$ mV from Fig. 6, (5) results in $\partial V_R/\partial q_{ox} \approx 6.9$ mV.

With this value for the change in the channel potential energy, the plausibility of the calculated depth of the defect z can be validated further by electrostatic calculations. Approximating the cylindrical nanowire by a square nanowire with the same cross-sectional area and modelling a single charge at the calculated depth of 2.7 nm with the method of image charges results in a change in the channel potential energy of around 2.2 meV. Although this value is somewhat lower than the experimental one, it is still very close, given the uncertainties in some of the parameters used. Possible explanations are as follows. First of all, the assumption of a 1D density of states might be too optimistic and a larger 2D C_q would yield even more similar results for the calculated and the measured values ($\partial V_R/\partial q_{ox} \approx 5$ meV for C_q in 2D). Also, C_{it} might increase from the value from [13] when moving the bands further into the on-state, or the single dominant defect could be located closer to the channel interface than 2.7 nm. This would imply that τ_0 is larger than our choice of $4 \cdot 10^{-11}$ s. Furthermore, of course, the simulated model of image charges might be too simple. Again, however, with these sources of uncertainty taken into account,

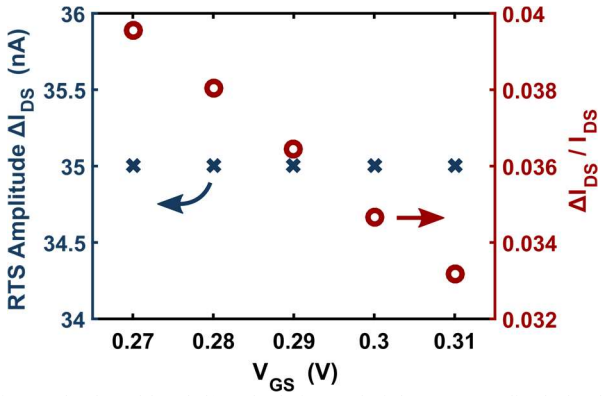

Fig. 7: Absolute (blue, left) and relative (red, right) RTS amplitude for the same RTS step as shown in the other figures. In accordance with (7), the relative RTS amplitude decreases with increasing gate voltage. Note that in accordance with (4), g_m is constant in this area.

both the experimental and the simulated values agree very well, which strongly supports the model of simple elastic tunneling as the mechanism for the observed RTS noise.

Finally, independent of the capture and release mechanism, the behavior of the relative RTS amplitude $\Delta I_{DS}/I_{DS}$ for the whole operation range can be described by extending (4) to

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\partial V_R}{\partial q_{ox}} \frac{\ln(10)}{S}, \qquad (7)$$

where ΔI_{DS} corresponds to $\partial I_{ID}/\partial q_{ox}$, I_{DS} to I_{ID} from (3) and S denotes the subthreshold slope calculated from (3) as well. Just as with (4), (7) also holds for the 3D case. This expression suggests a peak of the relative RTS amplitude in the subthreshold region, where S is steepest. Before and after this region it suggests a decay. And indeed, for the measurement series presented here, $\Delta I_{DS}/I_{DS}$ shows a monotonous decrease with increasing gate voltage, depicted in Fig. 7. For other devices and bias points, we were able to measure the other regions described by (7) as well, both increasing relative RTS amplitudes far into the subthreshold region and values around the expected peak. In the on-state, where the measurement series presented here was carried out, the relative RTS amplitude is as low as 3 – 4 %, but measurements in the subthreshold region showed values of up to 50 %. This large relative amplitudes strongly suggest a defect location close to the tunneling junction since defects far away from the junction will not affect the tunneling probability in a similarly strong way [4].

IV. Conclusions

We presented a detailed explanation of RTS noise in III-V nanowire TFETs with inverse subthreshold slopes well below 60 mV/decade. The origin of RTS noise are electrons captured in and released from individual gate oxide defects close to the tunneling junction and the behavior of the RTS amplitude can be explained by the expression of the TFET tunneling current in a straight forward manner. In the case presented here, the energy level of the defect is located far below the channel conduction band. For the explanation of the RTS time constants we assume elastic tunneling as the capture and emission process and the resulting depth of the oxide defect, $z \approx 2.7$ nm from the channel interface, agrees well with electrostatic calculations.

Acknowledgments

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