A 100MHz CMOS wideband IF amplifier

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Published in:
IEEE Journal of Solid-State Circuits

DOI:
10.1109/4.663569

1998

A 100-MHz CMOS Wide-Band IF Amplifier

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Abstract— **When the data rates of communication systems increase, wideband IF amplifiers are needed. It is also possible to use a single wideband intermediate frequency (IF) amplifier for a radio band with several narrow-band channels of varying strengths. The linearity is then critical, if intermodulation products are not to disturb weak channels.**

We try to find a topology for this new amplifier application, suitable for integration in a standard CMOS process. To get low distortion, we use an output stage with high linearity, which is further linearized by feedback in a double-nested Miller configuration.

A 0.8-μm standard CMOS IF amplifier design with low distortion up to 20 MHz is presented.

I. Introduction

WIDE-BAND intermediate frequency (IF) amplifiers are needed in wide-band communication systems. They can also be used in, for instance, base stations to amplify several channels simultaneously, some at the sensitivity limit and others strong.

In this paper we try to find a suitable topology for such an amplifier. The nonlinear distortion must be minimized, since the intermodulation noise is critical for the performance. To accomplish this we have used an output stage with high linearity, based on cancellation of nonlinearities. The output stage is further linearized by feedback. A double-nested Miller compensation is employed to maximize the feedback around the output devices [1]–[3]. A fully differential topology is employed to cancel out even order distortion.

The aim was to build a wide-band amplifier in a standard 0.8-μm CMOS process with a large dynamic range up to 20 MHz. The noise should thus be minimized and the linearity maximized. In [5] it is shown how to calculate the required total harmonic distortion (THD) figure, in order for the intermodulation products to have less power than the noise, if the input signal is Gaussian. The THD is to be less than about 0.06% at 3.6 $V_{\rm pp}$ output. The voltage gain is to be 100.

An amplifier fulfilling the above demands was designed and fabricated. The bandwidth was about 100 MHz and the measured harmonic distortion at 20 MHz, 3 $V_{\rm pp}$ into 1 kΩ was 0.06%. At 20 MHz, the third-order intercept point, IP_3, was 35 dBm = 33 dB·V referred to the output.

II. Output Stage

To achieve high linearity, we decided to let the output stage work in class A. The best linearity and efficiency is achieved by using a push–pull configuration. If the output transistors are matched and have an ideal square-law characteristic, the transconductance of the push–pull stage is linear [4]. To further improve the linearity, we used a double-nested Miller topology with large feedback around the output devices; see Fig. 1.

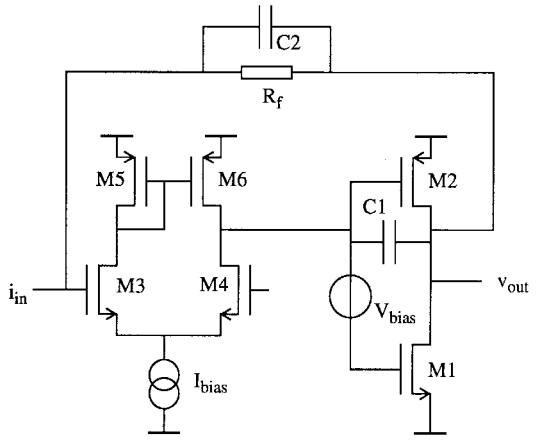

Fig. 1. The output stage.

There are conflicting requirements when selecting dimensions and quiescent current for the output transistors.

Class A operation at full output amplitude puts a lower limit on the quiescent current, and a large-output voltage swing combined with low distortion requires low effective $V_{\rm GS}$, which results in wide transistors. In order not to load the driving stage too much, the size of the output transistors must, however, be limited. The second pole of the current-driven combination of the output devices and the feedback capacitor is located at

$$p_{\rm 2nd} \approx -\frac{(g_{m1}+g_{m2})C_1}{C_L(C_{\rm gs1}+C_{\rm gs2}+C_1)} = \{C_1 = C_{\rm gs1}+C_{\rm gs2}\} = -\frac{(g_{m1}+g_{m2})}{2C_L}. \quad (1)$$

A pole at a high enough frequency requires a certain minimum value of g_m of the output devices. Finally, the power consumption must be kept down, which limits the acceptable quiescent current.

The output stage resembles a two-stage operational amplifier with a transresistance feedback R_f, including a phase-compensation Miller capacitor C1. The push–pull stage is different, though, since a normal two-stage op-amp uses a single ended output stage. In addition to the push–pull stage, capacitor C2 is also used in a nonstandard manner. It can be seen as a second nested Miller capacitor, or as a phantom zero feedback. It is important to note that the output devices are linearized by two nested feedback loops.

Manuscript received April 14, 1997; revised September 19, 1997.

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Publisher Item Identifier S 0018-9200(98)02334-8.

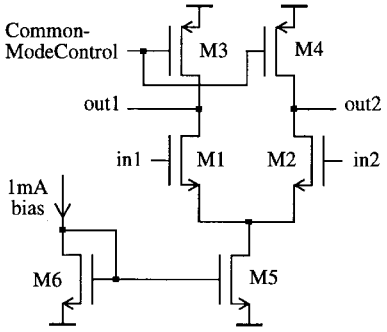

Fig. 2. The input stage.

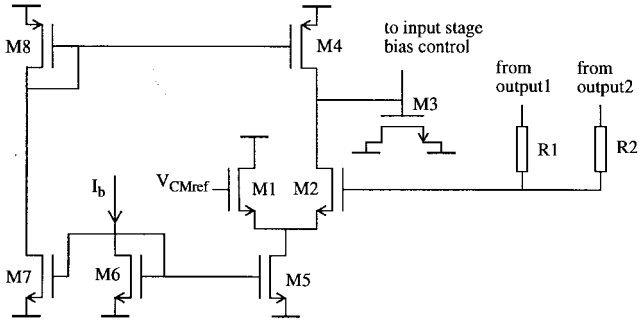

Fig. 3. The common-mode feedback circuit.

The loop gain of the outer loop of the output stage is given by

$$A_{\text{loop}} \approx g_{m_{\text{LTP}}} \cdot \frac{g_{\text{out}_{\text{LTP}}}}{1 + sR_{\text{out}_{\text{LTP}}}(1 + A_{v_{\text{out}}})C_1} \cdot A_{v_{\text{out}}} \cdot \frac{R_{\text{out}_{\text{input}}}}{R_{\text{out}_{\text{input}}} + R_f} = \{20\ \text{MHz}\} \approx g_{m_{\text{LTP}}} \cdot \frac{1}{sC_1} \cdot \frac{R_{\text{out}_{\text{input}}}}{R_{\text{out}_{\text{input}}} + R_f}. \quad (2)$$

The subscript out refers to the output devices (M1, M2), input to the input stage, and LTP to the long-tail pair stage with current mirror load (M3, M4, M5, and M6). To get a high loop gain, and thereby low distortion, high gain is needed in the LTP stage. This is achieved by using a large bias current (10 mA) and wide input transistors M3 and M4. In addition to this, the current mirror (M5, M6) doubles the gain (transconductance). If the power consumption is too high, a tradeoff between linearity and power consumption has to be done.

III. Input Stage

The input stage is a differential stage with differential outputs (Fig. 2). It is a transconductance stage that is followed by the transresistance output stages making the cascade a voltage amplifier.

The bias current through the input stage is set by the current mirror (M5, M6). The current through each of M1 and M2 is set to 2.5 mA. This amount of current is needed for low-noise operation. It also reduces distortion from the input stage and increases the gain. It is important that the input stage is very linear as it is not linearized by any feedback. The input transistors are wide to achieve low noise and high gain. The width is 740 μm and the length is 0.8 μm, which results in a transconductance of 20 mA/V.

The output impedance of the input stage affects the loop gain according to (2). To get as high linearity as possible, the output impedance must be maximized but without reducing the transconductance. Transistors M3 and M4 have therefore been made longer than minimum length. These devices must not be made too long, as the capacitance then instead reduces the output impedance.

The PMOS-transistors (M3, M4) are controlled by a common-mode feedback circuit (Fig. 3) which fixes the common-mode output of the entire amplifier at an appropriate value, ensuring that the input stage is correctly biased.

IV. Simulation and Measurement Results

The entire circuit with device parameters is shown in Fig. 4. This is what was simulated, fabricated and measured. A supply voltage of 3.3 V was used and the common-mode input voltage was set to 2.5 V. The load was 1 kΩ between the outputs and 1 kΩ from each output to ground. The source resistances (R_s) were 100 Ω.

The dc level at the outputs was 1.6 V with no input signal. This is controlled by the reference level fed to the common-mode feedback circuit.

The voltage gain was 100 in both the simulations and measurements.

The noise factor with $R_s = 100\ \Omega$ was simulated to 1.9 dB. This low noise figure is the result of the large input transistors and their large bias currents. The noise was measured at 20 MHz with 100-Ω source resistances, using a spectrum analyzer with a differential probe. The noise figure was then calculated to 4 dB. The measurement accuracy was probably not better than about one decibel. Several effects can explain that the noise is larger in the measurement than in the simulation. Noise due to hot electrons and layout parasitic resistances are not included in the simulation.

The harmonic distortion was simulated and measured for different signal levels and frequencies (see Table I). To make it easier to compare the performance in a system, the third-order intercept point was calculated for the different frequencies. The measured figures are between two and three times larger than the simulated ones. This gives an indication that distortion can be sensitive to parameter variations and hard to simulate. In spite of being larger than the simulated, the measured distortion is still very low. According to [5], the intermodulation products would probably be small enough to be masked by the amplifiers' thermal noise.

At about 15 pF differential load or more than 50 pF from each output to ground, the amplifier became unstable. At 3-pF external differential load, the response was flat and the phase margin of the outer loop was 30°. The inner loop is not a problem as it encloses just one transistor in a Miller loop. If for any reason more phase margin is desired the size of the bias resistors of the push–pull stage can be reduced, or the width of the LTP stage transistors can be reduced to decrease its gain and increase its speed. The Bode plot with just the

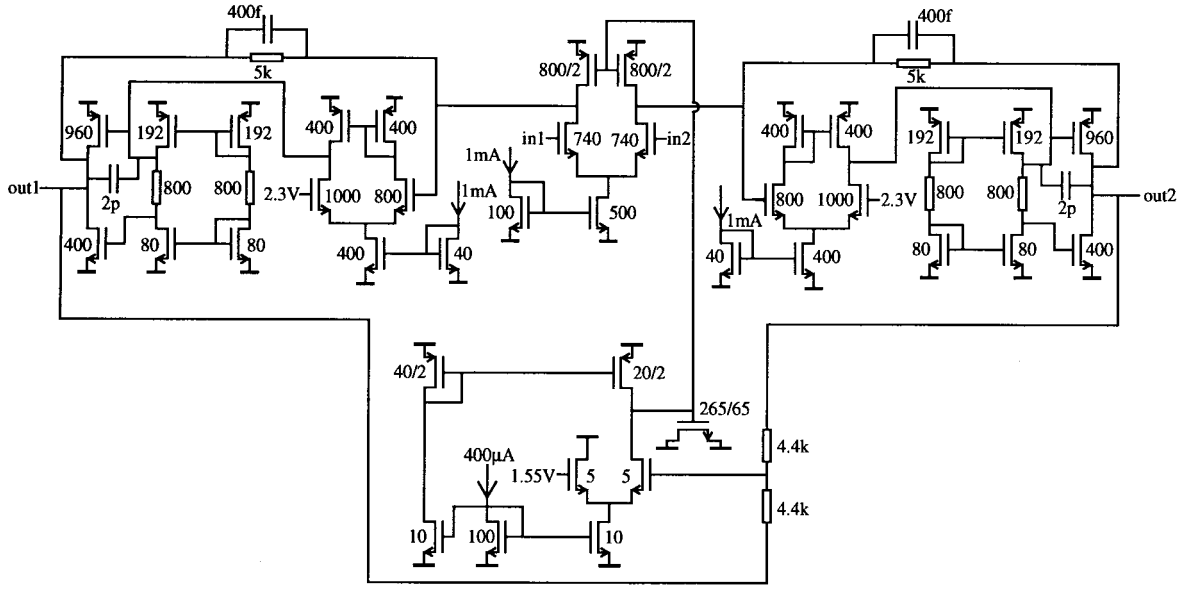

Fig. 4. The entire schematic with device parameters. Unless specified, the transistor length is 0.8 μm.

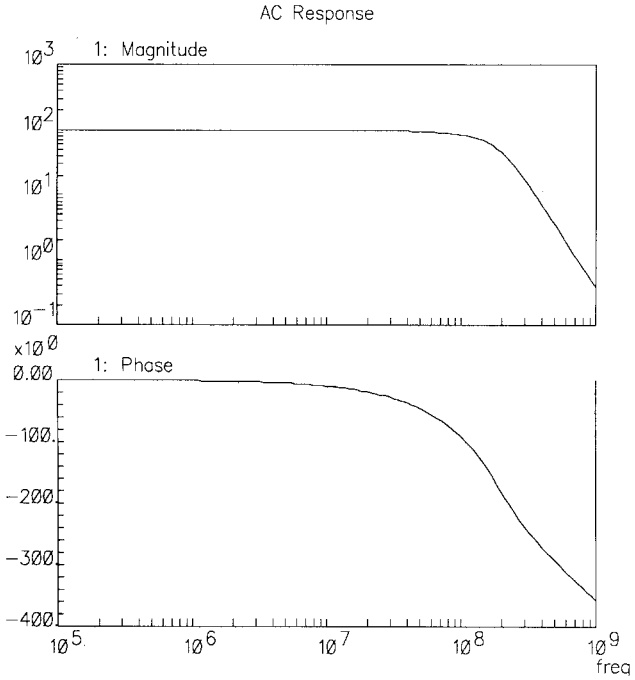

Fig. 5. Bode plot of the voltage gain with internal capacitive loading.

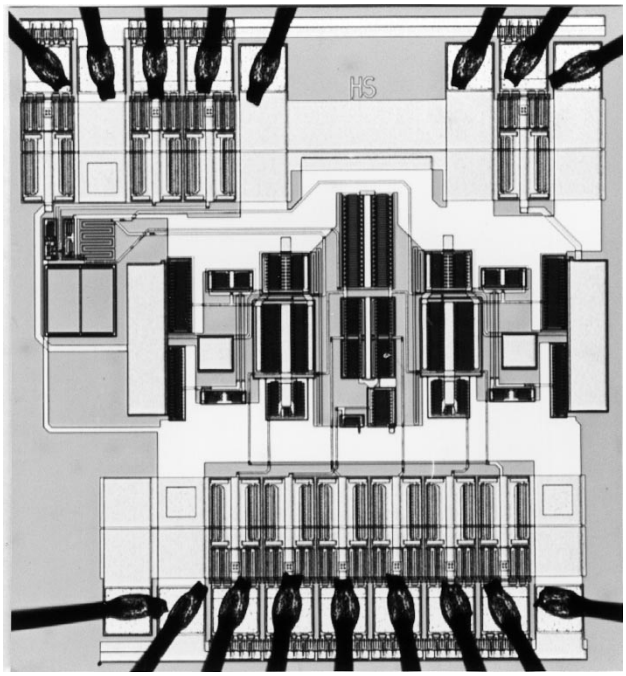

Fig. 6. Microphotograph of the amplifier.

internal load capacitances (pads) is shown in Fig. 5. The gain is flat in the operating band from dc to 20 MHz.

The total power consumption is 130 mW. This large figure can be explained by the balanced design and the demand for low noise and distortion over a large bandwidth. If more distortion can be accepted, the bias current of the LTP stages can be reduced, which will also increase the phase margin. If a differential output is not needed, the power consumption can be almost halved, as one output stage can be dispensed. The P devices of the input stage can then be connected as a current mirror, and the output stage can be biased by a current generator connected to its input.

The values above are about the same for common-mode input voltages in the range 1.4 to 3.5 V, which even exceeds the positive supply rail by 200 mV.

V. Conclusion

The simulation and measurement results show that we have designed an amplifier with high linearity from dc to 20 MHz. The design was made in a standard 0.8-μm CMOS process. It could be used as an IF amplifier in a base station to amplify several channels simultaneously or to amplify a wide-band signal.

TABLE I
MEASURED (M) AND SIMULATED (S) THD (1 kΩ)

	5MHz (M)	5MHz (S)	10MHz (M)	10MHz (S)	20MHz (M)	20MHz (S)
1 V_{pp} (out)	-	0.0016%	-	0.0016%	0.006%	0.0025%
2 V_{pp} (out)	0.013%	0.0068%	0.017%	0.0081%	0.026%	0.011%
3 V_{pp} (out)	0.037%	0.013%	0.035%	0.014%	0.062%	0.027%
4 V_{pp} (out)	0.066%	0.028%	0.060%	0.033%	0.16%	0.061%
5 V_{pp} (out)	-	0.11%	-	0.27%	-	0.75%
IP_3 (output)	35 dBV	39dBV	35 dBV	39 dBV	37 dBV	37dBV

The topology is thus possible to use for high-performance CMOS wide-band amplifiers. High-performance requirements tend to result in larger power consumption than lower requirements. The topology is also suitable for variable gain amplifiers, as there is no feedback loop around the input stage.

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