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# A Self-aligned Gate-last Process applied to All-III-V CMOS on Si

Adam Jönsson, Johannes Svensson, and Lars-Erik Wernersson

**Abstract**—Vertical nanowire n-type (InAs) and p-type (GaSb) transistors are co-processed and co-integrated using a gate-last process, enabling short gate-lengths ( $L_g=40$  nm) and allowing selective digital etching of the channel. Two different common gate-stacks, including various pre-treatments, were compared and evaluated. The process was optimized to achieve high n-type performance while demonstrating p-type operation. The best n-type device is scaled down to 12 nm diameter and has a peak transconductance of 2.6 mS/ $\mu$ m combined with a low  $R_{on}$  of 317  $\Omega \cdot \mu$ m while the p-type exhibit 74  $\mu$ S/ $\mu$ m. In spite of increased complexity due to co-integration, our n-type InAs transistors demonstrate increased drive-current, 1.8 mA/ $\mu$ m, compared to earlier publications.

**Index Terms**—Vertical, nanowire, III-V, MOSFET, CMOS, InAs, GaSb

## I. INTRODUCTION

COMPLEMENTARY metal-oxide-semiconductor (CMOS) circuits based on all-III-V channel materials require further development to achieve competitive p-type performance [1], [2]. Although antimonide-based materials such as GaSb have demonstrated high hole mobility [3], transistor performance is, in part, limited by the gate-stacks [4]–[6]. It has been suggested that combinations of a more conventional p-type SiGe channel combined with n-type III-V InGaAs channel is a viable alternative to current CMOS technology [7], [8]. This type of material integration is, however, not straightforward, mainly due to strong material selectivity during processing.

With continued transistor scaling, deteriorated electrostatics leads to various short channel effects [9]. Vertical nanowires with a gate-all-around (GAA) geometry is one alternative with beneficial performance at the 5 nm node [10]. The vertical nanowire geometry in particular decouples the gate length and contact geometry from the footprint area [11].

In this paper, GaSb p-type and InAs n-type MOSFETs are co-integrated in a vertical nanowire gate-all-around structure, utilizing a common gate-stack. The process uses hydrogen silsequioxane (HSQ) spacers with adjustable thickness for development of a self-aligned, gate-last, process compatible with vertical antimonide-based structures.

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All presented devices are scaled to sub-100 nm gate lengths and, for the n-type devices, nanowire diameters down to 12 nm are demonstrated. Improved drive-currents are also realized as compared to previous iterations of vertical InAs transistors, namely a 400% (gate-last) [12] and 150% (doped channel) [13] increase is shown with  $I_{DS} = 1.8$  mA/ $\mu$ m ( $V_{ds}$  and  $V_{gs} = 0.7$  V).

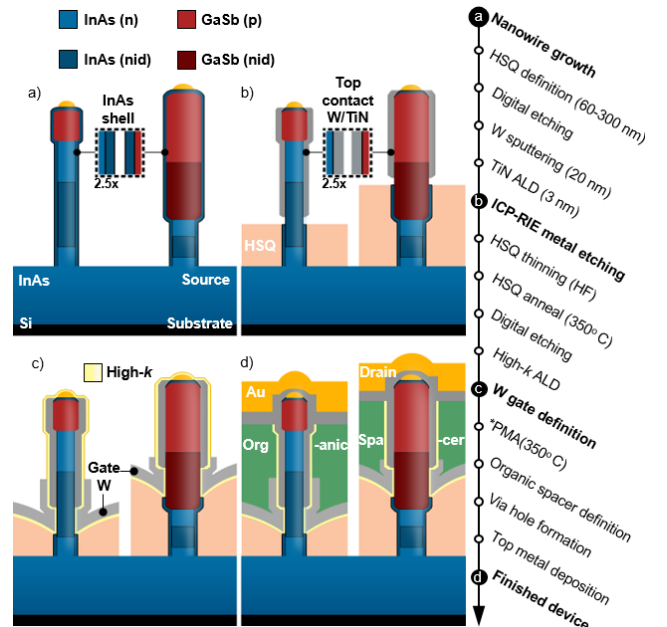


Fig. 1. Schematic illustration of crucial steps in the full process flow attached with an overview of fabrication. The illustrations show n-doped channel devices, notice that the process allows for varying gate placement along the nanowire. \*Post metal anneal (PMA) is performed only on specific samples.

## II. DEVICE FABRICATION

Fig. 1 schematically illustrates the process flow for co-integration of p-type GaSb and n-type InAs MOSFETs. The devices are fabricated on 1 cm<sup>2</sup> p-type silicon (111) substrates with a 260 nm epitaxially grown InAs layer [14].

InAs-GaSb nanowires are subsequently grown from 15-nm-thick Au seed particles defined by electron beam lithography (EBL). Sections of the InAs segment is n-doped by Sn and the top of the GaSb segment is p-doped by Zn, see Fig. 1. In the case of GaSb growth, significant background doping is present attributed to point defects ( $\sim 10^{16}$ ) [15]. By utilizing the Gibbs-Thomson effect during VLS growth, the GaSb growth rate can be significantly reduced for smaller gold particle sizes [16]

(diameter < 30 nm) which enables length control of the two separate materials in the heterojunction nanowires [17]. Therefore, 24 nm and 28 nm diameter Au dots are used for growing n-type wires and 44 nm for p-type wires. The Au dots

TABLE I  
SAMPLE DESCRIPTION

Sample	Sample A	Sample B
Top contact formation <sup>1</sup>	Ozone oxidation + citric acid 60 s + W/TiN	Ozone oxidation + citric acid 60 s + 1:500 + (NH <sub>4</sub> ) <sub>2</sub> S:H <sub>2</sub> O 3 min
Gate-stack Pre-treatment	HCL:IPA + 5x TMAI pulses	Citric acid + 8x {TMAI pulse and H <sub>2</sub> plasma}
High- <i>k</i>	<sup>2</sup> 6/36 cycles Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> EOT = 0.85 nm	<sup>3</sup> 40 cycles HfO <sub>2</sub> (+PMA) EOT = 0.76 nm
n-type doping	nid-channel	n-channel
<i>L<sub>g</sub></i>	50 nm	40 nm
diameter	20 nm	12 nm
<i>g<sub>m,peak</sub></i>	1.2 mS/μm	2.6 mS/μm
<i>SS<sub>lin</sub></i>	74 mV/dec	191 mV/dec
<i>R<sub>on</sub></i>	1039 Ω·μm	317 Ω·μm
p-type		
<i>L<sub>g</sub></i>	70 nm	100 nm
diameter	40 nm	38 nm
<i>g<sub>m,peak</sub></i>	74 μS/μm	11 μS/μm
<i>SS<sub>lin</sub></i>	273 mV/dec	622 mV/dec
<i>R<sub>on</sub></i>	5.9 kΩ·μm	20 kΩ·μm

Description of processing variations for two different samples highlighting the critical steps involved. An overview is given for the important performance metrics. *g<sub>m,peak</sub>* is extracted at drain bias  $|V_{ds}|=0.5$  V and *SS<sub>lin</sub>* at  $|V_{ds}|=0.05$  V.

<sup>1</sup>Contact annealing, post top metal definition, has been performed at 350 degrees C for 60 minutes (Fig. 1). <sup>2</sup>Al<sub>2</sub>O<sub>3</sub> (TMAI) and HfO<sub>2</sub> (TDMAHf) is deposited at 300 °C and 120°C respectively. <sup>3</sup>In situ remote plasma treatment of the surface is carried out inside the ALD chamber and HfO<sub>2</sub> (TDMAHf) is deposited at 250°C. Additional post metal anneal (PMA) at 350°C is also performed after gate-definition on sample B.

are patterned in structures with a pitch of about 300 nm.

In the first step, the top contact is defined with an HSQ mask, whose thickness is determined by the dose in an EBL process [9]. The thicknesses of the HSQ is gradually varied from 60 to 300 nm to define gate position in separate devices. The InAs shell on the protruding part of the nanowires, that will later constitute the top contact, is digitally etched by oxidation and citric acid treatment. An ammonium sulfide treatment is also used for some of the samples, to passivate the III-V surface [18], processing differences are outlined in Table I. Subsequently, 20 nm tungsten (W) is sputtered followed by a 3 nm TiN atomic-layer-deposited (ALD) film. The metal is removed from all planar surfaces by an ICP-RIE SF<sub>6</sub>:C<sub>4</sub>F<sub>8</sub> based dry-etch process leaving metal on the nanowire sidewalls defining the top metal contact.

The same HSQ mask is also used as a bottom spacer by thinning it with a diluted HF (1:1000) wet etch so that the nanowire part that constitutes the channel protrudes. This method allows for sub-100 nm gate-length definition. The exposed semiconductor surface is digitally etched by oxidation followed by either citric acid or an HCL:IPA (1:30) treatment. The number of digital etch cycles are adjusted to remove the overgrown doped InAs shell, restoring the core channel material for the p- and n-type wires, that finishes the gate recess.

To optimize the processing conditions, two types of high-*k*

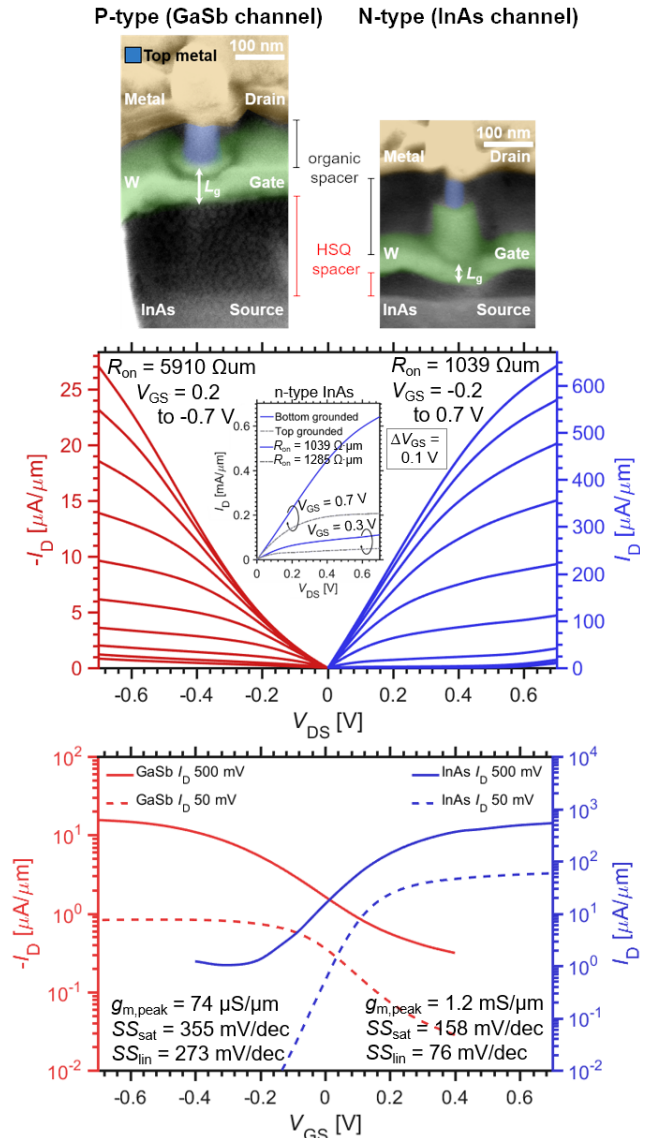


Fig. 2. Falsely colored SEM-images depicting single nanowires inside a p-type and n-type structure for Sample A (Table I), highlighting the different HSQ thickness. Combined transfer and output characteristics is presented for a selected p- and n-type device. The n-type (nid-channel) device consists of 184 nanowire array with a pitch of 300 nm, diameter of 20 nm, and  $L_g = 50$  nm. The p-type consists of 144 nanowires with a pitch of 350 nm, diameter of 40 nm, and  $L_g = 70$  nm. Increased resistance is shown in  $R_{on}$  by switching drain and source to realize a top grounded configuration.

are compared, a conventional bi-layer Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> [19] and a pure HfO<sub>2</sub> dielectric. The HfO<sub>2</sub> only gate-stack is preferred for aggressive EOT scaling [20]. High temperature ( $\geq 250^\circ\text{C}$ ) is necessary when forming the interface layers for more effective self-cleaning [19], [21]. The different high-*k* with corresponding pre-treatments are described further in Table I, representing the best optimization for GaSb p-type (Sample A) and InAs n-type (Sample B) device performance.

The gate metal is defined by sputtering 60 nm W followed by a back-etched S1813 spacer as mask for an SF<sub>6</sub> dry-etch process to remove the top of the gate W and vertically align the gate to the top contact. An organic spacer is then deposited, followed by sputtering of the top metal electrode consisting of W/Ni/Au.

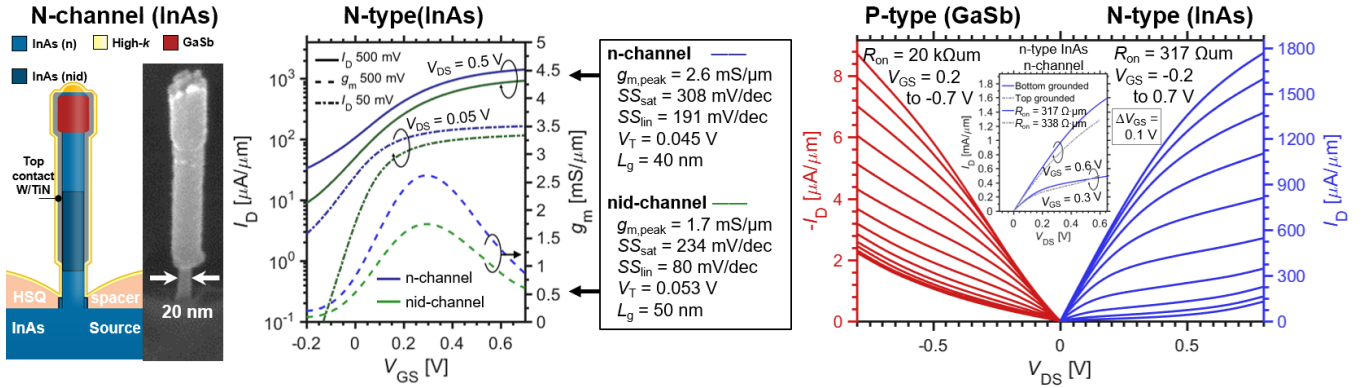


Fig. 3. Comparison between 184 nanowire arrays with  $L_g = 40$  and  $L_g = 50$  nm from sample B (Table I). Output characteristics of the p-type device in Sample B is also included. The SEM image is showing a 12 nm diameter nanowire, with doped channel (n-channel) after in-situ hydrogen plasma and high-k ALD comprised of 40 cycles  $\text{HfO}_2$  corresponding to 4 nm thickness. The lower curve of each curve-pair (n-type InAs) corresponds to a, not intentionally doped, nid-channel. The HSQ spacer thicknesses for n- and nid-channel devices are 10 and 50 nm, respectively. Contact resistance behaves symmetrically with closely matched  $R_{on}$  values for switched bias conditions, due to improved contact processing.

Notice that the InAs-GaSb combination introduces a tunneling source contacts with broken bandgap, for the p-type device, where reported values suggest that it may have sufficiently low resistivity (axial Esaki diodes:  $\sim 260 \Omega \cdot \mu\text{m}$ ) [22], [23]. Thus the InAs-GaSb structure, due to resemblance with state-of-the-art Tunnel-FETs [24], [25], lends itself for future CMOS Tunnel-FET implementations including co-integration of MOSFETs and Tunnel-FETs.

### III. DEVICE CHARACTERIZATION

Transfer and output characteristics for sample A with a bilayer gate-stack is presented in Fig. 2. Transconductance  $g_{m,peak}$  values of  $1.2 \text{ mS}/\mu\text{m}$  for n-type and  $74 \mu\text{S}/\mu\text{m}$  for p-type was achieved with minimum subthreshold slope  $SS_{lin}$  of 74 and 271 mV/dec. Both devices exhibit enhancement mode operation with  $V_T = 0.08$  and  $-0.02$  V. The limited n-type off-state performance is partly caused by drain tunneling due to the narrow bandgap of InAs [26]. However, for the p-type GaSb device the large diameter of the gate-segment in conjunction with a non-optimal high- $k$  interface degrades the off-state. The 24 times higher drive current for the n-type as compared to the p-type MOSFET is expected due to the large difference in charge carrier mobility [2]. Further, significant gate-length scaling and strained GaSb channels are needed to enable the p-type MOSFET semi-ballistic operation [27], [28].

The resistance originating from the top contact is reduced for the n-type device in sample B (Table I) by adding a sulfur passivation step during the top contact definition, which increases the on-state performance,  $g_{m,peak} = 2.6 \text{ mS}/\mu\text{m}$  (n-channel), Fig. 3. This is further quantified by switching the source and drain electrodes during measurement that displays a symmetrical behavior with low  $R_{on}$  values of 317 and 338  $\Omega \cdot \mu\text{m}$ , in contrast to the n-type device in sample A (Fig. 2 inset). This device also utilizes a pure  $\text{HfO}_2$  gate-stack with low EOT of 0.76 nm, see Table I. The off-state and electrostatics are limited, which can be attributed to a doped channel and a high-temperature deposition of  $\text{HfO}_2$  at  $250^\circ\text{C}$  [29]. The hysteresis window corresponding to the gate-stack is evaluated to 20 mV, on a representative device, at the minimum  $SS$  point ( $V_{ds} = -0.2$  to  $0.7$  V). An additional device with nid-channel, based on the

same type of nanowire that has a gate shifted upwards along the nanowire, is also available on the same sample and is presented in Fig. 3. Here, improved electrostatics is shown with  $SS_{lin}$  decreased from 191 (n-channel) to 80 mV/dec (nid channel). Even though  $\text{H}_2$ -plasma on InAs may result in increased surface roughness we find that high transconductance values still can be obtained. The n-type devices, on sample B, with peak transconductance  $g_{m,peak}$  of 2.6 (n-channel) and  $1.7 \text{ mS}/\mu\text{m}$  (nid-channel), at  $V_{ds} = 0.5$  V, indicate added source resistance due to varied HSQ spacer thickness. The spacer is varied from 10 (n-channel) up to 50 nm (nid-channel), see Fig. 3. Notably the saturation current for the device with doped n-channel is  $1.8 \text{ mA}/\mu\text{m}$  at  $V_{gs} = 0.7$  V. The improved drive current, compared to previous InAs transistor iterations, can be attributed to the addition of doping at the bottom nanowire-segment [12] and n-doped shell growth [13]. The p-type device is demonstrated although with reduced performance and electrostatics as compared to the n-type device quantified by  $g_{m,peak} = 11 \mu\text{S}/\mu\text{m}$  ( $V_{ds} = -0.5$  V) and  $SS_{lin} = 622 \text{ mV}/\text{dec}$ , see Table I.

### IV. CONCLUSIONS

A new process for n-type (InAs) and p-type (GaSb) MOSFET co-integration compatible with highly sensitive antimonide-based materials has been developed. Aggressively scaled devices with sub-100 nm gate-lengths and n-type diameters down to 12 nm have been demonstrated using gate-stack variation, giving a highest  $g_{m,peak}$  of  $2.6 \text{ mS}/\mu\text{m}$ , see Table I. P-type devices, demonstrating  $g_{m,peak}$  of 74 and  $11 \mu\text{S}/\mu\text{m}$ , are also co-integrated on the same samples. Further optimization of the GaSb gate-stacks combined with aggressive diameter scaling will increase the balance for the III-V CMOS. The HSQ-spacer utilization allows for future integration of p- and n-type on the same nanowire, ultimately reducing the diameter difference between the devices. The process also enables possibilities for co-integrating MOSFETs with state-of-the-art Tunnel-FETs.

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