Vertical Nanowire High-Frequency Transistors

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Doctoral Thesis

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Abstract

This thesis explores a novel transistor technology based on vertical InAs nanowires, which could be considered both for low-power high-frequency analog applications and for replacing Si CMOS in the continued scaling of digital electronics. The potential of this device - the vertical InAs nanowire MOSFET – lies in the combination of the outstanding transport properties of InAs and the improved electrostatic control of the gate-all-around geometry.

Three generations of the vertical InAs nanowire MOSFET are presented in this thesis; the first generation, integrated on semi-insulating InP substrate, provided the first RF measurements on vertical nanowire transistors with extrinsic f_t/f_{max} > 7/20 GHz. Utilizing the resilience towards dislocations inherent to the vertical nanowire growth, the second generation is integrated on highly resistive Si substrates by a thin InAs buffer layer. The RF performance is comparable to the first generation, indicating sustained crystal quality of the nanowires. In the third generation, however, a great boost in the RF performance is achieved by removing excess metal overlap and, hence, reducing the parasitic gate capacitance, which resulted in extrinsic f_t/f_{max} = 141/155 GHz at $L_g \approx$ 150 nm.

The main challenge for III-V MOSFETs is the high-κ integration as high densities of charge traps deteriorate the device performance. Focusing on the border traps, a method based on frequency dispersion in g_m (1 Hz-100 GHz) is developed for direct measurement of the trap density as a function of distance from the oxide-semiconductor interface. The method is demonstrated for vertical InAs nanowire MOSFETs and surface-channel InGaAs MOSFETs.

Contents

Populärvetenskaplig Sammanfattning

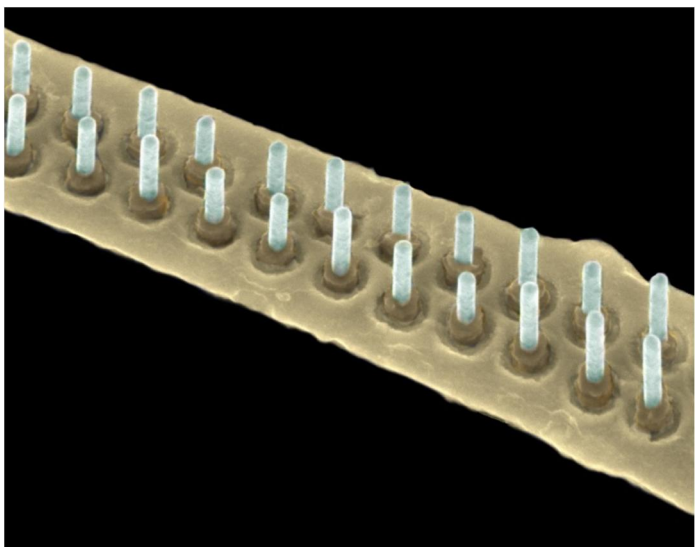
Minns du din första dator? Kanske köpte familjen den på avbetalning genom jobbet för 20 000 kr och kanske kan du såhär i efterhand tycka att effektförbrukningen var lite väl hög i relation till datorns prestanda. Den gick t.ex. inte att köra på batteri. Detta är ganska långt ifrån dagens datorer, smart-TV, smarta telefoner och surfplattor där vi kan streama filmer och musik. Den förhöjda datorkraften har givetvis haft en enorm påverkan på samhället och hur man arbetar. Forskningen är inget undantag. Nu är vi på väg in i nästa era som brukar benämnas *Sakernas internet* eller *Molnet*. Karakteristiskt för denna era är att en uppsjö av prylar kopplas till trådlösa nätverk: skidglasögon, husväggar, din puls… Bara fantasin sätter gränserna. Detta ställer grundläggande elektroniska komponenten – transistorn.

För varje generation av transistorer finns det tre kriterier som måste uppfyllas. De måste vara snabbare, ta upp mindre yta på chipet och förbruka mindre effekt. Från 1970 till ungefär 2003 skedde denna utveckling exponentiellt. Antalet komponenter per chip dubblades ungefär vartannat år. Men idag verkar det som att kiselteknologin som dominerat marknaden ända sedan 70-talet inte längre kan leverera snabbare och strömsnålare transistorer i den takt marknaden vant sig vid. Samtidigt är kraven som ställs på transistorerna från *Sakernas internet* mycket mer diversifierade än tidigare då transistorns användningsområde var mer begränsat. Behovet av att undersöka alternativa teknologier är därför större än någonsin och det är här min forskning kommer in.

I denna avhandling beskrivs en teknologi skiljer sig från kiselteknologin huvudsakligen i två avseenden. För det första är transistorerna inte gjorda i kisel (Si) utan i indiumarsenid (InAs). Valet grundar sig i hur elektronerna rör sig i de olika

materialen. I indiumarsenid är elektronerna mer rörliga och kan nå högre hastigheter än i kisel vilket i slutändan leder till snabbare transistorer.

Den andra stora skillnaden är geometrin. Kiselteknologin baserar sig traditionellt på en plan yta där en transistor skapas då man lägger tre kontakter på denna yta. Strömmen mellan två av kontakterna (source och drain) kontrolleras med hjälp av den tredje kontakten (gate). Mer specifikt styrs styrkan på det elektriska fältet under gaten genom att en spänning läggs på och därigenom förändras potentialen för laddningar som rör sig mellan source och drain. För att det inte ska gå för stora strömmar genom gaten brukar man isolera denna med ett tunt oxidskikt. Jag tillverkar samma typ av transistor men utgår ifrån vertikala nanotrådar istället för en plan yta. På de avlånga nanotrådarna med en diameter på ca 40 nm och en längd på ca 500 nm placeras de tre kontakterna vertikalt ovanpå varandra.



Nanotrådstransistorerna kontrolleras flera gånger under tillverkningsprocessen. Denna bild visar gate-kontakten (i gult) som omsluter nanotrådarna. Bilden är färglagd i efterhand och tagen snett uppifrån med ett elektronmikroskop.

Eftersom gaten kopplar hela vägen runt nanotråden kan laddningarna inne i den styras på ett effektivare sätt än i en plan transistor vilket förbättrar möjligheterna att skala ner transistor-storleken. Detta har länge varit känt men många har tyckt att det är ett för stor förändring att byta geometri eftersom man redan investerat väldigt mycket pengar i den befintliga tillverkningsmetoden. Det var därför en sensationell nyhet när det ledande företaget inom transistortillverkning, Intel, år 2011 offentliggjorde att de frångått plana transistorer till förmån för en slags liggande kiselnanotrådar med gate-kontakter som påverkar kanalen både uppifrån och från sidorna. Vertikala nanotrådarstransistorer skiljer sig ännu mer från de plana

transistorerna, men en sådan transistor kräver teoretiskt sett inte lika stor yta. Dessutom kan kristalltillväxten av vertikala nanotrådar vara väldigt förlåtande och ge ett högkvalitativt material även om man till exempel ändrar sammansättningen eller låter indiumarsenid-nanotrådar växa på kiselplattor.

År 2009, när arbetet i detta avhandlingsarbete påbörjades, fanns det väldigt få rapporter om hur snabba nanotrådstransistorer egentligen är. För att kunna mäta detta på ett trovärdigt och lättolkat sätt utvecklades en tillverkningsprocess där varje transistor, bestående av i storleksordningen 100 nanotrådar, isolerades från de övriga transistorerna. Det visade sig att strömmar kunde förstärkas upp till 7 GHz. För högre frekvenser hängde transistorn inte med. Efter ytterligare processutveckling kunde en enklare form av nanotrådstransistor på kiselsubstrat presenteras med en brytfrekvens på 9 GHz. Även om båda dessa rapporter var världsrekord för vertikala nanotrådarstransistorer kunde vi inte vara helt nöjda. Det var nämligen tydligt från transistormodelleringen att det var kontakterna, och inte nanotrådarna, som begränsade prestandan. I den nyaste versionen av nanotrådstransistorn är kontakterna omdesignade och brytfrekvensen har ökat till 140 GHz. I och med detta resultat har vi visat att den vertikala nanotrådstransistorn är en kandidat att räkna med för applikationer som kräver höga frekvenser.

Den största utmaningen för den här typen av transistorer som baseras på andra halvledarmaterial än kisel är det stora antalet defekter i oxidskiktet under gate-kontakten. Dessa defekter kan hålla fast laddningar som egentligen skulle ha rört sig mellan source och drain, och därigenom ökar transistorns effektförbrukning. De elektriska följdverkningarna har varit synliga i de högfrekvens-mätningar som gjorts på nanotråds-transistorerna och plana transistorer av liknande material och från detta har vi utvecklat en metod där oxidens defekt-densitet kan bestämmas direkt från transistormätningar. Speciellt för metoden är också att mätningar gjorts i ett väldigt stort frekvensintervall – från 1 Hz till 100 GHz (= 100 000 000 000 Hz).

Under min tid som doktorand har jag bytt institution från Fysik till Elektro- och Informationsteknik och man skulle kunna säga att nanotråds-transistorn har gjort detsamma: att den nu är ett steg närmare tillämpad användning.

Preface and List of Papers

This thesis summarizes my academic work for a Doctoral degree in Electrical Engineering. The work has been done within the Nanoelectronics group at the division of Solid State Physics (FTF), Lund University, and at the department of Electrical and Information Technology (EIT), Lund University.

My work includes device fabrication, electrical characterization and modeling. However, the epitaxial growth in the papers was performed by Sepideh Gorji Ghalamestani, Mattias Borg, Johannes Svensson, Jun Wu, and Elvedin Memisevic and the device processing of planar InGaAs transistors was performed by Jiongjiong Mo, and Erik Lind. This experimental work is, hence, not included in the thesis.

The first part of this thesis serves as an introduction to the work for a reader with some knowledge in semiconductor and device physics. In the second part, the included papers, which are listed in the following section, are appended.

List of Included Papers

I. Vertical InAs nanowire wrap gate transistors with $f_t > 7$ GHz and $f_{max} > 20$ GHz

M. Egard, S. Johansson, A.-C. Johansson, K.-M. Persson, A. W. Dey, B. M. Borg, C. Thelander, L.-E. Wernersson, and E. Lind, Nano Letters, vol. 10, no. 3, pp. 809-812, 2010.

I developed the process scheme and fabricated the devices together with A.-C. J., I did the RF characterization together with M. E., I did the DC characterization, and wrote parts of the paper.

II. RF characterization of vertical InAs nanowire wrap-gate transistors integrated on Si substrates

S. Johansson, M. Egard, S. G. Ghalamestani, B. M. Borg, M. Berg, L.-E. Wernersson, and E. Lind, IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 10, pp. 2733-2738, 2011.

I fabricated the device and did the DC characterization. I did the RF characterization together with M. E., and I was the main author of the paper.

III. Uniform and position-controlled InAs nanowires on 2" Si substrates for transistor applications

S. Gorji Ghalamestani, S. Johansson, M. B. Borg, E. Lind, K. A. Dick, and L.-E. Wernersson, Nanotechnology, vol. 23, no. 1, p. 015302 (7pp), 2011.

I did the pre-growth processing of the 2" substrate and participated in the analysis of the growth. I fabricated the transistors, did the DC and RF characterization and wrote parts of the paper.

IV. Temperature and annealing effects on InAs nanowire MOSFETs

S. Johansson, S. Gorji Ghalamestani, M. Borg, E. Lind, and L.-E. Wernersson, Microelectronic Engineering, vol. 88, no. 7, pp. 1105-1108, 2011.

I fabricated the devices, did the measurements, data analysis, and wrote the paper.

V. A high-frequency transconductance method for characterization of high-κ border traps in III-V MOSFETs

S. Johansson, M. Berg, K.-M. Persson, and E. Lind, IEEE Transactions on Electron Devices, vol. 60, no. 2, pp. 776-781, 2013.

I developed the method and did the data analysis together with E. L., I did the measurements and wrote the paper.

VI. Characterization of border traps in III-V MOSFETs using an RF transconductance method

S. Johansson, J. Mo, and E. Lind, 2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 53-56, 2013.

I developed the method and did the data analysis together with E. L., I did the measurements and wrote the paper.

VII. High-frequency gate-all-around vertical InAs nanowire MOSFETs on Si substrates

S. Johansson, E. Memisevic, L.-E. Wernersson, and E. Lind, IEEE Electron Device Letters, vol. 35, no. 5, pp 518-520, 2014.

I developed the process, fabricated the device, did the DC and RF characterization, and, wrote the paper.

List of Related Papers

During my PhD studies I have also contributed to the papers listed below. These papers are not included in this thesis either due to overlapping content or because the content is beyond the scope of this thesis.

viii. High frequency performance of vertical InAs nanowire MOSFET

E. Lind, M. Egard, S. Johansson, A.-C. Johansson, B. M. Borg, C. Thelander, K.-M. Persson, A. W. Dey, and L.-E. Wernersson, in Proceeding of the International Conference on Indium Phosphide & Related Materials (IPRM), 2010.

ix. Highly controlled InAs nanowires on Si(111) wafers by MOVPE

S. G. Ghalamestani, S. Johansson, B. M. Borg, K. A. Dick, and L.-E. Wernersson, Physica Status Solidi (c), vol. 9, no. 2, pp. 206-209, 2012.

x. High frequency vertical InAs nanowire MOSFETs integrated on Si substrates

S. Johansson, S. G. Ghalamestani, M. Egard, M. Borg, M. Berg, L.-E. Wernersson, and E. Lind, Physica Status Solidi (c), vol. 9, no. 2, pp. 350-353, 2012.

xi. (Invited) Extraction of oxide traps in III-V MOSFETs using RF transconductance measurements

E. Lind, and S. Johansson, ECS transactions, vol. 52, no. 1, pp. 415-419, 2013.

xii. Extrinsic and intrinsic performance of vertical InAs nanowire MOSFETs on Si substrates

K.-M. Persson, M. Berg, M. B. Borg, W. Jun, S. Johansson, J. Svensson, K. Jansson, E. Lind, and L.-E. Wernersson, IEEE Transactions on Electron Devices, vol. 60, no. 9, pp. 2761-2767, 2013.

xiii. RF and defect analysis of stressed III-V MOSFET
G. Roll, E. Lind, M. Egard, S. Johansson, L. Ohlsson, and L.-E.Wernersson, IEEE Electron Device Letters, vol. 35, no. 2, pp. 181-183, 2014.

xiv. RF reliability of gate last InGaAs nMOSFETs with high-κ dielectric

G. Roll, M. Egard, S. Johansson, L. Ohlsson, L.-E. Wernersson, and E. Lind, IEEE International Integrated Reliability Workshop Final Report (IRW), pp. 38-41, 2013.

xv. RF characterization of vertical InAs nanowire MOSFETs with f_t and f_{max} above 140 GHz

S. Johansson, E. Memisevic, L.-E. Wernersson, E. Lind, Proceeding of the International Conference on Indium Phosphide & Related Materials (IPRM), 2014.

1. Background

In 1947, the revolution of electronics began when the first transistor was invented by John Bardeen and Walter Brattain at Bell Labs [1, 2]. The overwhelming progress seen during the last 50 years, especially in Si complementary metal-oxide-semiconductor (CMOS) technology, is driven by Gordon Moore's prediction from 1965 that the number of components on integrated circuits would double roughly every two years [3]. An exponential increase in the number of transistors is accomplished to a large extent by geometrical down-scaling. In addition to a reduced cost per transistor, this has led to exponential increase in clock-frequency and an exponential decrease in the power consumed by each transistor. At least this was true until about 2003 when CMOS entered an era of power-constrained scaling as the power dissipation reached 100 W/cm^2 and the transistor speed had to be compromised to avoid overheating [4]. It is evident that scaling of CMOS becomes more and more difficult. Some major changes have already been introduced to the Si CMOS technology, for example the SiO_2/polysilicon gate has been replaced by a high-κ dielectric/metal gate and the planar geometry has been abandoned in favor of tri-gate geometry.

Simultaneously, a diverse future is anticipated as an era referred to as the Internet of Things (IoT) is entered [5]. Here, computing devices find new applications in all parts of our society. The use will mainly be in wireless communication between objects and collection of data rather than human-to-human communication. The number of computing devices per capita is expected to increase exponentially and the specifications that need to be met by different transistor technologies will become much more diversified. On the wish list are for instance disposable sensors and energy-harvesting devices with short or long range wireless communication. Hence, the need for research on new transistor technologies is greater than ever before.

This chapter provides an introduction to the field by first presenting some aspects of the metal-oxide-semiconductor field-effect transistor (MOSFET). This is followed by

a background to the choice of material and geometry in the vertical InAs nanowire transistor and a discussion on possible applications for this device. Finally, one of the main challenges for III-V MOSFETs, *i.e.* traps in the gate oxide, is introduced.

1.1 The Metal-Oxide-Semiconductor Field-Effect Transistor

The following text introduces the basic operation of a metal-oxide-semiconductor field-effect transistor (MOSFET) and some important metrics used to characterize its electrical performance. The metrics are later used for benchmarking, but needs to be considered already when designing the transistor. For a more thorough description of the physics behind conventional MOSFET operation, the reader is referred to one of the excellent books on the topic [6, 7].

1.1.1 Basic transistor operation

Transistors are three terminal devices used either for on/off switching, in *e.g.* logic applications, or signal amplification. Figure 1.1a presents a MOSFET in common-source configuration where an input signal, V_{IN}=V_{gs}, is applied to the gate terminal and an output signal, I_{OUT}=I_{ds}, is received at the drain terminal. The specific case treated in this thesis is a junction-less MOSFET with n-type doping in the semiconductor channel. A schematic structure is presented in figure 1.1b. If a negative gate voltage, V_{gs}, is applied to the gate, the current from drain-to-source, I_{ds}, is turned off since the electric field created underneath the gate repels electrons and deplete the channel.

Characteristic for the MOSET is the metal-oxide-semiconductor (MOS) structure of the gate where an oxide or dielectric material is inserted between the gate metal and the semiconductor channel. The reduction of the gate-to-source leakage current, I_{gs}, accomplished by the insertion of the oxide is one important reason why the MOSFET is suitable for low-power applications.

The ON-state and OFF-state of an n-type transistor are illustrated by band diagrams in figure 1.1c-f. When a voltage is applied to the gate, the bands of the semiconductor bend and electrons are either accumulated or depleted underneath the gate depending on the bias. For the junction-less channel, accumulation turns the transistor on and depletion turns the transistor off, see figure 1.1c and e. This is opposite to the operation of an inversion mode transistor, exemplified by the ordinary Si MOSFET, which has the opposite doping type in the channel underneath the gate as compared to the source and drain regions of the transistor. Here, the charge in the channel is

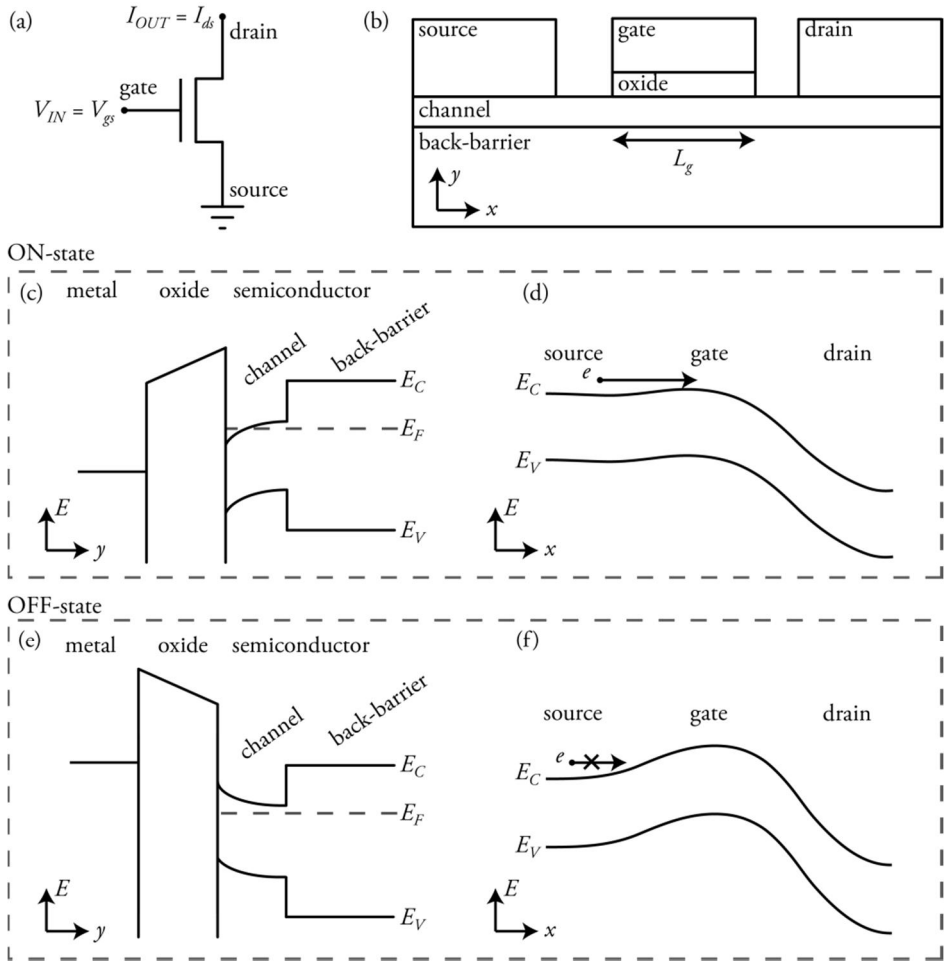


Figure 1.1: A junction-less n-type MOSET illustrated by (a) its circuit representation in common-source configuration, (b) a schematic cross-section where L_g is the gate length, and (c-f) band diagrams perpendicular to the channel and along the channel in the ON and OFF state where E_C is the conduction band edge and E_V is the valence band edge.

inverted to turn the transistor to the ON-state, *i.e.* the bands are bent beyond depletion until the majority charge carriers switch type from electrons to holes or vice versa.

The band diagrams along the channel are illustrated in figure 1.1 d and f. By applying a voltage between drain and source, V_{ds}, electrons move from source to drain in the ON-state. In the OFF-state the electrons are hindered by the energy barrier of the gate and I_{ds} is limited to thermal emission over the barrier.

1.1.2 Output and transfer characteristics

The DC characteristics of a transistor is obtained by either sweeping the gate voltage, V_{gs}, at a constant drain voltage, V_{ds}, which gives the transfer characteristics or sweeping V_{ds} at a constant V_{gs}, which gives the output characteristics. For benchmarking of DC performance, a number of metrics that describe the shape of the curves in the output and transfer characteristic are defined. Experimental output and transfer characteristics from a vertical InAs nanowire MOSFET is used to illustrate the typical appearance of the two plots in figure 1.2.

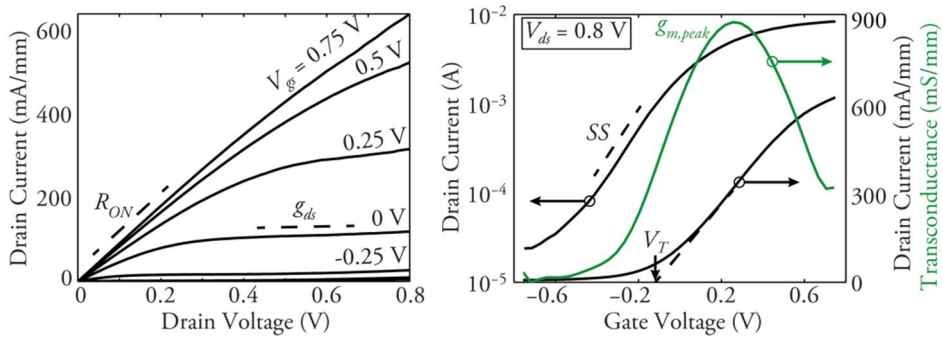


Figure 1.2: Electrical data of a vertical InAs nanowire MOSFET in terms of (a) output characteristic at V_{gs} from -0.75 V to 0.75 V in steps of 0.25 V and (b) transfer characteristics at V_{ds} = 0.8 V.

Output characteristics: The output characteristics measure the V_{ds} dependence on I_{ds}. At low V_{ds}, the channel functions as a resistor with a linear dependence of I_{ds} on V_{ds} and with a resistance controlled by V_{gs}. When V_{ds} is increased I_{ds} saturates as the current becomes limited by the amount of available electrons and their maximum velocity, *i.e.* the saturation velocity, v_{sat}, for short channel devices limited by scattering, and the injection velocity, v_{inj}, in ballistic regime. The amount of available electrons is controlled by V_{gs}.

Drive current: A high I_{ds} in the ON-state, *i.e.* a high normalized drive current, is desirable as this relates to the speed at which the transistor can be operated. I_{ds} is usually normalized to the width of the gate, W, and is expressed in mA/mm.

On-resistance: In the linear region of the output characteristics, I_{ds} is limited by the on-resistance, R_{ON}, which is obtained by the inverse slope dV_{ds}/dI_{ds} in the output characteristics at low V_{ds}, see figure 1.2a. R_{ON} is comprised of resistances in the source and drain, R_s and R_d, and the resistance in the channel, R_{ch} as

$$R_{ON} = R_s + R_d + R_{ch} \approx R_s + R_d . \qquad (1.1)$$

It should be noted that R_{ch} is small for short channel devices at high V_{gs}, and can in this case be omitted in equation 1.1.

Output conductance: The output conductance, g_{ds}, measures how well I_{ds} saturates. Its value is deduced as the slope in the saturation region, *i.e.* dI_{ds}/dV_{ds} at medium or high V_{ds}, see figure 1.2a. A small g_{ds} is desired as this is related to a high voltage gain, A_V. In turn, A_V could be expressed either in terms of differential voltage or conductance as

$$A_V = \delta V_{ds} / \delta V_{gs} = g_m / g_{ds} \qquad (1.2)$$

where g_m is the transconductance which will be defined below when considering the transfer characteristics.

Transfer characteristics: The transfer characteristics measure the V_{gs} dependence of I_{ds}. In figure 1.2b, I_{ds} is plotted both on a linear and a logarithmic scale to illustrate different aspects of the switching from the OFF-state at low V_{gs} to the ON-state at high V_{gs}. Alternatively, the transfer characteristics shows the V_{gs} dependence of the transconductance, g_m.

Transconductance: The definition of the transconductance is $g_m = dI_{ds}/dV_{gs}$, which means that it is a measure of how well the gate is able to control the current in the channel. Furthermore, g_m is an important metric for the speed of the transistor and is often represented by its peak value $g_{m,peak}$.

Threshold voltage: The threshold voltage, V_T, is in this thesis defined as the gate voltage at which the transistor switches between the ON-state and OFF-state. To extract V_T from experimental data, a support line may be drawn which is the tangent of I_{ds} at the V_{gs} corresponding to $g_{m,peak}$. V_T is the voltage where support line intersects with the *x*-axis, see figure 1.2b. Alternatively, V_T could be defined as the voltage at which I_{ON} = 100 nA/µm.

Sub-threshold slope: In the sub-threshold region, *i.e.* below V_T, I_{ds} increase exponentially with V_{gs} due to the energetic distribution of electrons in the conduction band of the semiconductor. Here, I_{ds} is limited by thermionic emission above the energy barrier induced by the gate voltage. The exponential increase is described by the inverse sub-threshold slope, *SS*. *SS* is deduced from the transfer characteristics in the region with the highest slope on the logarithmic scale, see figure 1.2b. For MOSFETs the lowest possible value is *SS* = 60 mV/decade at room temperature. This constrain on the sub-threshold slope for MOSFETs limits the theoretical minimum power consumptions since the power supply voltage cannot be further reduced without deteriorating the ON/OFF ratio. Therefore, alternative devices relying on other physical principles, such as tunnel FETs [8], are being investigated.

Moreover, two other phenomena that are sometimes visible in the output characteristics are impact ionization and band-to-band tunneling. The two can be difficult to distinguish from each other as both are characterized by a rapid increase in I_{ds} at high V_{ds}. In short, impact ionization occurs when the kinetic energy of the electrons is larger than the bandgap. Hence, the kinetic energy of one electron may generate an electron-hole pair. If the charge carriers continue to accelerate they may, in turn, generate even more electrons and holes and start an avalanche of charge carrier that increase I_{ds}. Typically, this occurs between gate and drain in figure 1.1d where the lateral electric field is strongest.

Band-to-band tunneling refers to electrons that tunnel from the valence band underneath the gate to the conduction band at the drain. The probability of tunneling increases exponentially when the voltage difference between gate and drain increases. Both phenomena are especially strong in small bandgap materials, such as InAs and InSb.

1.1.3 High-frequency metrics

For benchmarking of the high-frequency performance, which also called radio frequency (RF) performance, two figures of merits are common: the unity current gain cut-off frequency, f_t, and the maximum oscillation frequency, f_{max}. These frequencies represent the highest frequencies at which the transistor can operate without attenuating the signal between input and output with respect to the current and power, respectively. More specifically, f_t is deduced as the frequency at which the current gain, h_{21}, equals unity. It should be noted that the decrease in current and power gain with frequency is related to increasing currents through the capacitive elements of the transistor with frequency. For an intrinsic transistor, *i.e.* a transistor without any parasitic resistances or parasitic capacitances and with $g_{ds} = 0$, f_t can be calculated by

$$f_t = \frac{g_{mi}}{2\pi \cdot C_{gg,i}} \tag{1.3}$$

where $C_{gg,i}$ is the intrinsic gate capacitance and g_{mi} the intrinsic transconductance.

However, extrinsic performance that includes the parasitic impedances, originating from *e.g.* the contacts, gives a better representation of the real device performance. The addition of parasitic impedances to the intrinsic transistor is illustrated in figure 1.3. For an extrinsic transistor f_t is calculated by

$$\frac{1}{2\pi f_t} = \frac{C_{gg}}{g_{mi}} + \frac{C_{gg}}{g_{mi}}\left(R_s + R_d\right)g_{ds} + \left(R_s + R_d\right)\cdot C_{gd} \qquad (1.4)$$

where C_{gg} is the total gate capacitance and C_{gd} is the total gate-drain capacitance.

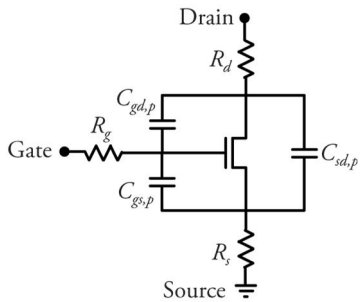


Figure 1.3: An extrinsic MOSFET including the intrinsic device and the parasitic capacitances and resistances. R_s, R_d, and R_g are the source, gate and, drain resistances, while $C_{gs,p}$, $C_{gd,p}$, and $C_{sd,p}$ are the parasitic gate-source, gate-drain, and source-drain capacitances.

For clarity, the following relationships are established where $C_{gd,p}$ is the parasitic gate-drain capacitance, $C_{gs,p}$, is the parasitic gate-source capacitance, and C_{gs} is the total gate-source capacitance:

$$C_{gg} = C_{gg,i} + C_{gd,p} + C_{gs,p} \qquad (1.5)$$

$$C_{gg} = C_{gd} + C_{gs} \qquad (1.6)$$

Furthermore, f_{max} is the frequency at which the Mason's unilateral power gain, U, equals unity. Here, U represents the power gain if a lossless passive feed-back network is added that gives complete reverse isolation. This means that any possible feed-back from the drain terminal to the gate terminal is not included when extracting U. The amount of feed-back sets the stability of the transistor and an alternative way to deduce f_{max} is to study the maximal stable gain (MSG) and maximal available power gain (MAG). In this case, MSG is used for frequencies where the device is potentially unstable and MAG for frequencies where the device is unconditionally stable. Both U and MSG/MAG give the same f_{max}. If f_{max} is instead calculated from simulated or extracted parameters, the following equation is used

$$f_{\max} = \sqrt{\frac{f_t}{8\pi \cdot R_g C_{gd}\left[1+\left(\frac{2\pi f_t}{C_{gd}}\right)\Psi\right]}} \qquad (1.7a)$$

where

$$\Psi = \left(R_s + R_d\right)\frac{C_{gg}^2 g_{ds}^2}{g_m^2} + \left(R_s + R_d\right)\frac{C_{gg} C_{gd} g_{ds}}{g_m} + \frac{C_{gg}^2 g_{ds}}{g_m^2} \qquad (1.7b)$$

and where R_g is the gate resistance. The second term in the square parenthesis in equation 1.7a is often small, provided that g_{ds} is small, and neglecting this term gives a simplified equation for f_{max},

$$f_{\max} \approx \sqrt{\frac{f_t}{8\pi \cdot R_g C_{gd}}}\,. \qquad (1.8)$$

More details on measurements and modeling of the high-frequency performance are presented in chapter 3.2.

1.2 III-V Semiconductors

III-V semiconductors (III-Vs) are compounds of elements in what was previously known as group III and V, and what is today known as group 13 and 15, of the periodic table. These materials have caught a lot of attention throughout the history of transistors due to their, in many cases, advantageous transport properties compared to Si. Today, III-V transistors such as GaAs and InGaAs metal-semiconductor field-effect transistors (MESFETs), hetero-junction bipolar transistors (HBT), and high electron mobility transistors (HEMTs) are widely used in RF systems and for wireless communication. Furthermore, III-V transistors demonstrate impressive RF performance; the record for f_t is held by a InP/InGaAs HBT with f_t = 765 GHz [9] and the record for f_{max} by a InGaAs/InP HEMTs with f_{max} above 1 THz [10].

One important parameter, when it comes to the transport properties, is the mobility, μ. In table 1.1, the electron mobility, μ_e, and hole mobility, μ_h, are displayed for a few semiconductors. The highest μ_e is found for InSb, InAs and InGaAs, which makes these materials suitable for n-type MOSFETs. The strongest candidates for p-type MOSFETs, with respect to μ_h, are Ge and GaSb. The general trend is that a high

mobility is associated with a narrow bandgap due to the small effective mass of the carriers.

In addition to the traditional semiconductors, two-dimensional materials, such as graphene, have received tremendous interest recent years. Graphene has very competitive mobilities in the order of about 70 000 $cm^2V^{-1}s^{-1}$ for both electrons and holes [11], but is inherently different in many ways compared to traditional semiconductors. For instance, graphene has the disadvantage that it lacks a bandgap, E_g, which leads to a high g_{ds} and, hence, a low f_{max} as compared to f_t [12]. Why f_{max} is reduced by a high g_{ds} can be understood by revisiting equation 1.7.

	E_g (eV)	μ_e ($cm^2V^{-1}s^{-1}$)	μ_p ($cm^2V^{-1}s^{-1}$)	m_e/m_0	a_0 (Å)
Si	1.12	1 400	450	0.36	5.43
Ge	0.66	3 900	1 900	0.22	5.66
GaAs	1.42	8 500	400	0.063	5.65
$In_{0.53}Ga_{0.47}As$	0.74	12 000	300	0.041	5.87
InAs	0.35	40 000	500	0.023	6.06
InP	1.34	5 400	200	0.08	5.87
InSb	0.17	77 000	850	0.014	6.48
GaSb	0.73	3 000	1 000	0.041	6.10

Table 1.1: Selected IV and III-V semiconductor material parameters, including the bandgap, E_g,, the mobilities μ_e and μ_h, the lattice constant , a_0, and the effective mass used for calculations of density of states, m_e, [13]. m_e is normalized to the electron rest mass, $m_0 = 9.11 \cdot 10^{-30}$ kg.

The choice of InAs, in this thesis, is a trade-off between high μ_e and sufficient E_g. Furthermore, ohmic contacts are easily realized on InAs due to pinning of the Fermi-level in the conduction band.

Another important transport parameter is the injection velocity, v_{inj}, which is the carrier velocity at the virtual source, *i.e.* at the highest point of the conduction band for electrons as shown in figure 1.1d and f. As the gate length is scaled down, the transistors are gradually entering the ballistic regime where the length of the channel is shorter than the mean free path of the charge carriers and no scattering events occur under the gate. In this regime, I_{ON} is independent of the gate length and proportional to v_{inj}. Measurements on InAs and InGaAs HEMTs, has demonstrated v_{inj} of about $2.8 \cdot 10^7$ cm^2s^{-1} and $2.3 \cdot 10^7$ cm^2s^{-1}, respectively, at $V_{ds} = 0.5$ V and $L_g = 100$ nm. For Si MOSFETs, the values are substantially lower with $v_{inj} \approx 0.9 \cdot 10^7$ cm^2s^{-1} at $L_g = 100$ nm

and V_{ds} = 1.1-1.3 V [14]. It should be noted that V_{ds} is more than twice as high for the Si MOSFET in this case.

As the drive current, I_{ON}, is ideally proportional to v_{inj} at a certain drive voltage, V_{DD}, an improved v_{inj} could either give a higher I_{ON} at a constant V_{DD}, which increase the transistor speed, or V_{DD} could be reduced while the same I_{ON} is maintained. For logic applications, the latter means that the power consumption can be lowered without compromising the transistor speed. This is the main reason why III-V MOSFETs are considered for digital applications. However, there are many challenges associated with III-V CMOS including the lack of a high performance p-type MOSFET, the difficulties to integrate the technology on Si substrates and the difficulty to achieve high quality integration of gate dielectric on III-Vs.

Ultimately, there is a window of opportunity for III-V MOSFETs in logic applications. In the ballistic regime, the I_{ON} could still be improved by scaling of *e.g.* the gate oxide thickness, which increases the oxide capacitance, C_{ox}, and hence improves the control of charge in the channel, Q, according to

$$Q = C_{ox}\left(v_{gs} - \varphi_S\right) \qquad (1.9)$$

where v_{gs}-φ_s is the voltage drop over C_{ox}. However, when the quantum capacitance limit is reached, scaling of the gate oxide thickness can no longer be utilized since the oxide capacitance, C_{ox}, becomes much larger than the semiconductor capacitance, C_S and, hence, only a small fraction of the gate voltage drops over C_{ox}. The quantum capacitance limit is material dependent as the size of C_S is set by the density of states for given geometry, which is in turn set by the effective mass. As shown in table 1.1, the effective electron mass is much larger for Si than for InAs and InGaAs. This means that Si could become advantages again for the extremely scaled MOSFETs. Ultimately, I_{ON} becomes a trade-off between v_{inj} and the density of states.

1.3 Non-Planar Transistor Geometries

Historically, scaling of MOSFETs followed the principle of keeping the electrical fields in the device constant and certain scaling rules were stipulated on how to shrink the dimensions, reduce the drive voltage, and modify the doping [15]. The driving force was the same as today; to improve the performance, reduce the cost per device and increase the packing density. The single most important enabler was the continually improved resolution of lithographic tools.

As the dimensions are scaled down, undesirable short channel effects (SCE), such as drain induced barrier lowering (DIBL) and poor subthreshold slope, have become an increasingly concern. The SCE reflects the difficulty to retain electrostatic control of

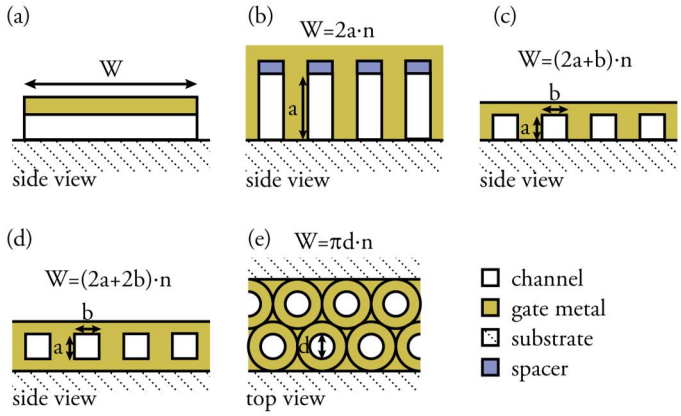


Figure 1.4: Different gate geometries seen from the cross-section of the channel. The gate width is indicated. (a) planar, (b) double-gate, (c) tri-gate, (d) lateral gate-all-around, and (e) vertical gate-all-around. In this schematic, the gate oxide between the channel and the gate metal is omitted.

the channel as the gate length, L_g, is reduced. SCE can, however, be suppressed by implementing non-planar transistor geometries where the transistor channel is gated from more than one direction.

Among the suggested geometries are double-gate (DG) [16], tri-gate and gate-all-around (GAA), illustrated in figure 1.4. Out of these, GAA gives the best electrostatic control as the ratio between gate width, W, and cross-sectional channel area is higher. In a comparison between DG and GAA, it is concluded that the minimum L_g compared to the thickness of the channel is 40% smaller for GAA than for DG [17]. This also means that at a given L_g, the channel diameter and oxide thickness can be larger in GAA geometries for the same transistor characteristics.

Using the definition that nanowires are rod-shaped crystals, which could be several micrometers long but must have a diameter below 100 nm, implies that nanowires are already used in commercial CMOS circuits as the tri-gate geometry is already employed by Intel in the 22 nm node [18]. Furthermore, InGaAs and InAs MOSFETs with tri-gate geometry have recently demonstrated excellent performance [19]. By removing the substrate under the tri-gate, as shown in figure 1.4d, it can be converted into the lateral GAA geometry. Also for this geometry, promising results have been reported [20, 21].

The vertical GAA geometry requires a vertical nanowire or pillar. These could either be epitaxially grown, as in this thesis, or etched from a bulk material. Also for this geometry, promising MOSFET data has been published both for Si [22] and III-Vs [23-25]. The main advantages with the vertical nanowire transistors compared to lateral nanowires are the potential for smaller device footprint, due to the vertical alignment of the contacts on top of each other, and the improved conditions for heteroepitaxy in the case of epitaxially grown nanowires. Due to the small nanowire

diameter, strain caused by lattice mismatch is easier released without causing defects. Heteroepitaxy could include both the integration of high quality III-V material on Si substrates [26, 27], and radial or axial heterostructures in the nanowire [28-30].

1.4 Applications of Vertical InAs Nanowire MOSFETs

The vertical InAs nanowire MOSFET combines the advantages transport properties of InAs and the improved electrostatic control of GAA geometries, which makes it suitable for high-frequency low-power applications. These applications could be either analog or digital.

For digital applications Si CMOS have dominated the market for several decades due to the excellent scalability and low power consumption. III-V CMOS, or CMOS with a III-V n-type MOSFET and a Ge p-type MOSFET, could potentially replace Si CMOS for logic applications. It is speculated that III-V CMOS might be used already at the ~10 nm node with the first products anticipated in 2018-2020 [31]. However, the requirements are very high; it has to outperform Si CMOS with a performance improvement of at least 30-50% and it has to be scalable for at least one more technology node. Furthermore, the manufacturing must be cost effective and reliable to a degree that has not yet been presented [32]. It is likely that a tri-gate or lateral GAA geometry would be used if III-Vs are used in future CMOS since the tri-gate geometry is implemented in the 22 nm Si CMOS node.

To accomplish III-V CMOS in vertical nanowires would require even more technology development. Recently, the first III-V CMOS inverter in a single nanowire was demonstrated [33], but with much room for improvement both in performance and design. Still, digital applications should not be excluded for the vertical InAs nanowire MOSFETs. The vertical geometry could potentially give a smaller footprint as the contacts are aligned on top of each other, which is attractive for extreme scaling. The vertical nanowires are also advantageous in the heterogeneous integration of III-Vs on Si substrates.

Closer at hand are the use of vertical InAs nanowire MOSFETs in analog applications. This market is more diverse and III-V technologies, such as HEMTs, MESFETs and HBTs, are important due to the excellent high frequency performance. The InAs nanowire MOSFET could find a niche by targeting low-power analog application.

1.5 High-κ Dielectrics on III-Vs

1.5.1 High-κ versus native oxide

A high quality gate dielectric is a key to good device performance. It is even so that the high quality native oxide of Si was one of the main reasons why Si MOSFETs became successful in the first place. However, as the oxide thickness is scaled down below a few nanometers, tunneling currents through the oxide becomes an increasing problem. This leakage current leads to an increased power consumption of the device.

A possibility to overcome this has been provided by the development of atomic layer deposition (ALD) where high-permittivity (high-κ) gate dielectric of high quality can be deposited. Compared to SiO_2, the high-κ dielectric has a larger physical thickness for the same oxide capacitance, which is expressed by

$$C_{ox} = \frac{\kappa \varepsilon_0 W L_g}{t_{ox}} \qquad (1.10)$$

where κ is the relative permittivity, ε_0 is the permittivity in vacuum, W is the gate width, and t_{ox} is the physical oxide thickness. For comparison, κ values of a few commonly used dielectrics are listed in table 1.2 together with the bandgap and the conduction band offset to InAs, $\Delta E_{c,InAs}$.

The electrical thickness is commonly characterized by the equivalent oxide thickness (EOT), which is the corresponding thickness of a SiO_2 film giving the same C_{ox}. This measure, which has become a standard, is used also for III-V semiconductors even though SiO_2 is not a natural choice for these materials. Furthermore, the quality of native oxides on III-Vs is poor and cannot be used. Hence, high-κ is widely used in III-V MOSFETs and EOT down to 1 nm with low gate leakage currents has been demonstrated on InAs using HfO_2 [34].

	κ	E_g (eV)	$\Delta E_{c,InAs}$ (eV)
SiO_2	3.9	9	4.1
Si_3N_4	7	5.3	2.7
Al_2O_3	9	8.8	3.6
HfO_2	25	5.8	2.5

Table 1.2: Material properties of a few selected dielectric materials [35, 36].

1.5.2 Interface traps and border traps

Interface traps and border traps are defect-induced states in the gate dielectric of a MOS structure that may trap charge carriers. The interface traps are located at the dielectric-semiconductor interface, while the border traps are distributed inside the dielectric. Their distribution in space and energy is schematically illustrated for an n-type MOSFET in figure 1.5. A third kind of charge traps are defects in the oxide that might be charged but cannot trap/de-trap charge carriers under normal operation. These are referred to as fixed oxide charge. The fixed oxide charge may shift the threshold voltage of the MOSFET and increase the scattering, but have little effect on the characteristics apart for that.

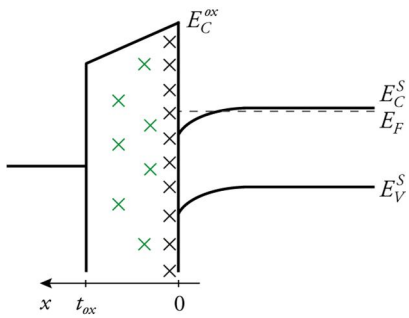


Figure 1.5: Schematic of the MOS structure including border traps (green crosses) and interface traps (gray crosses).

On the other hand, mainly interface traps, but also border traps, have a profound effect on the characteristics of the MOSFET including the subthreshold slope and the extrinsic transconductance. This is especially true for III-V MOSFETs since they typically suffer from very high densities of interface traps, D_{it}, and border traps, N_{bt}, typically in the order of 10^{12}-10^{13} $eV^{-1}cm^{-2}$ and 10^{18}-10^{19} $eV^{-1}cm^{-3}$, respectively [37-40].

In the literature, there is some confusion on the nomenclature that should be used to describe these defect-induced states, leading to that both interface traps and border traps may be reported in term of D_{it} [41]. Even though the two types of traps might sometimes be difficult to distinguish in measurements, their differences should be considered in the theoretical description

Some examples of defects are dangling bonds, semiconductor dimer pairs, oxygen interstitials, and oxygen vacancies [42]. In the interface region, which is in the order of 1 Å, defects are related both to atoms in the semiconductor and atoms in the dielectric, while, further into the dielectric, defects are related only to atoms in the dielectric. One reason to why high-κ integration on III-Vs is challenging is the higher complexity of an III-V-high-κ interface compared to a Si-SiO_2 interface. For example,

an InGaAs-HfO_2 interface has five different elements (In, Ga, As, Hf, and O) while a Si-SiO_2 interface has two (Si, and O). Further details on the modeling of traps are presented in chapter 4 together with a method to characterize traps with a focus on border traps.

2. Device Fabrication

Device fabrication based on vertical nanowires is a novel field with plenty of opportunities for innovation and often with a substantial need of process optimization. The general layout of a vertical nanowire MOSFET is illustrated in figure 2.1. In addition to the three contacts placed along the nanowires, it also constitutes of spacers to avoid short circuiting and control the parasitic capacitances.

Early work on vertical nanowire MOSFETs, *i.e.* before 2010, has mainly focused on process development and DC performance and did not include any reports on high-frequency performance [24, 43-47]. In this thesis the high-frequency performance has been the main design target. However, DC performance, reproducibility, yield, and scalability have also been important in the design.

In this chapter, the key enablers of our process, *i.e.* nanowire growth, gate-all-around contacts, and an RF compatible design are described. This is followed by a discussion on the development of the process scheme over time, where three generations of the vertical InAs nanowire MOSFET are presented. Furthermore, a detailed process step recipe can be found in Appendix.

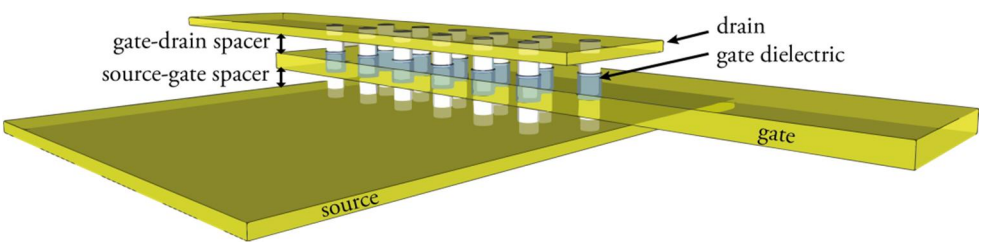


Figure 2.1: Schematic layout of a vertical nanowire MOSFET.

2.1 Nanowire Growth

The nanowires in this thesis are grown from gold particles on a semiconductor surface by the vapor-liquid-solid (VLS) growth mechanism [48, 49]. This is achieved by tuning the growth conditions so that epitaxial growth aided by the gold particle is favorable while other types of growth are suppressed. In the process, the sample is exposed to precursors in the gas phase which contains the group III and V elements of the desired compound; if a precursor is adsorbed at the surface of the sample it will move around diffusively after which it will either incorporate in one of the gold particles or desorb and return to the gas phase. The supply of material to the gold particle leads to a high super-saturation compared to the crystal resulting in crystal nucleation at the gold-semiconductor interface. After nucleation, the nanowire will grow by lifting the Au particle from the surface and continuously adding material underneath.

The technique that is used is metal-organic vapor-phase-epitaxy (MOVPE) which is also referred to as metal-organic chemical-vapor-deposition (MOCVD). The precursors used for InAs nanowires are trimethylindium (TMIn) and arsine (AsH_3). In addition, the nanowires are n-type doped by adding tetraethyltin (TESn).

To achieve ordered arrays the catalyst gold particles are defined by electron beam lithography (EBL). The exposed pattern is transferred from the e-beam resist to a thin gold film by evaporation and lift-off. The dot exposure dose and the Au film thickness sets the diameter of the nanowire, which typically ranges from 20 to 65 nm. Typical nanowire arrays fabricated by this method are depicted in figure 2.2.

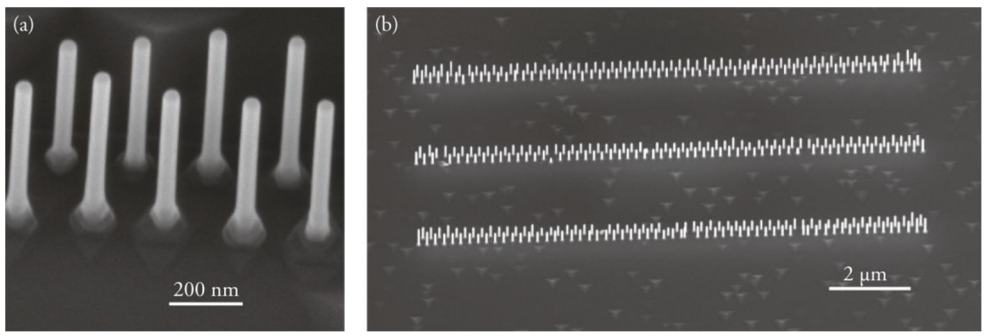


Figure 2.2: 30° tilted SEM image of nanowire arrays covered with high-κ dielectric film.

2.2 Gate-All-Around

In the vertical geometry, the gate length, L_g, is not set by lithography. Instead L_g is set by the film thickness of an anisotropically deposited film or by partial sidewall etching of a conformal film. The gate-all-around contacts, or wrap-gates, used in this thesis are fabricated by sputtering of a W film resulting in a film thickness on the nanowire which is about 1/3 of the thickness on the planar surface. L_g is set by spinning of a resist film and thinning it down to the desired thickness. The metal on the upper part of the nanowires that are not protected by the resist is subsequently etched by dry etching. The process is illustrated in figure 2.3 and is preferred over evaporated gates due to the higher yield and reproducibility. The main drawback is that scaling of L_g is limited by the conformity of the resist layer. For very short electrodes, such as gate length below 20 nm, the process needs to be modified or replaced.

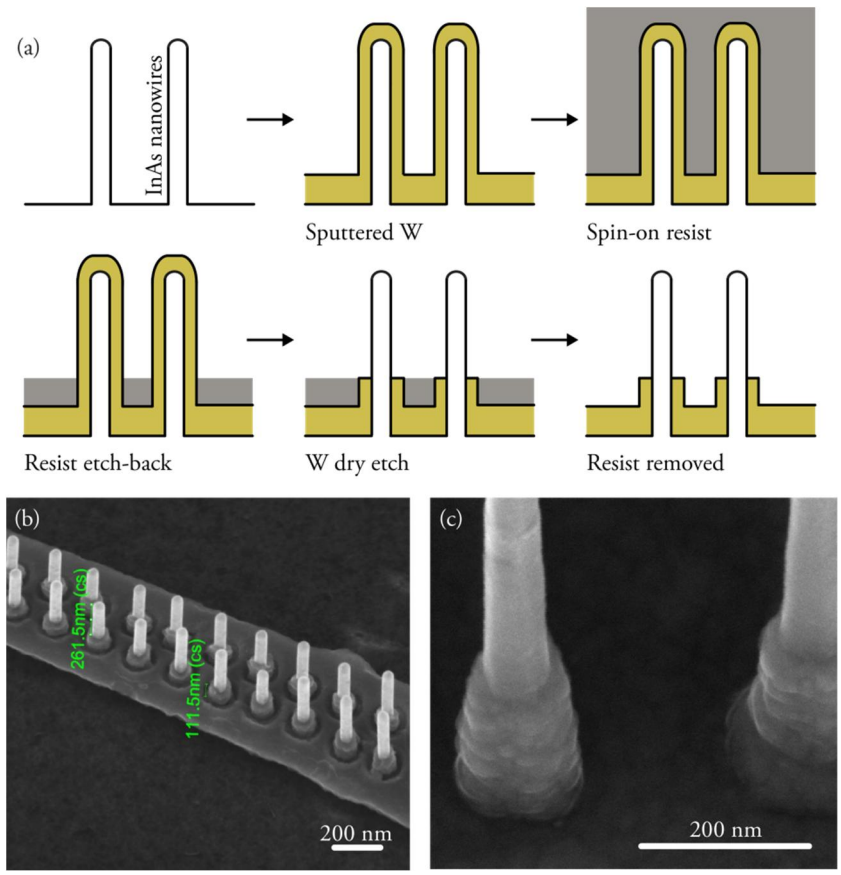


Figure 2.3: Cross-sectional schematic of the wrap-contact formation in (a) and 30° tilted SEM image of wrap-contacts represented by a W gate-all-around finger contact in (b) and an Al/W wrap-source contact covered with a high-κ dielectric in (c).

2.3 RF Compatible Design

Reliable RF characterization requires good impedance matching to the measurement equipment, which is normally calibrated to 50 Ω. A transistor based on a single nanowire has impedance in the order of kΩ, which is too high. Hence, the impedance is lowered using arrays with 20-600 nanowires in parallel in a single device.

To minimize losses in the contact pads at high frequency, a coplanar waveguide (CPW) layout is used where the width, *w*, of the gate and drain pads are separated from the ground plane, *i.e.* the source pads, by the distance *s*. A ratio of *w*/*s* = 1.5 is used. Micrographs of the completed transistors illustrate the layout of the probing pads in figure 2.4.

Furthermore, device isolation is a key for reliable RF measurements. Hence, the transistors are preferably placed on semi-insulating (S.I.) or highly resistive substrates. If a conductive substrate is used the 50-Ω-impedance matching will deteriorate at high frequencies due to the capacitive load between the probing pads and the substrate. This would also complicate the de-embedding of the transistor cell, which is described further in chapter 3.

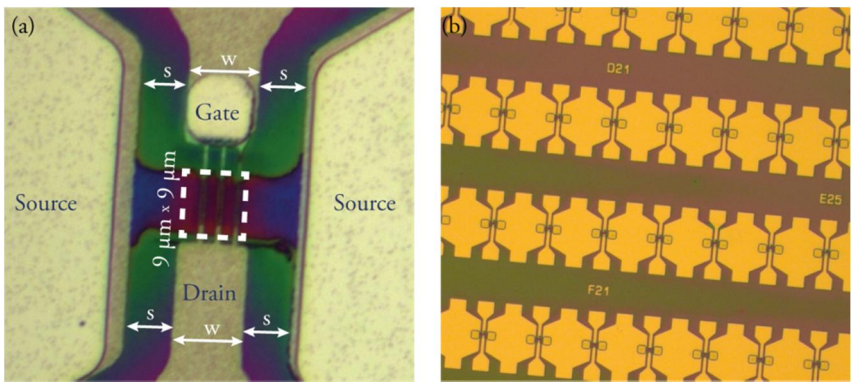


Figure 2.4: Micrographs of completed transistors using a 50-Ω coplanar waveguide with a close-up showing a 9 μm·9 μm transistor cell in (a) and an overview with in total 27 transistors in (b).

2.4 Three Generations of Vertical InAs Nanowire MOSFETs

Since the first vertical nanowire MOSFET was reported from Lund University in 2006, new materials and geometries have been tested for almost every part of the device. The process development over time is summarized in figure 2.5.

One of the largest changes is the replacement of the conductive InAs substrate to semi-insulating (S.I. InP) substrate and later to highly resistive Si substrate, which also required new source contacts to be developed. The epitaxial structures formed on the three substrates are schematically illustrated in figure 2.6. How the vertical InAs nanowire MOSFETs were realized on the new substrates and how a vertical structure with low parasitic capacitance was implemented is presented below in terms of three generations of the vertical InAs nanowire MOSFET.

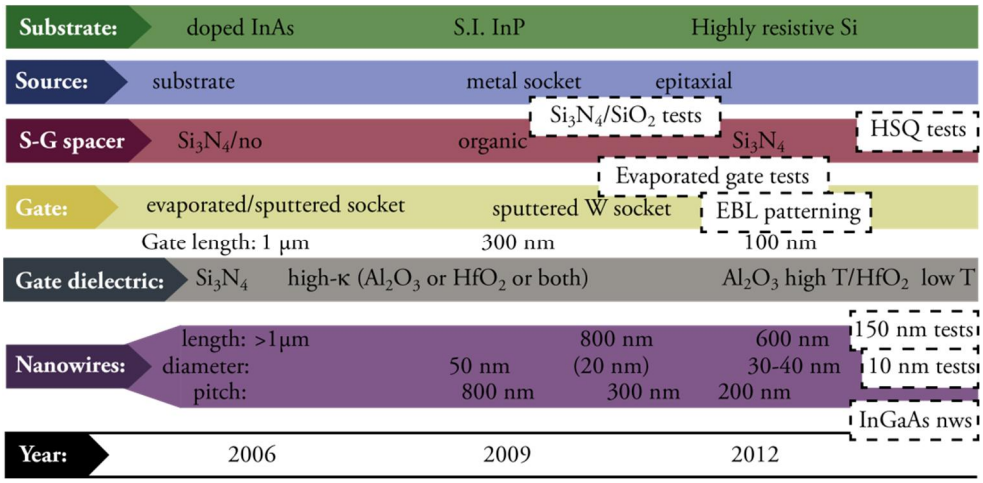


Figure 2.5: Timeline showing the development of the process scheme. White boxes indicate tests.

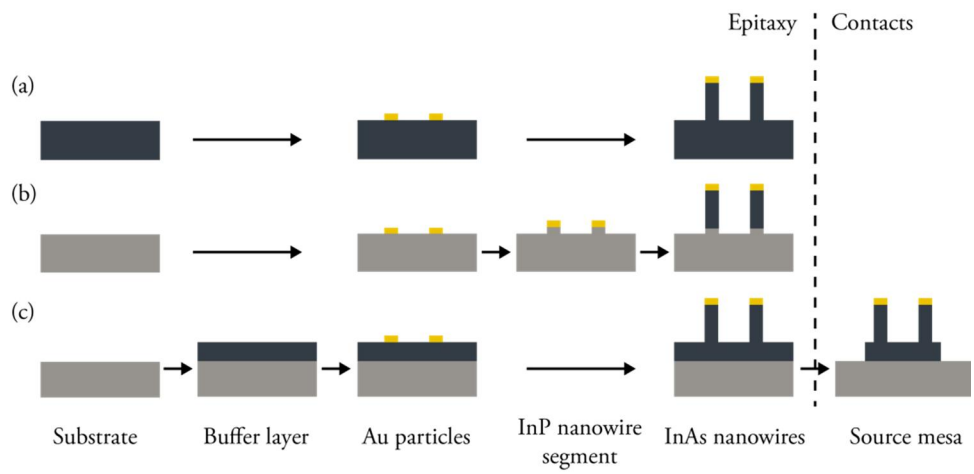


Figure 2.6: Schematic of the processing of three different epitaxial structures used for vertical InAs nanowire MOSFETs with (a) conducting InAs substrate, (b) semi-insulating InP substrate and, (c) highly resistive Si substrate.

2.4.1 Generation 1 - on semi-insulating InP substrate

In the first generation of high-frequency InAs nanowire MOSFETs, *i.e.* Paper I, the nanowires were integrated on S.I. InP (111). To achieve homogenous nanowire nucleation, a short InP nanowire segment was first grown, on top of which the InAs nanowire were heterogeneously integrated [49]. The resulting epitaxial structure is schematically illustrated in figure 2.6b. The transistors fabricated with these nanowires are presented in figure 2.7 by a schematic cross-section of a device and a cross-sectional SEM image of a reference sample.

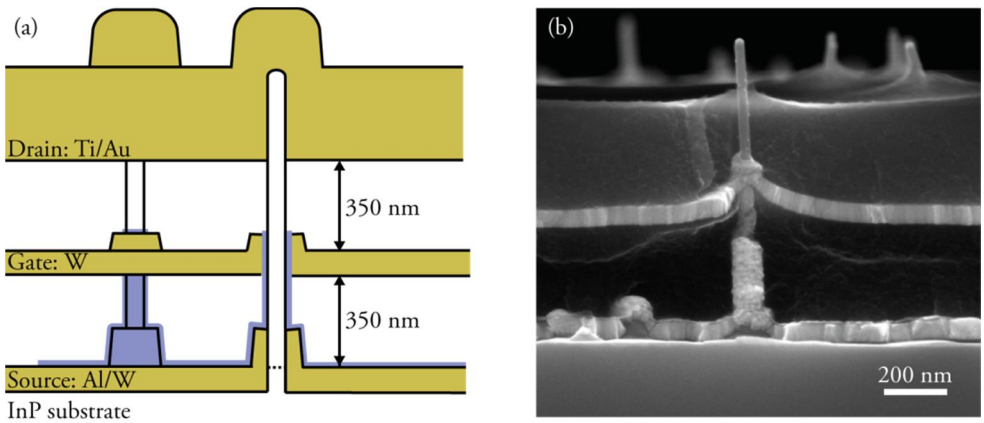


Figure 2.7: (a) Schematics of the transistor cross-section on InP substrate with metal source socket and resist spacers, and (b) cross-sectional SEM micrograph of the same structure on a reference sample with randomly distributed nanowires. The drain metal is not deposited in (b).

Previously, the InAs substrate was used as a source contact, but the use of a S.I. InP substrate requires a source contact formation at the lower part of the nanowires. A sputtered metal wrap-contact was formed as described in Ch. 2.2. The contact length had to be sufficient to achieve a good contact to the InAs part of the nanowire. For a 50-100 nm InP segment, a wrap-contact length of about 200 nm was used. A 10/60 nm Al/W metal film was used where the thin Al film was added to protect the nanowires from potential surface damage caused by the impingement of ions during the W dry-etch. Preserving a good surface was especially important as the Al_2O_3 gate dielectric was deposited after source formation.

To avoid leakage between source and gate, an organic spacer, which covered the source metal socket completely, was formed in etched-back S1818. When using etched-back resists, height differences occur on the sample both locally around structures and globally across the sample. Figure 2.8 exemplifies the color variations of the resist, which can be a good measure of the surface topology.

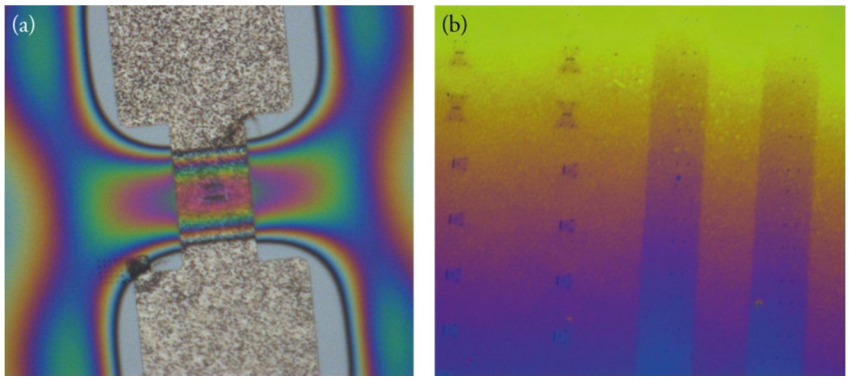


Figure 2.8: Color variations of etched-back S1800 series resist due to height differences. In (a) the resist is used as source-gate spacer and the openings are source vias. In (b) the resist is used for etch-back of a Si_3N_4 source-gate spacer on a sample with source pad pattern in the high-κ only. The height variations are approximately in the order of 200 nm in (a) and 50 nm in (b).

The device was completed by an Al/W wrap-gate, an organic gate-drain spacer and sputtered Ti/Au drain contact.

In conclusion, the use of S.I. InP substrates made the design RF compatible; however, the wafers are expensive, brittle and the size is limited to 4 inch. And, from a device fabrication point of view, this approach has an increased complexity as it requires a wrap-contact at the source.

2.4.2 Generation 2 - on highly resistive Si substrates

In the second generation of high-frequency InAs nanowire MOSFETs, *i.e.* Paper II-IV, InAs nanowires were instead integrated on highly resistive Si (111) substrates, which improves the potential of the technology in terms of large scale applications. The heterogeneous integration was realized by a buffer layer technique where a thin film of InAs with a lattice mismatch of about 11% to Si was first grown [50]. Sufficient crystal quality was achieved by cycling growth of nucleation layers at low temperature with annealing at high temperature during the individual steps of the growth. On top of the InAs buffer layer, InAs nanowires were grown as schematically illustrated in figure 2.6. Here, device isolation was achieved in a later process step by etching mesa structures the InAs film. The InAs mesas also constitute the source contacts in these devices. The complete device is presented in figure 2.9 by a schematic cross-section and cross-sectional SEM image of a reference sample.

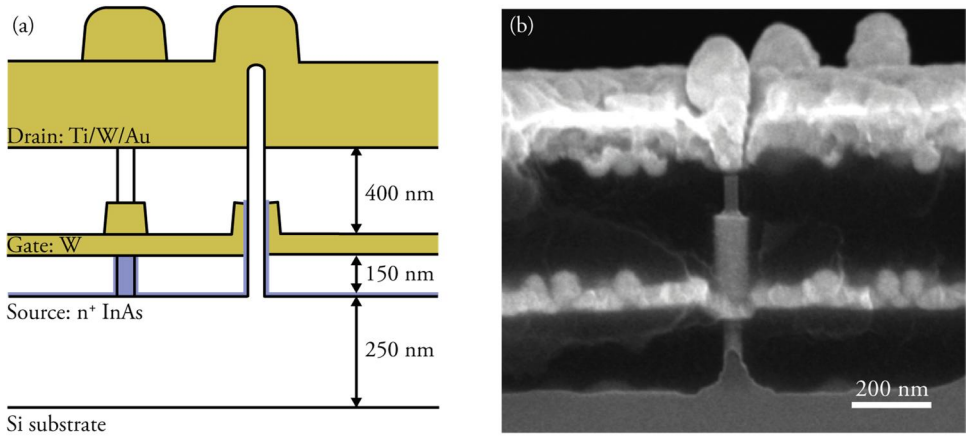


Figure 2.9: (a) Schematics of the transistor cross-section on Si substrate using the InAs buffer layer as a source contact and with resist spacers, and (b) cross-sectional SEM micrograph of the same structure on a reference sample with randomly distributed nanowires.

In paper III, the diameter and position control of the nanowires was targeted and the possibility of growing InAs nanowire arrays on 2 inch Si wafers in a controlled fashion was demonstrated. SEM inspection of the wafer revealed a nanowire growth yield of 100%. However, a diameter variation of 15 nm was observed, although having the same nominal dose, when comparing the first and the last nanowires according to the order of exposure in the EBL. This was most likely due to drift in the beam current of the EBL during the 10 h exposure time. For a single array the diameter variation around the nominal nanowire diameter was 6 nm.

The vertical process requires the high-κ gate dielectric to be deposited quite early in the process. In the first generation, high-κ was deposited after socket formation while, in the second generation, the high- κ was deposited right after growth and exposure time in air was kept as short as possible. Furthermore, post deposition annealing (PDA) in forming gas was employed in the second generation of transistors to improve the quality of the high-κ integration. The high-κ dielectrics that have been used are Al_2O_3 and HfO_2 deposited by atomic layer deposition (ALD). Al_2O_3 is etched faster and believed to give a better interface to the semiconductor, while HfO_2 has a higher permittivity, *i.e.* higher κ value.

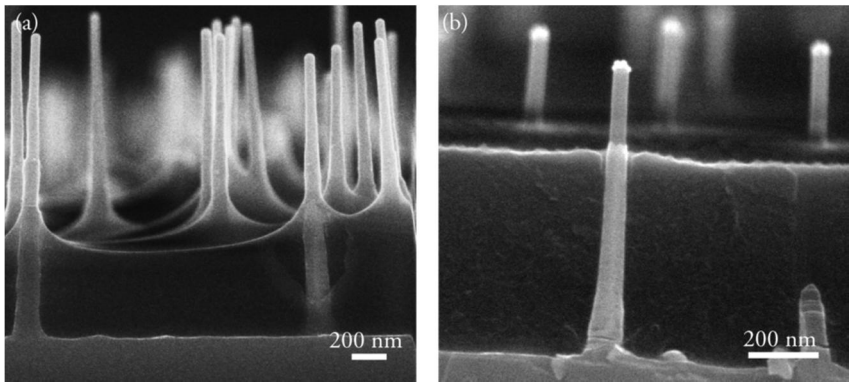


Figure 2.10: S1800 series resist profiles on nanowire reference samples (a) if permanently baked at 200°C after thinning down the resist thickness, and (b)) if permanently baked at 200°C before thinning down the resist thickness. In (b) the high-κ dielectric is removed from the top of the nanowire using the resist as an etch mask.

The source-gate spacer, gate, and gate-drain spacer are formed as in the previous generation; however, it was noted that permanent baking of the resist before defining the thickness is preferable as this gives a more planar profile compared to etching back first and baking afterwards. This is seen in the cross-sectional SEM images in 2.10 as well as in figure 2.7b and 2.9b.

In the first generation, the aggressive Au wet etch when patterning the drain contact was problematic since InAs nanowire close to the edge of the drain pad were also etched. To avoid this W was inserted in the metal stack giving a Ti/W/Au top metal layer. The W film protected the nanowires during Au etch and was removed by subsequent dry etching.

2.4.3 Generation 3 - with reduced metal overlap

In the third generation of high-frequency InAs nanowire MOSFETs, *i.e.* Paper VII, the RF performance was boosted by reducing the excess metal overlap and, hence, the parasitic gate capacitance, $C_{gg,p}$. Figure 2.11a presents a schematic of the device, while figure 2.11b shows a cross-section of a device enabled by focused ion beam (FIB) milling.

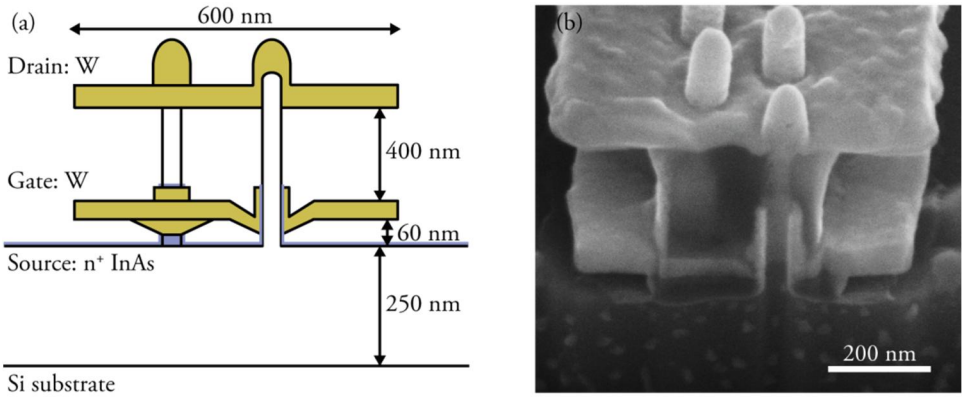


Figure 2.11: (a) Schematics of the transistor cross-section using finger gate and drain contacts both with a width of 600 nm, and with Si_3N_4 source-gate spacer, and (b) 52° tilted SEM micrograph of a device cross-section cut by focused ion beam (FIB).

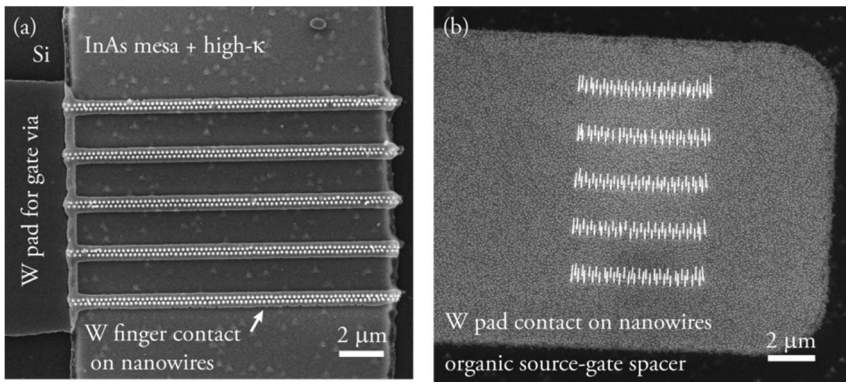


Figure 2.12: (a) Top view SEM image of the new design with finger gate contacts on nanowire double rows and, (b) 30° tilted SEM image of the old design using a large pad gate contact.

The metal overlap was reduced by replacing the pad contacts, which was used in previous publications, with finger contacts formed by EBL and dry etching. The new and old contact designs are compared in figure 2.12. In the new design, W contacts were used both for gate and drain. The EBL pattern was automatically aligned to the array using markers formed by vertical nanowires. For the gate contact shown in figure 2.12a, the mean width of the fingers is 670 nm with a standard derivation of 28 nm. The mean shift from the center is 29 nm. Furthermore, figure 2.13 depicts the complete transistor layout both for a device with finger contacts and for a reference device with pad contacts.

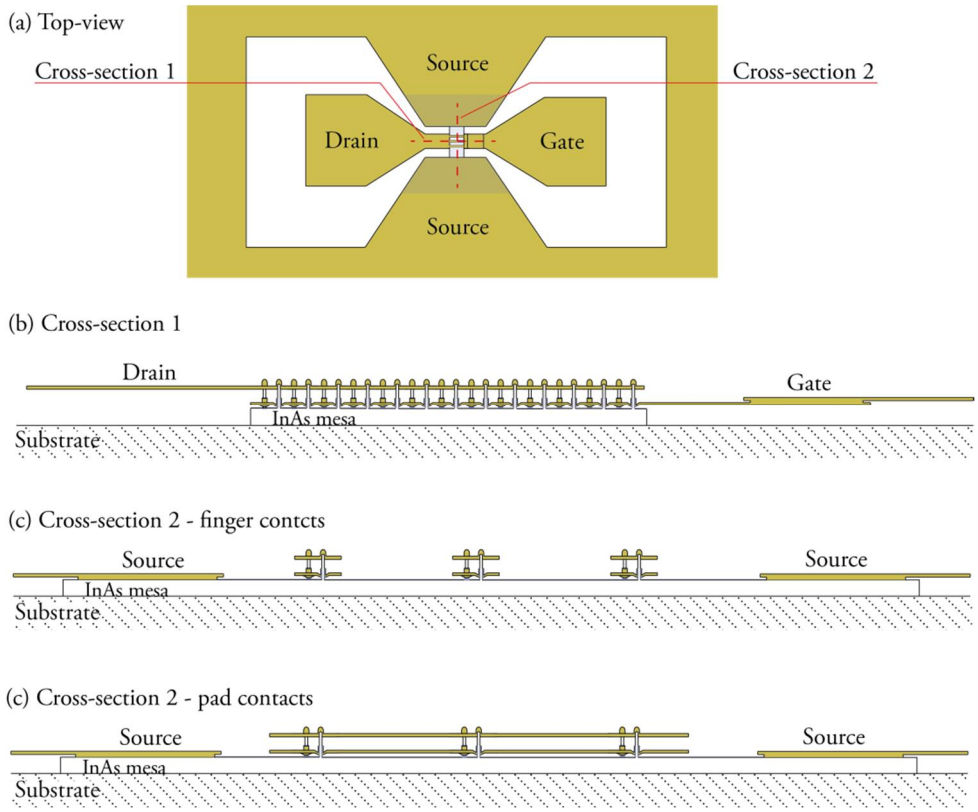


Figure 2.13: Illustration of the layout including (a) an overview, (b) gate-to-drain cross-section, (c) source-to-source cross-section using finger contacts, and (d) source-to-source cross-section using pad contacts. The spacers are omitted for clarity.

It should be noted that the nanowires do not need to be fully covered by resist when forming the finger contacts. The used resist was PMMA 950 A4, which has a thickness of about 300 nm. For the employed exposure settings, back scattering gives a large undercut in the resist profile for thicker resists, such as PMMA 950 A8, which has a nominal thickness of about 1 μm. The resist profiles in the two cases are depicted in figure 2.14. The resist profile in figure 2.14b is not suitable for finger contacts, but could possibly be used as a mask when etching at the lower part of the nanowire.

In future generations of the vertical InAs nanowire MOSFET, the parasitic capacitance could be reduced even more by scaling the width of the finger contacts. The positive effect is enhanced if the spacing between the nanowires is reduced as this will increase the screening of electric field between the contacts by the nanowires and, hence, reduce the capacitance [51]. However, increased resistance in the fingers must

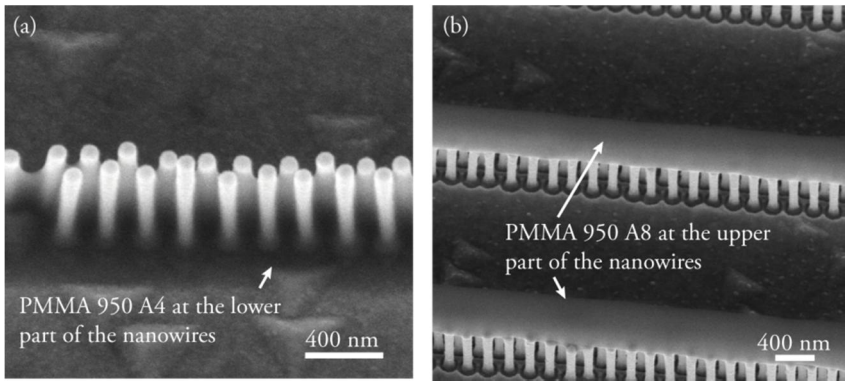


Figure 2.14: 30° tilted SEM images of fingers formed by EBL in two types of resist: (a) PMMA 950 A4, which was used the finger contacts formation, with a spin-on thickness of 300 nm, and (b) PMMA 950 A8 with a spin-on thickness of about 1 μm.

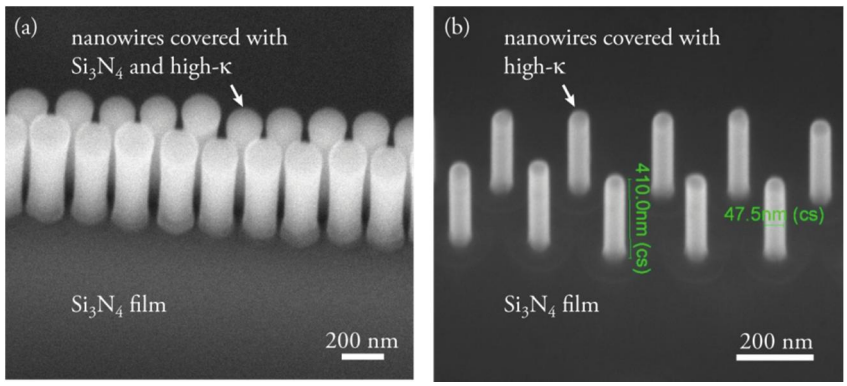


Figure 2.15: Si_3N_4 spacer (a) before and (b) after etch-back. 30° tilted SEM images.

be avoided either by shortening the fingers or by adding more metal in the vertical direction.

In a broader perspective, it is not a reduction of $C_{gg,p}$ that boost the RF performance, but an improved g_m/C_{gg} ratio. To increase this ratio, the length of the nanowire double rows can be extended so that the size of the nanowire array will be self-aligned to the width of the source pad. To achieve this, double rows are first fabricated that are longer than the width of the source pad. The nanowires outside the source pad will then be removed when forming the source mesa with an InAs wet etch. This method was used in figure 2.12a and 2.16a.

Another modification in the third generation of vertical InAs nanowire MOSFETs was that the organic source-gate spacer was replaced by a Si_3N_4 spacer. Si_3N_4 was deposited by chemical vapor deposition (CVD) and etched back by dry etching. The

Si_3N_4 spacer is shown in figure 2.15 before and after the back-etch. Compared to an organic spacer, Si_3N_4 has an improved mechanical stability and can withstand higher temperatures. Hence, a post-metallization annealing (PMA) after gate deposition could be implemented to improve the quality of the gate dielectric. Here, a PMA at 300°C in forming gas was used for the Al_2O_3/HfO_2 bilayer gate dielectric.

The height differences on the sample are always a potential problem. One example is the step at the edges of the InAs mesa, which is depicted in 2.16a. The step remains after forming the Si_3N_4 spacer and if the gate metal is sputtered on this structure, the risk is high for increased gate resistance caused by poor film coverage at the InAs mesa edge, see 2.16b. This problem was avoided by postponing the InAs etch and, hence, forming air bridges underneath the gate fingers as shown in figure 2.16c-d. The following process flow was used: First, a protection for the InAs source pads was formed in the gate dielectric by UV-lithography. Finger gate pads were formed in gate metal and source-gate spacer using a finger length which was extended at least 1 µm

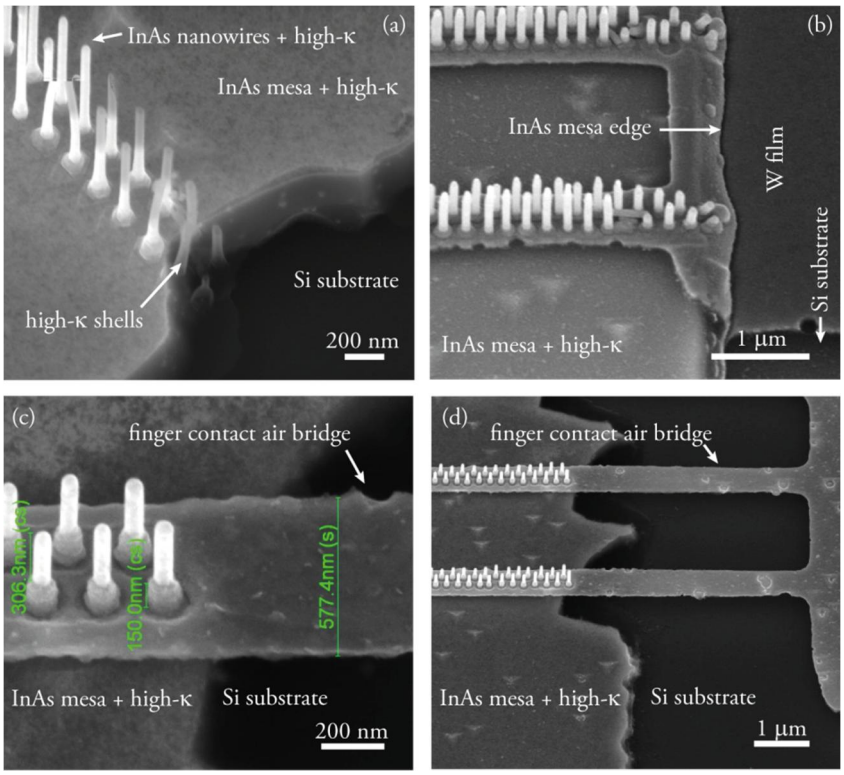


Figure 2.16: SEM images at 30° tilt showing (a) the edge of the InAs source mesa covered with high-κ. Here, also nanowires not protected by resist were etched in the source mesa wet etch. (b) Finger gate contacts with poor metal coverage at the InAs mesa edge. (c), (d) Air bridged finger gate contact formed by InAs mesa under etching.

from the source pad edge. Finally, the InAs layer was etch for to form the source mesa using the gate dielectric as an etch mask. The etch time was prolonged for complete under-etch of the gate fingers outside of the source pad.

3. Electrical Performance

3.1 DC Characterization

A completed transistor usually undergoes initial DC characterization before any other measurements are performed. The data is acquired by on-chip probing where DC voltages are applied to the source, gate, and drain terminals, and the resulting currents are measured. From this some fundamental metrics can be deduced as discussed in chapter 1.1.2. DC metrics for the devices with the best RF performance published in Paper I (on InP substrate, 2010), Paper II (on Si substrate, 2011), and Paper VII (with finger contacts, 2014) are compared in table 3.1.

	I_{ds} (mA/mm)	R_{ON} (kΩ-μm)	g_{ds} (mS/mm)	g_m (mS/mm)	SS (mV/dec)
Paper I	300	1.8	130	150	-
Paper II	550	1.6	260	155	-
Paper VII	450	1.4	72	730	420

Table 3.1: DC metrics for the three generations of vertical InAs nanowire MOSFETs. The applied biases was V_{ds} = 0.8 V for I_{ds} and g_m. R_{ON} was estimated from the highest measured V_{gs}, g_{ds} was measured at V_{ds} = 0.5 V and V_{gs} = 0 V, and *SS* was measured at V_{ds} = 0.5 V. All data is normalized to the circumference of the nanowires.

The devices have relatively good on-current and transconductance. However, the first two generations of transistors show worse subthreshold slope and output conductance than expected. The poor *SS* and g_{ds} is in part attributed to high channel doping,

which is estimated in the range of 10^{18} cm^{-3} from *C-V* measurements of MOS capacitors [52] and TCAD simulations. Another important factor for *SS* is the D_{it}, which is estimated to be in the range of 10^{13} $eV^{-1}cm^{-2}$. Furthermore, impact ionization and band-to-band tunneling needs to be considered in small bandgap materials such as InAs as these phenomena further degrade *SS* and g_{ds} and limit the drain voltage at which the device may be operated. Typically, the transistor cannot be biased at V_{ds} above 1 V due to the rapidly increasing I_{ds}. One way to suppress these effects that is currently explored within our group is to use InGaAs at the drain of the transistor to give a larger bandgap where electrical field along the channel is strongest. The growth of the InGaAs nanowires on InAs was recently published by Wu *et al* [53].

The improved DC performance in Paper VII as compared to Paper I and II is attributed to a number of different process modifications and optimizations. In Paper VII a doping profile was introduced along the channel to improve *SS* and g_{ds} without compromising R_{ON} by not intentionally dope the segment underneath the gate but only the source and drain region; a new recipe was adapted for the high-κ gate dielectric and post metal annealing (PMA) was introduced to reduce the number of traps; and a new source-gate spacer with reduced thickness was implemented, which should have a positive effect on R_{ON}. However, R_{ON} was simultaneously increased by the formation of finger drain contacts due to the higher resistance in the narrow metal stripes.

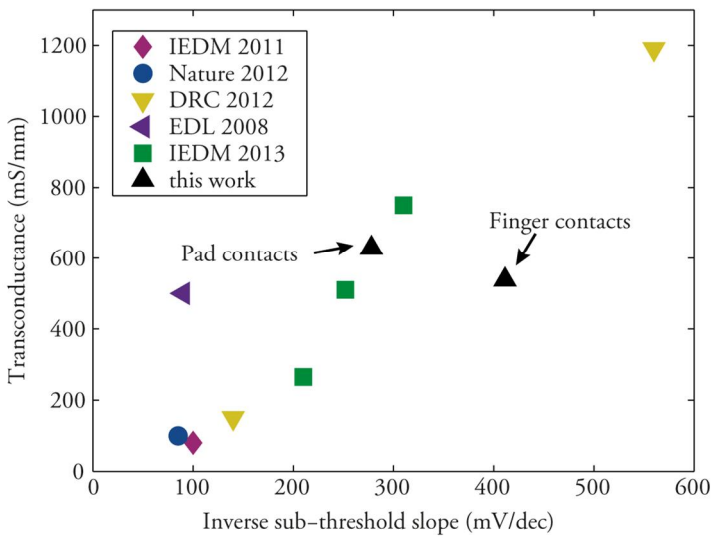


Figure 3.1: Trade-off between ON-performance and OFF-performance illustrated by g_m versus *SS* at V_{ds} = 0.5 V. The performance of different top-down and bottom-up vertical InAs and InGaAs nanowire MOSFETs is included [23, 25, 43, 54, 55]. This thesis is represented by devices with the best DC performance (pad contacts) and RF performance (finger contacts). The output and transfer characteristics of the device with pad contacts are presented in figure 1.2.

For the vertical InAs and InGaAs nanowire MOSFETs reported so far, a trade-off between ON-performance and OFF-performance has been empirically observed. This was illustrated in [25] by plotting g_m, which represents the ON-performance, versus *SS*, which represents the OFF-performance. As presented in figure 3.1, the transistors of generation 3 in this thesis are comparable with the best devices reported in this respect.

The ultimate target for the DC performance would be a device with $g_m \approx 6000$ mS/mm [56] and *SS* = 60 mV/decade where the increased transconductance may be reached for scaled nanowire diameters in the ballistic regime [57]. Recently, high transconductance was demonstrated for planar InAs MOSFETs with g_m = 2700 mS/mm [58, 59].

The trade-off in figure 3.1 is partly associated with the formation of the source and drain regions in the vertical nanowire geometry. The doping is often constant throughout the nanowires, including in the relatively long un-gated regions at the source and drain. For good *SS*, the channel doping needs to be low. At the same time, a high doping is required in un-gated regions to achieve low R_{ON} and, hence, high g_m. To improve the DC performance an improved doping profile should be implemented with high doping in the un-gated regions and low doping under the gate. Alternatively, the source and drain could be improved by reducing the length of un-gated region, by forming a Ni-InAs alloy in the un-gated regions [60, 61], or by using a geometry with smaller diameter under the gate.

The non-ideal behavior in figure 3.1 could also be related to the distribution of interface and border traps with respect to energy. High trap densities reduce the movement of the Fermi-level with the applied gate voltage at certain energies. Depending on the distribution of traps with respect to energy, difficulty to move the Fermi-level could occur either in the ON-state or the OFF-state.

In Paper II, the effect of post deposition annealing (PDA) is discussed. The use of post-deposition annealing (PDA) at 300°C in forming gas gave transistors with higher g_m compared to the transistors on the reference sample with no annealing. However, the annealed transistors showed very poor OFF-performance compared to the not-annealed reference. Since PDA targets the quality of the high-κ integration by passivating traps, we suggested that the difference is related to the trap distribution in the oxide and oxide-semiconductor interface.

Apart from the performance, the device yield has to be addressed. Chip-mapping of the yield in terms of g_m for the first generation of vertical InAs nanowire MOSFETs is presented in figure 3.2 (reprint from [51]). The yield is fairly good considering the early stage of process development with 67% yield for single nanowire transistors and 77% yield for 100-nanowire-array transistors. Furthermore, chip-mapping of transistors on Si substrate, *i.e.* second generation, was published Paper III, figure 7, with 100% yield for 190-nanowire-array transistors. However, 100% yield for all different device design on the chip has not yet been demonstrated. A typical total

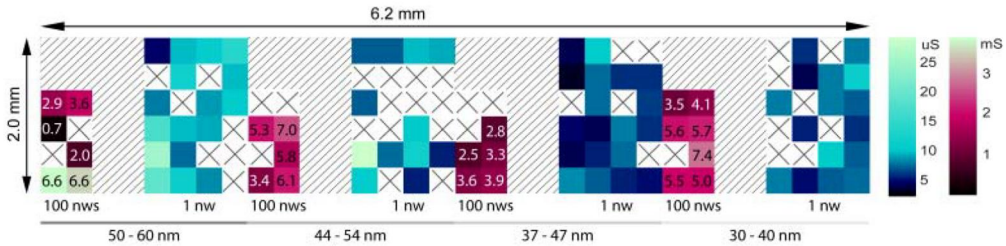


Figure 3.2: Chip-mapping of vertical InAs nanowire transistors on InP substrate over a 2 mm × 6.2 mm area. Peak transconductance is color coded for single nanowire transistors and for transistors with nominally 100 nanowires for four different nanowire diameters between 30 to 60 nm. Note the two different color scales for g_m. The numbers indicate f_t of RF characterized devices, and crosses indicate broken devices.

yield is about 70 %. It should be noted that high yield is especially important for circuit implementation as the circuit yield is roughly the transistor yield to the power of the number of transistors in the circuit, *i.e.* for a transistor yield of 70%, circuits with 5 transistors has a yield of $0.7^5 = 0.168$.

3.2 High-Frequency Characterization

3.2.1 Scattering parameter measurements

At DC and for low frequencies the device under test (DUT) is usually characterized by measuring voltages and currents. The linear small-signal relationship between the currents and the voltages for a specific DUT may be described by an admittance matrix as

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \qquad (3.1)$$

For a MOSFET in common-source configuration i_1 and v_1 are gate-source current and voltage, respectively, and i_2 and v_2 are drain-source current and voltage, respectively. The admittance parameters (*Y*-parameters) give a complete description of the electrical response of the DUT, which means that these parameters could be converted to other complete sets of parameters without any loss of information. One such complete set is the impedance parameters (*Z*-parameters). Another set, which is

commonly used for high-frequency measurements, is the scattering parameters (*S*-parameters). Instead of currents and voltages, the *S*-parameters use electromagnetic power waves as input and output as shown in the equation 3.2 and figure 3.3a where a_1 and a_2 are the incident power wave at port 1 and 2 of the DUT, respectively, and b_1 and b_2 are the reflected power waves.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (3.2)$$

S-parameters are used for high-frequency measurements because of the difficulty to achieve good short and open circuits at high frequency, which are required for measurements of currents and voltages. The *S*-parameters are instead measured using a constant impedance of the measurement equipment of 50 Ω when seen from the DUT.

The set-up used for RF measurements in this thesis is a PNA series network analyzer from Agilent Technologies with a frequency range of 10 MHz - 67 GHz, which is connected to 67 GHz ground-signal-ground probes with a pitch of 100 μm. DC biasing is applied by a Keithley sourcemeter through a bias tee internal to the network analyzer as illustrated in figure 3.3b. The *S*-parameters are measured by sweeping the frequency using a small RF power (-27 dBm) and repeating at each DC bias point.

To achieve a 50 Ω impedance of the measurement set-up, it is calibrated using load-reflect-reflect-match (LRRM) calibration. Basically, the calibration sets the 50 Ω reference planes at the probe tips and makes sure that the measurement is not influenced by impedance in the cables and probes.

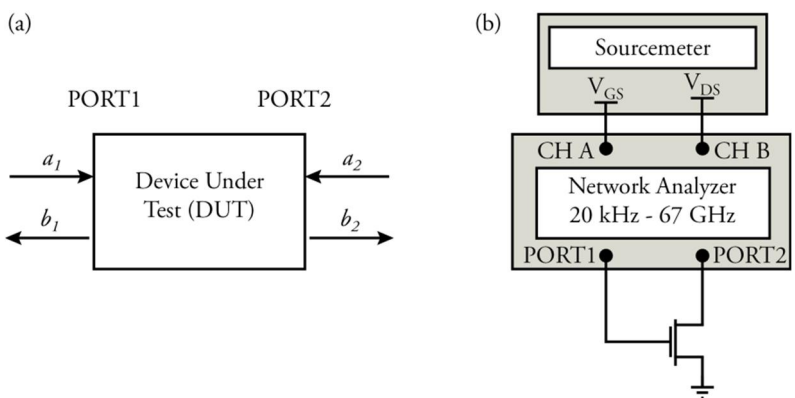


Figure 3.3: Schematic of (a) incident and reflected power waves at the DUT and (b) the *S*-parameter measurement set-up.

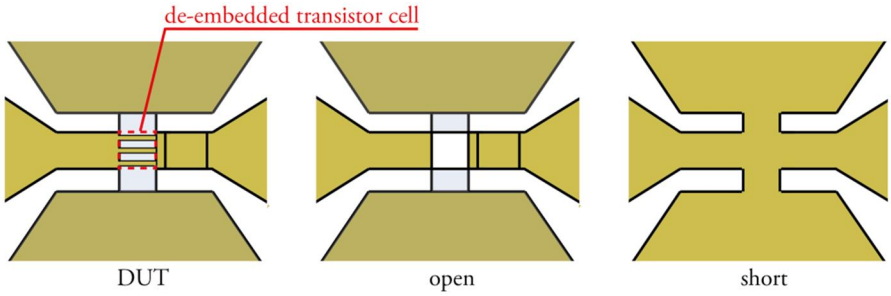


Figure 3.4: Illustration of (a) the device-under-test (DUT) including the transistor cell and surrounding probing pads, (b) the open structure, and (c) the short structure.

To make the on-chip probing practically feasible, large metal probing pads are used in the transistor layout as shown in figure 2.13. To remove the influence from these pads and define a transistor cell, which represents a realistic extrinsic device, de-embedding is performed using on-chip short and open structures. As schematically illustrated in figure 3.4, the short structure is short circuited by a metal film in the transistor cell and the open structure is similar to the transistor, however, all conducting material is removed inside the transistor cell. To de-embed the transistor cell, the *S*-parameters of the short and open structures are measured. The influence of the probing pads outside of the transistor cell is calculated and subtracted from the DUT data.

3.2.2 Cut-off frequency and maximum oscillation frequency

The cut-off frequency, f_t, and maximum oscillation frequency, f_{max}, may be graphically deduced from the de-embedded *S*-parameters by plotting the current gain, h_{21}, and unilateral power gain, U, as a function of frequency. The gain plot of a vertical InAs nanowire MOSFET using finger contacts, *i.e.* third generation, is provided in figure 3.5. Here, h_{21} is first calculated from the measured *S*-parameters from

$$h_{21} = \frac{S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} = \frac{Y_{11}Y_{22}-Y_{21}Y_{12}}{Y_{11}} \qquad (3.3)$$

U is calculated by first converting the *S*-parameters to *Z*-parameters [7] as

$$U = \frac{|Z_{21}-Z_{12}|^2}{4[\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{22})-\mathrm{Re}(Z_{12})\mathrm{Re}(Z_{21})]} \qquad (3.4)$$

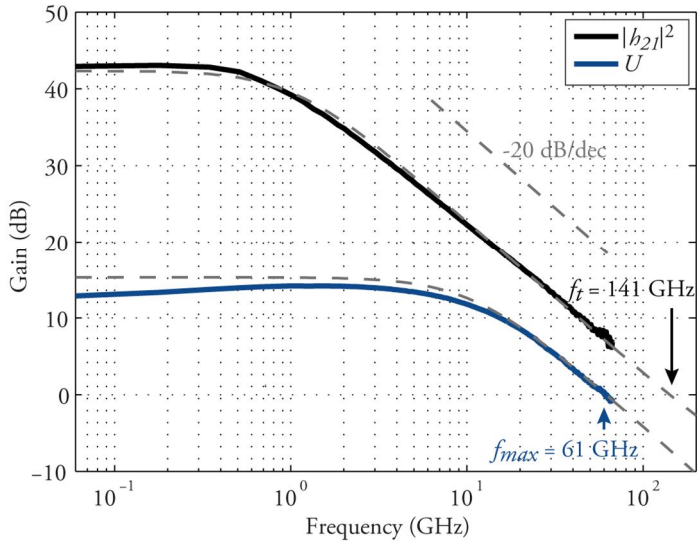


Figure 3.5: Gain plot of a vertical InAs nanowire MOSFET with finger contacts showing a record f_t=141 GHz and f_{max} = 61 GHz. The dashed lines are calculated from the small-signal model of the device in figure 3.6.

The data in figure 3.5 was presented at IPRM 2014 [62] and demonstrates f_t = 141 GHz by extrapolating the -20 dB/decade slope of $|h_{21}|^2$. This is to the best of my knowledge the current record for vertical nanowire transistors. f_{max} is lower in this device with f_{max} = 61 GHz. The current record for vertical nanowire transistors of f_{max} = 155 GHz was published in paper VII.

3.2.3 Small-signal modelling

In small-signal modeling, the non-linear equations that describe the MOSFET may be linearized within a small interval to analyze the change caused by a small signal. For *S*-parameters, the small signal is the RF signal at -27 dBm (≈ 2 μW), which is added to the large signal caused by the DC biasing. A physics-based hybrid-π model may be adapted to describe the transistor small-signal operation. One example is the small-signal model of the device in figure 3.5, which is depicted in figure 3.6.

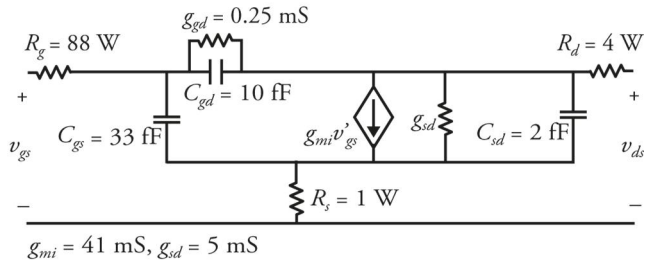


Figure 3.6: Small-signal model of a vertical nanowire MOSFET. The modeled h_{21} and U in figure 3.5 are calculated using this model.

Here, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, g_{mi} is the intrinsic transconductance, g_{ds} is the output conductance, and C_{sd} is the source-drain capacitance. Together these circuit elements constitute a standard MOSFET small-signal model [63]. To the standard model, parasitic resistances are added, including the source resistance, R_s, the drain resistance, R_d, and the gate resistance, R_g. Due to leakage between gate and drain in this specific device, a gate-drain conductance, g_{gd}, was also added, which limits the gains, h_{21} and U, at low frequencies. As opposed to planar MOSFETs, the RF characteristics of the vertical nanowire transistors have little or no coupling to the substrate, thus circuit elements related to that are not included.

The small-signal model is constructed by first estimating R_s and R_d from DC measurements. After subtracting R_s and R_d, the following relationship may be established by nodal analysis as described in [63].

$$Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = g_{gd} + \frac{j\omega\left(C_{gs}+C_{gd}\right)}{1+j\omega\left(C_{gs}+C_{gd}\right)R_g} \tag{3.5a}$$

$$Y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} = \frac{g_m - j\omega C_{gd}}{1+j\omega\left(C_{gs}+C_{gd}\right)R_g} \tag{3.5b}$$

$$Y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = -g_{gd} - \frac{j\omega C_{gd}}{1+j\omega\left(C_{gs}+C_{gd}\right)R_g} \tag{3.5c}$$

$$Y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0}$$
$$= g_{sd} + j\omega C_{sd} + j\omega C_{gd} + \frac{\omega^2 C_{gd}^2 R_g + j\omega g_m C_{gd} R_g}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (3.5d)$$

It should be noted that the mutual capacitance, C_m, is neglected in equations 3.5a-d and in figure 3.6. This means that C_{dg} is assumed to be equal to C_{gd}, which should have only minor effect on the model. However, with this assumption the error cause by noise in the extraction of C_{dg} is eliminated. Furthermore, to enable straightforward parameter extraction, the above equations may be simplified using the assumption that

$$\omega^2 (C_{gs} + C_{gd})^2 R_g^2 << 1. \quad (3.6)$$

Because the simplified equation might not be valid for high frequencies due to the high R_g, the simplified equation is used to deduce the circuit elements in the lower frequency interval, while the modeled *Y*-parameters are calculated using the full expression. An example is given below for the extraction of C_{gd}. First, the expression for Y_{12} in equation 3.5c is simplified using the assumption in equation 3.6, which results in

$$Y_{12} = -g_{gd} - \omega^2 C_{gd}(C_{gs} + C_{gd})R_g - j\omega C_{gd} \quad (3.7)$$

Here, the imaginary part of Y_{12} is directly proportional to the angular frequency by a factor of $-C_{gd}$. Hence, C_{gd} is deduced from the slope of $\mathrm{Im}(Y_{12})$ as a function of ω at low frequencies as shown in figure 3.7.

Table 3.2 summarizes the method used for modeling of the *Y*-parameters. In figure 3.8, the measured and modeled *Y*-parameters are compared to confirm the validity of the deduced circuit elements. It should be noted that the lowest frequencies are avoided when deducing the circuit elements in this example. At these frequencies the effect of impact ionization is the largest, which could be modeled through frequency dependent current sources as demonstrated in Paper II and [51]. However, to simplify the model the current sources could be neglected as the effect at high frequencies is very small.

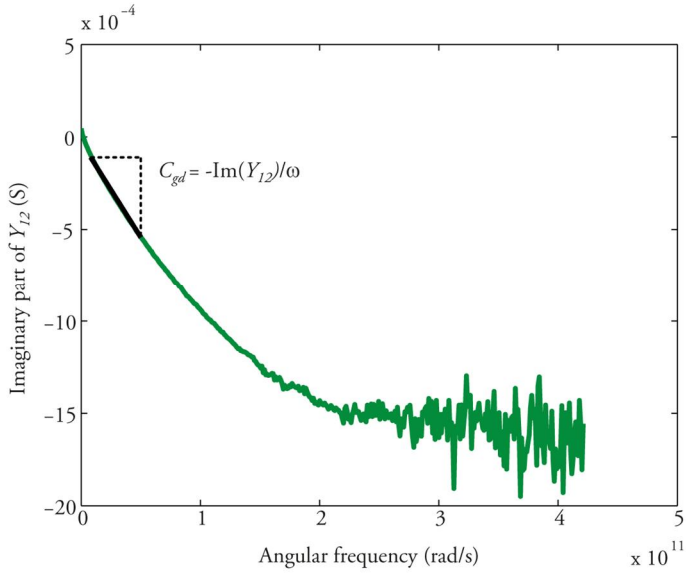


Figure 3.7: The imaginary part of Y_{12} is plotted as a function of ω to deduce C_{gd} at low frequency.

It should also be noted that according to equation 1.4 and 1.7, a high gate resistance lowers f_{max} but has no effect on f_t. In practice, this is not entirely true. To model high R_g, a distributed resistance in the narrow finger contacts could be used with n single nanowire transistors connected in series and where each device is associated with a partial gate resistance, R_g/n, and partial gate capacitance, C_{gg}/n. The resulting voltage drop along the finger contacts increase with frequency. Effectively, the number of single nanowire transistors that are active is reduced with frequency and the effect could be seen in the measured Y-parameters. One example is Im(Y_{12}) in figure 3.7, which is used to deduce C_{gd}, where the slope is reduced with frequency. The distributed RC network does not lead to a decreased current gain and f_t in itself as it scales I_{ds} and I_{gs} at the same rate [64]. However, some extrinsic impedance such as R_s and R_d might not scale down, which would lead to a reduced f_t with increasing R_g.

Step	Description	Equation
1	Estimate R_s, R_d	$R_{ON} \approx R_s + R_d$
2	Subtract R_s, R_d	$Z_{i,meas} = Z_{e,meas} - \begin{bmatrix} R_s & R_s \\ R_s & R_s + R_d \end{bmatrix}$
3	Extract parameters	$C_{gd} = -\mathrm{Im}(Y_{12})/\omega$ $C_{gs} = \mathrm{Im}(Y_{11})/\omega - C_{gd}$ $g_{mi} = \mathrm{Re}(Y_{21})$ $R_g = \mathrm{Re}(Y_{11})/\omega^2 / (C_{gs} + C_{gd})^2$ $g_{sd} = \mathrm{Re}(Y_{22})$ $C_{sd} = \mathrm{Im}(Y_{22})/\omega - C_{gd} - g_m R_g C_{gd}$ $g_{gd} = \mathrm{Re}(Y_{11})$ at low freq.
4	Calculate intrinsic *Y*-parameters	Equation 3.5 a-d
5	Add R_s, R_d	$Z_{e,\mathrm{mod}} = Z_{i,\mathrm{mod}} + \begin{bmatrix} R_s & R_s \\ R_s & R_s + R_d \end{bmatrix}$
6	Check the error between modeled and measured data	$\varepsilon = \frac{25}{N_{freq}} \sum_{ij} \sum_{freq} \frac{\lvert Y_{ij,meas} - Y_{ij,\mathrm{mod}} \rvert^2}{\lvert Y_{ij,meas} \rvert^2}$

Table 3.2: Step-by-step method for modeling of the *Y*-parameter from measured *S*-parameters. Z_i and Z_e are the intrinsic and extrinsic *Z*-parameters, respectively. Equations for conversion between *Y*-,S-, and *Z*-parameters may be found in [7]. ε is the error in the *Y*-parameters and N_{freq} is the number of frequencies in the data set. For parameter extraction (step 3), a frequency interval is used where the assumption in equation 3.6 is valid. However, the intrinsic *Y*-parameters are calculated for all frequencies in step 4.

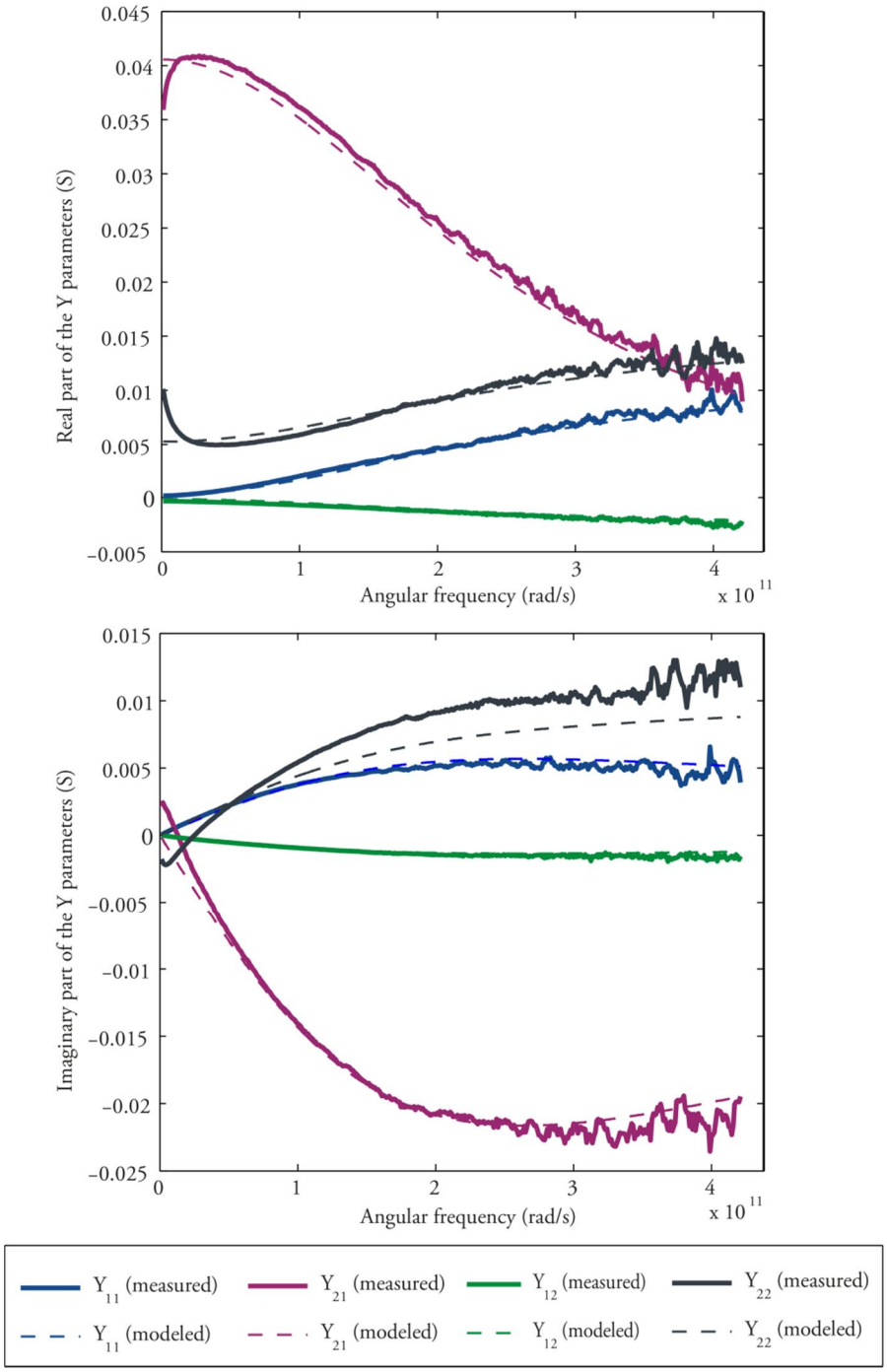


Figure 3.8: Modeled and measured *Y*-parameters of a vertical InAs nanowire MOSFET with finger contacts showing a record f_t=141 GHz using the small-signal model in figure 3.6.

3.2.4 Reduced parasitic capacitance

In Paper VII, the significant improvement in RF performance when using finger contacts as compared to pad contacts is reported. To investigate the effects of the

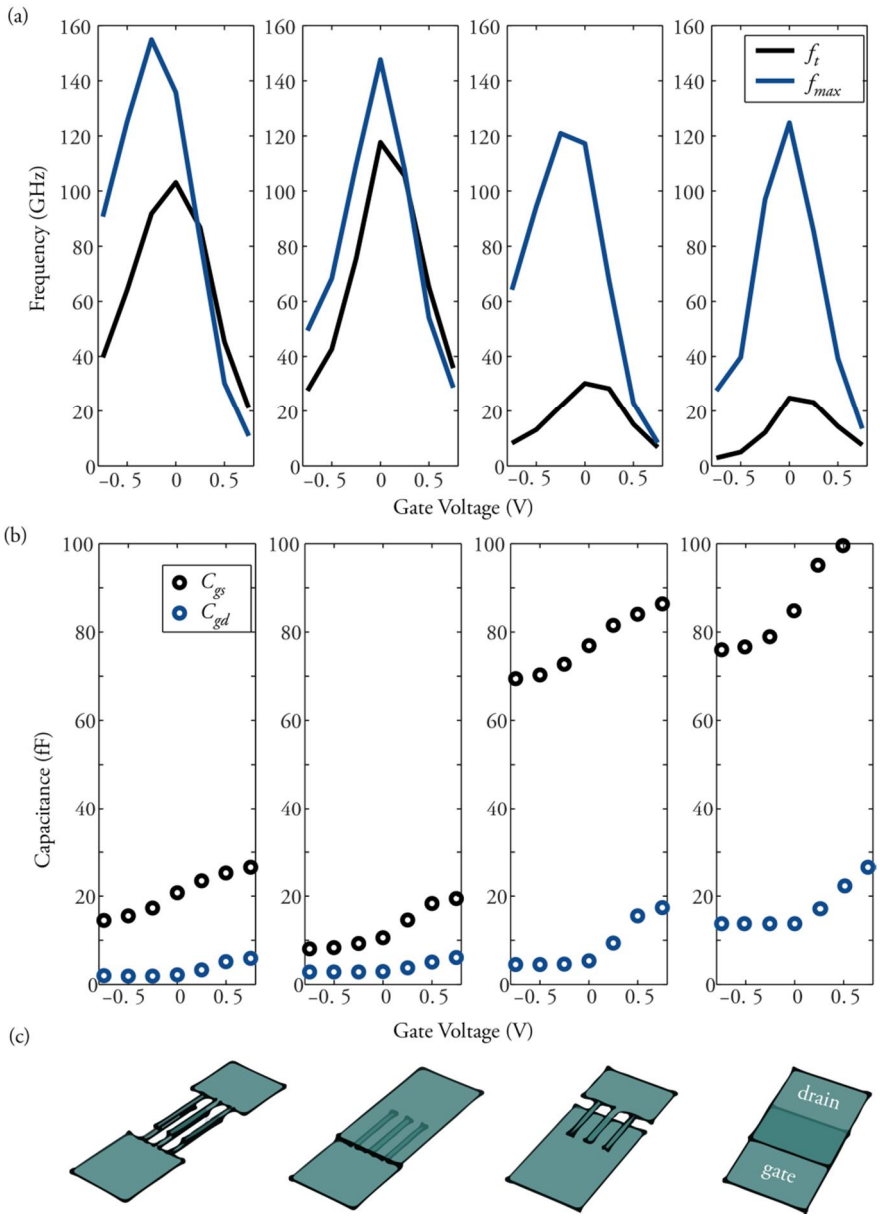


Figure 3.9: The gate voltage dependence of 165-nanowire-array devices in terms of (a) f_t and f_{max}, and (b) C_{gd} and C_{gs}. The contact layout of the devices above is displayed in (c).

contact layout even further, the gate voltage dependence of f_t and f_{max} as well as the deduced C_{gd} and C_{gs} is plotted for four different layouts in figure 3.9 [62]. The layouts have finger contact either for both gate and drain, for only gate or only drain, or pad contacts for both gate and drain. Except for the contact layout, the devices were nominally identical. However, one difference that was noted was a somewhat shorter gate length for the finger gate contact devices caused by the topology of the etch-back resist on top of the finger contacts. The gate length was about 150 nm for the devices with finger gates and about 250 nm for the devices with pad gates.

The effect of finger contact patterning correlates well with simulations of the parasitic capacitances including both parallel plate capacitance and fringe capacitance [62]. It can be concluded that patterning of the gate pad is the key for good f_t as this has the largest effect on the parasitic gate capacitance, $C_{gg,p}$. Here, the parasitic capacitances could be approximated as the capacitances at V_{gs} = -0.75 V. Furthermore, $C_{gs,p}$ is reduced when the gate is patterned while $C_{gd,p}$ is reduced when either the gate or the drain pad is patterned. Also the highest f_{max} is found for finger contact devices, which is expected due to the higher f_t and lower C_{gd} according to equation 1.8. However, the positive effect of gate patterning becomes less pronounced for f_{max} as the gate resistance increases from about 7 Ω with pad gates to 70 Ω with finger gates.

Moreover, the parasitic capacitances could also be reduced by lowering the dielectric constant, κ, of the spacer materials. Using the finger contact layout, this could be accomplished by replacing the spacer materials with air after completion of the device. By replacing the Si_3N_4 source-gate spacer, $C_{gs,p}$ could be reduced by a factor of 7, and by replacing the organic gate-drain spacer, $C_{gd,p}$ could be reduced by a factor of 3 due to the lower dielectric constant of air.

In initial experiments, the spacer materials were only partly removed as illustrated in figure 3.10 and as could be observed in the cross-sectional SEM image in figure 2.11. Here, the gate-drain spacer was dry etched by oxygen plasma and the gate-source spacer was wet etched by buffered oxide etch. It should be noted that both these etches may damage the device. The dry etch is fairly physical and impinging ions may

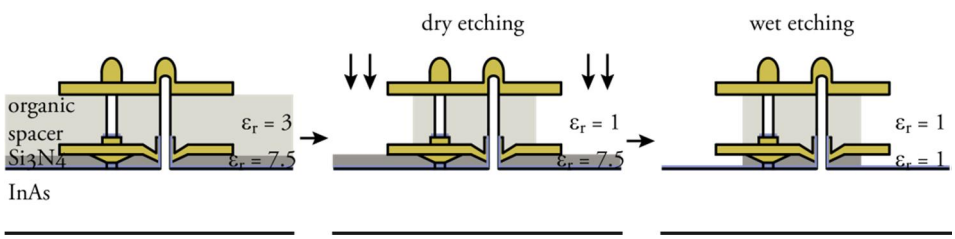


Figure 3.10: Schematic illustration of the partial spacer removal; (a) no spacer material removed, (b) gate-drain spacer partially removed by dry etching, and (c) gate-source spacer partially removed by wet etching.

damage the metal contacts, the gate dielectric, and the semiconductor channel. The wet etch was expected to mainly etch the source-gate spacer and the gate dielectric. However, cracking of the metal finger contact was observed for many devices after wet etching, which could be due to the release of strain in the W contacts.

The capacitance was deduced and compared through RF measurements and small-signal modeling. For this test sample, no significant change was observed for $C_{gd,p}$ while a reduction of $C_{gs,p}$ from about 65 fF to 45 fF was observed. Furthermore, g_m decreased by about 25%, and f_t and f_{max} was reduced. The degradation of the electrical performance is most likely caused by the physical and/or chemical damage caused by the etching, and it is concluded that more gentle etching processes need to be developed to advantage from the spacer removal.

3.2.5 Benchmarking of RF performance

Due to the device improvements presented in this thesis, an exponential increase in f_t and f_{max} is observed for the vertical InAs nanowire MOSFET as a function of time as depicted in figure 3.11. The strong increase in the performance holds great promise for the future and was possible because the technology is not yet mature. Further improvement in the RF performance is expected if R_{ON}, R_g or $C_{gg,p}$ is reduced, if the high-κ integration is improved, or if the dimensions of the transistor are scaled down.

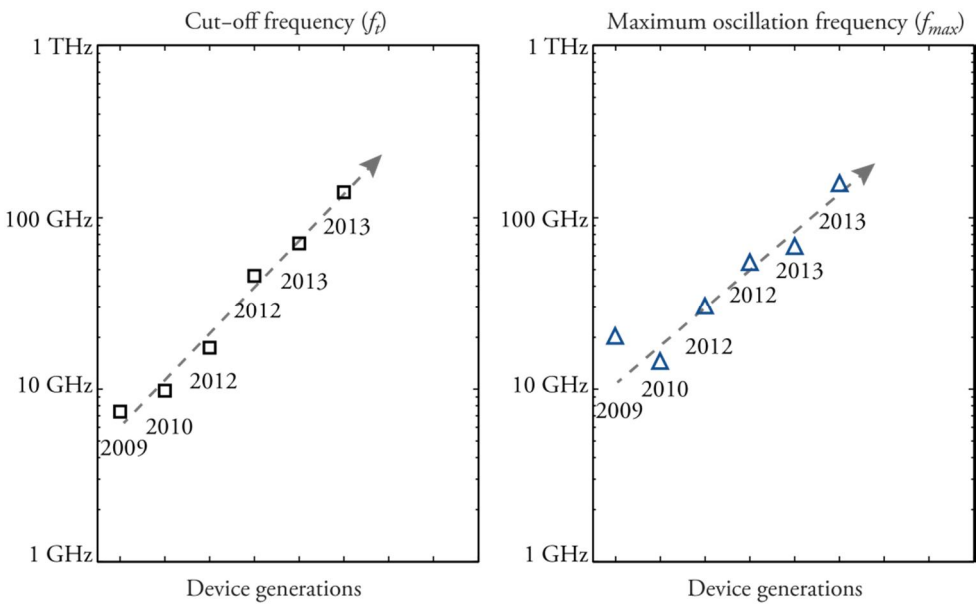


Figure 3.11: The RF performance of vertical InAs nanowire MOSFETs represented by progress charts for f_t and f_{max}.

According to realistic modeling of the InAs nanowire technology, extrinsic f_t and f_{max} above 1 THz are predicted for an optimized process at L_g = 30 nm [65].

Only a few reports are published by other groups on the RF performance of InAs nanowire transistors [66, 67]. In these reports, modest RF performance is demonstrated for lateral nanowire MOSFET with f_t and f_{max} in the order of 1-15 GHz, which are limited by the parasitic impedance.

For benchmarking of the RF performance, the vertical InAs nanowire MOSFET is also compared to other technologies that target high frequency and low power applications. Planar InAs and InGaAs MOSFETs have recently shown impressive RF performance with f_t = 245 GHz and f_{max} = 355 GHz for an InAs quantum-well MOSFET [68], and f_t = 370 GHz and f_{max} = 292 GHz for InGaAs MOSFETs [69, 70]. Also, InGaAs FinFETs have recently demonstrated promising RF performance with f_t = 210 GHz and f_{max} = 250 GHz [19].

Two more established technologies are silicon-on-insulator (SOI) Si MOSFETs and InGaAs HEMTs. In figure 3.12, f_t and f_{max} is plotted as a function of L_g for these technologies and for the III-V MOSFETs discussed above. As expected, the RF performance improves as L_g is reduced, but is limited by the scalability of the technology at very short L_g.

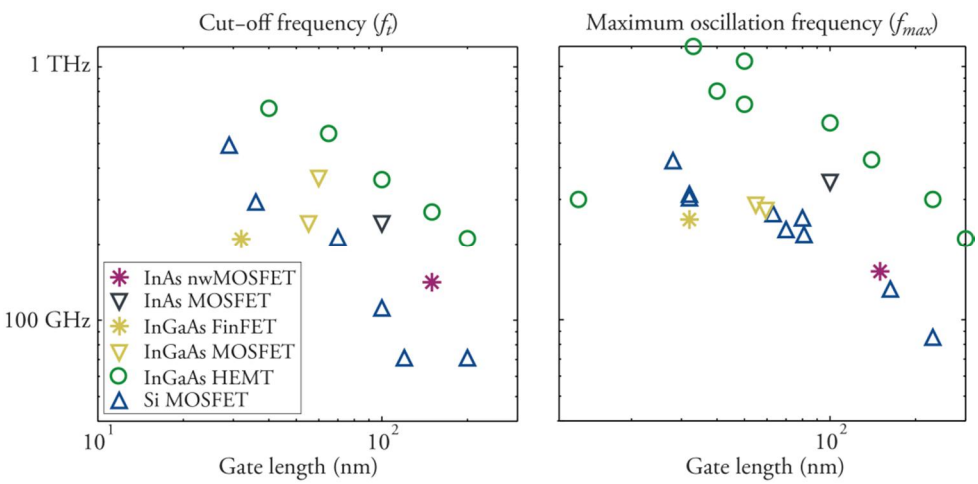


Figure 3.12: Benchmarking of different RF technologies by cut-off frequency and maximum oscillation frequency as a function of gate length after [71]. This thesis is represented by the best RF performance of the vertical InAs nanowire MOSFETs with f_t = 141 GHz and f_{max} = 155 GHz at L_g = 150 nm. The data is compared to an InGaAs FinFET [19], an InAs quantum-well MOSFET [68], InGaAs MOSFETs [69, 70], Si MOSFETs [72], and InGaAs HEMTs [73].

3.3 Temperature and Annealing Effects

Only small temperature dependences of the drive current are generally expected in MOSFETs [74]. However, the presence of a parasitic energy barrier along the channel could lead to a substantial increase in the current with temperature. In this case, the drive current is limited by the degree of thermionic emission over the barrier, which could be modeled by the by

$$I \propto T^2 e^{-\phi_B/kT} . \qquad (3.7)$$

Here, T is the temperature, ϕ_B is the barrier height, and k is Boltzmann's constant. Paper IV presents a 5 to 10 fold increase in the drive current for a temperature increase of 180°C using second generation vertical InAs nanowire MOSFETs with low nanowire doping and long un-gated regions of about 200 nm at both source and drain. The un-gated source-gate section was covered by HfO_2 gate dielectric while the gate dielectric was removed from the un-gated gate-drain section. In common-source configuration, a ~100 meV barrier was obtained in the gate-source region using equation 3.7. By connecting the devices in common-drain configuration, the gate-drain region was probed but no major energy barrier was found. One interpretation of the results is that the barrier is caused by negative charge in the gate dielectric along the un-gated source-gate section of the nanowire.

Furthermore, long term annealing effects were observed in Paper IV. It is known from capacitance-voltage (*C-V*) investigations of Al_2O_3 and HfO_2 on InAs that annealing of the gate stack improves the high-κ integration and reduces D_{it} [75, 76]. The present state-of-the-art annealing is post metallization annealing in forming gas at about 400°C. However, the early vertical InAs nanowire MOSFETs used a very primitive annealing at 200°C on hot plate. The long term effect of this annealing was documented in terms of I_{ds} variations. By annealing, the I_{ds} increased about 10 times after which it slowly returned to a steady-state level after a few weeks. One explanation to the slow degradation is that charge traps along the un-gated sections of the nanowires are slowly passivated or created.

4. Characterization of Border Traps

A number of methods have been used for characterization of border traps including noise measurements, deep-level transient spectroscopy (DLTS) [77], charge pumping [78], and *C-V* measurements [79]. In this chapter, a fairly new method inspired by frequency dependent transconductance measurements on HEMTs [80] is described, which is referred to as the AC transconductance method. Here, the traps are modeled as an *RC* network, which is included in the small-signal model of the transistor. From the small-signal model, an analytical expression is deduced for simple extraction of the number of border traps, $N_{bt}(x)$, and, in the end of this chapter, three examples are presented where the AC transconductance method is applied to vertical InAs nanowire MOSFETs and surface-channel InGaAs MOSFETs.

4.1 Traps as an *RC* Network

Different mechanisms are used to describe trapping of charges at interface traps and border traps, respectively. *Interface traps* are often described by a Shockley-Read-Hall process where holes from the valence band and electrons from the conduction band relax to localized states in the bandgap of the semiconductor at the dielectric-semiconductor interface [81]. The process is associated with separate time constants for electrons, $\tau_{it,n}$, and holes, $\tau_{it,p}$ as

$$\tau_{it,n} = \left(n_s v_{th} \sigma_{n,it}\right)^{-1} \tag{4.1a}$$

$$\tau_{it,p} = \left(p_s v_{th} \sigma_{p,it}\right)^{-1} \qquad (4.1b)$$

where v_{th} is the thermal velocity, n_s and p_s are the electron and hole densities at the interface, and $\sigma_{n,it}$ and $\sigma_{p,it}$ are the capture-cross sections for electrons and holes, respectively. The energy at which the density of interface traps, D_{it}, is probed is set by E_F. It should be noted that the time constants are calculated in the same way for all applied voltages including the case where E_F is not in the bandgap, which implies that a corresponding trapping mechanism exists for the conduction band and valence band.

Trapping in *border traps* is described by a tunneling mechanism where the probability of trapping decreases exponentially with the distance, x, into the dielectric due to the attenuation of the charge carrier wave function. Here, elastic tunneling is assumed, *i.e.* the energy level of the probed traps is the same as E_F. The x-dependence is set by the time constant of trapping for border traps

$$\tau_{bt}(x) = \left(n_s v_{th} \sigma_{n,bt}\right)^{-1} \cdot e^{x \cdot \sqrt{8 m_{ox}^{*}(E_{C,ox} - E)} / \hbar} = \tau_0 \cdot e^{x/\lambda} \qquad (4.2)$$

where τ_0 is the time constant at $x = 0$, λ is the attenuation coefficient of the electron wave function, $\sigma_{n,bt}$ is the capture cross-section for electrons, m^*_{ox} is the effective mass in the oxide and $E_{C,ox}$ is the conduction band edge of the oxide. Note that the capture cross-section is written with the index *it* and *bt* for interface traps and border traps, respectively. This is done because the capture cross-section of the two processes may differ. Alternatively, equation 4.2 can be rewritten to describe the relationship between the angular frequency, $\omega = 2\pi/\tau$, and the distance into the oxide, x, as

$$x = \lambda \ln(\omega_0 / \omega) \qquad (4.3)$$

where ω_0 is the characteristic angular frequency at $x = 0$.

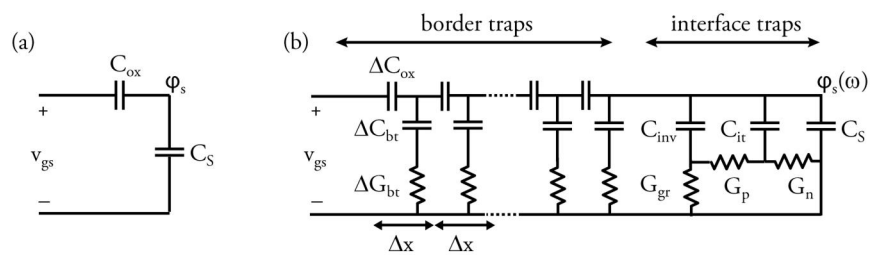


Figure 4.1: Small-signal model of the MOS structure (a) without any charge traps, and (b) including *RC* networks that capture the electrical response of border traps, $N_{bt}(x)$, and interface traps, D_{it}.

Storing of charge in traps is modeled by capacitors. A model of an n-type MOS structure is presented in figure 4.1 where C_{it} stores charge in interface traps and $\Delta C_{bt}(x)$ store charge in border traps at a distance x from the interface [79]. The relationships between the capacitors and the number of border traps, $N_{bt}(x)$, and the density of interface traps, D_{it}, is

$$\Delta C_{bt}(x) = qN_{bt}(x) \cdot \Delta x \tag{4.4}$$

$$C_{it} = qD_{it} \tag{4.5}$$

In this thesis, $N_{bt}(x)$ and D_{it} are measured in $cm^{-3}eV^{-1}$ and $cm^{-2}eV^{-1}$, respectively.

The charge traps in figure 4.1 are assigned correct time constants according to equation 4.1 and 4.2 by adding conductances of the appropriate size in series with the capacitors, C_{it} and ΔC_{bt}, as

$$\tau = C/G\,. \tag{4.6}$$

To model trapping of holes at the interface, the conductance G_p is connected to a minority-carrier generation-recombination conductance, G_{gr}, and an inversion capacitance, C_{inv}. In accumulation, the contribution from holes may be neglected and G_p, C_{inv} and G_{gr} can be removed from the model.

For the border traps, C_{ox} is divided into ΔC_{ox} contributions connected in series so that the traps at a certain depth, x, can be connected at the corresponding portion of C_{ox}. Moreover, C_S, which is the semiconductor capacitance, can be estimated for small bandgap III-V quantum-well FETs according to

$$C_S \approx \frac{q^2 \cdot m_e}{\pi \cdot \hbar^2}\,. \tag{4.7}$$

Here, m_e is the effective mass of an electron in the semiconductor and q is the elementary charge.

4.2 The AC Transconductance Method

The AC transconductance method is presented in Paper V and VI. Here, the *RC* network used for modeling of $N_{bt}(x)$, which is presented in figure 4.1 b, replaces C_{ox} in the 2-port small-signal model of the MOSFET as illustrated in figure 4.2 a. D_{it} is

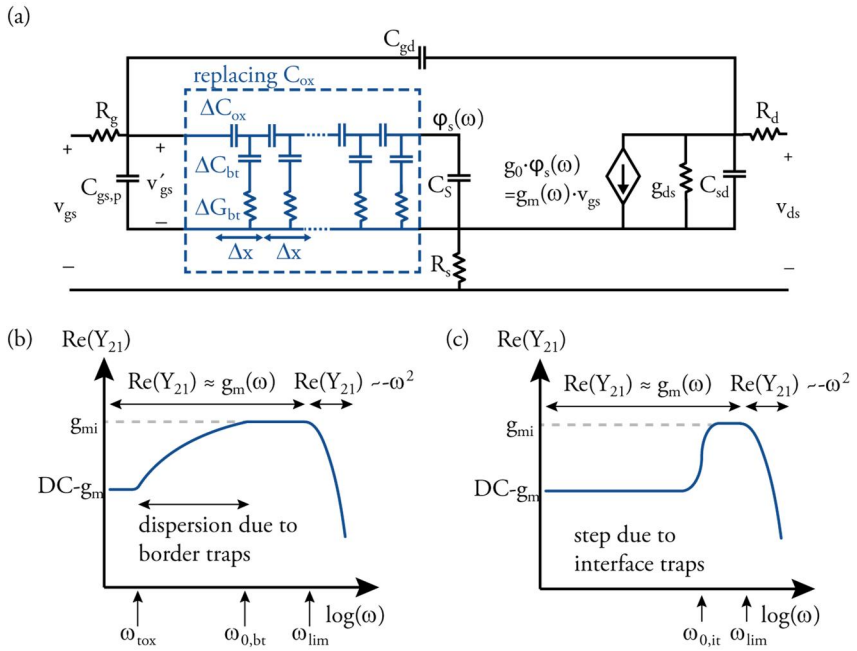


Figure 4.2: (a) Small-signal model with an *RC* network replacing C_{ox} to models the effect of border traps. (b) A schematic of the expected frequency dispersion of g_m caused by border traps provided that $D_{it} << N_{bt}$. (c) The expected frequency dispersion of g_m caused by interface traps provided that $D_{it} >> N_{bt}$ and that $\omega_{it,n}$ is within the investigated frequency range.

not included in this model, but only discussed in general. However, the single frequency at which interface traps respond could be treated separately or added as a *RC*-leg with the time constant $\tau_{it,n}$ at $x = 0$ for a MOSFET in the ON-state.

$N_{bt}(x)$ is deduced from the frequency dependence of g_m caused by the border traps. The transconductance is, in turn, deduced from the admittance as the real part of Y_{21} using the expression below, which is a simplified version of equation 3.5b using the assumption in equation 3.6.

$$\mathrm{Re}(Y_{21}) = \mathrm{Re}(g_m(\omega)) - \omega^2 R_g C_{gd}\left(C_{gd} + C_{gs}\right) \qquad (4.8)$$

$g_m(\omega)$ may be approximated as $\mathrm{Re}(Y_{21})$ up to relatively high frequencies where $\mathrm{Re}(Y_{21})$ become proportional to $-\omega^2$. The negative slope at high frequencies is indicated schematically in figure 4.2 b and c. Recalculating using the simplified equations for f_t and f_{max}, *i.e.* equation 1.3 and 1.8, the high frequency limit can be defined as $\omega_{lim} << 4\pi \cdot f_{max}$.

Furthermore, figure 4.2 b and c illustrate two different cases: $N_{bt}(x) >> D_{it}$ in b and $N_{bt}(x) << D_{it}$ in c. In both cases the characteristic frequencies of trapping is below ω_{lim}.

Starting with figure 4.2 b, the extrinsic g_m is reduced at low frequencies by charging of the border traps, which causes a voltage drop between v'_{gs} and φ_s. For sufficiently low frequencies, $g_m(\omega)$ is frequency independent as all border traps respond, *i.e.* tunneling of charge to traps at any distance into the oxide, even to the very slowly responding border traps, is possible. It should be noted that the lower level of g_m is found at frequencies below $\omega_{tox} = \omega_0/\exp(\lambda/t_{ox})$, which is expected to be smaller than 1 Hz for a high-κ thickness of 5 nm.

As the frequency is increased from ω_{tox} to ω_0, a larger and larger portion of the border traps are unable to follow the signal and the trap response is sequentially cancelled starting at the metal-oxide interface and moving towards the oxide-semiconductor interface. The shape of the curve in figure 4.2 b is characteristic for a constant $N_{bt}(x)$ with respect to x. At frequencies above ω_0, no border traps are able to respond and the transconductance reaches the intrinsic level. Note that the intrinsic transconductance, g_{mi}, is related to g_0, which is used in the small-signal model in figure 4.2 a, by

$$g_{mi} = \frac{C_{ox}}{C_{ox} + C_s} \cdot g_0 \,. \tag{4.9}$$

Figure 4.2 c shows the ideal frequency dispersion of g_m due to interface traps. If a device in accumulation is considered only the electron contribution needs to be included as the minority carrier concentration is negligible. When crossing $\omega = \omega_{it,n}$, g_m increases as the time constant associated with trapping at the interface is exceeded and the voltage drop caused by the interface traps is eliminated. The extrinsic g_m measured at DC is increased to the intrinsic g_m by a step.

4.2.1 Analytical expression for $N_{bt}(x)$

For simple calculations, an analytical expression for $N_{bt}(x)$ is used in Paper V and VI. To deduce this expression, the decrease in admittance of the *RC* network in figure 4.2 as the angular frequency is increased from ω-$\delta\omega$ to ω is first considered. The change in admittance is explicitly shown in figure 4.3.

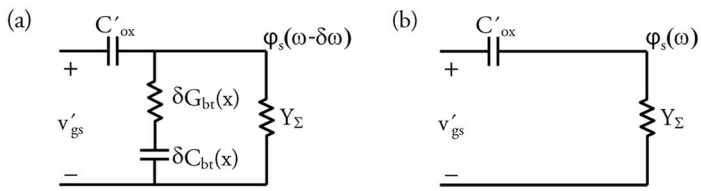


Figure 4.3: MOS structure for *RC* modeling of border traps showing the decrease in admittance as the frequency is increased from ω-$\delta\omega$ in (a) to ω in (b).

Here, C'_{ox} is the portion of the oxide capacitance located at a distance larger than x from the semiconductor-oxide interface, which means that the trap response in this part is cancelled and the capacitance can be treated as an ordinary capacitance

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox} - x}. \tag{4.10}$$

Furthermore, Y_Σ is the equivalent admittance of the RC network between x and the semiconductor-oxide interface, including C_S. The difference between the two cases is the parallel admittance at x, which can be described, using equation 4.4 and 4.6, as

$$Y_T = \frac{1}{1/j\omega\delta C_{bt}(x) + 1/\delta G_{bt}(x)} = \frac{j\omega q N_{bt}(x)\cdot\delta x}{1 + j\omega\tau(x)} \tag{4.11}$$

Y_T is considered to store charge at ω-$\delta\omega$, but not at higher frequencies, such as ω, since the frequency corresponding to the time constant of Y_T will then be exceeded. By nodal analysis of figure 4.3 b, $\varphi_s(\omega)$ can be expressed as

$$\frac{\varphi_s(\omega)}{v'_{gs}} = \frac{j\omega C'_{ox}}{Y_\Sigma + j\omega C'_{ox}} = \frac{g_m(\omega)}{g_0} \tag{4.12}$$

where the relationship between $\varphi_s(\omega)$ and $g_m(\omega)$ in the small-signal model, *i.e.* $g_0\cdot\varphi_s(\omega) = g_m(\omega)\cdot v'_{gs}$, is employed to translate the expression into the frequency dependence of g_m.

In the following, $N_{bt}(x)$ is deduced from the slope of $g_m(\omega)$, *i.e.* $\delta g_m(\omega)/\delta\ln(\omega)$, by first considering the change in φ_s between ω-$\delta\omega$ and ω. For this, $\varphi_s(\omega$-$\delta\omega)$ is derived by nodal analysis of the circuit in figure 4.3 a and approximated by a first order Taylor series in δx as

$$\begin{aligned}
\frac{\varphi_s(\omega-\delta\omega)}{v'_{gs}} &= \frac{j\omega C'_{ox}}{Y_\Sigma + Y_T + j\omega C'_{ox}} \\
&= j\omega C'_{ox}\,\frac{1}{Y_\Sigma + j\omega C'_{ox} + \dfrac{j\omega q N_{bt}(x)\cdot\delta x}{1+j\omega\tau(x)}} \\
&\approx \frac{j\omega C'_{ox}}{Y_\Sigma + j\omega C'_{ox}} - \frac{j\omega C'_{ox}}{\left(Y_\Sigma + j\omega C'_{ox}\right)^2}\cdot\frac{j\omega q N_{bt}(x)\cdot\delta x}{1+j\omega\tau(x)}
\end{aligned} \tag{4.13}$$

Hence, the incremental increase in $\varphi_s(\omega)$ can be expressed using equation 4.12 and 4.13 as

$$\begin{aligned}
&\delta\varphi_s(\omega) = \varphi_s(\omega - \delta\omega) - \varphi_s(\omega) \\
&= \frac{j\omega C'_{ox}}{Y_\Sigma + j\omega C'_{ox}} v'_{gs} - \frac{j\omega C'_{ox}}{\left(Y_\Sigma + j\omega C'_{ox}\right)^2} \cdot \frac{j\omega q N_{bt}(x) \cdot \delta x}{1 + j\omega\tau(x)} v'_{gs} \\
&- \frac{j\omega C'_{ox}}{Y_\Sigma + j\omega C'_{ox}} v'_{gs} \\
&= -\frac{j\omega C'_{ox}}{\left(Y_\Sigma + j\omega C'_{ox}\right)^2} \cdot \frac{j\omega q N_{bt}(x) \cdot \delta x}{1 + j\omega\tau(x)} v'_{gs}
\end{aligned} \tag{4.14}$$

The equation is re-written using $\delta x = -\lambda\delta \ln(\omega)$ and equation 4.12.

$$\begin{aligned}
&\frac{\delta\varphi_s(\omega)}{v'_{gs}} = \frac{j\omega C'_{ox} \cdot j\omega}{\left(Y_\Sigma + j\omega C'_{ox}\right)^2} \cdot \frac{q N_{bt}(x) \cdot \lambda\delta \ln(\omega)}{1 + j\omega\tau(x)} \\
&= \frac{g_m^2(\omega)}{g_0^2 C'_{ox}} \cdot \frac{q N_{bt}(x) \cdot \lambda\delta \ln(\omega)}{1 + j\omega\tau(x)} = \frac{\delta g_m(\omega)}{g_0}
\end{aligned} \tag{4.15}$$

The slope of $g_m(\omega)$ may now be expressed by re-arranging as

$$\frac{\delta g_m(\omega)}{\delta \ln(\omega)} = \frac{\delta\varphi_s(\omega) g_0}{v'_{gs}\delta \ln(\omega)} = \frac{g_m^2(\omega)}{g_0 C'_{ox}} \cdot \frac{q N_{bt}(x) \cdot \lambda}{1 + j\omega\tau(x)}. \tag{4.16}$$

Finally, the analytical expression for $N_{bt}(x)$ is obtained by combining equation 4.16 with equation 4.9 and 4.10, and by approximating $N_{bt}(x)$ as the real part of the expression.

$$\begin{aligned}
&N_{bt}(x) = \frac{\left(1 + j\omega\tau\right) \cdot g_0 C'_{ox}}{q\lambda g_m^2(\omega)} \cdot \frac{\partial g_m(\omega)}{\partial \ln(\omega)} \\
&= \frac{\left(1 + j\omega\tau\right) \cdot \left(C_s + C_{ox}\right) \cdot g_{mi}}{q\lambda g_m^2(\omega)} \cdot \frac{\partial g_m(\omega)}{\partial \ln(\omega)} \cdot \frac{t_{ox}}{t_{ox} - x} \\
&\approx \frac{\left(C_s + C_{ox}\right) \cdot g_{mi}}{q\lambda g_m^2(\omega)} \cdot \frac{\partial g_m(\omega)}{\partial \ln(\omega)} \cdot \frac{t_{ox}}{t_{ox} - x}
\end{aligned} \tag{4.17}$$

Note that ω is related to x by equation 4.3 and that N_{bt} has the unit of $eV^{-1}cm^{-3}$.

If the frequency dispersion of g_m is assigned to interface traps, the same expression may be used to find D_{it} by integrating in the x-direction. Since interface traps are considered to be located at the oxide-semiconductor interface, the density of traps should, in this case have a peak at $x = 0$, which would correspond to $\omega_{it,n}$.

4.2.2 $N_{bt}(x)$ in InAs nanowire MOSFETs with different high-κ

The AC transconductance method is applied to two different InAs nanowire MOSFETs with nanowire diameter of about 35 nm to deduce $N_{bt}(x)$. The gate dielectric in the two devices are, 80 cycles (c) of HfO_2 deposited at 250°C and annealed after high-κ deposition at 300°C for 30 min in forming gas, and 10c/50c Al_2O_3/HfO_2 deposited at 250°C/100°C and annealed after gate metal deposition at 300°C for 2 min in forming gas. The detailed processing scheme is presented in Paper II and Paper VII, respectively. For the Al_2O_3/HfO_2-nwMOSFET, a contact layout with pad gate and finger drain contacts was used. This combination gave the highest ω_{lim} for deducing $g_m(\omega)$ due to the comparably low R_g and C_{gd}. A few metrics for the two devices are summarized in table 4.1.

	DC-g_m (mS/μm)	f_{max} (GHz)	C_{gs}/C_{gd} (fF)	$R_s/R_d/R_g$ (Ω)
HfO_2-nwMOSFET	0.16	12	59/27	30/25/15
Al_2O_3/HfO_2-nwMOSFET	0.81	108	81/6.5	1/4/6

Table 4.1: Comparison of a few metrics of the two vertical InAs nanowire MOSFETs used for border trap extraction.

Figure 4.4 shows the frequency dependence of $\mathrm{Re}(Y_{21})$ after subtracting R_s and R_d as well as the deduced $N_{bt}(x)$ using equation 4.17. Here, $C_{ox} = 3.54$ μF/cm^2, $\lambda = 1.1 \cdot 10^8$ cm, $\tau_0 = 4 \cdot 10^{-11}$ s was used for both gate stacks. Furthermore, g_{mi} was approximated by the maximum in $\mathrm{Re}(Y_{21})$ for each bias point. For practical applications of this method, the frequency of the maximum in $\mathrm{Re}(Y_{21})$ may be considered as the frequency limit of the method. Extraction of $N_{bt}(x)$ beyond this frequency were $g_m(\omega)$ has a negative slope would require very precise knowledge of the small-signal model as $\mathrm{Re}(Y_{21})$ is, here, a combination of $g_m(\omega)$ and other terms. As a consequence, the deduced $N_{bt}(x)$ in figure 4.4 is only valid roughly above 0.4 nm for the HfO_2-nwMOSFET and 0.3 nm for the Al_2O_3/HfO_2-nwMOSFET.

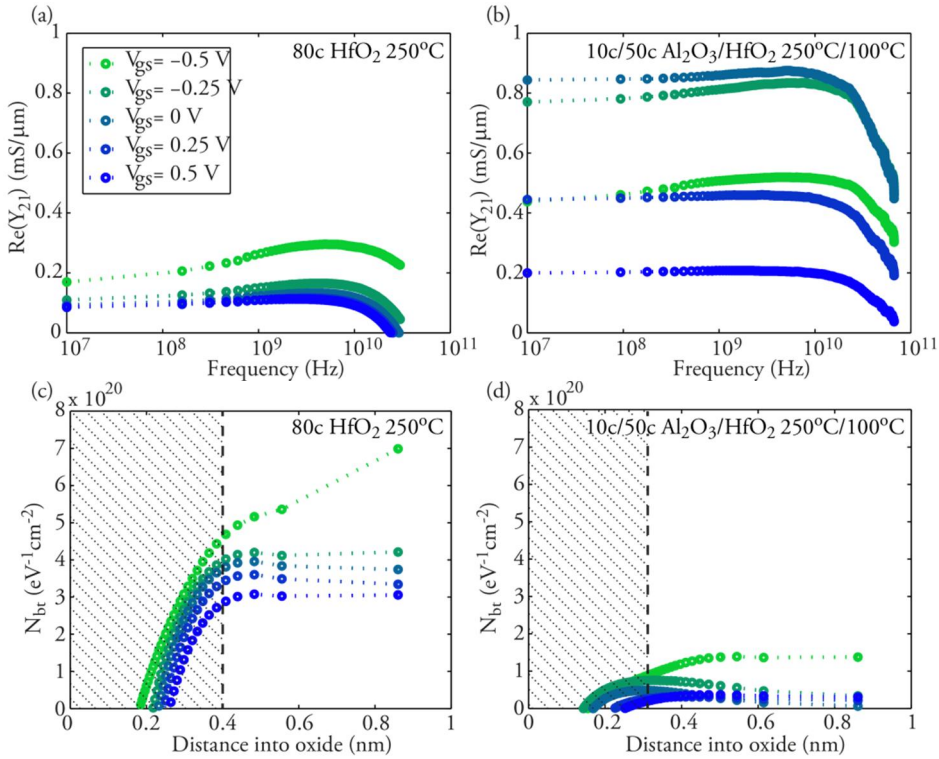


Figure 4.4: (a) and (b) depicts Re(Y_{21}) as a function of frequency for the HfO_2-nwMOSFET and the Al_2O_3/HfO_2-nwMOSFET, respectively. Biasing of V_{ds} = 0.75 V was used for the HfO_2-nwMOSFET and V_{ds} = 0.8 V was used for the Al_2O_3/HfO_2-nwMOSFET. (c) and (d) depicts the deduced $N_{bt}(x)$ for the two devices using equation 4.17. The shaded area approximately marks the region where the extraction is inaccurate.

The deduced $N_{bt}(x)$ is comparable to the data reported for nwMOSFETs in Paper V. The V_{gs} dependence reveals a slightly decreasing $N_{bt}(x)$ as the probed energy level is moved further up in the bandgap of the dielectric. Moreover, the deduced $N_{bt}(x)$ is larger for the HfO_2-nwMOSFET than for the Al_2O_3/HfO_2-nwMOSFET. The better quality of the Al_2O_3/HfO_2 gate stack is assigned to the use of PMA instead of PDA, the lowered deposition temperature for the HfO_2 film, the use of an Al_2O_3 interface layer or a combination of these reasons.

4.2.3 Border traps in surface-channel InGaAs MOSFETs

In paper V, the AC transconductance method was employed to an $In_{0.53}Ga_{0.47}As$ surface-channel MOSFET. The device has similar high-κ and f_{max} as the nwMOSFET in figure 4.4 b and d. One difference, however, is that the surface-channel MOSFET

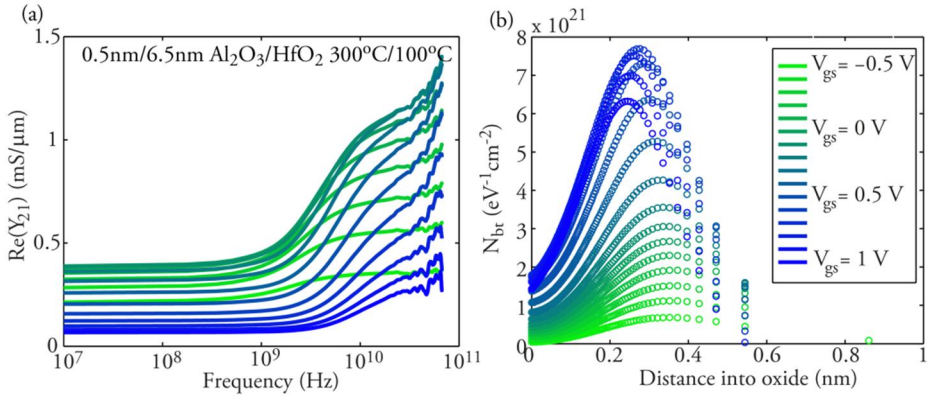


Figure 4.5: (a) $g_m(f)$ and (b) $N_{bt}(x)$ for a surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET at V_{ds} = 0.55 V. $N_{bt}(x)$ is deduced using equation 4.17.

was treated by sulfur passivation prior to high-κ deposition. In figure 4.5, $g_m(f)$ and $N_{bt}(x)$ is plotted for the device at different gate voltages using the same λ and τ_0 as for the nwMOSFET, *i.e.* $\lambda = 1.1 \cdot 10^8$ cm, $\tau_0 = 4 \cdot 10^{-11}$ s. A remarkably large increase in g_m is observed, which indicate a poor high-κ quality. The steep slope at about 10 GHz gives a peak in the deduced $N_{bt}(x)$ close to the oxide-semiconductor interface. The peak could be interpreted either as border traps or interface traps, or possibly as defects in the Al_2O_3/HfO_2 interface. The exact position of the peak depends on the values used for λ and τ_0. Furthermore, integrating with respect to x gives a density of 10^{13}-10^{14} $eV^{-1}cm^{-2}$.

In this example, $N_{bt}(x)$ increase strongly with V_{gs} implying that $N_{bt}(x)$ increases as the probed energy moves further up into the bandgap of the dielectric. This is opposite to the trend observed for the nanowire MOSFET. The number of traps is also up to 100 times larger, but the probed region is located closer to the oxide-semiconductor interface. It cannot be excluded that a similar peak would be observed also for the nanowire MOSFET if it was possible to deduce $N_{bt}(x)$ closer to the interface in this device.

4.2.4 Effects of InP interfacial layer

Addition of an InP interface layer between the InGaAs channel and the high-κ gate dielectric have demonstrated improved device performance attributed to reduced scattering caused by interface traps [82, 83]. In Paper VI, $In_{0.53}Ga_{0.47}As$ surface-channel MOSFET with two different gate stacks were compared using the AC transconductance method; one with an InP cap and one with high-κ directly on the InGaAs channel. The transconductance deduced at different frequencies is plotted as a function of V_{gs} for the two devices in figure 4.6. Here, the transconductance at

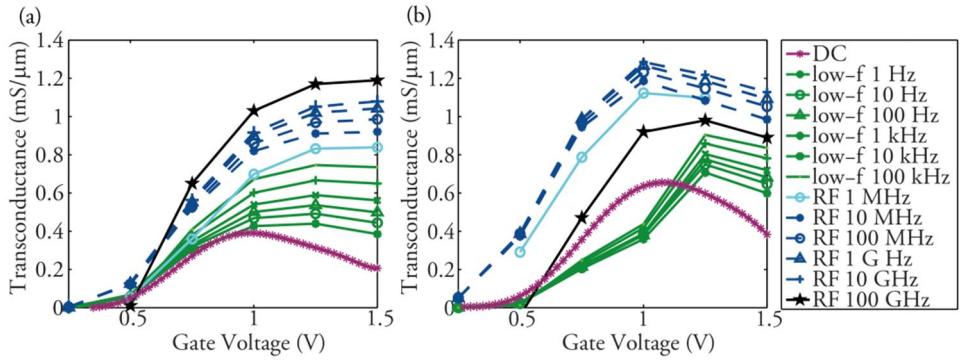


Figure 4.6: Transconductance as a function of frequency for the device without InP cap in (a) and with InP cap in (b). The DC-g_m is from the transfer characteristics, the low-f g_m is measured using a lock-in amplifier, and the RF-g_m is measured using network analyzers with different frequency ranges and approximating g_m as Re(Y_{21}).

100 GHz, measured by a PNA-X from Agilent with extenders from 75 GHz to 110 GHz, is added to the data published in Paper VI. For the device without InP cap the trend with increasing g_m, especially at high V_{gs}, continues at 100 GHz, which implies a high density of traps very close to the semiconductor-oxide interface. For the device with InP cap, however, g_m is decreasing with frequency at 100 GHz.

The resulting $N_{bt}(x)$ is somewhat higher for the device without InP cap and a peak in $N_{bt}(x)$ close to the oxide-semiconductor interface is observed, which is not found for the device with an InP cap. Ideally, no charge carriers should occupy a high quality InP cap, which would imply an epitaxial interface without defects. Hence, the absence of the peak in $N_{bt}(x)$ for the device with InP cap was expected.

As a final comment, the most important finding in these measurements is the huge increase in g_m with frequency throughout the entire frequency range. The measurements imply that GHz frequencies should be considered when characterizing the high-κ integration on III-V semiconductors. Another consequence of this is that the RF performance may be much better than what is expected from the DC measurements since f_t depends on the transconductance at f_t, which could be substantially larger than the DC-g_m due to the trap response.

5. Conclusion and Outlook

In the work of this thesis, high-frequency operation of vertical nanowire transistors was demonstrated for the first time. By developing the fabrication scheme and design, the high-frequency performance was greatly improved, and is now, with f_t and f_{max} above 140 GHz at L_g = 150 nm, comparable to established RF technologies. As opposed to a majority of the RF technologies, the vertical InAs nanowire high-frequency transistors are integrated on Si substrates, which could be an advantage for possible commercialization in terms of cost, wafer size, and co-integration with other Si-based technologies.

The fundamental scientific question concerns the potential of the vertical nanowire geometry for transistor applications. Compared to planar and semi-planar transistors, the improved scalability is one of the greatest advantages. Here, the device footprint is decoupled from the length of the contacts, which could be beneficial when increasing the transistor density and when operating in the ballistic regime. Moreover, epitaxial growth of nanowires allows for axial and radial heterostructures which are resilient to lattice mismatch and could be utilized to realize new epitaxial structures.

However, the novelty of the field leads to non-ideal device characteristics. For the vertical InAs nanowire MOSFET, great boost in the DC and RF performance is still expected through optimization of the device processing and design. One aspect that was not the focus of this thesis, but needs further improvement is to reduce the power consumption of the device. Improving the quality of the high-κ integration by reducing the number of traps would enhance both the ON-performance (g_m) and the OFF-performance (SS), and is one of the key challenges, not only for nanowire devices, but for any III-V MOSFET.

Targeting the challenge of the high-κ integration, this thesis presents a method for characterization of border traps directly from measurements of $g_m(f)$ using an analytical expression. For the first time, $g_m(f)$ at high frequencies, *i.e.* up to 100 GHz, was considered when deducing the number of border traps. The remarkably large

increase in g_m at GHz-frequencies implies that the high frequencies cannot be neglected. Furthermore, the simple use of the method makes it easy to implement in the standard protocol for groups that characterize high-frequency performance of III-V MOSFETs. In future work, the method could be extended, *e.g.* to include also interface traps.

Despite the challenges facing the vertical InAs nanowire MOSFET, commercial products might be considered relatively soon for analog applications if the RF performance continues to improve. Already, the first circuit using vertical InAs nanowires have been demonstrated by an active single balanced down-conversion mixer [84, 85].

Appendix - Processing Recipes

This appendix provides a detailed recipe for fabrication of high-frequency vertical InAs nanowire MOSFETs. The aim is to give the interested reader guidance on how processing is performed both before growing nanowires and after. The epitaxial growth, however, is not described in detail.

Pre-Nanowire Growth Processing

Substrate preparation

A highly resistive Si (111) 4 inch wafer is cleaned by a standard RCA cleaning method.

A 250 nm thick InAs layer is epitaxially grown by MOVPE using trimethylindium (TMIn) and arsine (AsH_3), which is n-type doped using tetraethyl (TESn). Good crystal quality is achieved by growing 4 nucleation layers at 350°C and annealing at 600°C. Subsequently, growth is continued at 600°C.

The wafer is cleaved into 2 cm × 2 cm pieces.

Au seed particle definition

Sample cleaning:

- Clean in acetone heated to 50 °C for ~3 min, rinse in IPA for ~3 min

Applying resist:

- Pre-bake for ~1 min on hotplate at 180°C
- Apply PMMA 200 A5:anisole 1:1 and spin on at 6000 rmp for 30 s. A recipe that ramps up the speed for a few seconds gives the best coverage.
- Bake in an oven at 180°C for 45 min.
- Apply PMMA 950 A4 and spin on at 6000 rpm for 30 s. This time, a recipe without ramping is preferable as this gives the desired resist thickness.
- Bake in oven at 180°C for 45 min.

Patterning resist:

- Load the sample into the EBL (Raith 150)
- Set up for exposure with an acceleration voltage of 20 kV and an aperture size of 10 μm. Good focus is achieved by burning contamination spots and performing 3-point adjustment with automatic focus correction enabled.
- Use a position list with single pixel dots at the nanowire position. A dose of 9 fAs gives a nanowire diameter of about 38 nm for zigzag arrays with 200 nm nanowire pitch. At the outermost dots of the zigzag array, double dose can be used to give nanowires with about the same length.
- Develop in MIBK/IPA 1:3 for 90 s, rinse in IPA for 30 s
- Check that the exposure was successful with optical microscope

Au deposition:

- Clean the sample by 15 s ashing in Plasma Preen with cage
- Remove native oxide by wet etching in $HCl:H_2O$ 1:1 for 1 min, rinse in water for ~1 min
- Evaporate 150 Å Au in Pfeiffer Classic 500 at a deposition rate of 1 Å/s

Lift-off:

- Prepare 3 beakers of acetone heated to 50°C and 2 beakers of IPA for each sample
- Leave the sample in the first acetone beaker until the surface of the sample has completely shifted color from blue to brown plus 1 min. Agitate and use squeeze bottle to rinse and move to the next beaker.
- Leave the sample in the second acetone beaker until lift-off is complete
- The third acetone beaker removes possible residues that one cannot detect by eye. Leave the sample for ~5 min.
- Rinse the sample in the first IPA beaker for ~20 s and then the second for ~5 min

Cleaving samples:

- Scribe the sample into 1 cm x 1 cm pieces
- Cleave by placing the sample on a ridge and applying vertical force with tweezers
- Rinse with IPA to remove particles from the scribing

Cleaning before nanowire growth:

- Clean the sample by 15 s ashing in Plasma Preen with cage
- Remove native oxide by wet etching in $HCl:H_2O$ 1:1 for 1 min, rinse in water for ~1 min
- Rinse in IPA for ~2 min

Nanowire Growth

InAs nanowires are grown by MOVPE at 420°C using TMIn and AsH_3. TESn is added to give n-type Sn doping. The growth is continued until the length of the nanowires is about 500 nm.

The nanowires are inspected by SEM. This is normally done after high-κ deposition.

Post-Nanowire Growth Processing

Gate dielectric

High-κ deposition:

- Transfer the samples to the ALD chamber (Savannah-100) for high-κ deposition directly after growth

Deposit 10 cycles Al_2O_3 at 250°C using TMA and water precursors and 50 cycles HfO_2 at 100°C using TDMA Hf and water precursors

High-κ patterning:

- Spin on S1813 at 4000 rpm for 60 s
- Soft-bake at 115°C for 90 s
- Use the MJB4 (soft UV) mask aligner and align the sample to a UV mask with source pads

- Expose for 6 s
- Develop in MF319 for 40 s
- Inspect the result by optical microscopy
- Hard-bake at 120°C for 15 min
- Clean the surface by ashing in Plasma Preen for 30 s
- Etch in BOE 1:10 for 7 min, rinse in water for 20 s in one beaker and for at least 1 min in a second beaker
- Remove the resist by 30 s ashing in Plasma Preen and clean in acetone for ~5 min at RT, rinse in IPA for ~1 min

Source-gate spacer

Si_3N_4 deposition:

- Deposit a conformal film of 60 nm Si_3N_4 by PECVD

Si_3N_4 etch-back:

- Spin on S1818 at 4000 rpm for 60 s
- Hard-bake at 120°C for 15 min
- Etch-back the resist by RIE (Trion T2) for ~20 min using an O_2 flow of 15 sccm, an RF power of 50 W and a chamber pressure of 300 mTorr
- Inspect the sample by SEM. The resist thickness should be ~150 nm close to the nanowires.
- Etch-back the resist for some additional time if needed. The etch rate is ~50 nm/min.
- Etch the Si_3N_4 on the nanowires by RIE (Trion T2) using an SF_6 flow of 45 sccm, an Ar flow of 5 sccm, RF power of 140 W and a chamber pressure of 160 mTorr. The etch time increase almost linearly with the nanowire length and is ~20 s for a length of 400 nm. Precondition the chamber by running the same recipe, possibly following a pre-cleaning step using oxygen plasma.
- Remove the resist by 45 s ashing in Plasma Preen and clean in acetone for ~5 min at RT, rinse in IPA for ~1 min

Gate definition and device isolation

W deposition:

- Deposit 700 Å W by sputtering (AJA Orion 5) using a power of 150 W

W, Si_3N_4 and InAs patterning:

- Spin on PMMA 950 A4 at 2000 rpm for 60 s
- Soft-bake at 180°C for 5 min
- Use the Karl Süss MJB 4 (deep UV) mask aligner and align the sample to a UV mask with gate pads
- Expose for 9×90 s
- Develop in MIBK/IPA 1:3 for 90 s and rinse in IPA for 30 s
- Set up for exposure in the EBL (Raith 150) with an acceleration voltage of 20 kV and an aperture size of 10 μm. Align the coordinate system globally using known positions on the sample, such as UV markers.
- Use automatic alignment on 3 markers in each write-field and expose a proximity corrected design (settings in proximity correction wizard: Advice for 500 nm PMMA on Si, acc. 4) and pattern 600-nm-wide finger gates at 90 $\mu C/cm^2$. The fingers need extend at least 1 μm outside the source pad to enable device isolation.
- Develop in MIBK/IPA 1:3 for 90 s, rinse in IPA for 30 s
- Etch W and Si_3N_4 by RIE (Trion T2) using an SF_6 flow of 45 sccm, an Ar flow of 5 sccm, RF power of 140 W and a chamber pressure of 160 mTorr for 45 s. Precondition the chamber by running the same recipe and possibly oxygen plasma.
- Etch InAs in H_3PO_4:H_2O_2:H_2O 1:1:25 for 6 min.
- Remove the resist by 45 s ashing in Plasma Preen and clean in acetone for ~5 min at RT, rinse in IPA for ~1 min

Gate length definition:

- Spin on S1813 at 4000 rpm for 60 s
- Hard-bake at 120°C for 15 min
- Etch-back the resist by RIE (Trion T2) for ~15 min using an O_2 flow of 15 sccm, an RF power of 50 W and a chamber pressure of 300 mTorr
- Inspect the sample by SEM. The resist thickness should be ~120 nm close to the nanowires.
- Etch-back the resist for some additional time if needed. The etch rate is ~50 nm/min.

- Etch W by RIE (Trion T2) using an SF_6 flow of 45 sccm, an Ar flow of 5 sccm, RF power of 140 W and a chamber pressure of 160 mTorr for 45 s. Precondition the chamber by running the same recipe and possibly oxygen plasma.
- Remove the resist by 45 s ashing in Plasma Preen and clean in acetone for ~5 min at RT, rinse in IPA for ~1 min
- Inspect the gate length by SEM

Post metallization annealing:

- Anneal the sample at 300°C for 2 min in forming gas using RTP 1200 from UniTemp. It is preferable to use ramping of the temperature to avoid a temperature overshoot.

Gate-drain spacer

Applying an organic spacer:

- Spin on S1813 at 4000 rpm for 60 s
- Permanent-bake at 200°C for 45 min

Etch-back of spacer:

- Etch-back the resist by RIE (Trion T2) for ~13 min using an O_2 flow of 15 sccm, an RF power of 50 W and a chamber pressure of 300 mTorr
- Inspect the sample by SEM. The resist should be ~120 nm above the wrap-gate.
- Etch-back the resist for some additional time if needed. The etch rate is ~60 nm/min.

Forming vias:

- Spin on S1813 at 4000 rpm for 60 s
- Soft-bake at 115°C for 90 s
- Use the MJB4 (soft UV) mask aligner and align the sample to a UV mask with gate vias
- Expose for 7 s
- Develop in MF319 for 40 s
- Inspect the result by optical microscopy
- Use the MJB4 (soft UV) mask aligner and align the sample to a UV mask with source vias

- Expose for 7 s
- Develop in MF319 for 40 s
- Hard-bake at 120°C for 15 min
- Etch the gate-drain spacer in the openings by RIE (Trion T2) for ~10 min using an O_2 flow of 15 sccm, an RF power of 50 W and a chamber pressure of 300 mTorr
- Strip the hard-baked resist in acetone for ~5 min at RT, rinse in IPA for ~1 min

Top contact

W deposition:

- Etch the high-κ on the top part of the nanowires and in the source vias in BOE 1:10 for 8 min, rinse in water for 20 s in one beaker and for at least 1 min in a second beaker
- Immediately transfer the sample to the sputterer (AJA Orion 5)
- Deposit 700 Å W by sputtering using a power of 150 W

W patterning:

- Spin on PMMA 950A4 at 2000 rpm for 60 s
- Soft-bake at 180°C for 5 min
- Use the Karl Süss MJB 4 (deep UV) mask aligner and align the sample to a UV mask with probing pads
- Expose for 9×90 s
- Develop in MIBK/IPA 1:3 for 90 s and rinse in IPA for 30 s
- Set up for exposure in the EBL (Raith 150) with an acceleration voltage of 20 kV and an aperture size of 10 μm. Align the coordinate system globally using known positions on the sample, such as UV markers.
- Use automatic alignment on 3 markers in each write-field and expose a proximity corrected design to pattern 600-nm-wide finger drains at 90 $\mu C/cm^2$.
- Develop in MIBK/IPA 1:3 for 90 s, rinse in IPA for 30 s
- Etch W by RIE (Trion T2) using an SF_6 flow of 45 sccm, an Ar flow of 5 sccm, RF power of 140 W and a chamber pressure of 160 mTorr for 45 s.

Precondition the chamber by running the same recipe and possibly oxygen plasma.

- Remove the resist by 45 s ashing in Plasma Preen and clean in acetone for ~5 min at RT, rinse in IPA for ~1 min

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