Low-Power Nanowire Circuits and Transistors

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Low-Power Nanowire Circuits and Transistors

Doctoral Thesis

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How hard can it be?
- Jeremy Clarkson

Abstract

This thesis explores several novel material systems and innovative device concepts enabled by nanowire technology. State-of-the-art fabrication techniques such as electron beam lithography and atomic layer deposition are utilized to achieve high control and quality in the device fabrication. The devices in this thesis are based on two main types of design geometries, lateral and vertical, each of which have strengths and weaknesses. The first part of the thesis describes the goals of future metal–oxide–semiconductor field-effect transistors (MOSFETs) and discusses the ultimate scalability surrounding experimental results for 15-nm-diameter InAs nanowires and how they compare to other state-of-the-art transistors. The extracted ON-resistance ($R_{on} = 250\,\Omega{\cdot}\mu m$) and drive currents ($I_{on} = 1250\,\mu A/\mu m$) are comparable to state-of-the-art high-electron-mobility transistors (HEMTs) from MIT and quantum-well field-effect transistors from Intel. The outstanding performance is mainly attributed to the reduced access resistance achieved through an n^+-i-n^+ doping profile. The extracted mobilities also agree well with state-of-the-art and theoretical predic-

tions for extremely scaled devices.

The second part of the thesis discusses how nanowires may be employed to enable III-V complementary metal–oxide–semiconductor (CMOS) digital logic. Nanowires enable the formation of both n-type semiconductors and p-type semiconductors, which are a requirement for CMOS, in a single nanowire and allow for integration on a Si platform. III-V MOSFETs are frequently employed for analog applications, but there is a disconnect regarding p-type devices, which are also required for digital logic. The individual segments of the nanowire are evaluated as well as the entire nanowire in an inverter configuration. This thesis then presents a strategy for matching the drive currents n- and p-type MOSFETs.

The final part of the thesis deals with a family of devices that operate according to principles fundamentally different from those of a traditional MOSFET, namely tunnel FETs (TFETs). There is a demand for steep-slope devices such as TFETs to enable supply-voltage scaling to reduce the power dissipation. Although devices have demonstrated $<$60 mV/decade operation, they commonly suffer from low ON-currents. To maximize the drive current, the broken band gap alignment of GaSb/InAs is exploited to allow for a direct tunneling mechanism. The material system is first explored as Esaki diodes and in various doping profiles to understand the influence of doping on device performance. The devices are further evolved into TFETs by the addition of a high-κ gate dielectric and an additional terminal. Experimental results display high ON-currents of $I_{on} = 310\,\mu\text{A}/\mu\text{m}$ comparable to other state-of-the-art TFETs. Finally, an innovative design concept combining axial and radial heterostructures is utilized to design a radial TFET with a small footprint. A radial GaSb/InAs core/shell TFET provides an attractive way to increase the drive current of a TFET without compromising either device electrostatics or chip area. The functionality of radial Esaki diodes and TFETs is demonstrated and evaluated by the maximum peak currents, which

are much improved as compared to their axial counterparts when normalized to the largest cross-sectional area of the nanowire, assuming a vertical device geometry, illustrating the advantage of a core–shell architecture. The dimensions of the InAs shells are below 15-nm and display clear quantization effects revealed in low-temperature electrical characterization.

Populärvetenskaplig sammanfattning

Hur hade vår värld sett ut utan den teknologiska revolutionen som skett de senaste decennierna? Inget internet, inga mobiltelefoner, inga surfplattor? Drivkraften bakom att det hela är en väldigt liten beståndsdel som sitter i nästan all elektronik, den så kallade *transistorn*. En transistor kan se lite olika ut men är i stora drag en elektrisk komponent där man styr strömmen mellan två kontakter med hjälp av en tredje kontakt kallad för gate eller styre. Man kommer inte så långt med bara en transistor men när man börjar närma sig ett antal miljarder så kommer man upp i antalet transistorer som sitter i en modern processor.

Redan 1925 patenterades den första transistorn av Julius Edgar Lilienfeld men eftersom uppfinnaren inte skrev om sin upptäckt i några vetenskapliga tidsskrifter så uppmärksammades inte upptäckten. Det var inte förrän 1947 då William Shockley, John Bardeen och Walter Brattain på AT&T Bell Labs byggde en fungerande transistor baserad på Lilienfelds patent som halvledarutvecklingen verkligen började ta fart. Det kontinuerliga kravet på allt snabbare och energisnålare elek-

tronik i allt mindre och mindre format har rullat på i ett par decennier enligt en förutsägelse från Gordon Moore, en av Intels grundare, som förutspådde ett samband, att antalet transistorer på ett chip skulle fördubblas var 18:e månad. Denna förutsägelse kallas för Moores lag och har hittils följts väldigt väl. Denna 'lag' är något som halvledarindustrin nu börjat oroa sig för då dimensionerna på transistorerna snart börjar närma sig atomära dimensioner. På den skalan börjar kvantfenomen som t.ex. tunnling ställa till med bekymmer. Tunnling är ett fenomen som gör att strömmen t.ex. kan hoppa genom en isolator som den i vanliga fall inte ska kunna göra vilket i sin tur förstör funktionaliteten man har byggt upp i sin processor.

Ett mer angeläget bekymmer idag handar om effektförbrukningen och i förlängningen värmeutvecklingen på ett chip vilket har följt naturligt av Moores Lag. Det är väldigt många transistorer som ska samsas om ytan och den värme som de utvecklar måste ta vägen någonstans. Detta syns väldigt tydligt i utvecklingen idag då både datorer och bärbara enheter som t.ex. mobiltelefoner som istället för ökade klockfrekvenser utrustas med fler processorer som jobbar vid en något lägre frekvens. Denna avhandling behandlar ett antal idéer och koncept på hur man skulle kunna fortsätta halvindustins fantastiska resa och som ibland kallas för 'more than Moore'.

Majoriteten av all elektronik idag är kiselbaserad eftersom kisel är mycket vanligt och återfinns som kiseloxid i naturen i t.ex. sand och lera, och är därför väldigt billigt. Kiseltekonologin är mycket välutvecklad men kisel som material har sina begränsningar. Man pratar ofta om elektronmobilitet när man pratar om halvledarmaterial och det är en egenskap som beskriver hur lätt det är för elektroner, eller ström, att flyta i materialet. Man kan t.ex. använda lite mer exotiska material som t.ex. indiumarsenid, InAs, där elektronerna kan röra sig över 20 gånger lättare än i kisel. Är det mycket lättare att flytta elektronerna behöver man inte lika mycket energi för att få igenom motsvarande ström som i en kiseltransistor och alltså blir även effek-

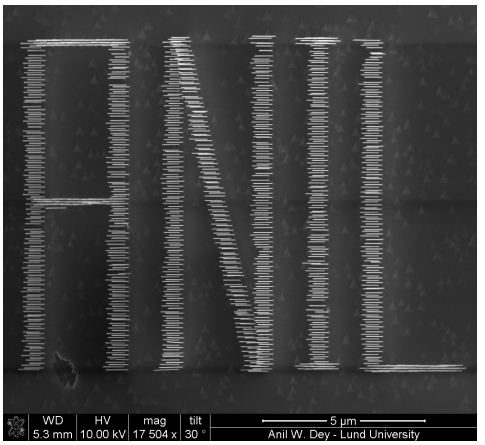

Figure 1: *En matris av InAs nanotrådar som har växt på ett kiselsubstrat. InAs förträffliga egenskaper är väl lämpade för att tillverka transistorer som är bättre än motsvarande i kisel.*

tförbrukningen lägre. Vill man ta det hela steget längre så behöver man byta designgeometri på sin transistor. Denna utvecklingen har gått från planära eller 'platta' transistorer till dagens transistorer som ser ut som fenor. Vill man sedan förbättra sin transistor ytterligare så formar man sin transistor som en nanotråd vilket ytterligare ökar effektiviteten på transistorn.

Det finns en familj av transistorer, så kallade tunneltransistorer, där man utnyttjar tunnlingsfenomenet till sin fördel. Genom att kombinera väl valda material med varandra kan man se till att styra tunnlingsströmmen med hjälp av en gate, men med en mycket lägre energiförbrukning eftersom tunneltransistorerna är lättare att stänga av än mer konventionella transistorer.

Denna avhandling omfattar ett antal nya material- och komponentkoncept inom 'more than Moore' och ger en inblick i teknologier som

framtidens transistorer skulle kunna vara baserade på.

List of papers

MOSFETs

I. High-Performance InAs Nanowire MOSFETs
A. W. Dey, C. Thelander, E. Lind, K. Dick Thelander, M. Borg, M. Borgström, P. Nilsson, L.-E. Wernersson
Electron Device Letters, IEEE, **33**, 791-793 (2012)
I fabricated the sample, did the measurements and data analysis and wrote the paper.

II. Vertical InAs nanowire wrap gate transistors with $f_t > 7$ GHz and $f_{max} > 20$ GHz
M. Egard, S. Johansson, A. C. Johansson, K. M. Persson, A. Dey, M. Borg, C. Thelander, L. E. Wernersson, E. Lind
Nano Letters, **10**, 809-812 (2010)
I developed parts of the device processing and was actively involved in discussions regarding the paper. I did some of the electrical measurements and helped to write the paper.

III-V CMOS

III. Single InAs/GaSb Nanowire Low-Power CMOS Inverter
A. W. Dey, J. Svensson, M. Borg, M. Ek, L.-E. Wernersson
Nano Letters, **12**, 5593-5597 (2012)
I fabricated the sample. Johannes Svensson and I did the measurements and data analysis and wrote the paper.

Diodes and TFETs

IV. Combining axial and radial nanowire heterostructures: Radial Esaki diodes and tunnel field-effect transistors
A. W. Dey, J. Svensson, M. Ek, E. Lind, C. Thelander and L.-E. Wernersson
Submitted *Nano Letters*, **xx**, xxxx-xxxx (2013)
I fabricated the samples, did the measurements and data analysis and wrote the paper.

V. High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors
A. W. Dey, B. M. Borg, B. Ganjipour, M. Ek, K. A. Dick, E. Lind, C. Thelander, and L.-E. Wernersson
Electron Device Letters, IEEE, **34**, 211-213 (2013)
I fabricated the sample, did the measurements and data analysis and wrote the paper.

VI. High current density Esaki tunnel diodes based on GaSb-InAsSb heterostructure nanowires
B. Ganjipour, A. Dey, M. Borg, M. Ek, M. E. Pistol, K. Dick Thelander, L. E. Wernersson, C. Thelander
Nano Letters, **11**, 4222-4226 (2011)
I developed parts of the device processing and measurement setup and was actively involved in discussions regarding the paper and I helped write the paper.

VII. Influence of doping on the electronic transport in GaSb/InAs(Sb) nanowire tunnel devices
M. Borg, M. Ek, B. Ganjipour, A. Dey, K. Dick, L. E. Wernersson, C. Thelander
Applied Physics Letters, **101**, 043508 (2012)
I developed parts of the device processing and measurement setup and was involved in discussions regarding the paper and helped to write the paper.

Additional Papers

Other papers have also been published but are not included because they deal with subjects beyond the scope of this thesis or have overlapping contents.

viii. 15 nm diameter InAs nanowire MOSFETs (accepted as oral presentation)
A. Dey, C. Thelander, M. Borgström, M. Borg, E. Lind, L. E. Wernersson
69th Annual Device Research Conference (DRC), Santa Barbara, CA, USA, 21-22, 2011-06-20

ix. High Current Density InAsSb/GaSb Tunnel Field Effect Transistors (accepted as oral presentation)
A. Dey, M. Borg, B. Ganjipour, M. Ek, K. Dick Thelander, E. Lind, P. Nilsson, C. Thelander, L. E. Wernersson
70th Annual Device Research Conference (DRC), University Park, PA, USA, 205-206, 2012-06-18

x. GaSb nanowire pFETs for III-V CMOS (accepted as oral presentation)
A. Dey, J. Svensson, M. Borg, M. Ek, E. Lind, L.-E. Wernersson
71th Annual Device Research Conference (DRC), Notre Dame, IN, USA, 13-14, 2013-06-24

xi. Self-seeded, position-controlled InAs nanowire growth on Si: A growth parameter study
B. Mandl, A. Dey, J. Stangl, M. Cantoro, L. E. Wernersson, G. Bauer, L. Samuelson, K. Deppert, C. Thelander
Journal of Crystal Growth, **334**, 51-56 (2011)

xii. Growth Mechanism of Self-Catalyzed Group III-V Nanowires
B. Mandl, J. Stangl, E. Hilner, A. Zakharov, K. Hillerich, A. Dey, L. Samuelson, G. Bauer, K. Deppert, A. Mikkelsen
Nano Letters, **10**, 4443-4449 (2010)

xiii. Effects of Crystal Phase Mixing on the Electrical Properties of InAs Nanowires
C. Thelander, P. Caroff, S. Plissard, A. W. Dey, K. A. Dick
Nano Letters, **11**, 2424-2429 (2011)

xiv. Formation of the axial heterojunction in GaSb/InAs(Sb) nanowires with high crystal quality
Crystal Growth and Design, **11**, 4588-4593 (2011)
M. Ek, M. Borg, A. Dey, B. Ganjipour, C. Thelander, L. E. Wernersson, K. Dick Thelander

xv. Diameter reduction of nanowire tunnel heterojunctions using in situ annealing
M. Borg, M. Ek, K. Dick Thelander, B. Ganjipour, A. Dey, C. Thelander, L. E. Wernersson
Applied Physics Letters, **99**, 203101 (2011)

xvi. Low-frequency noise in vertical InAs nanowire FETs
K. M. Persson, E. Lind, A. Dey, C. Thelander, H. Sjöland, L. E. Wernersson
Electron Device Letters, IEEE, **31**, 428-430 (2010)

xvii. Laboratory instructions as a cause of student dissonance
A. Dey, M. Hell, C. C. Rolf, P. Stankovski, M. Ågren
LTHs 6:e Pedagogiska Inspirationskonferens, Lund, Sweden, 2010-12-15

xviii. High-performance 15 nm diameter InAs nanowire Ω-gate MOSFETs (accepted as oral presentation)
A. Dey, C. Thelander, E. Lind, M. Borgström, M. Borg, P. Nilsson, L. E. Wernersson
GigaHertz 2012, Stockholm, Sweden, 2012-03-06

xix. Vertical InAs nanowire wrap gate transistors for integration on a Si platform
A. Dey, M. Egard, S. Johansson, A. C. Johansson, K. M. Persson, M. Borg, C. Thelander, P. Nilsson, H. Sjöland, E. Lind, L. E. Wernersson
GigaHertz 2010, Lund, Sweden, 2010-03-09

xx. High Frequency Performance of Vertical InAs Nanowire MOSFET
E. Lind, M. Egard, S. Johansson, A. C. Johansson, M. Borg, C. Thelander, K. M. Persson, A. Dey, L. E. Wernersson
22nd International Conference On Indium Phosphide And Related Materials (IPRM), Kagawa, Japan, 2010-05-31

Patent Applications

xxi. Radial Nanowire Esaki Diode Devices and Methods
A. W. Dey, C. Thelander, L. E. Wernersson, E. Lind, J. Ohlsson, L. Samuelson, M. Björk
Patent Cooperation Treaty application PCT/US2013/049433, submitted to *European Patent Office (EPO)*, July 2013.
US provisional patent: No. 61/668,777

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Contents

CHAPTER 1

Background

The semiconductor industry has been on an incredible journey since 1947 when William Shockley, John Bardeen, and Walter Brattain at AT&T Bell Laboratories demonstrated the first point-conctact transistor. The transistor is regarded by many as the most important scientific achievement of the 20th century. The first transistor was large and bulky, but over the last few decades it has become so small that it can be depicted only with advanced instruments such as scanning electron microscopes (SEM). The intensive development in circuit miniaturization has provided an extensive toolset for fabrication and manipulation of nanometer-scale structures.

The scaling of the transistor dimensions has provided exponential improvements in, e.g., transistor density, performance, and power efficiency. Since 2003, Si complementary metal–oxide–semiconductor (CMOS) technology has entered a stage of power-constrained scaling, i.e., a power density saturation at approximately $100\,\mathrm{W/cm^2}$.[1–3] This

	a_0 (Å)	E_g (eV)	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)
Si	5.431	1.12	1400	450
Ge	5.658	0.661	3900	1900
GaAs	5.653	1.424	8500	400
GaSb	6.096	0.726	3000	1000
InP	5.869	1.344	5400	200
$In_{0.53}Ga_{0.47}As$	5.869	0.75	12000	300
$In_{0.7}Ga_{0.3}As$	5.937	0.588	20200	3-400
InAs	6.058	0.354	40000	500
InSb	6.479	0.170	77000	850

Table 1.1: *Lattice constant (a_0), band gap (E_g), and electron and hole mobility (μ_e and μ_h) for commonly used semiconductors.*[5]

has led to the introduction of multicore technology in mainstream computers and portable devices such as mobile phones and tablets. The dynamic power dissipation is proportional to the cube of the supply voltage V_{dd}, and thus a reduction would be attractive. However, the goals of scaling are to minimize the transistor dimensions while achieving a maximum ON-current I_{on} for a given OFF-current I_{off}. The concern is the diminished ON-performance of Si with a reduction in supply voltage.[4] To address this issue, the electron velocity could be increased, i.e., replacing Si with materials that have higher mobilities, such as graphene or III-V semiconductors, as displayed in Table 1.1. Alternatively, or in conjunction with high-mobility semiconductors, devices with the ability to modulate the current in a transistor faster than a traditional metal–oxide–semiconductor field-effect transistor (MOSFET), e.g., tunnel FETs (TFETs) may be introduced.

The drawback of high-mobility materials is the narrow band gap and low density of states. For CMOS, high mobilities are necessary

for both the nFETs and the pFETs; however, it is difficult to find such a combination (Table 1.1). Furthermore, in the interest of easier gate stack integration and device processing, the same semiconductor material would be preferred.[6] However, in terms of materials integration, specifically the integration of high-permittivity (high-κ) dielectrics, some materials may be suitable as nFETs while problematic as pFETs, or vice versa. It is possible to fabricate high-electron-mobility transistors (HEMTs) that exhibit excellent device metrics down to gate lengths of $L_g = 30\,\text{nm}$; however, further scaling will require the introduction of a high-κ dielectric because the gate starts to lose electrostatic control of the channel as the distance between the source and the drain decreases.[7] HEMTs offer a convenient model system to explore III-V semiconductors without needing to worry about the complications of a MOS stack. The take-home messages from HEMTs are (i) the high mobilities and injection velocities allow for high drive currents and near-ballistic operation for gate lengths below 50 nm, but (ii) scaling below 30 nm will require a MOS structure. The contact resistance is another figure of merit that must be much improved to conform to the demands of extremely scaled devices.

Currently, much research is being conducted into nanowires, which are semiconductors shaped as rod-like crystal structures grown from Au particles.[8–10] Chapter 2 provides more details on nanowire growth. These nanowires can be grown with high aspect ratios, i.e., diameters far below 100 nm and several microns long. This self-assembled bottom-up process is distinct from common practice in industry, where a top-down approach is generally employed to create nanoscale structures from bulk-like materials. Nanowires are not restricted to materials that can be grown in bulk or as layered structures and open up new opportunities to explore novel semiconductor materials and exotic heterostructures that are impossible to grow in bulk.[11]

From a device point of view, a nanowire is a semiconductor crystal that confines the movement of electrons in the radial direction and

allows free movement only along the main axis of the nanowire. This provides an intrinsic well-defined transport channel for the electrons. By introducing a capacitively coupled gate, electrostatically modulating the carrier density in the nanowire, the resistivity of a nanowire device can be controlled. A gate is particularly effective if placed around a cylindrical geometry[12] such as a nanowire channel and has been successfully demonstrated in nanowire MOSFETs.[13–16] The electrostatics of a nanowire geometry enable less stringent demands on the thickness of the gate dielectric than, e.g., planar transistors. The intrinsic confinement properties of nanowires may be advantageously employed for quantum devices.[17–19] The detrimental effect of a narrow band gap semiconductor may be alleviated in an extremely scaled nanowire.[20]

In summary, III-V CMOS has a number of challenges remaining. A suitable materials combination must be chosen that co-integrates n- and p-type devices together. A gate stack must be demonstrated with near-ideal properties for both material types. The access resistance to the devices must be much improved in order to deliver the performance required for extremely scaled devices.

Many of these challenges are suitably addressed by nanowires because nanowires can accommodate a wider variety of materials combinations than conventional bulk materials and allow for devices with ideal electrostatics in a gate-all-around (GAA) device architecture.

This thesis examines a number of novel materials and materials combinations as well as innovative device concepts that may or may not be incorporated when traditional CMOS fails.

Chapter 2 provides background information regarding nanowire growth and nanowire device fabrication in both lateral architectures and vertical architectures. The general concepts discussed in this chapter are relevant in all the listed papers to some extent.

Chapter 3 introduces some basic MOSFET theory and important figures of merit and discusses ultimate scaling based on experimental results on 15-nm-diameter InAs MOSFETs. This chapter also includes benchmarking against state-of-the-art transistors in various other technologies. The chapter provides a general background to papers I and II.

Chapter 4 concerns the implementation of n- and p-type semiconductors on the same chip, which is necessary for full III-V CMOS implementation. This chapter provides background information and summarizes the results of paper III.

Chapter 5 provides background information to papers IV–VII in terms of the underlying theory of tunneling. This chapter summarizes the results in papers IV–VII, discusses the results in a broader context, and provides benchmarking against state-of-the-art devices.

Chapter 6 discusses some insights gained over the years regarding academia and device research in general. There is also a short section discussing my view on beyond-CMOS technologies.

CHAPTER 2

Device fabrication

This chapter briefly introduces some of the processing technicalities and device designs employed in this thesis. This chapter also familiarizes the reader with the basics of nanowire growth. Two main processes have been used during this thesis: (i) lateral devices fabricated from single nanowires transferred to Si chips and (ii) devices and circuits designed in a vertical architecture from as-grown nanowires.

2.1 Nanowire growth

Before any nanowire devices can be fabricated, nanowires must of course be grown. The method employed for nanowire growth in this thesis is called metal-organic vapor-phase epitaxy (MOVPE), which is also known as metal-organic chemical vapor deposition (MOCVD). The main motivation for using MOCVD is a high degree of freedom

of available doping sources and good composition control.

A simplistic image of a MOCVD growth reactor is an oven into which gaseous semiconductor precursors are introduced. In the case of InAs nanowires, these precursors are usually trimethylindium (TMIn) and arsine (AsH_3) (see Fig. 2.1). There are two main methods of nanowire growth: (i) growth from Au seeds or from other metal particles such as Cu[21–24] or (ii) seed-particle free growth, also called selective-area growth, where nanowires instead nucleate from openings, e.g., in an oxide.[25–27] The primary method used for devices in this thesis is Au-assisted growth, because of the excellent composition control and the ample in-house knowledge on the subject. For lateral devices, where exact placement control is not required, the nanowires are grown from randomly dispersed Au aerosols. However, for vertical devices, where there are stringent demands on placement and particle density, electron beam lithography (EBL) is used to define the Au seeds followed by a thermal evaporation of Au and lift-off. This will be discussed further in the section on vertical devices (Section 2.3). After the formation of Au seeds, the sample is placed on the susceptor of the MOCVD reactor. The first step is an annealing stage at high temperature ($\approx$ 470–550 °C) to desorb unwanted materials from the surface and alloy the Au seed with the substrate. The temperature is then lowered to approximately 420 °C, and the metal-organic semiconductor precursors are introduced into the chamber. The precursors land on the surface and diffuse until they reach a Au seed, or they desorb again if no incorporation site can be found. Indium is incorporated into the particle, and as it becomes supersaturated, an InAs crystal starts to grow at the particle–substrate interface, forming a nanowire as the particle is lifted up. If doping incorporation is desired, the corresponding gases are also added to the reactor.[28] After the desired length of nanowire is reached, the reactor is cooled, and an AsH_3 overpressure is maintained in the reactor to prevent the Au particle from "consuming" the nanowire.

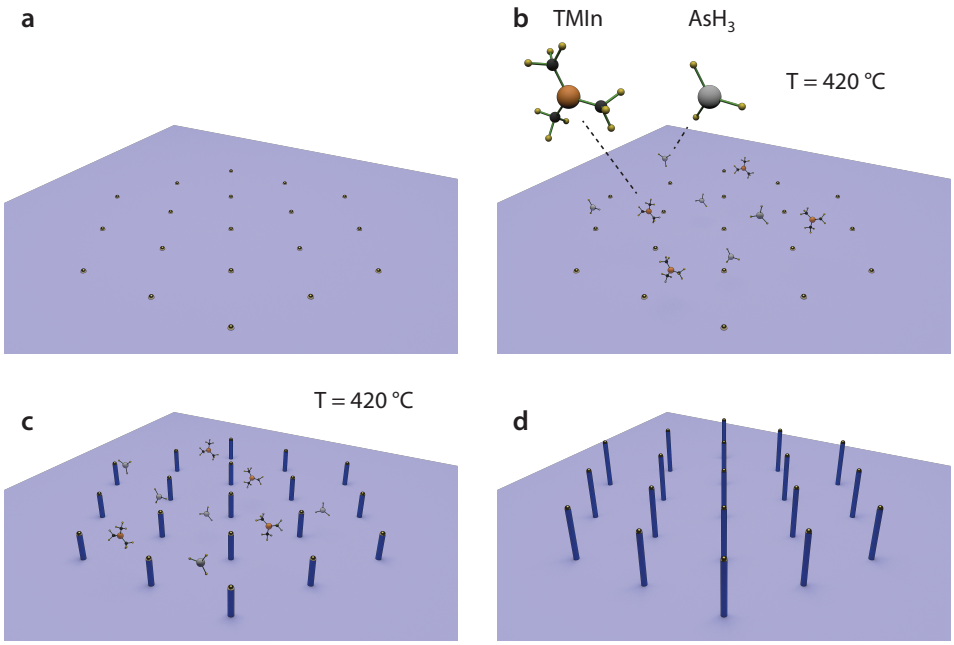


Figure 2.1: *Schematic nanowire growth. (a) Au seed particles are dispersed as aerosols on a substrate or defined by EBL followed by metal evaporation and lift-off. (b) The sample is placed in the MOCVD growth reactor, which is heated to 420°C, and metal-organic semiconductor precursors are supplied to the reactor chamber by a H_2 carrier gas. (c) For InAs nanowires, TMIn and AsH_3 decompose and diffuse, forming an InAs crystal below the Au seed. In the process, the Au seed is lifted up, and a nanowire begins to take shape below. (d) After the desired length has been achieved, the gas flows are turned off, with the exception of AsH_3. The temperature is then lowered, and the AsH_3 overpressure prevents the reaction from occurring in reverse, where the Au seed would "consume" the InAs nanowire.*

During the growth, it is possible to switch semiconductor materials abruptly, allowing for the formation of various heterostructures.[29] One of the main advantages of growing III-V semiconductors in the shape of a nanowire, compared with planar growth, is the ability to switch between materials with different lattice constants with a low probability of defect formation.[30] In contrast to planar growth, the strain due to mismatch in lattice constants between two materials can relax by radial expansion or contraction when grown in the shape of a nanowire.

2.2 Lateral devices

To evaluate the electrical properties of nanowires from various growth runs, for making circuits, devices are usually designed and fabricated in a lateral architecture.[28] Nanowires grown from an aerosol sample are dispersed onto a prepatterned Si chip with markers and with 100 nm of thermally grown SiO_2 by a dry-deposition technique, as illustrated in Fig. 2.2. Source and drain electrodes are patterned by EBL followed by thermal evaporation of a metal. Before the metal evaporation, the contact interface surface is treated to further reduce the contact resistance and remove any native oxide. The selection of surface treatment is dependent on the nanowire, but a short dip in buffered oxide etch HF:H_2O (1:10) has proven to work well for InAs nanowires. The choice of metal also depends on the semiconductor material. For InAs, Ni/Au or Ti/Au have proven to be suitable combinations, offering low resistive ohmic contacts to InAs. At this stage a two-terminal device is ready for electrical measurements. A two-terminal device has limited functionality and provides only a limited amount of information. A complete transistor must include a third input terminal: the gate.

Before the gate electrode can be fabricated, the gate dielectric win-

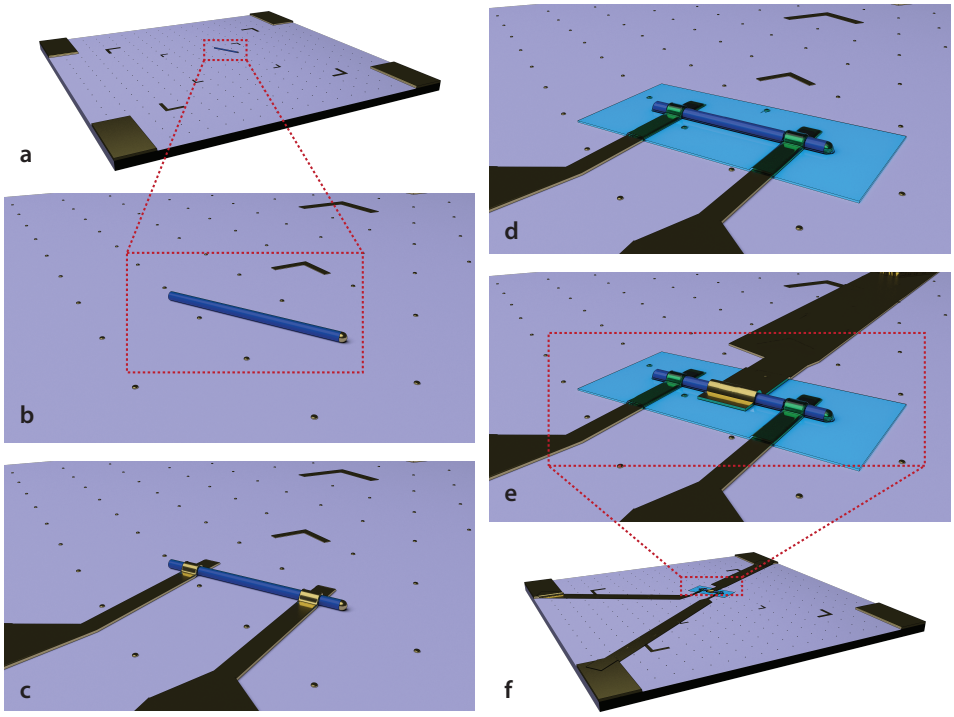


Figure 2.2: *Schematic fabrication of devices in a lateral architecture. (a), (b) Nanowires are dry-deposited on a prepatterned Si chip with 100 nm of thermally grown SiO_2. The chip back-side is covered with Au to allow for a back-gate to electrostatically modulate devices on the top-side of the chip. (c) Source and drain electrodes are defined by EBL, which is followed by metal thermal evaporation and a lift-off step. (d) A window for the gate dielectric is defined by EBL, followed by an ALD step of a high-κ dielectric such as Al_2O_3 or HfO_2. This fabrication step is finalized with a lift-off step, which also limits the ALD reactor temperature to approximately 100°C. (e), (f) The final step in creating a transistor includes forming a top gate by similar means to the source and drain electrodes.*

dow is patterned by EBL. An atomic layer deposition (ALD) process is used to deposit the high-κ gate dielectric, which is commonly Al_2O_3, HfO_2, or a combination of the two. A bi-layer is used because Al_2O_3 has been shown to offer a better interface to III-V semiconductors[31,32] and because HfO_2 has a high relative permittivity, which increases the gate capacitance. The ALD is followed by a lift-off of the oxide outside the device area, which limits the ALD process to approximately 100 °C.[33] The final stage of the process is the formation of a top gate, which follows a similar process scheme to the source and drain electrodes.

2.3 Vertical devices

Vertical processing introduces new challenges compared with lateral processing, but also presents significant advantages over lateral devices. The main advantages include (i) arrays of nanowires resulting in an impedance suitable for radio frequency (RF) probing, (ii) fabrication of complex circuits in a 3D architecture, and (iii) improved gate electrostatics enabling aggressive channel length scaling and nonlithography-based gate length definition. One of the main challenges is the fabrication of densely packed nanowire arrays with diameters below 10 nm (Fig. 2.3). Aerosols are generally available from approximately 5 to 80 nm, but lack the position control necessary for circuit design. Si integration is important for industry to keep down the fabrication costs, and thus the InAs nanowires are grown on a Si substrate by means of a ∼300 nm InAs buffer layer. The Si substrate is highly resistive, thus enabling RF characterization.

To realize these densely packed arrays of nanowires in a controlled fashion, two main challenges must be addressed: (i) controllable and reproducible fabrication of Au seeds around or below 10 nm in diameter by means of EBL and (ii) stringent epitaxial control (Fig. 2.4). Al-

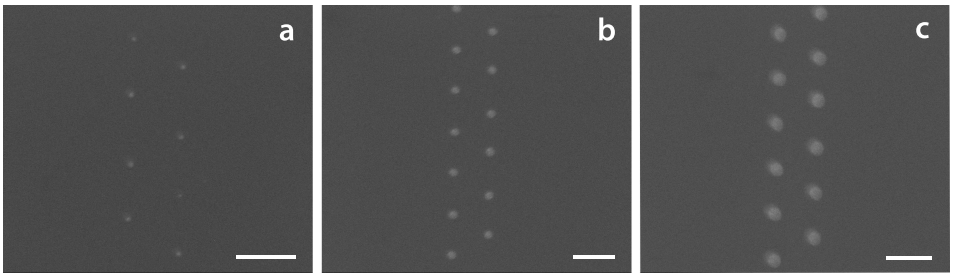


Figure 2.3: *SEM images of the scaling of Au seeds. (a) 8 nm seeds. (b) 20 nm seeds. (c) 35 nm seeds. (a–c) Scalebars are 150 nm. (d) After nanowire growth and high-κ deposition; scalebar is 2 μm.*

ternative methods of fabrication include so-called digital etching, i.e., growing nanowires thicker than desired that are subsequently partially oxidized, followed by a selective etch of the oxide.[34–36] This process allows for the nanowire to be thinned in incremental steps.

The epitaxial parameter window is quite small for extremely scaled Au seeds. The Au seeds may move during the annealing stage of the growth, much more so for sub-20-nm particles, which could impair transistor performance and circuit functionality. Removing the annealing step appears to alleviate the issue to allow for arrays with less displacement. It remains unclear how the interface quality between the substrate and Au seed particle is affected compared to growths with higher annealing temperatures.

To minimize the time for the formation of a native oxide, the sample is quickly moved between the MOCVD reactor and the ALD reactor where an Al_2O_3/HfO_2 bi-layer is deposited as the gate dielectric. At this stage there are many processing paths to reach the goal of a functioning chip, and thus a generalized overview is presented here. A transistor consists of three terminals connected to a semiconducting channel as illustrated in Fig. 2.5. The InAs buffer layer at the base of the nanowire is utilized as the source contact, leaving the formation

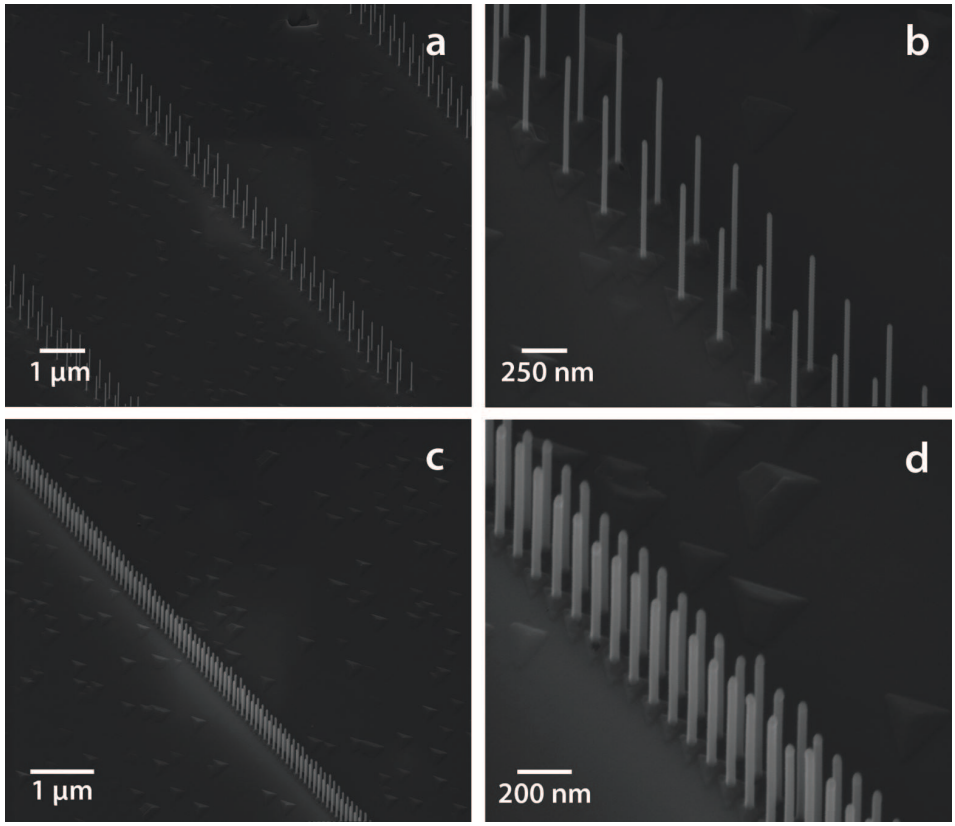


Figure 2.4: *Nanowire pitch scaling for nanowires below 20 nm in diameter. The nanowires are covered in a high-κ film (≈5 nm). All images are taken at an angle of 52°. (a), (b) 300 nm pitch. (c), (d) 100 nm pitch, which translates to a spacing of approximately 70 nm. The nanowires are also slightly wider because of the proximity effect in the EBL.*

of a gate and drain terminal. Device isolation is performed in the InAs buffer layer via a wet etch solution of H_3PO_4:H_2O_2:H_2O (1:1:25) to enable RF characterization and circuit functionality. Before the gate terminal can be fabricated, electrically isolating materials must be introduced so that the source–gate and gate–drain terminals do not short circuit. These spacers can be manufactured in several ways such as through SiO_2 or Si_3N_4 by plasma-enhanced chemical vapor deposition, organic photoresist or hydrogen silsesquioxane by a spin-on technique, or evaporated SiO_x. The spacer should be electrically insulating and have a low dielectric permittivity to reduce the parasitic capacitance of the devices. The spacers commonly require a planarization step before a gate can be placed on top, and this is achieved by reactive ion etching, usually with a protective photoresist mask.

The gate is generally fabricated by either a sputtering technique or thermal evaporation. In a sputtering approach, tungsten is preferred because of its dry-etching properties. A sputtered gate has good coverage of the nanowire, but it is difficult to specify a gate length, because it is defined by a spin-on technique and dry-etching as illustrated in Fig. 2.5. In contrast, an evaporated approach allows for gate length control with a precision of a few Ångströms, but presents difficulties in coverage.[14–16] A second spacer of preference is formed atop the gate, forming an isolation layer before the drain fabrication. The drain terminal is often formed by sputtering of, e.g., Ti/W/Au, but may also be fabricated by metal thermal evaporation and lift-off. All patterning during processing is performed by soft-UV lithography, with the exception of the Au seeds for nanowire growth.

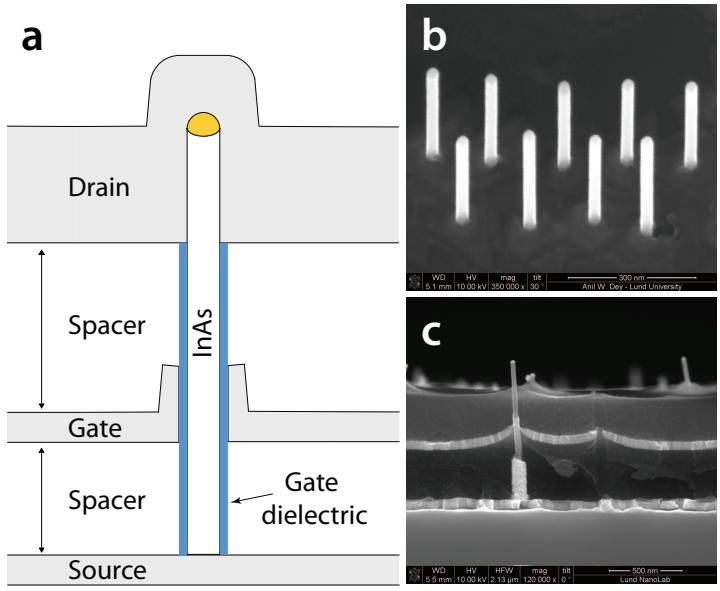


Figure 2.5: *(a) Schematic image of a vertical nanowire MOSFET. (b) InAs nanowires grown on a Si substrate covered in a 5-nm-thick HfO_2 film with a planarized 20 nm SiO_2 spacer. (c) Cross-sectional image of an older-generation vertical MOSFET where InAs nanowires were grown from an InP substrate and the spacers comprised organic polymers. The semi-insulating InP requires a source socket contact to form a connection to the bottom of the nanowire.*

CHAPTER 3

MOSFETs

This chapter deals with InAs nanowire FETs and is mainly based on papers I and II. There are many types of transistors, but a large number of them operate in a similar fashion. This chapter discusses a family of transistors called MOSFETs and, more specifically, nanowire MOSFETs.

The semiconductor community has voiced concerns regarding how long Moore's law, which states that the number of transistors on a chip will double every 18 months, will hold. This fantastic advancement has been driven by consumers continuously expecting more and more functionality in ever more portable devices. For the last few decades the semiconductor industry has mostly focused on scaling the Si transistors to fit more of them on the same chip.

Although the nanowire device architecture offers superior electrostatics and the ability to combine semiconductor materials with a high lattice mismatch,[30] other technologies have produced transistors with

impressive figures of merit.[37–41] As the gate length is scaled down, the gate must retain its ability to maintain the potential in the channel to enable efficient switching of the transistor. One common route is to thin the gate oxide or replace it with a material with higher permittivity. However, at some point the leakage current becomes too large, and alternative device geometries must be used that lessen the constraints on the gate dielectric thickness. For extremely scaled devices, the device architectures of choice are usually FinFETs or extremely thin silicon-on-insulator films (also known as SOI) to maintain good electrostatics.[42,43] Much research into high-performance transistors is directed toward an alternate channel material. Si, which has been the workhorse of the industry for many decades, is a mature technology and is naturally used as a benchmark to evaluate emerging technologies. Si technology is in fact so good that it is difficult to find examples of emerging technologies that demonstrate sufficient improvement over Si transistors to replace Si as the next-generation transistor technology. Alternate channel materials are mainly explored to take advantage of higher mobilities, which is a metric used to define how easily carriers move in a material. InAs, one of the principal III-V semiconductors explored in this thesis, in bulk form has approximately 20 times higher mobility than Si. The remainder of this chapter will discuss the principles of a well-tempered transistor.

3.1 MOSFET fundamentals

A simplistic description of a MOSFET is a voltage-controlled resistor or a current source depending on the biasing conditions. A MOSFET has three terminals: (i) a source, (ii) a drain, and (iii) a gate terminal. At low drain bias (V_{ds}), the current flows from the source to the drain terminal when the source is grounded, following a linear current–voltage relationship, as it would through a regular resistor.

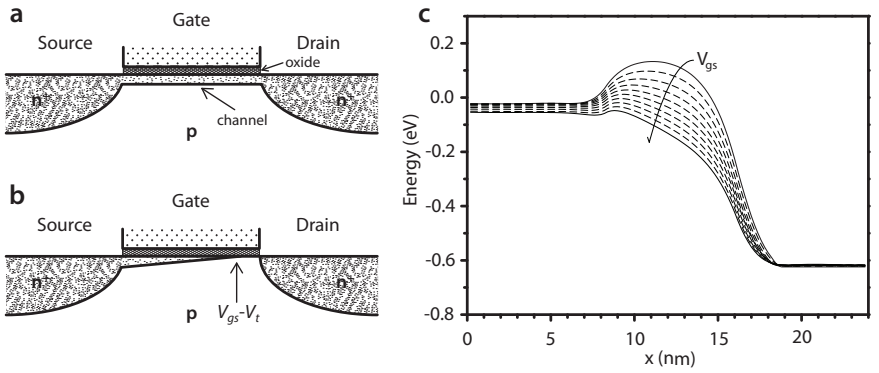


Figure 3.1: *Schematic cross section of a planar n-type MOSFET. An inversion layer charge forms beneath the gate when the applied gate voltage is larger than the threshold voltage, $V_{gs} > V_t$. (a) Schematic of the channel at low V_{ds}. (b) At high V_{ds}, the inversion layer is "pinched off." (c) Schematic band diagram at high V_{ds} for varying V_{gs}.*

The advantage of a MOSFET is that the resistance can be controlled by a voltage on the third terminal, the gate. At high V_{ds}, the current–voltage relationship will no longer be linear and the MOSFET will instead behave as a current source, i.e., a constant current independent of the applied V_{ds}. This means that above a certain drain bias, called the saturation voltage (V_{sat}), the current only increases marginally with larger V_{ds}.

The traditional approach to describe MOSFET operation is often explained by images similar to Fig. 3.1a and b. An n-type (a semiconductor with a surplus of free electrons) MOSFET is fabricated on a p-type (a semiconductor with a lack of electrons or a surplus of holes) substrate where the source and drain sides are then heavily n-doped, creating pockets with a high density of charge carriers.[44] For a current to flow between the source and the drain, an inversion layer of electrons must be formed below the gate. This occurs when the gate

potential V_{gs} is larger than the threshold voltage V_t, in other words, when $V_{gs} - V_t > 0$. At high V_{ds}, the channel near the drain end will begin to diminish because the potential difference between the gate and the channel will be too small to maintain the inversion layer, which is the traditional explanation for why the current begins to saturate at high V_{ds}.

A more fundamentally correct and also simpler description is a top-of-the-barrier description of a MOSFET, also known as the "virtual source" (VS) model.[45,46] By describing the operation of a MOSFET as a device where a barrier is modulated by the imposed gate action, it is easier to understand the principle of operation and compare technologies, because most operate by the same basic principles. One flaw in the traditional model is the understanding of current saturation. In 1992, D.J. Frank et al., using Monte Carlo simulations, showed that the electrons' velocity actually saturates at the *beginning* of the channel rather than at the end as the traditional model would suggest.[47] For short gate lengths (L_g) near the end of the channel where the electric field is the strongest, the electrons actually experience a velocity overshoot because the carriers simply do not have time to scatter before they are swept out through the drain. The VS model instead incorporates a parameter called the injection velocity v_{inj},[48,49] which is the average velocity at the beginning of the channel. A succinct derivation of the equations describing the I_{ds}-V_{ds} characteristics by means of the VS model is available in the Appendix.

To complicate matters, the saturation velocity v_{sat} for Si happens to be very close to v_{inj}, and therefore the traditional model has so far been able to predict current–voltage characteristics successfully. The VS model has been used to fit a multitude of experimental data in various transistor technologies such as Si and III-Vs, ranging from long-channel devices to extremely scaled, basically ballistic devices with much success.

3.2 Key figures of merit

In the following sections, several important figures of merit are presented. Although some of these are explored in more detail than others, the key figure of merit depends on the specific application for the transistor.

3.2.1 Drive current

One important figure of merit is the ON-current or drive current, I_{on}. In digital circuitry, capacitors are typically charged and discharged in order for a circuit to operate correctly. The speed at which it is possible to charge and discharge these capacitors will set the speed of the circuit, which is why it is preferable to have as high an ON-current as possible. Generally, the ON-current of a device is determined when both the gate and the drain terminals are at the same bias as the supply voltage, $V_{dd} = V_{gs} = V_{ds}$. However, a more useful evaluation of the ON-current should be performed at a fixed overdrive voltage instead, $V_{ov} = V_{gs} - V_t = V_{ds} = V_{dd}$. An alternative means to determine the ON-current, as well as the OFF-current, is by defining a window around the threshold voltage V_t such that the ON-current is determined at $V_t + 1/3\ V_{dd}$ and the ON-current at V_t - $2/3\ V_{dd}$.[50]

The semiconductor industry usually has two main types of transistors in their product line: a high-performance type and a low-power type. For the former, the industry has decided that a device is off when $I_{off} = 100\,\mathrm{nA/\mu m}$, which occurs at a certain gate voltage V_{off}, ideally $0\,\mathrm{V}$.[43] The corresponding value for the low-power devices is $30\,\mathrm{pA/\mu m}$ and that for ultra-low-power devices is $15\,\mathrm{pA/\mu m}$.

Another definition available to circuit designers is instead general purpose and low-power transistors. These in turn both have three sub-categories to choose from; high, standard and low V_t. To compare the drive current across different device architectures, it is necessary

to normalize the value in some fashion. A common method is to normalize the current to the gate perimeter of the device. For a planar MOSFET, this would mean normalizing to the gate width, whereas in a FinFET, this would involve the width of the fin together with the length of both sides of the fin. For nanowire devices, in a GAA architecture, the normalization would be done to the circumference of the nanowire.

From the I_{ds}-V_{ds} characteristics, it is possible to can extract the ON-resistance R_{on} as illustrated in Fig. 3.2a. The ON-resistance, also called the total resistance R_{tot}, is a combination of source, channel, and drain resistance, $R_s + R_{ch} + R_d$. The output conductance g_o is also an important metric and for an ideal MOSFET should be as close to zero as possible.

3.2.2 Transconductance and threshold voltage

Using the I_{ds}-V_{gs} characteristics of a transistor, the transconductance, g_m, can be calculated. The transconductance is a figure of merit that describes how efficiently the current of the device can be modulated with the gate. The values are often presented as maximum values at a fixed V_{ds}, commonly the supply voltage at which the transistor is operated. The transconductance is calculated by differentiating the I_{ds}-V_{gs} characteristics, such that

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \tag{3.1}$$

as illustrated in Fig. 3.2c. The transconductance is expressed in units of Siemens (S) or in the normalized case (μS/μm).

One method of extracting the threshold voltage, V_t, is through linear extrapolation from the maximum transconductance, to where the line intersects the x-axis, as illustrated in Fig. 3.2c. Usually the transfer characteristics are presented biased at the supply voltage,

which gives the *saturation* threshold voltage. At a low source-drain bias, the linear threshold voltage may be calculated and is usually higher than the saturated value. Generally, for an n-type device, a slightly positive threshold voltage is desirable so that the device is in its OFF-state at $V_{gs} = 0$ V to avoid unnecessary power consumption.

One method of extracting the threshold voltage, V_t, is through linear extrapolation from the maximum transconductance, to where the line intersects the x-axis, also illustrated in Fig. 3.2c. Usually the transfer characteristics are presented biased at the supply voltage, which gives the *saturation* threshold voltage. At a low source-drain bias, the linear threshold voltage may be calculated and is usually higher than the saturated value. Generally, for a n-type device, a slightly positive threshold voltage is desired in order to have the device in its OFF-state at $V_{gs} = 0$ V so that unnecessary power is not consumed.

3.2.3 Subthreshold swing and drain-induced barrier lowering

The previous figures of merit mainly relate to the ON-state of the device; however, the OFF-state of the transistor is in many cases more significant than the ON-state. Most emerging technologies generally demonstrate exceptional ON-performance, such as high drive currents, but commonly lack in OFF-performance or vice versa. This is where Si technology truly shines where many years of development has led to transistors that combine excellent ON- and OFF-characteristics simultaneously. A small leakage current in the OFF-state may not be a problem for a single device, but in a modern processor with billions of transistors, the small leakage current in each device could turn into a huge leakage current for the entire chip. To evaluate a device's OFF-state performance, a common practice is to evaluate the I_{ds}-V_{gs} on a

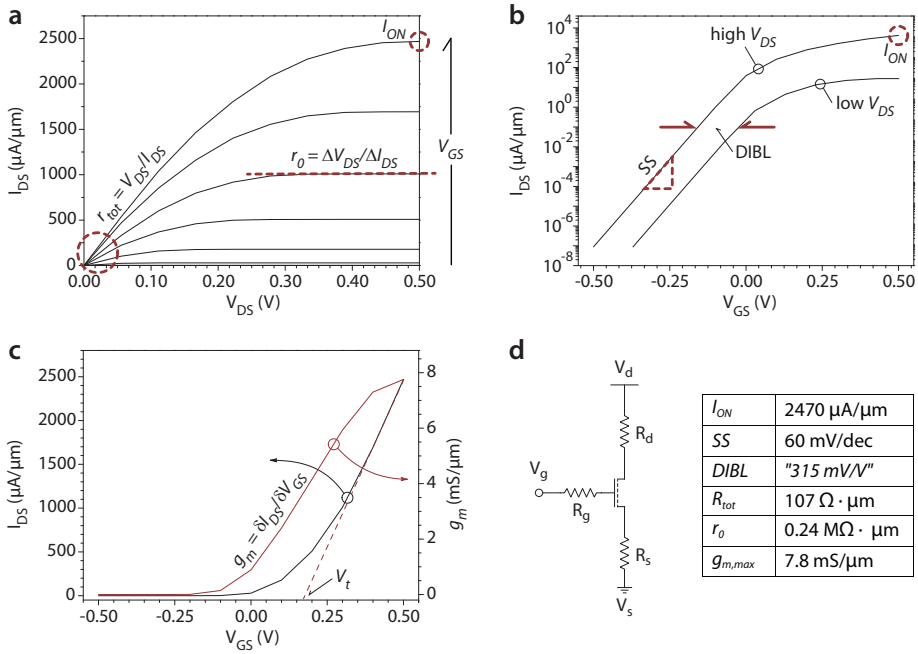


Figure 3.2: *Typical output and transfer characteristics of a MOSFET. The data has been normalized to the nanowire circumference. The figures display simulated data of a 15-nm-diameter InAs nanowire MOSFET operating in the ballistic regime. (a) I_{ds}-V_{ds} or output characteristics of the MOSFET. This curve is often used to evaluate the* ON*-state performance of a MOSFET. (b) I_{ds}-V_{gs} plot on a semi-logarithmic scale. The high V_{ds} curve is simulated, whereas the low V_{ds} curve is sketched to illustrate clearly the effect of drain-induced barrier lowering (DIBL). (c) I_{ds}-V_{gs} plot on a linear scale, also known as the transfer characteristics, commonly used to extract V_t by the maximum transconductance method. (d) The schematic drawing shows the circuit symbol normally used for a MOSFET where some parasitic series resistances have been added. In a ballistic device, as has been used in the simulated data (a–c), these resistances are zero. The table presents some of the key device metrics.*

semi-logarithmic scale to clarify the characteristics below the threshold voltage. Firstly, the subthreshold swing or inverse subthreshold slope (SS) is a figure of merit determining how many mV in gate potential change is required to obtain a tenfold change in current as

$$SS = \frac{\delta \log_{10}(I_{ds})}{\delta V_{gs}} = 2.303 \left(\frac{k_B T}{q}\right) \left(\frac{\delta \psi_s}{\delta V_{gs}}\right)^{-1} \tag{3.2}$$

where k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, and ψ_s is the semiconductor surface potential. Ideally, we want to get as much current out as possible for a very small change in gate voltage. This requires that the applied gate voltage is efficiently modulating the bands as described by the last term in Equation 3.2. Ideally, $(\delta\psi_s/\delta V_{gs})^{-1} = 1 + C_d/C_{ox} = 1$, where C_d is the depletion capacitance and C_{ox} is the oxide capacitance. Therefore, in a MOSFET, there is a lower limit of $SS_{min} = 60$ mV/decade at room temperature, which is related to the Fermi distribution of carriers and thermal injection of carriers into the channel.

Drain-induced barrier lowering (DIBL) is another figure of merit and refers to the influence of the drain potential on the channel. This figure of merit should be maintained at a low value for a well-tempered device. This effect is most pronounced in MOSFETs with very short gate lengths. The degradation of the SS and DIBL as the gate length is scaled is commonly referred to as short-channel effects. The effect of DIBL can be minimized by stringent constraints on the gate in a short-channel device by introducing improved electrostatics, as a GAA found in nanowire devices, and the introduction of a high-κ dielectric.

3.2.4 Cut-off frequency and maximum oscillation frequency

The figures of merit discussed so far are mostly associated with the direct-current mode of operation of the transistor; however, some RF

or alternating-current metrics are also of great importance.[51] The cut-off frequency (f_t) is defined as the frequency at which the current gain is equal to 1 and is given by

$$\frac{1}{2\pi f_t} = \frac{C_{gg}}{g_m} + \frac{C_{gg}}{g_m}(R_s + R_d)\, g_d + (R_s + R_d)\, C_{gd} \tag{3.3}$$

In an ideal MOSFET, R_s and $R_d = 0\ \Omega$, and the cut-off frequency simplifies to

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3.4}$$

The maximum oscillation frequency (f_{max}), defined as the frequency when the power gain is equal to 1, is given by

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_g C_{gd}\left[1 + \left(\frac{2\pi f_t}{C_{gd}}\right)\Psi\right]}} \tag{3.5}$$

where Ψ is

$$\Psi = \frac{C_{gg}^2\, g_d^2}{g_m^2}(R_s + R_d) + \frac{C_{gg}\, C_{gd}\, g_d}{g_m}(R_s + R_d) + \frac{C_{gg}^2\, g_d^2}{g_m^2} \tag{3.6}$$

Again, in an ideal MOSFET, $R_s = R_d = g_d = 0$, and therefore $\Psi = 0$, and the equation for f_{max} simplifies to

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_g C_{gd}}} \tag{3.7}$$

In paper II, a f_t of 7 GHz and a f_{max} of 20 GHz are reported for a vertical nanowire MOSFET consisting of an array of 70 InAs nanowires and $L_g = 100$ nm. Direct-current electrical characterization revealed high ON-currents but diminished OFF-performance, which is attributed to the nanowires being doped throughout the growth with tin. A small signal model was developed to evaluate the device parasitics, and parasitic capacitances between source, gate, and drain were found to limit the performance of the device.

3.3 The ultimate scalability

The basic design rules when scaling the transistors have followed a few simple rules set out by R.H. Dennard et al.[52] The rules stipulate that scaling the device dimensions by a factor of κ must be accompanied by scaling the oxide thickness by the same factor along with the voltages used. The idea behind the rules is: If the electrostatic configuration of the device is kept constant by following the scaling rules, the new device should behave as a well-tempered, smaller version of the initial transistor. This has worked well over the past few decades; however, when the oxide shrinks below the thickness of a few atomic layers to maintain the electrostatics of very short gate-length devices, the leakage current through the gate will be substantial. For this reason, high-κ dielectrics such as Al_2O_3 and HfO_2 are being integrated into modern devices, allowing for thicker oxides while maintaining a high capacitive coupling between the gate and channel. However, simply working on oxide integration from a materials standpoint is not sufficient. Planar technologies have been evolved into FinFETs for increased electrostatic control because the gate field is more efficiently imposed on the channel. Extremely scaled planar devices, so-called silicon-on-insulator devices, are also being considered as an option to manage short-channel effects.[53] Next-generation devices with nanowire channels are currently being investigated because nanowire devices offer GAA device designs that should allow for "ultimate electrostatics".[54,55]

Although nanowires provide excellent electrostatics in a GAA configuration, scaling L_g below 10 nm will require nanowires with diameters of 5 nm and below, as illustrated in Fig. 3.3. One concern of the semiconductor community is how pronounced the surface scattering effects will be in such extremely scaled nanowire MOSFETs. As short-channel effects begin to dominate the transport, it is vital to be able to predict the performance of future devices. A.C.

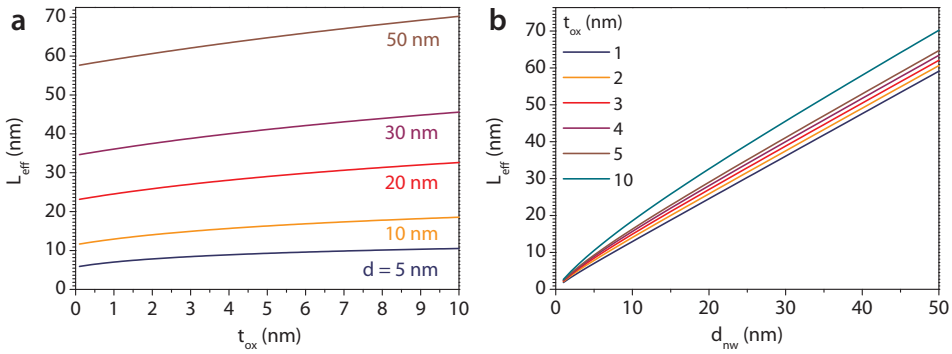
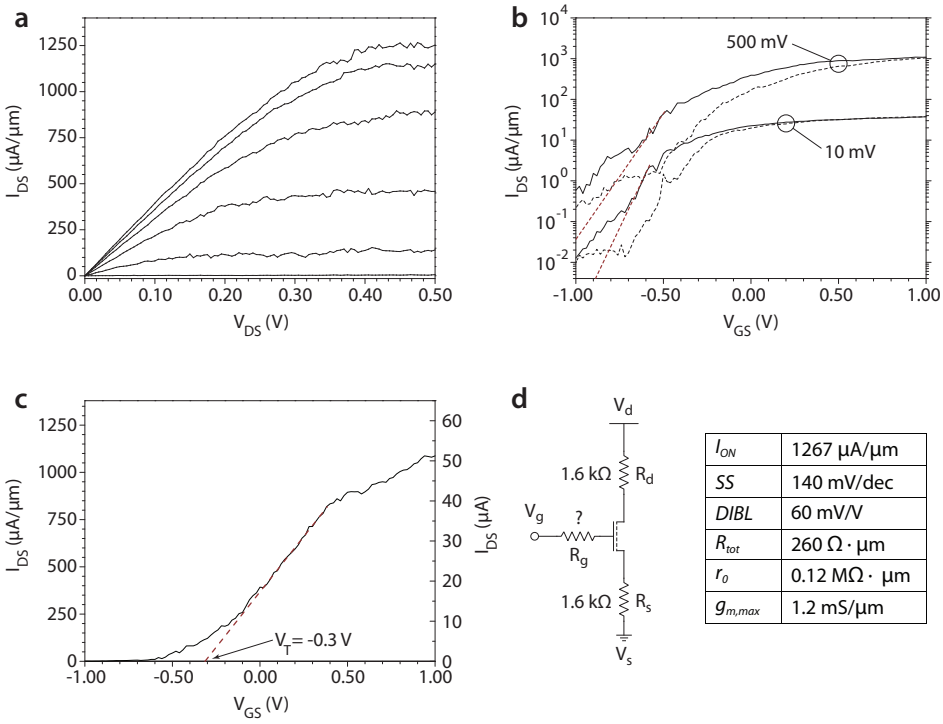


Figure 3.3: *The minimum effective gate length necessary to maintain $SS < 70\,mV/decade$ and $DIBL < 50\,mV/V$ as a function of (a) oxide thickness and (b) nanowire diameter for an InAs GAA device architecture.*[56] *The oxide is assumed to be HfO_2 with $\epsilon_r = 20$.*

Ford et al. have shown a linear relationship of the field-effect mobility and the InAs nanowire diameter on long-channel MOSFET devices such that $\Delta\mu_n/\Delta r = 422\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$ per nm.[57] Inserting values into Equation A.15, assuming Maxwell–Boltzmann statistics, we find $\mu_B = 6900\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, and from the work from Ford et al., we deduce $\mu_n = 1985\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$ for a 15-nm-diameter InAs nanowire. This results in an apparent mobility $\mu_{app} = 1541\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$. In paper I, the apparent mobility for a 15-nm-diameter MOSFET was extracted by using a non-parabolic model to calculate the flat-band gate capacitance ($L_g = 100\,\mathrm{nm}$ and oxide thickness $t_{ox} = 5\,\mathrm{nm}$) resulting in $\mu_{app} = 1510\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, which is very close to the theoretical value.

Although the mobilities are indeed much lower in scaled InAs nanowires than in the bulk InAs,[44] high drive currents of $1267\,\mu\mathrm{A}/\mu\mathrm{m}$ ($34\,\mathrm{MA}/\mathrm{cm}^2$) are still achieved for these scaled InAs nanowire MOSFETs. Quantifying devices today solely by means of long-channel metrics governed by diffusive transport, such as classical mobility, is



I_{ON}	1267 μA/μm
SS	140 mV/dec
DIBL	60 mV/V
R_{tot}	260 Ω · μm
r_0	0.12 MΩ · μm
$g_{m,max}$	1.2 mS/μm

Figure 3.4: *Measured output and transfer characteristics of a 15-nm-diameter InAs nanowire MOSFET. The gate length is 100 nm, and the data has been normalized to the nanowire circumference. (a) I_{ds}-V_{ds} characteristics showing a maximum drive current of 1250 μA/μm. $V_{g,max}$ = 2 V, ΔV_g = 0.5 V. (b) I_{ds}-V_{gs} plot on a semi-logarithmic scale for two drain biases: 10 mV and 500 mV. The dashed lines show the down sweep, and the solid lines show the up sweep, indicating some hysteresis in the device. (c) I_{ds}-V_{gs} plot on a linear scale showing $V_t = -0.3$ V. (d) The schematic drawing shows the parasitic series resistances, extracted by fitting the ballistic data with added series resistances on both the source and the drain. The table displays some of the key device metrics of the 15-nm-diameter InAs MOSFET nanowire.*

becoming outdated. Classical mobility still plays its part, but as the transport mechanism begins to be dominated by ballistic transport, other parameters are playing an increasingly crucial role in device performance. To achieve high drive currents in ballistic devices, the v_{inj} and the density of states must be high, that is, a large number of carriers are needed, and they need to move fast.

The v_{inj} is inversely proportional to the square root of the effective mass, and therefore InAs ($m^* = 0.023$) is able to achieve higher injection velocities, of almost a factor of 3, than Si ($m^* = 0.19$). The drawback is that the density of states is proportional to the effective mass, and hence the density of states is lower for III-V semiconductors than for Si semiconductors. This effect is further worsened by reducing the dimensionality of a device. Even so, modern Si MOSFETs operate at approximately half the ballistic limit, whereas III-V devices such as HEMTs can operate much closer to the ballistic limit. This is mainly because the mean free path in III-Vs is longer than for a corresponding Si device.

Figure 3.4a illustrates the output characteristics of a 15-nm-diameter InAs nanowire MOSFET, which exhibits similar drive currents to modern HEMTs,[7] although HEMTs operate at a lower overdrive. This is a consequence of the integration of high-κ dielectrics on III-Vs as seen in the transconductance and *SS*. Whereas HEMTs have a good-quality channel interface, high-κ dielectrics on III-V channels often form a high density of interface traps (D_{it}), which degrade the electrostatics. The drawback of HEMTs is a large leakage current between the gate terminal and the channel. The interface quality in a MOSFET could be improved by surface passivation techniques[58] and the ALD conditions[31,32] as well as post-deposition annealing.[59]

The InAs nanowire MOSFETs studied in paper I also show a maximum voltage gain, $g_m/g_0 = 50$, which is an indication of a low DIBL (60 mV/V) and low series resistance in the source and drain. The low access resistance is attributed to the selective overgrowth of the source

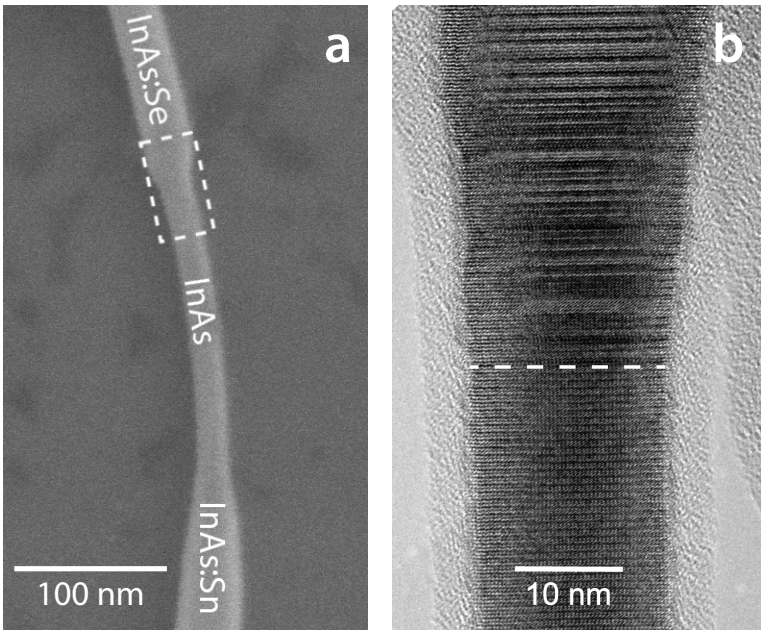


Figure 3.5: *(a) SEM image of the "neck" structure of the nanowire. The highlighted area is studied in closer detail in (b). (b) Transmission electron microscope image of the upper i-n$^+$, InAs-InAs:Se, neck region. The dashed line indicates the onset of a twinned zinc blende structure and an increase in nanowire diameter as Se is introduced to the growth reactor. Nanowire diameters are found down to 15 nm, including a 1-nm-thick native oxide.*

D (nm)	L_g (nm)	I_{on} (A/mm)	g_m (S/mm)	SS (mV/dec)	Ref.	Technology
15	100	1.25	1.23	140	I	NW
10	30	0.7	1.9	80	[7]	HEMT
30	250	0.38	0.56	120	[60]	III-V FinFET
10	75	0.49	1.75	85	[38]	QWFET
25	170	1.02	0.8	260	[61]	radial NW
13	230	1.5	1.72	180	[62]	XOI
22	30	1.08	-	71	[43]	Si FinFET
11.2	25	0.52	-	∼100	[63]	Si NW

Table 3.1: *Data on a list of devices with varying dimensions (D, diameter/thickness) and gate lengths (L_g). The values for I_{on} and g_m of nanowire devices are normalized to the circumference. The values are given for V_{ds} = 0.5 V, with the exception of Majumdar et al. ,[63] which is given for V_{ds} = 0.75 V. Here, I_{on} is presented for the highest reported gate overdrive (V_{ov}).*

and drain by InAs:Sn and InAs:Se, forming a n^+-i-n^+ doping profile as illustrated in Fig. 3.5. An estimate of the series resistances was obtained by setting $R_s = R_d = 1.6$ kΩ in the ballistic model as illustrated in Fig. 3.2. Interchanging the source and drain bias produces the same I_{ds}-V_{ds} characteristics, which suggests that the source and drain resistance are similar in size. Furthermore, from the extracted $R_{on} = 5.3$ kΩ, assuming ballistic transport in the channel, we can deduce that only six sub-bands, or channels for current flow, contribute to the transport of electrons in this highly scaled device.

An overview of advanced transistors reveals competitive figures of merit for InAs nanowire MOSFETs compared with state-of-the-art devices in various technologies (Table 3.1). The ON-characteristics of 15-nm-diameter InAs nanowires are excellent and are likely to improve further with shorter gate lengths. A challenge remains in the OFF-state performance, mainly in the *SS*, which should be improved by

a transition to a vertical design architecture allowing for a GAA. In addition, the gate stack must be improved to allow for a higher-quality interface between the high-κ and InAs nanowire, and this is expected to improve both ON- and OFF-state performance.

CHAPTER 4

III-V CMOS

This chapter examines the integration of n- and p-type III-V semiconductors with the purpose of fabricating III-V CMOS circuitry. The topic of III-V CMOS is relatively unexplored, even though it is important for integration of III-V for logic circuits. This chapter is mainly based on paper III.

4.1 CMOS basics

Most of the efforts into researching III-V semiconductors have focused on n-type materials and have often been applied toward analog applications. The main reason for this is that the electron mobilities of n-type III-Vs are higher than the hole mobilities of p-type III-Vs.[40] However, for efficient operation in CMOS digital logic, both n-type devices and p-type devices are essential. This chapter examines the

implementation of both n-InAs and p-GaSb on a single chip for the fabrication of III-V CMOS circuits.

Among the III-V binaries, InAs has one of the highest electron mobilities ($\mu_e = 33000\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$), which makes it suitable as a channel material in an nFET. On the other hand, GaSb has one of the highest hole mobilities of the binary III-V semiconductors ($\mu_h = 1000\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$) and is thus a suitable choice for a pFET. To grow III-V semiconductors epitaxially as planar layers, a lattice-matched substrate or a thick buffer layer is necessary to avoid dislocations. Such defects could otherwise be detrimental to the device operation. However, lattice-matched substrates are often conducting, which would result in a high parasitic capacitance and could also cause difficulties in circuit path routing. In an effort to avoid this disadvantage, some elegant work has been undertaken in which epitaxially grown nanoribbons were mechanically transferred onto an insulating substrate.[64–66]

However, to circumvent the issue, III-V semiconductors can instead be grown as nanowires, which allow for radial relaxation capable of accomodating a lattice mismatch of up to 15%.[67] Threading dislocations terminate at the nanowire surface close to the heterointerface and do not extend into the nanowire. A nanowire-based III-V CMOS solution allows for direct integration on, e.g., a Si substrate.[30,68] In addition to integration on Si, nanowires can accommodate several III-V semiconductors in one nanowire, as illustrated in Fig. 4.3a.

One of the main advantages of CMOS is the prospect of low-power circuits. This is achieved by using two (or more) complementary devices, one n-type (also called the pull-down network) and one p-type (or pull-up network), as illustrated in Fig. 4.1a–c, exemplifying an inverter configuration. This configuration ensures that there is never a direct-current path between the supply and ground unless a switching event occurs. Figure 4.1b illustrates the current path through the inverter assuming a “low” input signal or a digital “0”. In this scenario, the nMOS is turned *off* while the pMOS is *on*, which results in an

output of "high" or "1". Correspondingly, a "high" input signal to the inverter will turn the nMOS *on* while the pMOS is turned *off*, which will result in an output of "low" or "0", as illustrated in 4.1c. This operation is inverting because a "low" input turns into a "high" output and vice versa. A ring oscillator consists of an odd number of inverters connected in series, and the output of the final stage is connected to the input of the first stage (Fig. 4.1d). This is a self-oscillating circuit and is often used to evaluate emerging technologies to assess their viability by measuring the speed or oscillating frequency. High-performance devices may oscillate at frequencies that are difficult to measure, and thus it is common to increase the number of stages in order to reduce the oscillating frequency. Single-stage performance is evaluated by dividing the oscillation time by the number of stages.

4.2 CMOS metrics

A few more metrics are important when evaluating CMOS circuits, such as speed and power. The analysis begins by evaluating the switching event of shifting from a "1" to a "0" on the input of an inverter (Fig. 4.2a). At this switching event, the output capacitance C_{out} must discharge through the pull-down network. Ideally, a CMOS inverter should only consume energy during a switching event as illustrated in Fig. 4.2b.

The current through the pull-down network is given by

$$I_{ds}(t) = -C_{out}\frac{\delta V_{out}(t)}{\delta t} \tag{4.1}$$

and correspondingly

$$V_{out}(t) = V_{dd} - \frac{I_{ds}(sat)}{C_{out}}(t - t_0) \tag{4.2}$$

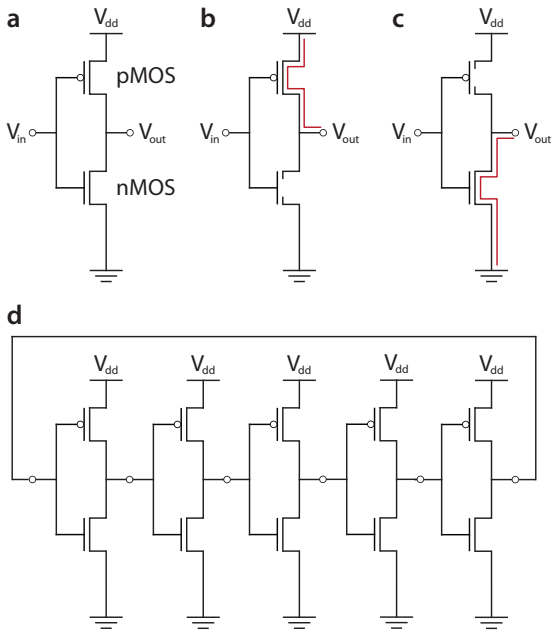


Figure 4.1: *Schematics of inverter and ring oscillator operation. (a) A series connection of a pMOS and an nMOS with a common input forms an inverter. (b) A "low" input signal or a digital "0" turns the pMOS device on, whereas the nMOS is turned off. This will result in a "high" or "1" signal on the output. (c) A "high" input signal or a "1" will turn off the pMOS and turn on the nMOS device. The output will correspondingly turn into a "low" or "0". (d) An odd number of inverters form a ring oscillator. A ring oscillator is a self-oscillating circuit commonly used to benchmark emerging technologies.*

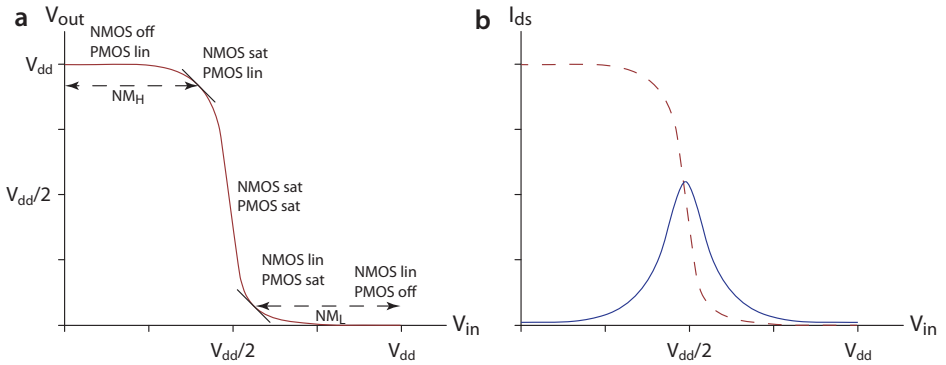


Figure 4.2: *Schematic inverter voltage and current transfer characteristics. (a) Inverter voltage transfer characteristics. NM_H and NM_L describe the high and low noise margins, respectively, and are determined at the point where the gain is -1. Ideally the noise margin should be as large as possible. (b) The solid line depicts the current transfer characteristics of an inverter. This highlights the advantage of a CMOS design because the circuit does not draw power unless a switching event occurs.*

where t_0 is the time of the switching event. Equations 4.1 and 4.2 are valid in a quasi-static assumption where it is assumed that the current through the transistor is constant $I_{ds,sat}$ above $V_{ds,sat}$ and acts like a resistor below $V_{ds,sat}$, which in the time domain would correspond to $t_0 \leq t \leq t_1$, where t_1 is the time at which the transistor crosses into triode operation. At time t_1, the system can be modeled as a simple resistor–capacitor circuit, which is known to have a time constant $\tau = R_{ch} \cdot C_{out}$ at which point the output voltage discharges as

$$V_{out}(t) = V_{out}(t_1)e^{-t/\tau} \tag{4.3}$$

To evaluate the speed of the circuit, a metric commonly used is the propagation delay, denoted as τ_n and defined as the point at which

the output voltage has been reduced by a factor of two.

$$\tau_n = \frac{C_{out} V_{dd}}{2 I_{ds,sat}} \tag{4.4}$$

The key conclusion is that, to have very fast switching in a circuit, a high ON-current is necessary. If the CMOS performance is instead discussed in terms of power, a suitable starting point is the energy stored in a capacitor $W_c = \frac{1}{2} C V_{dd}^2$. Here, T is the time it takes for the input to switch from "0" to "1" and back again to 0 (i.e., one period) and can be used to determine the dynamic energy consumption during a switching event $T/2$ as

$$P_{dyn} = \frac{\Delta E}{T/2} = \alpha f C V_{dd}^2 \tag{4.5}$$

where α is an activity factor. All the transistors are not always active in a circuit, which is regulated by the factor α. Furthermore, the frequency of operation f is dependent on the drive current or the overdrive voltage $V_{ov} = V_{dd} - V_t$. This means that, to increase the speed of the circuit, either the supply voltage may be increased, which will cost more energy, or V_t may be lowered. However, lowering V_t will result in a higher *static* power dissipation because

$$P_{stat} \sim e^{-qV_t/mk_BT} V_{dd} \tag{4.6}$$

Hence there is a trade-off between speed and power that must be considered when designing a circuit. Another approach to reducing the power consumption without sacrificing the speed of the circuit would be to implement a device that is not limited by the 60 mV/decade limit of MOSFETs. One promising approach involves replacing traditional MOSFETs with TFETs and is discussed further in Chapter 5.

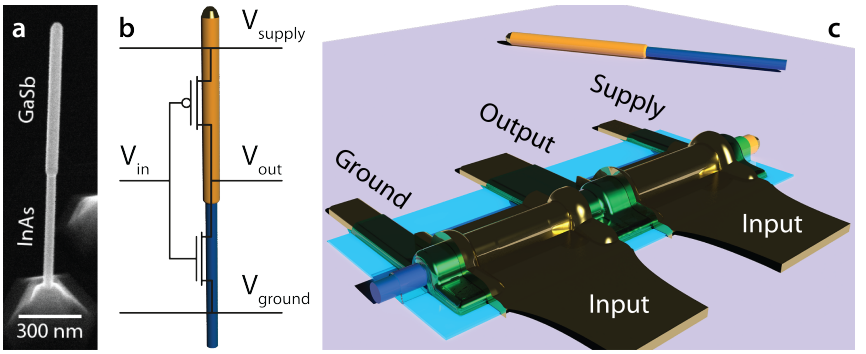


Figure 4.3: *SEM and schematic images of a III-V CMOS inverter realized in a single InAs/GaSb nanowire. (a) SEM image of an InAs/GaSb nanowire. The image is taken at 30°. (b) Schematic inverter design for a single nanowire. (c) Schematic layout of a completed inverter.*

4.3 Lateral circuits

InAs/GaSb nanowires were grown by MOVPE from 30-nm-diameter Au aerosols deposited on an InAs(111)B substrate. AsH_3 and TMIn were used as precursors to grow the InAs segment at 450 °C, followed by the GaSb segment grown at 500 °C, where trimethylgallium and trimethylantimony were used as precursors. Energy-dispersive X-ray spectroscopy (XEDS) revealed that the GaSb was $In_{0.03}Ga_{0.97}Sb$ because it was difficult to empty the Au catalyst particle of all the In from the growth of the first segment. Both segments were grown approximately 1 µm long and 55 nm and 65 nm in diameter for the InAs and GaSb segment, respectively. Inverters were fabricated as described in Section 2.2, including ground, supply, and input and output electrodes, as illustrated in Fig. 4.3 b and c.

Electrical measurements on the individual n-type segment and p-type segment reveals an asymmetry in drive current for the InAs nFET and the GaSb pFET. Long channel devices with $L_g = 750$ nm display

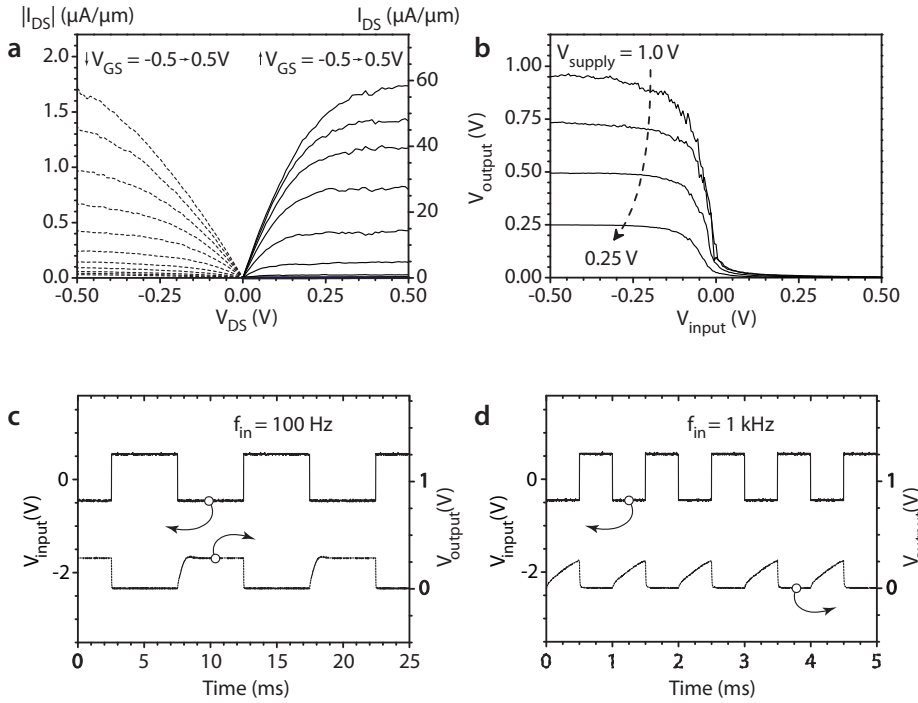


Figure 4.4: *Electrical characterization of an InAs/GaSb single nanowire inverter. (a) Output characteristics for the individual nFET InAs and pFET GaSb segments. (b) Inverter voltage transfer characteristics at various suppy voltages. The maximum gain is 10.5 for a supply voltage of 1 V. (c), (d) Time-resolved inverter characteristics for a square wave input signal of (c) 100 Hz and (d) 1 kHz and a supply voltage of 0.5 V.*

drive currents of 58 and 1.7 µA/µm (Fig. 4.4a), which coincidentally corresponds well to the difference between the bulk mobilities of electrons in InAs and holes in GaSb. Electrical measurements in an inverter configuration display correct inverting operation and resolve a full swing as illustrated in Fig. 4.4b. After smoothing and differentiation, the maximum gain of 10.5 is calculated at a supply voltage of 1 V. The asymmetry will limit the switching speed of the inverter because a low input should charge the capacitance on the output through the GaSb pFET. The discharge cycle will be significantly faster through the InAs nFET to the ground terminal, as illustrated in Fig. 4.4 c and d. In this device layout, the main limiting factor of the inverting frequency is attributed to the large capacitance on the output node, estimated to be 17.3 pF, rather than the drive currents alone (Equation 4.4). Integrating I_{supply}, for $V_{supply} = 0.5\,\mathrm{V}$, over a switching event results in a power consumption of 93.6 nW.

4.4 GaSb pFETs for III-V CMOS

It has been shown that the performance in InAs nanowire MOSFETs can be greatly improved by device scaling and reducing the access resistance. A similar scheme for GaSb pMOS devices may be applied in which the drive current I_{on} and the transconductance g_m may be boosted by incorporating an InAs(Sb) shell to improve the contacts to GaSb and by introducing doping to further reduce the resistance. GaSb nanowires were again grown from Au aerosols by MOVPE. In contrast to the GaSb grown for III-V CMOS application, the nanowires were grown with a GaAs stem as a base to facilitate the nucleation of the GaSb segment. The GaSb segment was doped with Zn at a molar flow ratio of $\mathrm{Zn/Ga} = 0.07$ to reduce the resistance of the segment. The GaSb was followed by an InAs segment that also formed a parasitic InAs(Sb) shell surrounding the GaSb segment. The nanowires

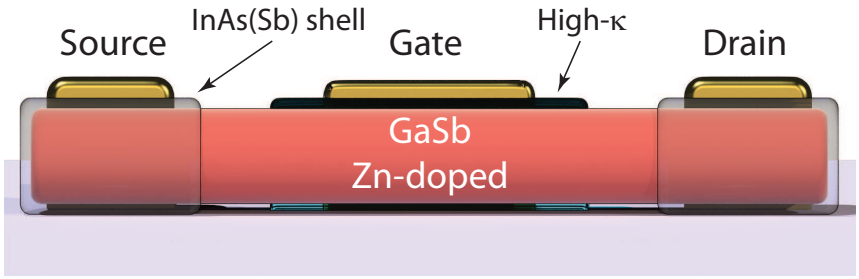


Figure 4.5: *Cross-sectional schematic image of an improved pFET. The advancements include an InAs(Sb) shell to lower the contact resistance, and a lightly Zn-doped GaSb channel.*

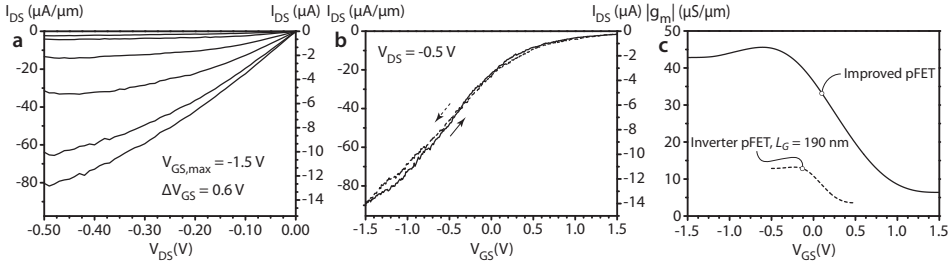


Figure 4.6: *(a) I_{ds}-V_{ds} characteristics of the improved GaSb pFET, $L_g = 200\,nm$. (b) Transfer characteristics of the improved GaSb pFET at $V_{ds} = 0.5\,V$. (c) Comparison of the transconductance of the inverter pFET, $L_g = 190\,nm$, and the improved GaSb pFET.*

L_g	I_{on} (μA/μm)	I_{on} *bias conditions*	$g_{m,max}$ (μS/μm)	*SS* (mV/dec)	*Channel material*	*Ref.*
200 nm	85	V_{ds} = -0.5 V, V_{gs} = -1.5 V	45	880	GaSb	-
190 nm	10	V_{ds} = -0.5 V, V_{gs} = -0.5 V	13	400	GaSb	III
750 nm	70	V_{ds} = -3 V, V_{gs} = -4 V	26	600	GaSb	[70]
5 μm	4	V_{ds} = -2 V, V_{gs} = -4 V	-	250	GaSb	[71]
2.6 μm	58	V_{ds} = -1 V, V_{gs} = -1 V	-	156	InGaSb	[72]
30 nm	582	V_{ds} = -1 V, V_{gs} = -1.2 V	-	80	SiGe	[73]

Table 4.1: *Benchmarking of a few figures of merit for various pFET technologies.*

were transferred to a prepatterned Si chip as described in Section 2.2. To evaluate solely the GaSb core, the InAs(Sb) shell was selectively etched away in a middle section, which was later to be defined as the channel of the transistor, i.e., the ends of the GaSb segments remained covered in an InAs(Sb) shell, as illustrated in Fig. 4.5. The regions of the GaSb with a remaining InAs(Sb) shell would be defined as the source and drain regions of the transistor. The InAs(Sb) shell allows for excellent contacts because of the Fermi-level pinning in the conduction band and the narrow band gap, which results in a small Schottky barrier. Furthermore, the broken gap alignment of InAs(Sb)/GaSb provides an ohmic junction, which allows for a low access resistance to the GaSb core.[69] Figure 4.6a illustrates the I_{ds}-V_{ds} characteristics of the improved GaSb pMOS. The contacts improved by introducing an InAs(Sb) shell combined with a lightly Zn-doped GaSb channel result in an increased maximum drive current I_{on} = 85 µA/µm compared with the pMOS in the inverter. The ON-resistance R_{on} of the undoped pFET, 293 kΩ or 48 Ω·mm, was reduced by a factor of 10 to 29 kΩ or 5 Ω·mm for the improved GaSb pFET. This illustrates that there is much untapped potential in GaSb considering the improvement achieved in ON-performance by only minor modifications. Similarly, the maximum transconductance is boosted from 13 mS/mm

to 45 mS/mm at a bias of 0.5 V. Benchmarking the improved GaSb pMOS to state-of-the-art pFETs reveals much potential in the technology (Table 4.1).

CHAPTER 5

Tunnel devices

In this chapter, tunnel devices are explored as an alternative to traditional MOSFETs. These devices are mainly being considered for low-power applications, but recent reports indicate their promise as high-performance devices. This chapter is chiefly based on papers IV–VII.

5.1 Introduction to tunneling

As discussed in Chapter 1, there are two main paths to supply-voltage scaling. The first concerns the implementation of high-mobility materials, which was addressed in Chapter 3. The second approach involves steep-slope devices with SS lower than 60 mV/decade, which is the limit of conventional MOSFETs. As a result, much effort is being spent in the pursuit of TFETs, which do not suffer from the same

fundamental limit as MOSFETs that rely on the thermionic emission of carriers over a barrier. TFETs allow for SS below 60 mV/decade by filtering out electrons in the Fermi tail, which in turn would allow circuit designers to lower the supply voltage V_{dd} while maintaining a high drive current I_{on} without sacrificing I_{off} as would a conventional MOSFET as illustrated in Fig. 5.1a. A few interesting device concepts such as source-filtered MOSFETs have been reported in the literature, but they are complicated to realize experimentally.[74]

The tunneling through a barrier can be approximated by a triangular potential, and the tunneling probability for a uniform electric field can be calculated by the Wentzel–Kramers–Brillouin approximation[75]

$$T_{WKB} \approx exp\left[-2\int_a^b k(x)dx\right] \tag{5.1}$$

Inserting the E-k relationship of the wave vector in a triangular barrier into Equation 5.1 and solving the equation yields

$$T_{WKB} \approx exp\left(\frac{-4\lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\phi + E_g)}\right) \tag{5.2}$$

where λ is the tunneling barrier width, m^* is the effective mass, E_g is the band gap, $\hbar$ is the reduced Planck constant, and $\Delta\phi$ is the energy windows through which tunneling can take place. For band-to-band tunneling to occur, there must be states available in the channel to which carriers in the source can tunnel. For maximum tunneling probability, the barrier λ must be sufficiently thin so as not to hinder tunneling, i.e., the source–channel junction should be as steep as possible. Because the momentum must be conserved during tunneling, direct band gap semiconductors are preferred in tunneling devices, whereas indirect semiconductors such as Si must rely on a phonon-assisted tunneling process. To further maximize the tunneling current, a low m^* is desired; however, m^* is also closely related to E_g, which is

directly connected to I_{off} by thermal emission. Consequently, there is a trade-off in the I_{on}/I_{off} ratio when selecting material systems for TFET applications.

TFETs operate by carriers tunneling through a potential barrier, resulting in currents that are invariably lower than in a corresponding MOSFET.[76] For this reason, the tunnel devices in this thesis are based on a GaSb/InAs heterojunction that forms a type II broken band alignment,[77] which allows for tunneling without a potential barrier, as illustrated in Fig. 5.1b. Furthermore, the heterojunction is a natural p–n junction, even without doping, and both semiconductor materials are direct band gap materials. The relatively small effective masses of electrons and holes of III-Vs is an attractive feature to exploit to achieve high drive currents in tunneling devices because the tunneling current is directly related to the carrier mass. Moreover, III-V semiconductor heterostructures may be engineered to include a wide range of band gaps and band alignments between source and channel, which is key to achieving excellent ON- and OFF-properties in TFETs.[76,78–82] Promising work has been undertaken on InAs/GaSb TFETs with drive currents of up to 180 µA/µm, which are mainly attributed to the broken band gap alignment.[83–85] There have also been reports of TFETs in various material systems where sub-60-mV/decade slopes have been reported, but these devices suffer from low drive currents.[86–89] As discussed in Chapter 3, for a technology to truly be considered as a replacement for Si technology, it must be *at least* as good as Si in all aspects and additionally have one or more figures of merit that surpass those of Si. Preferably, the technology should also be easy to integrate directly on a Si platform to keep the manufacturing costs low.

For an ideal TFET, the OFF-state leakage current should be low, but real devices are rarely ideal and may be afflicted by a number of leakage paths.[90] Many devices, particularly III-V-based TFETs, suffer from defect-assisted tunneling, often due to mid-gap traps.[91] Further leakage paths include gate leakage through the oxide and Schottky–

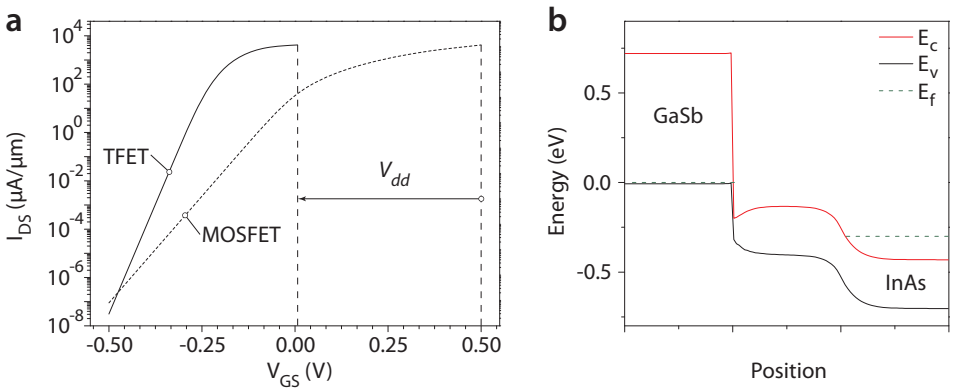


Figure 5.1: *(a) Schematic comparison of the transfer characteristics between a TFET and MOSFET, illustrating the advantage of a steep-slope device that can maintain a high I_{on}/I_{off} ratio when scaling the supply voltage. (b) Simulated band structure of a GaSb/InAs(Sb) heterojunction including an exponentially graded Sb composition from 0.4 to 0.1 over 10 nm at the interface and reverse biased at $V_{ds} = 0.3$ V.*

Read–Hall generation in the heavily doped source and drain regions. For extremely scaled devices, direct tunneling will begin to dominate the leakage, and the influence of defect-assisted tunneling will also increase and be particularly severe to narrow band gap materials. Ambipolar conduction is another leakage path that may impair the OFF-state performance of a TFET and is also particularly problematic in devices with narrow band gap semiconductors.

5.2 Axial Esaki diodes

Although the ultimate goal is to attain TFETs that outperform Si MOSFETs, emerging technologies are often evaluated with the simpler Esaki diode first.[92] A typical characteristic of an Esaki diode is a

so-called negative differential resistance (NDR), which is a signature of tunneling transport and is commonly used to evaluate planar epitaxial growth. A clear NDR region at room temperature is a sign of high crystal quality and homogeneity at the tunnel junction. Paper VI reports a peak current of $67\,\mathrm{kA/cm^2}$ at room temperature and a maximum reverse current of $1750\,\mathrm{kA/cm^2}$, which was the highest observed at the time of publication. The GaSb/InAs nanowires were grown by MOVPE, and to facilitate the growth, a short GaAs stem was first grown followed by a GaSb segment. Lastly, an InAs segment was grown on top of the GaSb, which also formed a thin parasitic InAs around the GaSb segment. To confine the transport to the axial GaSb/InAs heterojunction and avoid transport through the InAs shell, the nanowires were annealed in H_2 at $490\,^\circ\mathrm{C}$. This resulted in a thinning of the nanowire at the heterojunction where the InAs shell was selectively etched away to prevent any leakage along the shell.[93] The nanowires were transferred to a prepatterned Si chip and processed as described in Section 2.2.

The parasitic InAs(Sb) shell was utilized to aid in the contact formation to GaSb. The excellent contact resistance was attributed to the Fermi-level pinning of InAs and the broken band gap alignment of the GaSb/InAs, which resulted in an ohmic contact behavior. In forward bias, nominally undoped Esaki diodes presented an NDR, which was found to be bias dependent. As the bias increased, the peak voltage shifted slightly in the positive direction. The shift in peak voltage is believed to originate from a trap-charging effect, with a decay time of several minutes. The long decay time indicates an effect of surface traps rather than deep traps, which are expected to have a time constant on the order of nanoseconds.[94] Esaki diodes with some added Zn doping to the GaSb (Zn/Ga molar flow ratio $= 0.07$) display no hysteresis effect of high bias and an almost constant peak-to-valley current ratio for a series of bias sweeps. Simulations indicate that the introduction of Zn broadens the GaSb well and hence lifts

the hole sub-band, which effectively increases the conduction–valence band overlap, leading to an increase in the tunneling current in forward bias. Temperature-dependent measurements reveal a weak dependence on the reverse current, attributed to the small change in band gap and band offset as well as the increased series resistance, mainly in the GaSb.

To attain the performance required to be competitive compared to Si, one approach includes better doping control to reduce access resistance and control threshold voltage. To understand this in greater detail, a series of GaSb/InAs nanowires were grown with varying doping profiles. In addition to nominally undoped nanowires and a low Zn doping in the GaSb (Zn/Ga = 0.07), two batches of nanowires were grown with a high Zn flow (Zn/Ga = 0.56) during the GaSb segment growth, and in the first batch, the InAs segment was nominally undoped, whereas for the second batch of nanowires, Se was introduced into the InAs segment (Se/In = 0.26). What is immediately clear in Fig. 5.2 and Table 5.1 is the influence of the heavier Zn doping on the peak and reverse currents. Furthermore, the incorporation of Se in the InAs segment provides further significant improvement. The peak voltage shifts to more positive values with increased Zn doping, and this result agrees well with the expected Fermi-level movement. Simulations of ideal GaSb/InAs diodes indicate that the reverse current should only be marginally affected by the p-side doping level, and thus the increase in reverse current is attributed to the reduction in access resistance of the device. Additionally, Esaki diodes fabricated from nanowires where the InAs is also doped display a further increase in peak and reverse current by mainly reducing the access resistance further.

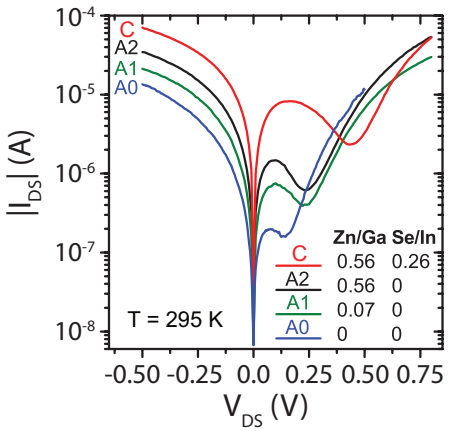


Figure 5.2: *I_{ds}-V_{ds} characteristics of GaSb/InAs(Sb) Esaki diodes with various doping profiles. Simulations indicate that heavier p-doping should only have a minor effect on the reverse current (types A0 ⇀ A2). Instead, the increase in reverse current is attributed to the lower access resistance. The access resistance is further lowered by introducing Se into the InAs(Sb) segment (type C).*

Device type	Zn/Ga	Dop/In	J_{ds} at V_{ds} = -0.5 V (MA/cm^2)	J_{peak} (kA/cm^2)	ρ_{GaSb} (mΩ·cm)	$\rho_{InAs(Sb)}$ (mΩ·cm)
A0	0	0	0.55	8	40	3.4
A1	0.07	0	1.75	67	25	-
A2	0.52	0	2.2	94	7.1	-
B	0.26	0.31 (Zn)	0.16	-	-	80
C	0.52	0.26 (Se)	3.6	420	7.3	0.67

Table 5.1: *Summary of a few figures of merit for GaSb/InAs Esaki diodes with various doping profiles.*

5.3 Axial TFETs

Although the GaSb/InAs Esaki diodes display excellent current densities, the ultimate goal is to attain TFETs with high drive currents and steep-slopes. A TFET has more stringent device design considerations such as an additional terminal and the introduction of an oxide enabling electrostatic modulation at the tunneljunction. In favor of an efficient gate action on the heterostructure, the Se-doped Esaki diode is not suitable in a TFET application. For an n-type TFET, the InAs(Sb) segment at the heterojunction should be undoped or compensation doped to enable efficient gate action. For this reason, type A2 nanowires solely with Zn/Ga = 0.56 and with no intentional doping in the InAs segment were implemented in a TFET device design.

As a reference, devices were fabricated from GaSb/InAs nanowires where the neck formation was omitted, i.e., a continuous ∼5 nm InAs shell covered the entire nanowire. After the formation of a source and a drain at either end of the nanowire, a gate was formed over the axial GaSb/InAs(Sb) heterojunction. The dual channel path, one through the n-type channel in the InAs shell and one through the GaSb/InAs(Sb) heterojunction, was manifested as an ambipolar conduction through the device.[69] At positive gate bias, electrons accumulate in the InAs shell, enabling n-type conduction and a reduced tunneling through the heterojunction at the core. In contrast, a negative bias depletes the InAs shell from electrons, and the majority of the current is forced through the GaSb/InAs(Sb) heterojunction as illustrated in Fig. 5.3a. These devices cannot be turned off.

Devices with a constriction at the heterojunction were evaluated. Figure 5.3b illustrates the output characteristics of a device where the gate has been placed on the InAs(Sb) segment by an underlap of 35 nm to the heterojunction. The maximum ON-current is calculated at 310 µA/µm, normalized to the periphery of the constriction, and at $V_{ds} = 0.5$ V. The 35 nm underlap of the gate effectively forms

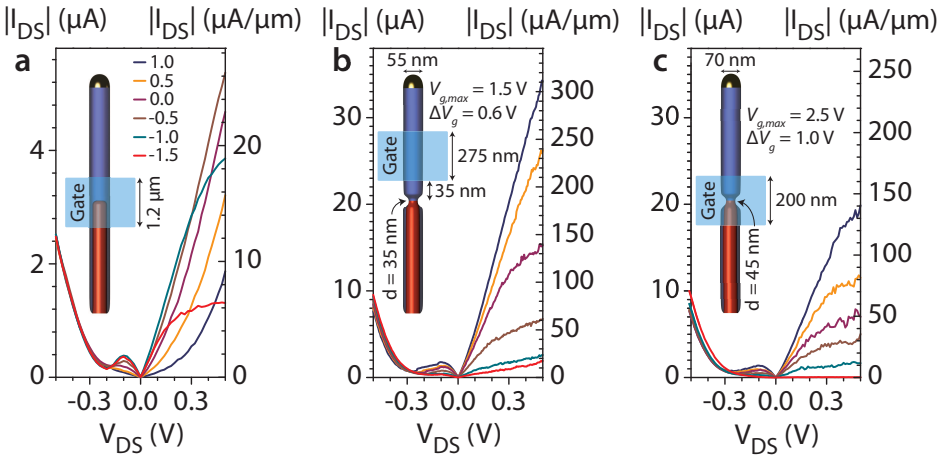


Figure 5.3: *Electrical characteristics of various axial TFET device geometries and designs. (a) I_{ds}-V_{ds} characteristics of an undoped device where the formation of a neck at the heterojunction has been omitted ($d = 65\,nm$). (b) Output characteristics of a device with a Zn-doped GaSb core ($Zn/Ga = 0.56$) and an underlapping gate by 35 nm to the heterojunction. The diameter at the constriction is 35 nm. (c) Same as (b) but with a 120 nm overlap of the gate and a diameter of 45 nm at the constriction.*

an nMOSFET in series with a broken gap tunnel junction, which by default is open for conduction. This device design will suffer in the OFF-state, allowing tunneling through the heterojunction. A maximum peak current density is observed at $J_{peak} = 240\,\mathrm{kA/cm^2}$, and upon closer examination of the NDR region, the peak voltage remains almost constant or moves to slightly higher V_{ds} bias. Such properties indicate that the underlapping gate still imposes some action on the heterojunction.

Figure 5.3c illustrates the I_{ds}-V_{ds} characteristics of a TFET where the gate has been placed over the constriction at the axial heterojunction. These devices promote improved OFF-state characteristics because of (i) the improved electrostatics of a narrower channel, in agreement with prior work,[87] i.e., the constriction at the GaSb/InAs(Sb) heterojunction and (ii) the device design where the gate action is imposed on both the GaSb and InAs(Sb) segments. It is argued that, although the GaSb is heavily p-doped, some movement of the bands may still be possible; however, the gate action will mainly be imposed on the bands of InAs(Sb). As a consequence, in the ON-state, the tunneling path may be compromised as the bands of both the GaSb and the InAs(Sb) will bend downward. The movement is expected to be small for the GaSb, but it may deplete carriers near the junction. In the OFF-state, the device should turn off more efficiently than the underlapping device because here the band gap of GaSb is available to turn off the current. Figure 5.4 illustrates the more efficient turn-off mechanism of an overlapping gate electrode design compared with an underlapping design.

Intuitively an ideal gate electrode placement would be exactly at the heterojunction or possibly a very small overlap onto the GaSb segment. Figure 5.5 illustrates the data for a TFET where the gate, $L_g = 290\,\mathrm{nm}$, has been placed exactly at the axial heterojunction interface ($\sim$5 nm overlap) and where the gate oxide has been scaled to an equivalent oxide thickness of 1.3 nm, i.e., equivalent to a corre-

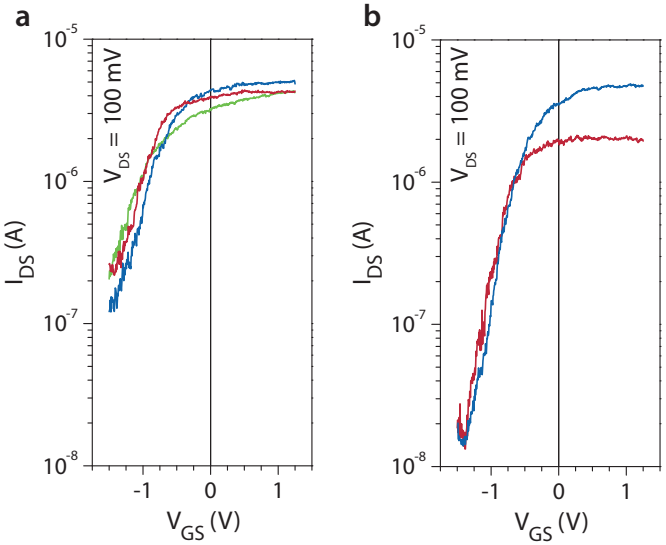


Figure 5.4: *Comparison of the off-state characteristics of several devices with gate electrodes (a) underlapping and (b) overlapping the GaSb/InAs(Sb) heterojunction.*

sponding SiO_2 gate oxide. The maximum ON-current is normalized at 130 µA/µm for $V_{ds} = 300$ mV. The *SS* decreases from 320 mV/decade at room temperature to 17 mV/decade at 4.2 K and is similar to values reported on other III-V TFETs.[91] The temperature-dependent *SS* is believed to originate from trap-assisted tunneling from a high D_{it} at the semiconductor/high-κ interface. An ambipolar device characteristic is also evident in Fig. 5.5 a and b that originates from band-to-band tunneling at the gate–drain junction relating to the narrow band gap of InAs(Sb). Figure 5.5c illustrates an nearly temperature-independent transconductance at $V_{ds} = 300$ mV and indicates that temperature-dependent scattering mechanisms do not limit the ON-state of the device.

The ON-state may be improved further by drawing on knowledge from the Esaki diodes regarding doping profiles where incorporating a dopant also on the n-side of the heterojunction yields substantial improvement to the access resistance and current levels. A similar approach to a TFET structure is expected to provide similar benefits. However, the doping profile must be modified to accommodate a channel region directly at the heterojunction interface where efficient gate action is imperative to achieve the desired functionality, i.e., an undoped InAs(Sb) segment directly after the GaSb followed by a heavily n-doped segment.

A common approach to increasing the current levels and decreasing the access resistance is to increase the doping in the source and the in drain. In a TFET, there are several aspects to consider regarding source doping. A highly degenerate source will negate the source filtering operation or cold-carrier injection of a TFET. On the contrary, a lightly doped source is not desired either because of the increase in access resistance and a reduced electric field at the tunnel junction. It has been shown that heavily degenerate source doping compensates the effect of cold-carrier injection by the strong increase in electric field in the tunnel region.[95] The influence of source dop-

Ref.	Material system	Band alignment	I_{on} (μA/μm)	SS (mV/dec)
Paper V	GaSb/InAs(Sb)	Broken	310	300
[84]	GaSb/InAs	Broken	180	200
[79]	$GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$	Staggered	60	∼200
[97]	InAs/Si	Staggered	2.4	150
[89]	Si	Homojunction	0.15	36
[98]	$In_{0.53}Ga_{0.47}As$	Homojunction	24	∼200
[86]	$In_{0.53}Ga_{0.47}As$	Homojunction	5	58

Table 5.2: *Benchmarking of experimental TFETs with varying band alignments. The general trend points toward high drive currents for broken band gap TFETs and sub-60-mV/decade SS for homojunction TFETs.*

ing on the output characteristics has also been shown to influence strongly the saturation voltage such that lower doping levels in the source are directly correlated to a delayed saturation.[96] Most likely, advanced band/materials engineering is required to achieve optimum performance, perhaps by introducing a heavily δ-doped pocket in the source at the heterojunction. On the drain side, a low drain doping near the channel–drain junction may be suitable to minimize any ambipolar behavior. The general trend in TFETs is that high ON-currents are achieved in devices with broken band gap alignments, whereas homojunctions operate below 60 mV/decade, as indicated in Table 5.2.

A higher-quality high-κ/semiconductor interface would also improve the ON-state by reduced surface scattering as well as the OFF-state by providing improved electrostatics. A lower OFF-current may be achieved by replacing the narrow band gap InAs(Sb) on the n-side with a wider band gap semiconductor, e.g., InGaAs. It has been proposed that a device without gate–drain overlap would reduce the ambipolar behavior without affecting I_{on}.[99] In the OFF-state, the reduced inversion carrier concentration will also reduce the built-in electric field

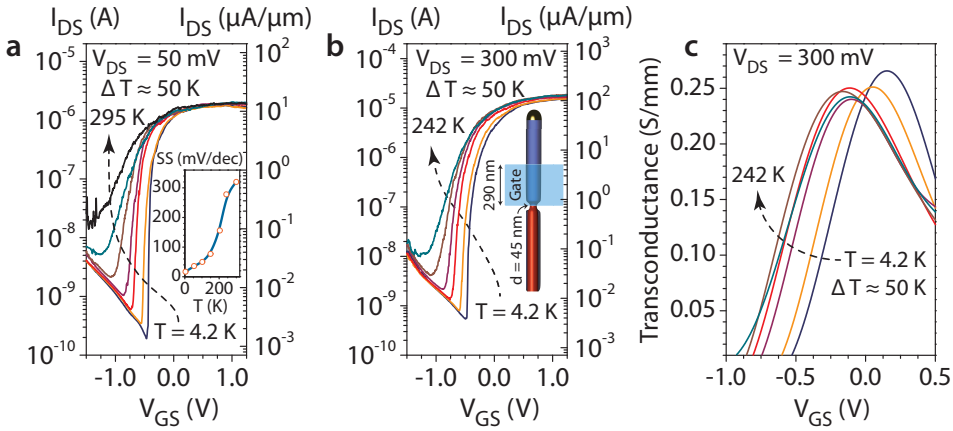


Figure 5.5: *Temperature-dependent transfer characteristics and transconductance of a device where the gate has been aligned to the heterojunction (∼5 nm overlap) and with a scaled effective oxide thickness from 1.8 nm to 1.4 nm (a) Transfer characteristics at 50 mV bias from 4.2 K to room temperature in increments of approximately 50 K. The inset shows the temperature-dependent SS. (b) Temperature-dependent I_{ds}-V_{gs} characteristics and (c) transconductance at 300 mV bias.*

at the channel–drain junction and could be further improved by a low drain doping near the channel–drain junction. This methodology has been successfully implemented in the literature.[100,101]

5.4 Radial Esaki diodes and TFETs

There is evidently much room for improvement regarding the axial TFET device design; however, an axial device design may not be the ideal architecture for a nanowire TFET. It is clear that nanowire devices gain in drive current by scaling the cross-sectional area of the channel at a fixed supply voltage. It is also possible to maintain a

constant drive current by reducing the supply voltage while increasing the nanowire diameter. Both approaches will suffer from deteriorated electrostatics. Alternatively, the cross-sectional area of the nanowire may be kept constant, and a boost in drive current can be achieved by arranging nanowires in parallel arrays, preferably in a vertical device architecture favoring the superior gate electrostatics of a GAA design. This approach will, in the same way as the cross-sectional approach, consume valuable chip area. For this reason, the use of a core–shell nanowire where the heterojunction is engineered in the radial direction provides an attractive means of boosting the drive current without compromising either chip area or device electrostatics.

The combination of axial and radial III-V heterostructures, i.e., along and perpendicular to the main axis of the nanowire, enables the control of the current path through the nanowire without physical or electrostatic constrictions. Figure 5.6 illustrates the principle of operation of a radial nanowire TFET. Here the nanowire segments have been grown in a reverse order to the axial GaSb/InAs nanowires. InAs/GaAs/GaSb 1.3 µm / 100 nm / 1 µm segmented nanowires were grown by MOVPE with diameters of 45–55 nm. Because the growth sequence began with an InAs segment and was finalized by a GaSb segment, no parasitic InAs shell was available to form a radial InAs heterojunction and electrically interconnect the top and bottom segments of the nanowire. Consequently, a 5–15 nm InAs(Sb) shell was grown around the nanowire. Two sets of nanowires were grown with differing doping profiles in the GaSb core, one with $\mathrm{Zn/Ga} = 0.21$ and another with $\mathrm{Zn/Ga} = 0.39$, and thus both were significantly lower than their axial counterpart.

The design and processing of a radial device is notably more challenging than the more traditional lateral process for nanowire devices. The upper section of the InAs(Sb) must be selectively etched away to allow for contact formation directly to the GaSb core. High-precision alignment is necessary for the source and drain electrodes, formed by

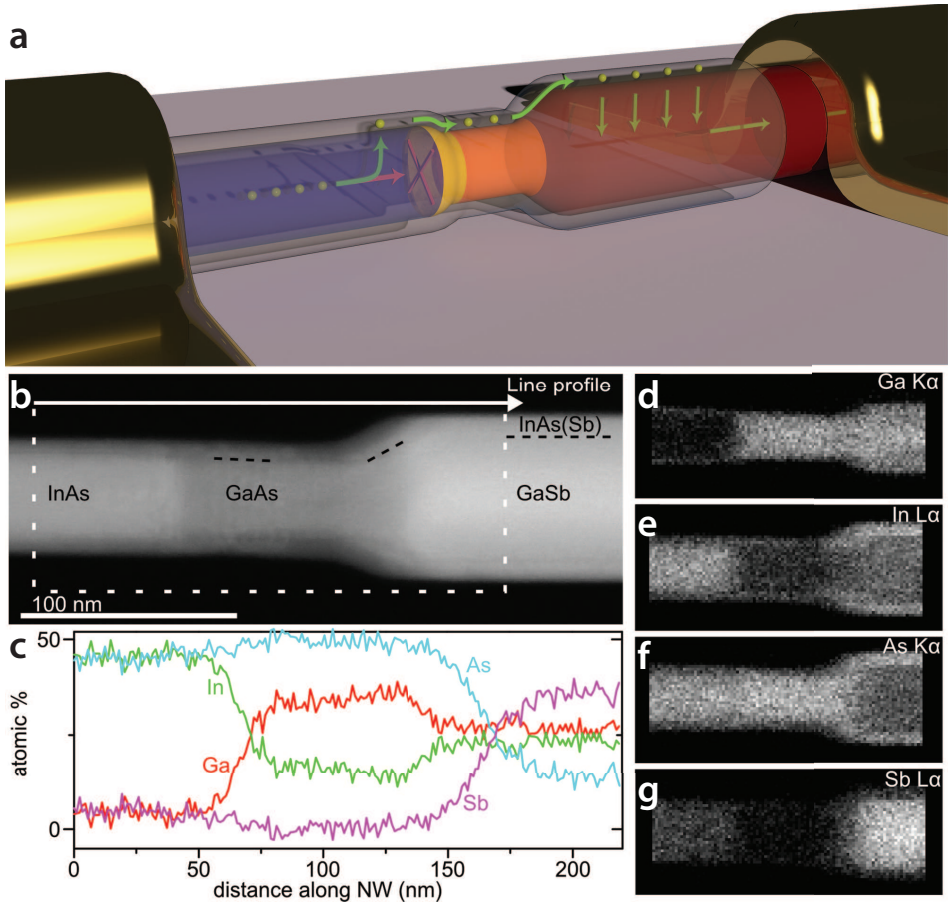


Figure 5.6: *(a) Schematic illustration of the principle of operation of a radial TFET. Carriers enter from the InAs and are blocked by the GaAs barrier and constrained into the InAs(Sb) shell. From the shell, the carrier may tunnel into the GaSb core, where they are swept out through the drain. The gate (not shown) is placed such that it covers the radial GaSb/InAs heterojunction and is mainly imposed on the radial heterojunction. (b) High-angle annular darkfield image taken by a 1 nm probe in scanning transmission electron microscopy mode of the InAs/GaAs/GaSb heterostructure and (c) a corresponding compositional line profile calculated from the XEDS spectrum image. (d–g) XEDS elemental maps recorded from the nanowire.*

EBL and thermal metal evaporation, because the gap between drain and GaAs barrier should be as small as possible and, correspondingly, the source electrode should be as close to the radial tunnel junction as possible without a direct connection to the InAs(Sb) shell. Source and drain formation is followed by an EBL step and high-κ deposited by ALD. Finally, a top gate is formed to enable efficient gate action of the radial GaSb/InAs(Sb) heterojunction. Again, the precision of the gate placement is crucial for efficient TFET operation, becausethe aim is a slight overlap to the GaAs barrier segment.

The design of a radial tunnel junction requires an axial heterostructure barrier segment to suppress axial leakage between the InAs and GaSb core segments, which would be substantial considering the nature of the broken gap alignment of InAs and GaSb. The GaAs barrier segment redirects the current into the InAs shell from which electrons may tunnel radially into the GaSb core, on the other side of the barrier. On the GaSb side, the InAs shell must be partially etched away to allow for contact formation directly to the GaSb core, enabling radial core–shell tunneling. At this point, some devices were evaluated as Esaki diodes, but by adding a high-κ gate dielectric and a top gate at the radial InAs(Sb)/GaSb heterojunction, the simpler Esaki diode can be evolved into a TFET with expanded functionality.

The unique advantage of a radial device architecture is the smaller footprint than that of an axial or planar device layout. An axial or planar device will have a direct correlation between gate length and occupied chip area, whereas a radial vertical device architecture allows for a longer gate without impacting the chip area. As a demonstration of an increased current per unit chip area, two-terminal electrical data of radial GaSb/InAs Esaki diodes was evaluated. Zn-doped Esaki diodes, $\mathrm{Zn/Ga} = 0.39$, displayed current densities of $J_{peak} = 2311\,\mathrm{kA/cm^2}$ (Fig. 5.7a). The data is normalized to the largest cross-sectional area of the nanowire, which would correspond to the occupied on-chip real-estate. Normalizing the data to the active tunneling area (ATA) yields

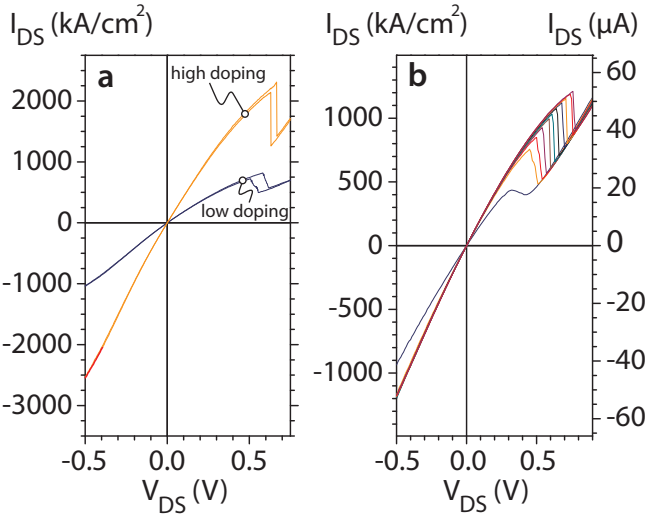


Figure 5.7: *Electrical output characteristics of forward-biased radial Esaki diodes and TFETs. (a) I_{ds}-V_{ds} characteristics of two radial Esaki diodes. One has high doping in the GaSb core (Zn/Ga = 0.39) and one has a lower doping level (Zn/Ga = 0.21). The dual trace indicates two sweep directions. (b) Radial TFET with high doping in the GaSb core. $V_{g,max}$ = 1 V, ΔV_g = 0.2 V.*

$J_{ATA} = 335\,\mathrm{kA/cm^2}$. Keeping in mind that the best axial Esaki diodes thus far were more heavily doped, $\mathrm{Zn/Ga} = 0.56$ *and* $\mathrm{Se/In} = 0.26$, yield $J_{peak} = 350\,\mathrm{kA/cm^2}$ and $J_{ATA} = 420\,\mathrm{kA/cm^2}$, the radial device architecture displays clear evidence of current density per unit chip area seven times higher, although at higher V_{peak}. Axial Esaki diodes where the doping of the n-side was omitted are limited at $J_{peak} = 40\,\mathrm{kA/cm^2}$ ($J_{ATA} = 94\,\mathrm{kA/cm^2}$), and therefore further improvement is expected by also introducing doping into the radial InAs(Sb) shell.

A radial device architecture implies a gate field parallel to the tunneling direction, which has been shown to improve the tunneling efficiency.[84,102,103] Moreover, a radial design architecture has only a single high-κ/semiconductor interface to optimize compared with two in the axial case. In addition, the high-κ interface is moved away from the tunneling junction, which may further improve the performance of radial TFETs as compared with their axial counterpart.[104]

Figure 5.7b illustrates the electrical characteristics of a radial TFET with high doping in the GaSb core ($\mathrm{Zn/Ga} = 0.39$) and $L_g = 180\,\mathrm{nm}$. The peak current density $J_{peak} = 1211\,\mathrm{kA/cm^2}$ ($J_{ATA} = 258\,\mathrm{kA/cm^2}$) again demonstrates the advantage over an axial GaSb/InAs TFET ($\mathrm{Zn/Ga} = 0.56$) with $J_{peak} = 77\,\mathrm{kA/cm^2}$ ($J_{ATA} = 240\,\mathrm{kA/cm^2}$). Both the radial Esaki diodes and the radial TFETs demonstrate clear NDR regions at room temperature, which again elucidates the high crystal quality at the interface and homogeneity at the junction.

The electrical characterization of radial TFETs with lower doping in the GaSb core ($\mathrm{Zn/Ga} = 0.21$) and $L_g = 80\,\mathrm{nm}$ is illustrated in Fig. 5.8a. We observe a high output conductance at high V_{ds}, indicating a transport limited by series resistance and/or a leakage path along the underside of the device, which is a flaw inherent to the Ω-gate device design. Figure 5.8b illustrates the temperature-dependent transfer characteristics at $V_{ds} = 50\,\mathrm{mV}$. The *SS* increases from 17 mV/decade at 4.2 K to 300 mV/decade at room temperature, which is similar to the axial devices. Moreover, the traces at 4.2 K and 55 K display a

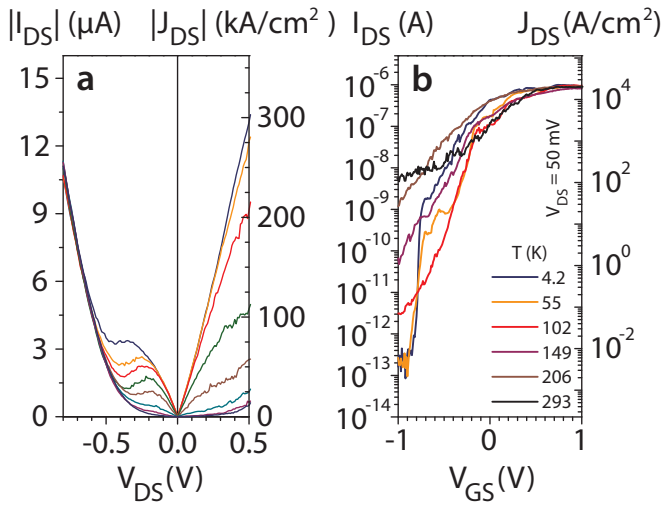


Figure 5.8: *Reverse-biased electrical characterization of radial TFETs with lower doping in the GaSb core (Zn/Ga = 0.21) and L_g = 80 nm. (a) I_{ds}-V_{ds} characteristics with $V_{g,max}$ = 1.5 V, ΔV_g = 0.4 V. (b) Temperature-dependent I_{ds}-V_{gs} characteristics from 4.2 K to room temperature in approximately 50 K increments. The traces at 4.2 K and 55 K display a distinct change in transport mechanism compared with the remaining traces.*

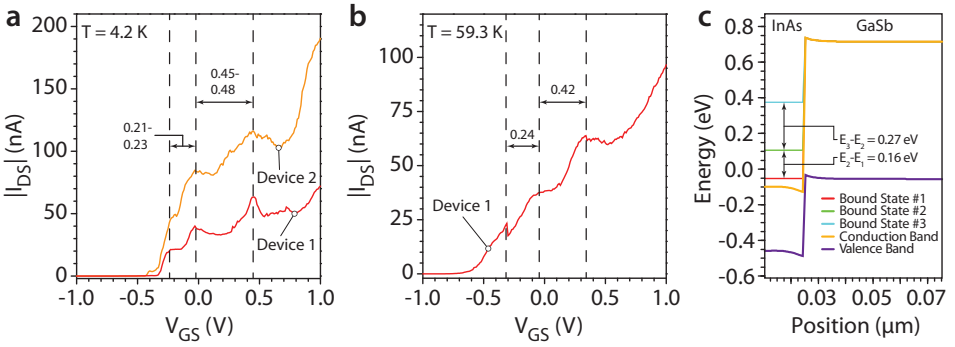


Figure 5.9: *(a) Forward-biased transfer characteristics at 50 mV bias of two devices with similar InAs shell thicknesses at T = 4.2 K. The steps in the transfer characteristics are attributed to the bound states formed by the confinement in the shell. (b) Same as (a) but for device 1 at T = 59.3 K. (c), (d) Effective-mass simulations of the energy levels of (c) a 15 nm wide InAs quantum well. By scaling the InAs shell, it is possible to move the first sub-band above the valence of GaSb, allowing for a device to be normally off at 0 V bias. The shell thickness may be used as a parameter to tune the threshold voltage of the device.*

categorical shift in transport mechanism compared with the traces at higher temperatures. The issue of the OFF-state characteristics is likely to be an artifact of the inherent drawback of an Ω-gate device design that does not wrap fully around the nanowire. An additional leakage path is likely to occur through mid-gap states due to interface states at the gate dielectric interface or crystal defects. It has been demonstrated that even a single defect may deteriorate the *SS* and that the effect is more pronounced in TFETs than in MOSFETs.[105–107]

The confinement effects of a thin InAs shell offer unique properties at low temperatures, as illustrated in Fig. 5.9. The transfer characteristics at 4.2 K and 55 K display clear steps in the current at 50 mV bias. Similar characteristics have been reported in other 2D-2D tun-

neling systems.[108] Furthermore, the characteristics are not limited to a single device but have been observed in devices with similar shell thicknesses. This observation may be explained by two quantum-well systems connected in series. Transmission electron microscopy shows that the InAs shell surrounding the GaSb is approximately 15 nm, whereas the shell thickness is substantially thinner across the GaAs segment and strained. This will induce two differing sets of quantization levels in the connected quantum wells, where it is argued that the quantum well surrounding the GaAs has a single bound state available for transport whereas the 15-nm-thick shell enclosing the GaSb core has three bound states. Effective-mass simulations are used to determine the energy levels of the bound states as illustrated in Fig. 5.9 c and d. The gate action is assumed to impose mainly on the InAs shell surrounding the GaSb, i.e., the band bending in the GaSb core is neglected, and can be used to access the three discrete bound states. Simulations predict an energy spacing of $E_2 - E_1 = 0.16\,\mathrm{eV}$ and $E_3 - E_2 = 0.27\,\mathrm{eV}$, i.e., a ratio of 1.7. Correspondingly, the gate bias must increase from $-0.31\,\mathrm{V}$ to $-0.07\,\mathrm{V}$ ($V_{g,1\to2} = 0.24\,\mathrm{V}$) to reach the second bound state. A leverage factor on the gate action imposed on the quantum well is estimated to be 1.5 ($V_{g,1\to2}/E_{1\to2} = 0.24/0.16$). The gate bias must be further increased by $V_{g,2\to3} = 0.42\,\mathrm{V}$ to access the third bound state of the 15-nm-thick InAs quantum well. The experimental ratio between the peaks, $V_{g,2\to3}/V_{g,1\to2} = 1.75$, is recognized to agree well with the simulated values.

It has been highlighted that the GaSb/InAs broken gap alignment is open for conduction at 0 V bias, which may not always be desirable. The method of exploiting quantization effects to move the bound states of the InAs is an elegant way to control the threshold voltage of a TFET.

CHAPTER 6

A few last words...

Having spent a few years in academia, I would like to share a few thoughts in this final chapter.

Many of us are required to produce results for a conference deadline or are faced with the notion that a rival group may publish on our topic before we do, sometimes pressuring us into taking the easy option. The competition never sleeps, as the saying goes. Often, a quick literature study may be conducted to find a suitable theory to explain the experimental results we just plotted, in an attempt to add substance and credibility to our work. In truth, simulation environments are often highly idealized and neglect many of the practical issues of devices in the real world. I would therefore like to share some words of of my own reflections taking a step back when a model or theory, particularly someone else's, agrees well with our experimental data. It is often too easy to accept without question a model or theory if it appears to support our results, which is why I urge more self-scrutiny

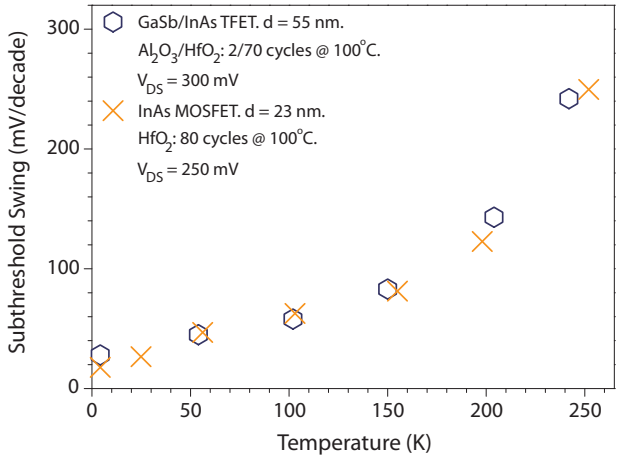


Figure 6.1: *The SS properties of a 23nm InAs MOSFET compared to a 55nm GaSb/InAs TFET with similar high-κ deposition. The similarity indicates that we are probing not the intrinsic device properties, which should by definition be fundamentally different, but rather the high-κ gate dielectric. There is always the possibility of pure coincidence.*

among researchers. *Does this model really apply to my problem? What simplifications has the theory assumed?* The resources of academia are often limited and do not produce results in such quantities that they may be assumed to be statistically significant, and hence there is always a danger when drawing generalized conclusions from a small set of data.

As an example, you may remember from Chapter 5 that the *SS* of the axial and radial GaSb/InAs TFETs showed strong similarities. This begs the question: *Are we really probing the intrinsic properties of our device?* Digging through some old data, I put together Fig. 6.1. It is remarkable to compare the *SS* of an InAs nanowire MOSFET

of another diameter to that of a GaSb/InAs nanowire TFET. The matching *SS* could, of course, be a coincidence, but it may also indicate that the subthreshold characteristic is mainly probing the high-κ/III-V semiconductor interface rather than the intrinsic properties of the device.

The exceptional fit of the modeled band-structure of the InAs shell on the GaSb core, for the radial TFETs, to the steps in the transfer characteristics was difficult to accept at first but was found to be the most plausible explanation. Models usually have a myriad of parameters to tune to achieve the best fit to the data. The VS model is lighter on input parameters, but researchers may still be deceived if they lack experience and confidence in the input parameters. Because our laboratory does not have the facilities to measure the capacitance on single nanowires, the parameter extraction through VS modeling becomes uncertain as we begin to speculate about C_{inv}. Figure 6.2 illustrates the fits for two different assumed C_{inv}. Although the fitting appears to be similar, there is a large disparity in μ_{app} and $VS_{velocity}$. To be able to trust the extracted values, the number of unknown parameters should be kept at a minimum, preferably not exceeding one. This often requires reference devices to measure parameters, such as long-channel mobilities.[110]

Although there is still much that we do not understand, some truly spectacular physics and amazing device technologies are being researched today, and I am confident that we are only just beginning our technological journey. I remain unconvinced that any one transistor technology will be the mainstream replacement for Si anytime soon, but there are a few viable candidates. I do believe that many of the technologies suffer from similar issues, although they attempt to distinguish themselves from each other as much as possible. Let us take MOSFETs vs. TFETs as an example. TFETs do indeed appear promising for low-power applications as steep-slope switches and may give the industry a few more years of leeway in continuing Moore's

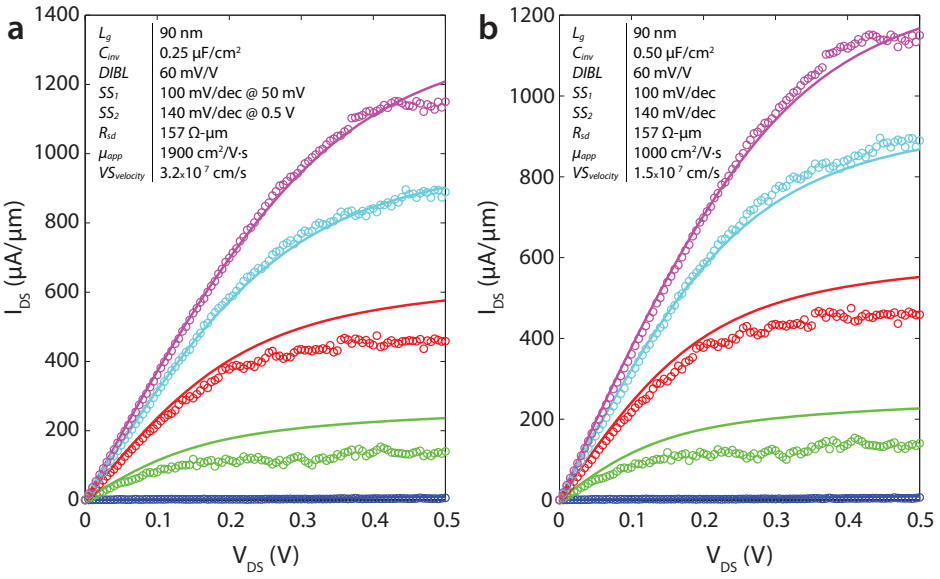


Figure 6.2: *VS modeling of 15-nm-diameter InAs nanowire MOSFETs.*[109] *(a) An assumed inversion capacitance of 0.25 µF/cm² results in μ_{app} = 1900 cm²/V·s and $VS_{velocity}$ = 3.2×10⁷ cm/s. (b) Corresponding modeling for an inversion capacitance of 0.50 µF/cm² results in μ_{app} = 1000 cm²/V·s and $VS_{velocity}$ = 1.5×10⁷ cm/s. This illustrates the necessity of additional measurements that can provide supporting information to validate the modeling. Because our laboratory is not equipped to measure the capacitance of single nanowires, the extracted mobilities and injection velocities must be viewed with some skepticism.*

law. They are, however, still barrier-controlled devices, which means that when we shrink the gate length sufficiently far, we will have the "same" source–drain tunneling leakage as we would in a MOSFET. Maybe we need to think far outside the box when considering future transistor technologies?

As of late, the Higgs boson has gained much attention, and perhaps it would be possible to locally control the Higgs field to control the mass of the carriers. Such a transistor could effectively increase the electron mass just at the beginning of the channel, which would reduce the tunneling probability in the OFF-state of an extremely scaled transistor and lower the effective mass for the ON-state, i.e., the field manipulation would work in unison with the gate. This idea may not be possible to realize in practice, but there are several other approaches being explored for future electronics. Must a transistor operate by the motion of charge? A few examples where other physical properties are manipulated or exploited include: electron spin in spintronics,[111] electron wave quantum number in valleytronics,[112] magnetic cellular automata,[113] quantum computing,[114] and microelectromechanical systems.[115]

I would like to go out on a limb and state that the most valuable contribution to the field of III-V devices at the moment would be a method of managing a perfect gate dielectric on a III-V surface. This key issue would not only allow for high-performance devices but would also facilitate the analysis of many devices. Some work has demonstrated this, but the methodology is a closely guarded secret.[38]

In terms of MOSFETs, access resistance is a crucial parameter and must be addressed for high-performance devices. In a vertical nanowire device geometry, this means either heavily doped source and drain regions or more sophisticated methods such as controlled overgrowth. Naturally, short spacers, i.e., ungated segments, and extremely scaled gate lengths are desirable to achieve maximum performance. Despite this, there is actually more to gain by addressing

the issue of parasitics in the device layout. To date, little research has been undertaken on the optimization of vertical nanowire architectures, particularly 3D circuit designs.

Regarding a full III-V CMOS technology, there are still few reports in the literature on viable solutions. N-type III-V devices have displayed excellent performance figures, whereas the p-type devices have been falling behind. Arguing in terms of bulk mobilities, there is a huge disparity between the best n-type binary III-Vs and the p-type counterparts. Technological tricks can be used when attempting to match the n-type and p-type networks, but the gap may be too large to enable the combination of binary III-Vs. There is a notion that, as the dimensions of the devices shrink, the transistors will approach to the ballistic regime where the mobility may no longer be the limiting performance metric.

Although successful high-κ integration has been demonstrated on n-type III-Vs, the question is whether the same methodology could be applied to, for example, GaSb. It may not be absolutely necessary to fabricate the gate dielectric for both n- and p-type simultaneously, but it would be a preferred solution. Possibly, n- and p-type may be fabricated from the same III-V material system, which may facilitate the high-κ integration.[6]

What about TFETs? TFETs are beginning to show impressive figures of merit and may realize the requirements for low-power devices, probably with moderate performance, but I remain doubtful as to whether TFETs are the solution to the problem of replacing the high-performance Si line. Ultimately, TFETs will suffer from the same scaling drawbacks as a MOSFET because of their principle of operation, but they may buy industry a few more golden years of Moore's law.

At a conference this summer, there were some discussions regarding which technology would be *the* next-generation replacement for Si, and the consensus appeared to be that transistors today are already

extremely good but that there is a disconnect on the application front. Many fields remain uncharted with respect to transistor applications, and one comment at the conference went something like, "If we can find novel applications for the transistors we have today, we don't have to worry about transistor performance. As long as we don't tell the general public what goes into the devices, they would be none the wiser." At this time I think it is too early to decide which technology will be the winner. Only time will tell.

APPENDIX A

Appendix

A.1 The Virtual-Source Model

The current in a MOSFET, I_{ds}, is given by

$$I_{ds} = W \cdot Q_n(V_{gs}, V_{ds}) \cdot \langle v(0) \rangle \tag{A.1}$$

where W is the width of the device, Q_n is the inversion layer charge, and $\langle v(0) \rangle$ is the velocity at the beginning of the channel. After some algebraic exercise, where we input the drift velocity as $\mu_{eff} \cdot V_{ds}/L$, the equation for the current in the linear or triode regime, i.e., $V_{ds} < V_{sat}$, results in

$$I_{ds,lin} = \frac{W}{L} \cdot \mu_{eff} \cdot C_{inv} \cdot (V_{gs} - V_t) \cdot V_{ds} \tag{A.2}$$

where μ_{eff} is the effective mobility, and the inversion capacitance C_{inv} relates to the semiconductor inversion capacitance $C_S(inv)$ and the

oxide capacitance C_{ox} as

$$C_{inv} = \frac{C_{ox} \cdot C_{s,inv}}{C_{ox} + C_{s,inv}} \tag{A.3}$$

Correspondingly, the equation describing the current in the saturated regime is

$$I_{ds,sat} = W \cdot C_{inv} \cdot (V_{gs} - V_t) \cdot \upsilon_{sat} \tag{A.4}$$

where $\langle v(0) \rangle$ has been replaced by the saturation velocity υ_{sat}.

To transform the simplistic piecewise model into a more comprehensive model and achieve a smooth transition between the triode and saturation regions of the transistor, the VS model introduces an empirical function called the saturation function F_{sat}, which is defined as

$$F_{sat}(V_{ds}) = \frac{V_{ds}/V_{sat}}{[1 + (V_{ds}/V_{sat})^{\beta})]^{1/\beta}} \tag{A.5}$$

where β is a fitting parameter, which is usually approximately 1.8 for nFETs. The complete VS I_{ds}-V_{ds} characteristics are thus given by

$$I_{ds} = W \cdot Q_n(V_{gs}, V_{ds}) \cdot F_{sat}(V_{ds}) \cdot \upsilon_{sat} \tag{A.6}$$

A.1.1 Landauer approach

To describe nanoscale devices on a more fundamental level, we may apply a Landauer–Büttiker approach to analyze the transport on the nanoscale.[116] The current can be described by

$$I_{ds} = \frac{2q}{h} \int T(E)M(E)(f_s - f_d)dE \tag{A.7}$$

where q is the elementary charge, h is Planck's constant, $T(E)$ is the transmission, $M(E)$ is the number of conducting modes, and f_s and

f_d are the equilibrium Fermi distributions at the source and drain reservoirs, respectively. The number of modes is given by $M(E) = g_v W \frac{\sqrt{2m^*(E-E_c)}}{\pi\hbar}$. We begin by evaluating the current at the beginning of the channel and under low V_{ds} bias. If we also assume ballistic transport and Maxwell–Boltzmann statistics, we may apply a Taylor expansion series to the Fermi distributions and write the current as

$$I_{ds,lin} = \frac{2q^2}{h}\left(\int_{E_c}^{\infty} g_v W \frac{\sqrt{2m^*(E-E_c)}}{\pi\hbar}\frac{f_0}{k_B T} dE\right) V_{ds} \tag{A.8}$$

which after integration turns into

$$I_{ds,lin} = WQ(V_{gs}, V_{ds})\frac{\upsilon_T}{2(k_B T/q)} V_{ds} \tag{A.9}$$

where υ_T is the unidirectional thermal velocity

$$\upsilon_T = \sqrt{\frac{2k_B T}{\pi m^*}}\frac{\mathcal{F}_{-1/2}(\eta_F)}{\mathcal{F}_0(\eta_F)}. \tag{A.10}$$

where $\mathcal{F}$ are Fermi–Dirac integrals. Corresponding calculations for high V_{ds} yield

$$I_{ds,sat} = WQ(V_{gs}, V_{ds})\upsilon_T \tag{A.11}$$

The above derivations were performed under the assumption of ballistic transport; however, Si MOSFETs usually operate at approximately 50% of the ballistic limit whereas III-V MOSFETs operate close to the ballistic limit. This is addressed by a simple fractional expression that relates the transmission coefficient to the mean free path and the length of the device. These resulting equations from the VS model are in fact similar to the traditional drift–diffusion equations with a few minor modifications such as the introduction of a so-called ballistic mobility.[117] To more clearly see the similarity between the equations

produced by the Landauer approach and the traditional equations, a few more steps are required. If we relate the mobility and mean free path λ to the diffusion coefficient by the Einstein relation, we may write

$$\mu_{eff} = \frac{\upsilon_T \lambda}{2k_B T/q} \tag{A.12}$$

If we insert Equation A.12 into Equation A.9, we obtain

$$I_{ds,lin} = \frac{W}{L} \mu_{app} Q(V_{gs}, V_{ds}) V_{ds} \tag{A.13}$$

and Matthiessen's rule gives the apparent mobility μ_{app} as

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_{eff}} + \frac{1}{\mu_B} \tag{A.14}$$

The apparent mobility μ_{app}, also known as the measured mobility of a short-channel MOSFET, will be limited by the effective mobility μ_{eff} or the ballistic mobility μ_B, depending on which is lower. The effective mobility μ_{eff} is the average mobility in the inversion layer and is generally lower than the bulk mobility μ_n because of effects such as scattering from surface roughness. In an extremely scaled device, the ballistic mobility begins to influence the apparent mobility. The ballistic mobility is given by

$$\mu_B = \frac{\upsilon_T L}{2k_B T/q} \frac{\mathcal{F}_{-1/2}(\eta_F)}{\mathcal{F}_0(\eta_F)}. \tag{A.15}$$

Assuming Maxwell–Boltzmann statistics, the ballistic mobility is linearly dependent on the channel length. Comparing Equation A.13 to the more traditional Equation A.2, we note a striking resemblance and can conclude that the Landauer approach yields the same type of equations describing the current through a barrier-controlled device.

Finally, in saturation, if we replace the transmission coefficient with an injection velocity v_{inj}, we may write the current as

$$I_{ds,sat} = WQ(V_{gs}, V_{ds})v_{inj} \tag{A.16}$$

where the injection velocity is a reciprocal addition of v_T and the average velocity at which electrons diffuse across the bottleneck region at the top of the barrier at high V_{ds}. Again, the slowest mechanism will limit the entire transport.

A.2 Tunneling probability

The tunneling through a barrier from the conduction band, at position a, to the valence band, at position b, can be approximated by a triangular potential and the tunneling probability for a uniform electric field can be calculated using the Wentzel-Kramers-Brillouin approximation

$$T_{WKB} \approx exp\left[-2\int_a^b |k(x)|\, dx\right] \tag{A.17}$$

Assuming a triangular potential barrier illustrated in Fig. A.1, the wave vector k(x) can be written as

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(V-E)} = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - q\mathcal{E}x\right)} \tag{A.18}$$

Inserting the *E-k* relationship of the wave vector in a triangular barrier into equation A.17 and solving the equation with the boundary condition $V - E = E_g$ (x = a) and $V - E = 0$ (x = b) yields

$$T_{WKB} \approx exp\left(\frac{-4\lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\phi + E_g)}\right) \tag{A.19}$$

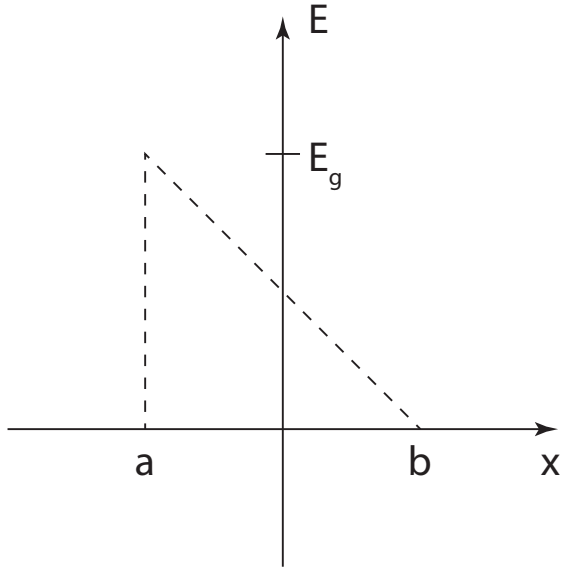


Figure A.1: *A triangular barrier approximation*

where $\Delta\phi$ is the energy window over which tunneling can occur and λ is the tunneling barrier width.

The triangular barrier is a simplified description of the tunneling barrier. Instead, a parabolic barrier is better suited to describe the wave vector inside the barrier i.e.[75,118]

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\frac{\left(\frac{E_g}{2}\right)^2 - E_0^2}{E_g}} = k(x) = \sqrt{\frac{2m^*}{\hbar^2}\frac{\left(\frac{E_g}{2}\right)^2 - (q\mathcal{E}x)^2}{E_g}} \quad \text{(A.20)}$$

which inserted into equation A.17 yields

$$\begin{aligned} T_{WKB} &\approx exp\left[-2\int_a^b \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{\frac{E_g^2}{4} - q^2\mathcal{E}^2x^2}{E_g}\right)}dx\right] \\ &= exp\left[-\frac{\sqrt{m^*}E_g^{3/2}}{2\sqrt{2}q\hbar\mathcal{E}}\int_{-1}^{1}(\sqrt{1-y^2})dy\right]_{y\equiv 2q\mathcal{E}x/E_g} \\ &= exp\left(-\frac{\sqrt{m^*}\pi E_g^{3/2}}{2\sqrt{2}q\hbar\mathcal{E}}\right) \end{aligned} \quad \text{(A.21)}$$

Comparing the resulting equation for the tunneling probability through a parabolic barrier to a triangular barrier, the equations are similar with the exception of an offset in the numerical constants in the exponential expression by approximately a factor of 0.6. Hence the general conclusions drawn from the simpler triangular barrier in chapter 5 are still valid.

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