A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology

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A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology

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***Abstract* — A 24 GHz System-on-Package (SOP) VCO is demonstrated. The core operates at 6 GHz and employs a high-Q on-carrier inductor. Using two cascaded on-chip frequency doublers the centre frequency is 24.6 GHz with a 20 % tuning range. The phase noise is below -107 dBc/Hz at 1 MHz offset over the tuning range, with a FOM between 188 and 192 dB at a power consumption of 6.9 mW.**

***Index Terms* — CMOS integrated circuits, Flip-chip devices, Microwave oscillators, Phase noise, Voltage controlled oscillators.**

I. Introduction

Microwave link transceivers put stringent performance requirements on the local oscillator signals. They must have both low phase noise and preferably also a high tuning range to cover multiple frequency bands. This is a major challenge to achieve at microwave frequencies, as the limited quality factor of large varactors and on-chip inductors degrade the performance of oscillators. The System-on-Package, SOP, concept can improve the performance by moving critical passive components from chip to a low loss glass carrier [1]. However, at microwave frequencies, reliable models for chip to carrier transitions are vital, otherwise package parasitics can seriously degrade the performance. An illustrative example of the SOP concept possibilities is shown in Fig. 1.

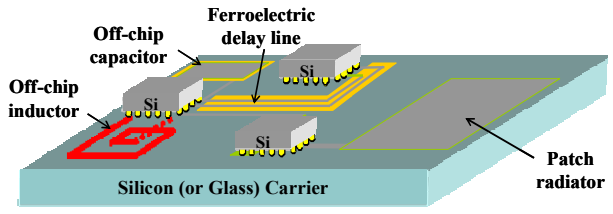

Fig. 1. Example of the System-on-Package (SOP) concept.

We demonstrate a 24 GHz VCO with a 20% tuning range in a 130 nm RF CMOS process using the SOP concept. The differential LC-oscillator core operates at 6 GHz, using a high-Q inductor on the glass carrier. The lower frequency reduces both the impact of package parasitics, and the losses of the large on-chip MOS varactors. The frequency of the signal is then multiplied by four using two cascaded frequency doublers. Using this technique a frequency tuning range of 20% is achieved, combined with a phase noise below -111 dBc/Hz at 1 MHz offset from a 24 GHz carrier, at a total power consumption of 6.9 mW.

II. Circuit Design

The schematic of the VCO including frequency doublers is shown in Fig. 2. A source node filtering technique is used to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state [2], i.e. when one transistor is off and the other one is in triode region. The source node inductor then approximates a high impedance current source as it resonates the parasitics at the source nodes at twice the operating frequency. A FET current source is used to set the DC current, and thereby also the oscillation amplitude. A capacitor in parallel with the current source shunts the high frequency noise from the current source to ground.

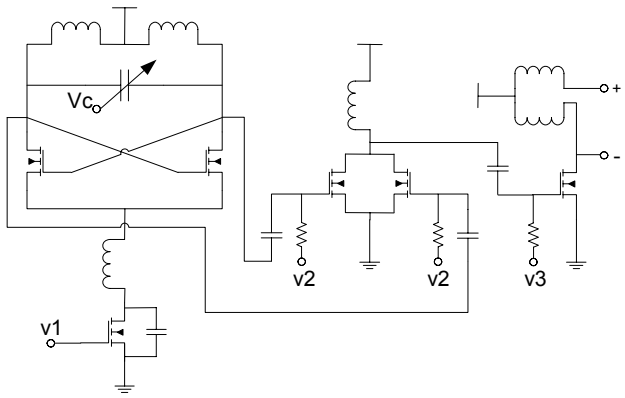

Fig. 2. Schematic of the VCO including frequency doublers.

The symmetric inductor of the LC-oscillator is realized on a glass carrier, fabricated in STMicroelectronics commercial integrated passive process optimized for high-

Q RF passive components. The carrier uses three metal layers and the process stack-up is shown in Fig. 3. The Q of the inductor at 6 GHz is above 80.

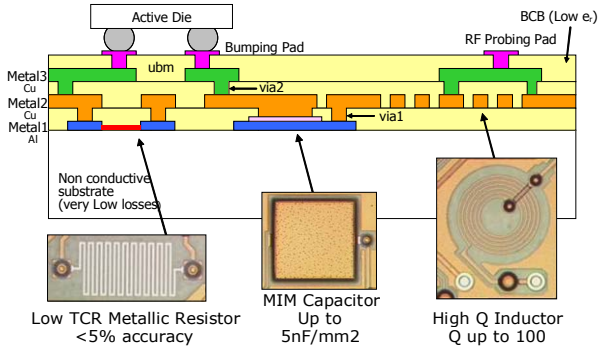

Fig. 3. Glass carrier process stack-up.

The varactor is continuously tuned, realized on-chip, and operates in the inversion and depletion regions. The varactor Q-value has been simulated in Fig. 4 at the VCO operating frequency, 6 GHz, and at the output frequency after the frequency doublers, 24 GHz. As can be seen the large varactor has a limited Q at the higher frequency. This would degrade the phase noise significantly if used in an oscillator at 24 GHz. Introducing the frequency doublers allows the oscillator to operate at 6 GHz, resulting in an acceptable varactor Q. The lower frequency also reduces the impact of the parasitics of the flip-chip interface between chip and carrier. To increase the second order non-linearity of the two frequency doublers their gate bias is set below the threshold voltage of the transistors. The outputs are tuned to 12 GHz and 24 GHz, respectively, using on-chip inductors. A symmetric inductor is used in the last frequency doubler to provide a differential output signal. Patterned ground shields are used beneath all on-chip inductors to block capacitively coupled substrate losses.

III. Layout

The die microphotograph is shown in Fig. 5. Stud bumps used for flip-chipping can be seen on top of the pads. The chip is fabricated in a 6 metal layer, 4 Cu and 2 AlCu, 130 nm RF CMOS process from Infineon Technologies and is 0.97 mm^2, with an active area of 0.11mm^2.

A photograph of the chip mounted on carrier, using a regular commercial surface mount pick-and-place process, is shown in Fig. 6. The symmetric single-turn inductor on carrier can be seen to the left of the chip. To the right the differential output signal is seen, where CPW lines connect the RF signals to the probing pads. The supply and bias signals were wire bonded from the carrier to a PCB and the lines are decoupled using capacitors on the chip, carrier and PCB.

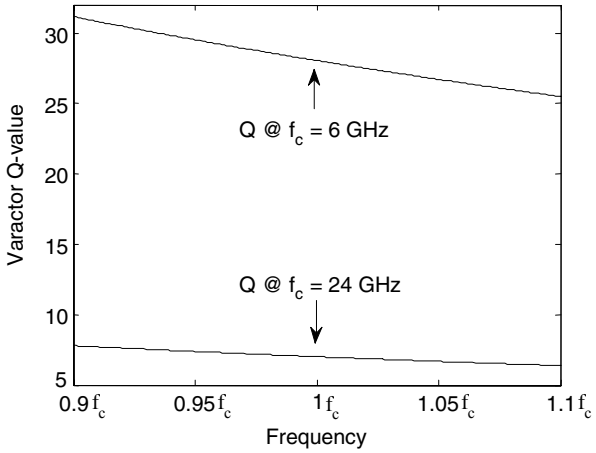

Fig. 4. Simulated varactor Q-values at 6 and 24 GHz over 20% tuning range.

Also included on the chip for measurement purposes, but not shown in the schematic of Fig. 2, are open-drain buffers designed to drive 50 ohm loads.

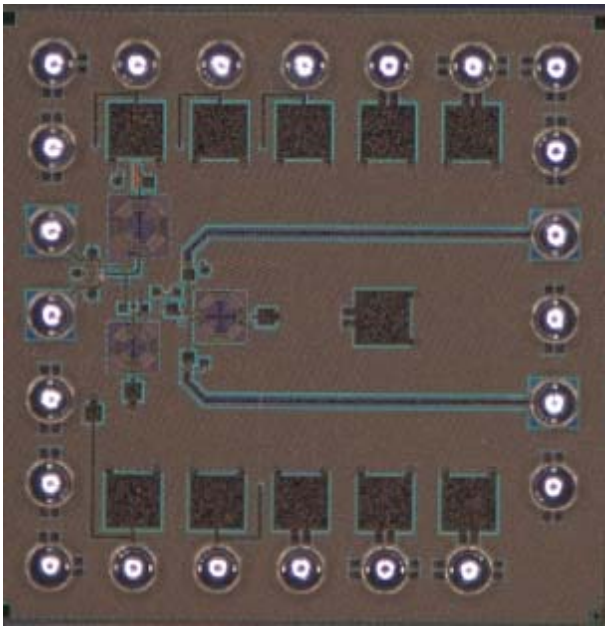

Fig. 5. Die microphotograph, 0.97 mm^2. The active area is 0.11 mm^2.

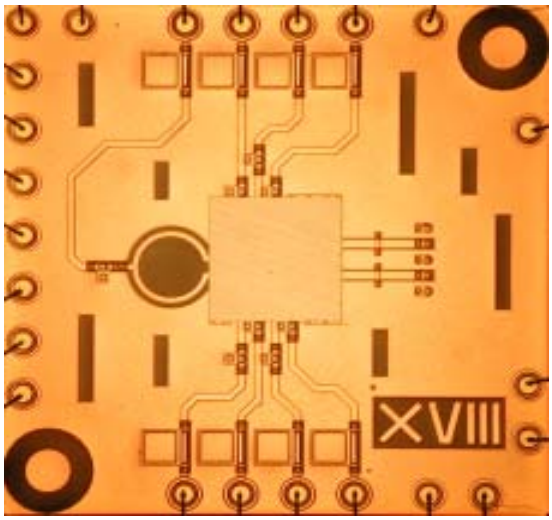

Fig. 6. Photograph of chip mounted on carrier, 5x5 mm^2.

IV. Measurement Results

There are two VCO versions, one using regular Vt and one using low Vt transistors. Two samples of each VCO version have been measured. The RF output signal was measured on the carrier using Infinity probes from Cascade Microtech. A supply of 1.3 V was used for the VCO core and 1 V for the frequency doublers. The regular Vt VCO consumed 7.3 mW, with a core current consumption of 4.1 mA and 2 mA used in the doublers. The low Vt VCO consumed slightly less, 6.9 mW, with 3.9 mA and 1.8 mA in the doublers. A Rhode & Schwarz FSU50 Spectrum Analyzer was used to measure the frequency tuning characteristic and the buffer output power. The output power was between -19.6 and -16.5 dBm for the regular Vt VCO, and slightly lower at -20.8 to -17.6 dBm for the low Vt VCO. The frequency tuning characteristic of the VCO is shown in Fig. 7. As can be seen the tuning range is 20%.

The phase noise was measured using a Europtest PN9000 phase noise measurement system with an external down conversion mixer, Marki M90765. A signal generator, Agilent E8257D, was used to generate the LO signal to the mixer. In Fig. 8 the phase noise is plotted versus varactor control voltage, Vc. As can be seen it is below -107 dBc/Hz at 1 MHz offset over the tuning range for both VCO versions. The phase noise is also plotted versus offset frequency, for chip 3, in Fig. 9. The phase noise figure of merit, FOM, is between 188 and 192 dB over the tuning range.

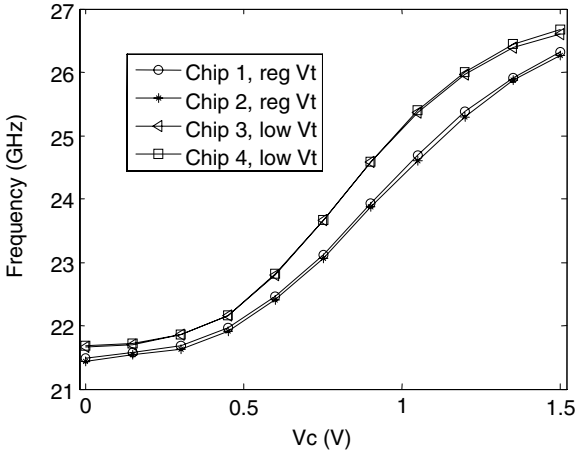

Fig. 7 Frequency tuning characteristic of the VCO.

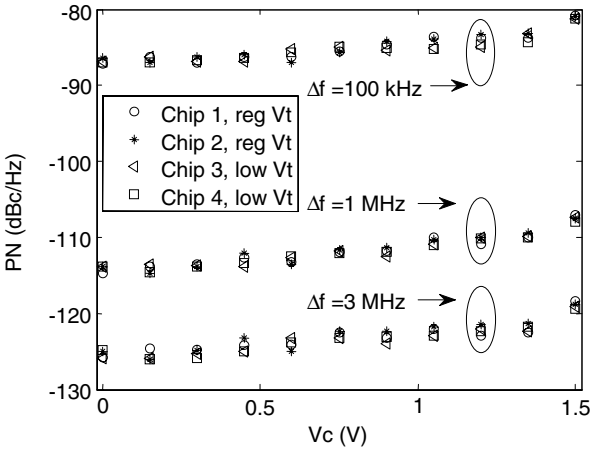

Fig. 8. Phase noise versus varactor control voltage.

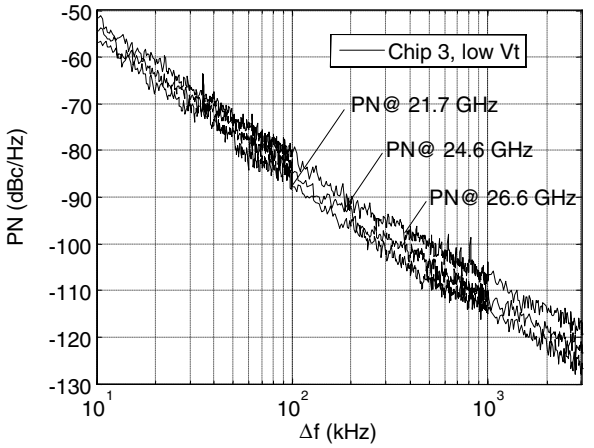

Fig. 9. Phase noise versus offset frequency, for three different frequencies, Chip 3.

TABLE I
SUMMARY OF SOME STATE-OF-THE-ART PUBLISHED VCOS

Ref.	Technology (μm)	F_C (GHz)	Tuning range (%)	P_{DC} (mW)	PN@1MHz* (dBc/Hz)	FOM (dB)	FOM_T (dB)
This work	CMOS 0.13 SOP	24.6	20	6.9	112	191	197
[4]	CMOS 0.13 SOP	28	17	5.3	109	191	195
[5]	CMOS 0.13	24.7	4.3**	24	111.6	186	178
[6]	CMOS 0.18	40	20**	27	100	178	184
[7]	CMOS 0.09 ***	18	8.3	4.2	120	199	197

* measured at centre frequency ** not continuously tuned ***post-processed

The oscillator frequency pushing was also measured, Fig. 10. There is approximately a 1.9 GHz and 1.8 GHz frequency increase for a supply voltage change from 1.5 to 1 V for the low Vt and reg Vt versions, respectively. This frequency shift is mainly due to the large varactors, and by referencing the control voltage to vdd instead of ground the pushing can be significantly reduced. In practise this can be accomplished by connecting the RC loop filter of the frequency synthesizer to vdd instead of ground.

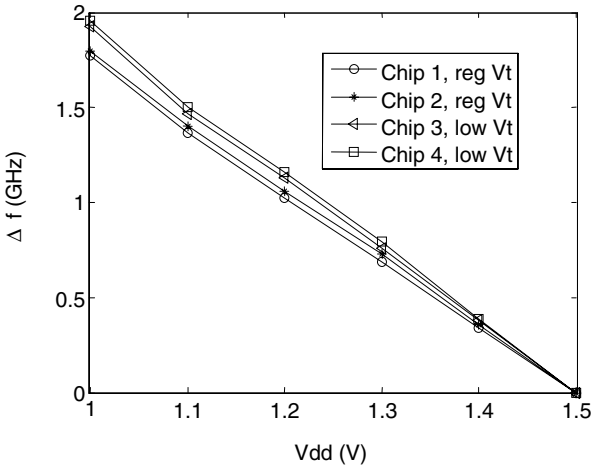

Fig. 10. Oscillator frequency pushing, Vc=0.75V.

The performance of some previously published state-of-the-art VCOs and this work is shown in Table I. The performance listed is measured at centre frequency. Also shown is the figure of merit taking tuning range into account, FOM_T, [3]. For this work it is between 194 and 198 dB over the tuning range. This is comparable to [4], which uses high-Q ferroelectric varactors.

V. CONCLUSION

The System-on-Package concept has been demonstrated for a microwave VCO. A high-Q symmetric inductor on a glass carrier is used in an LC-oscillator operating at 6 GHz. The VCO core and two frequency doublers, realized on a CMOS chip in 130 nm technology, was flip-chipped on the glass carrier. Thanks to the high Q value of the inductor on the carrier, excellent phase noise performance is achieved over a wide tuning range. It is below -107 dBc/Hz at 1 MHz offset over a 20% tuning range centered at 24.7 GHz, at a power consumption of 6.9 mW.

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