Model Based Engine Control Using ASICs: A Virtual Heat Release Sensor

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Abstract — *High resolution real time heat release analysis will become increasingly important in the future development of engine control systems. The increased demands on efficiency and emissions will put high demands on future engine control. Future engine concepts, for example the HCCI engine concept might crave cylinder pressure based Closed-Loop Combustion Control (CLCC). The analysis of cylinder pressure is a relatively computationally expensive task that is difficult to implement in existing engine controllers due to the real time demands. This paper describes an approach to obtain such a high speed heat release analysis. The described system could act as a platform for further feedback control experiments.*
Keywords: ASIC, closed-loop engine control, FPGA, heat release analysis, virtual sensor

INTRODUCTION

As commonly known the price of fuel in combination with the urge to create internal combustion engines that are less harmful to the environment pushes the development of new internal combustion engine concepts. In this development new combustion concepts like Homogeneous Charge Compression Ignition (HCCI), Partially Premixed (Diesel) Combustion (PPC), Spark Assisted Compression Ignition (SACI), Controlled Auto Ignition (CAI), etc. emerge. These new combustion concepts could all be thought of as variants of the traditional types of combustion (Otto or Diesel) with one thing in common separating the new concepts from conventional Otto and Diesel engines, a lowered maximum combustion temperature. The desire with these new combustion concepts is to lower the emissions both of the green house gas, carbon dioxide (CO_2) and the other harmful compounds like nitric oxides (NO_x), hydrocarbons (HC), carbon monoxide (CO) and particulate matter (PM). Using the conventional Otto and Diesel engine techniques it is difficult to reduce fuel consumption (and hence CO_2) and at the same time avoid emissions of the other harmful compounds. The conventional Otto

engine fitted with a three way catalyst emits very low concentrations of NO_x, CO, HC and PM, it does on the other hand suffer from a poor break efficiency resulting in higher fuel consumption and hence more CO_2 emissions than a corresponding Diesel engine. The Diesel engine on the other hand emits much NO_x and PM but it has a higher efficiency. The new engine concepts are trying to maintain the high efficiency of the Diesel engine and combine this with the low emissions of the other harmful compounds.

The new compression ignited combustion concepts of course also share some drawbacks. Low combustion temperature causes the combustion efficiency to decrease which in turn causes higher emissions of HC compared to the Otto and Diesel engines. Higher HC emissions is however possible to deal with using a cheap and well-known oxidising catalyst. Another, more serious drawback with the low temperature combustion concepts is the lack of a direct means for combustion phasing control. Most of the low temperature combustion concepts do not have any of these direct actuators, combustion is instead initiated when the charge temperature is high enough for the current fuel-

air mixture to autoignite. The strong connection between temperature, fuel properties and start of combustion makes it more difficult to control combustion phasing using the low temperature combustion concepts compared to the Otto and Diesel ones.

Application Specific Integrated Circuit (ASIC) technology is, as internal combustion engines, an area where development is explosive. ASIC technology is getting more and more available since the introduction of the Field Programmable Gate Array (FPGA). An FPGA can be described as a reconfigurable ASIC, and it makes it possible to utilize the high performance of the ASIC without having to pay the cost/time penalty of traditional ASIC design. Using an FPGA it is hence possible to realize small series of fully customized hardware systems allowing very high performance due to the fact that the implementation resides in hardware rather than in software/processor. FPGA:s have already been utilized in a large number of very high performance applications such as batch computing, scientific simulations, real time image treatment/analysis and real time signal processing. Even though FPGA:s can be customized to perform much better than a more general purpose processor on a specific task, it is however not as versatile as a processor. The FPGA internal layout has to be redesigned to fit it's specific task, this redesign is a more complex task than to reprogram a general purpose processor. Since an FPGA features high performance and a processor high flexibility the next given question is if it would be possible to combine these two systems. The answer is yes, it is possible to obtain a system with both high flexibility and high performance combining hardware parts (residing in an FPGA) with software parts (run on a processor) to a complete high performance flexible hardware/software system. A nice survey of the different FPGA related design methodologies is provided by Todman et al. in [3]. A more specialized survey on signal treating applications is provided by Tessie and Burleson in [4].

1   RELATED WORK

Even though FPGA technology for some time has been utilized in for example signal processing applications the development of closed-loop control systems residing in FPGA systems seems just to be starting. Not much is published in the area. Two very interesting publications deserve attention. Wei et al. in [5] implemented and evaluated different PID controller architectures residing in an FPGA environment. They also give further references of this topic. The evaluation of different structures of known closed-loop controllers is an important topic in order to find forms of the closed-loop controllers suitable for hardware implementation on an FPGA.

2   EXPERIMENTAL SETUP

The experimental setup necessary for these experiments consists both of software and hardware. The hardware parts are made up of an FPGA prototype board, a board simulating the engine pulses and cylinder pressure, an expansion module for the FPGA board featuring AD/DA converters and some surrounding circuitry adjusting signal levels etc. The FPGA system is connected to a Personal Computer through a JTAG cable, enabling display of debugging data, FPGA/PC co-simulation and reconfiguration of the FPGA. The design of the FPGA configuration and the hardware co-simulation are carried out in MATLAB/Simulink with the aid of a Simulink toolbox supplied by Xilinx, "Xilinx System Generator DSP". In order to generate an FPGA design from the Simulink diagrams the Xilinx development suite "Xilinx ISE" is necessary. Please note that it is not possible to implement "standard" Simulink blocks in the FPGA, it is necessary to possess a VHDL implementation of the blocks to implement (a number of such blocks comes with System Generator). This is somewhat limiting. The main part of the setup is the experimental card fitted with the FPGA. The card is a Commercial Off the Shelf (COTS) product supplied by "MEMEC/Avnet", the (rather long) name of the card is "Memec Xilinx Virtex-4 LX XC4VLX25-SF363 LC Kit". As understood the card holds a "Xilinx Virtex-4 LX XC4VLX25-SF363 LC" FPGA, which holds 24,192 logic cells, 168 Kb distributed RAM memory and 448 user IO ports. The total FPGA system price was at the time of purchase $\approx$ euro 700 and must hence be considered as a low cost system, it is never the less a high performance system!

3   TEST ENVIRONMENT

Desktop tests were carried out during the development. The "interface" to the simulated /real engine consists of three signals, Crank Angle Degree Pulses (CADP), Top Dead Center Pulses (TDCP) and analogue cylinder pressure P_{cyl}. Current engine position is assumed to be measured with 0.2 Crank Angle Degree (CAD) accuracy, the engine hence produces 5 CADP every physical CAD. Besides CADP the angle sensor is assumed to give one TDCP every time the engine has revolved two complete revolutions. This engine "interface" concurs with the setups in [1] and [2].

4   ALGORITHM

A net HR (Q_{HR}^{net}) calculation was implemented in the FPGA, that is the HR calculation disregards heat transfer losses and crevice losses. Heat transfer losses are caused by convective energy loss to the combustion chamber walls. Crevice losses are caused by trapping fuel-air mixture in the crevices between the piston and the cylinder wall, thus

avoiding combustion. The calculation of Q_{HR}^{net} is carried out in a non-conventional manner. It is possible to calculate Q_{HR}^{net} through (1) which origins from the conservation of energy. This is a promising optional method to calculate the HR which Tunestål showed in [6].

$$Q = \underbrace{\frac{1}{\gamma - 1}p(\theta)V(\theta) + \int_{\theta_{start}}^{\theta} p(\theta)\frac{dV}{d\theta}d\theta}_{\text{Calculated on-line}} -$$
$$- \underbrace{\frac{1}{\gamma - 1}(p(\theta_{start})V(\theta_{start}))}_{\text{Estimated constant, added off-line}} \qquad (1)$$

5 RESULTS

The major result of this investigation was of course the successful implementation of the described HR algorithm in the FPGA environment as described. The performance of the implementation is a point that can not be stressed enough, a P_{cyl} sample that arrives to the FPGA from the AD converter is, considering the timescale of an engine, calculated immediately. Immediately in this case means 12 FPGA clock cycles, clk_{fpga} = 100 $MHz \rightarrow$ 120 ns! This does in other words mean that when the AD converter has delivered a sample on the FPGA pins it takes 120 ns before the FPGA has delivered the corresponding Q_{HR}^{net} sample on the pins of the DA converter! In 120 ns an engine revolving at 1200 rpm moves 0.000864 CAD, if the engine were revolving at 24000 rpm it would move 0.01728 CAD! The latency between an arriving P_{cyl} sample and the output of the corresponding Q_{HR}^{net} sample is in other words negligible. Since it is possible to measure the Q_{HR}^{net} with as high frequency as P_{cyl} and concurrently with P_{cyl}, it is motivated to call the system a "virtual Q sensor" meaning that Q_{HR}^{net} is calculated the moment P_{cyl} is measurable. Besides very low latency the system does feature a very high throughput. If the engine would be able to produce pressure in a rate high enough it would be possible to perform 12 "complete" (meaning 120*5 point) heat release analyses each CAD at 1200 rpm! The limit of the throughput is the AD conversion speed.

CONCLUSION

− The paper has shown the possibility to implement an internal combustion analysis related algorithm in an ASIC/FPGA environment.
− The developed system can be thought of as a "virtual Q sensor".
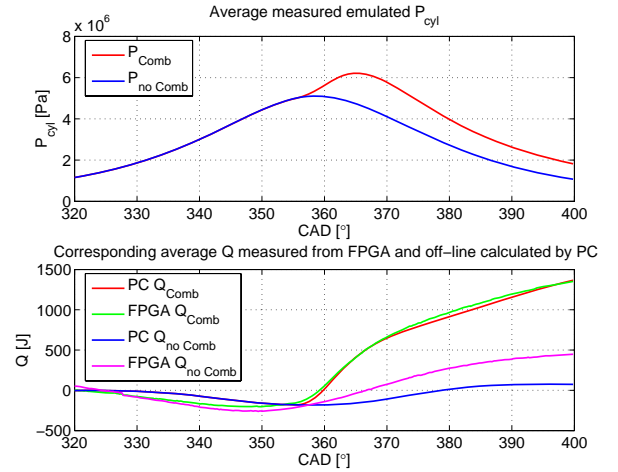− Extraordinary performance can be achieved using the described system:

Figure 1

average output from the FPGA system compared to the corresponding values corrected in the PC.

− A sample of cylinder pressure P_{cyl} is processed and corresponding Q_{HR}^{net} is calculated before any engine can move 0.02 CAD.
− A throughput of 50 MHz enables the FPGA system to perform 12 120*5 sample HR analyses within a single CAD @ 1200 rpm.

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