Second Harmonic 60-GHz Power Amplifiers in 130-nm CMOS

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Second Harmonic 60-GHz Power Amplifiers in 130-nm CMOS

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***Abstract*— Two different frequency doubling power amplifier topologies have been compared, one with differential input and one with single-ended, both with single-ended output at 60 GHz. The frequency doubling capability is valuable from at least two perspectives, 1) the high frequency signal is on the chip as little as possible 2) the voltage controlled oscillator and power amplifier are at different frequencies easing the isolation of the two in a transceiver. The topologies have been simulated in a 1p8M 130-nm CMOS process.**

The resonant nodes are tuned with on-chip transmission lines. These have been simulated in ADS and compared to a standard Cadence component, *tline3*. The Cadence component gives a somewhat pessimistic estimation of the losses in the transmission line.

The single ended input amplifier outputs a maximum of 3.7 dBm and draws 27 mA from a 1.2 V supply, while the one with differential input outputs 5.0 dBm and draws 28 mA. The 3-dB bandwidth of the amplifiers are 5.9 GHz and 6.8 GHz, respectively.

I. Introduction

The drive for gigabit transmission rates in future WLAN/WPAN systems forces design of new systems to use wider bandwidth. The Federal Communication Commission (FCC) has opened a 7 GHz wide spectrum from 3-10 GHz for UWB communication with low power levels so it can coexist with existing applications. A 7 GHz wide unlicensed band at 60 GHz [1] is also available. Both these spectrum allocations will permit communication at several gigabits per second. Also in Japan and Europe [2] frequency bands at 60 GHz are opened for unlicensed WLAN communications.

To meat the stringent cost requirements of the consumer electronics market, the 60 GHz transceiver must be realized in low cost CMOS technology. Especially the power amplifier is difficult to design. In this work we try to increase the performance of the power amplifier using frequency doubling.

With a harmonic power amplifier the high frequency signal is produced as close to the antenna as possible, which makes signal processing easier on chip and reduces the losses due to capacitive coupling to the substrate. An harmonic amplifier also make the frequency planning easier, since the voltage controlled oscillator and power amplifier are separated in frequency.

II. Circuit Topologies

Two different power amplifier topologies have been simulated (Fig. 1). Both amplifiers perform a frequency doubling, converting a 30 GHz input to a 60 GHz output. The frequency doubling takes place in the first stage, and the drain node of M1 (and M3) is tuned to 60 GHz, filtering out the second harmonic. The second stage is a 60 GHz common source amplifier with an L-match transforming the 50 Ω output impedance to 390 Ω. The L-match consists of the drain-bulk capacitance of M2 and the Transmission Line (TL) to the pad.

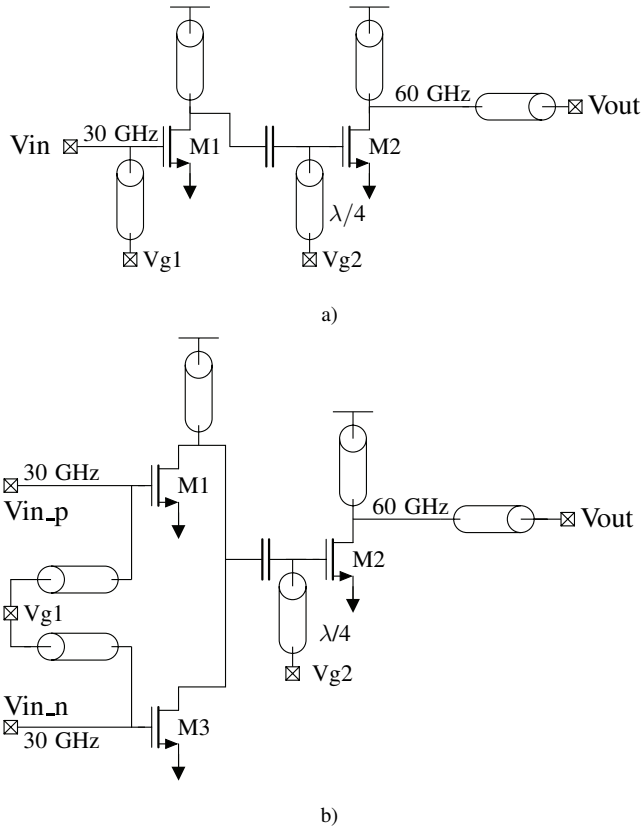

Fig. 1. The two power amplifier topologies investigated. a) single-ended input b) differential input

The first stage in the differential amplifier [3] (Fig. 1(b)) conducts both then the signal is high and low, contribut-

ing to a larger effective g_m of that stage compared to the Single-ended Input (SI). The drain-bulk capacitance, however, is correspondingly larger, making the first stage gain approximately equal for the to topologies.

When the signal is high the upper branch is conducting and then the signal is low the lower branch is, due to the Differential Input (DI) signal. The fundamental tone at the drains of M1 and M3 is 180° out of phase, but the second harmonic is in phase. Combining the drains together results in a signal with twice the frequency of the input. All odd order harmonics are suppressed by this connection [3] making LO leakage through the power amplifier less of a problem, see Table I. In the second stage a single-ended signal is amplified.

Furthermore, the differential input amplifier is suitable for on-chip implementation since differential signal schemes are dominating there thanks to there high common mode noise/interference suppression. In addition to that, the power amplifier produces a single-ended output, making an otherwise necessary lossy balun at the output now unnecessary.

The SI amplifier is easier to measure, however, since no balun in front of the power amplifier is needed.

Both amplifiers are taped-out for comparison reason.

A. Transmission Lines

All the resonant nodes are tuned by grounded Transmission Lines (TL). A model of the silicon substrate has been used to simulate the TL in Advanced Design System (ADS) [4]. The width of the TL has been chosen to give a 50 Ω characteristic impedance, which also gives a high Q-value, see [5], [6] for a more thorough investigation of TL in silicon processes.

The ADS simulation results have been compared to the component *tline3* from the library *rfExamples* in Cadence (Fig. 2). Lines are ADS simulations and markers are corresponding *tline3* values. The inductance, series resistance, and Q-value have been plotted as a function of TL length at 60 GHz. The Cadence component agrees well with ADS for the inductance but overestimates the losses by roughly 20%. Despite this *tline3* has been used to simulate the amplifiers, so the simulation results are in this respect somewhat pessimistic. Assuming 20% larger parallell resistance in all the three resonant nodes would give 4.8 dB larger voltage gain. The Q-values and inductances are in the same range as in [5], [6].

B. Layout Considerations

To achieve an AC-ground at the end of the TL, Metal-Insulator-Metal (MIM) capacitances (grey squares in Fig. 3) have been used. An array of small MIM capacitors with a total of 1 pF is used to ground the TL with low series resistance. Further out from the end larger capacitances is shunting the signal, if any, to ground. In total more than 11 pF is shunting every DC node to ground, corresponding to an impedance of 0.24 Ω @ 60 GHz. To verify that the decoupling is sufficient, simulations including parasitics and bond wires have been performed. A π-model con-

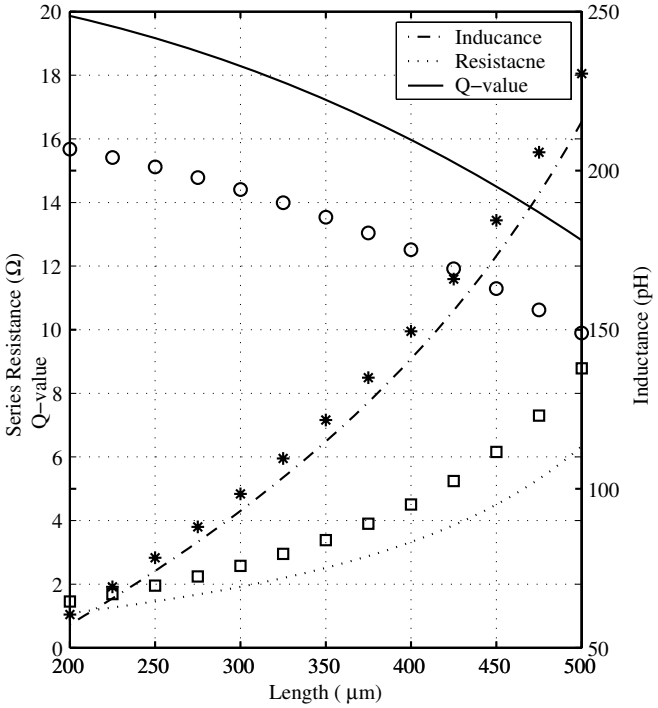

Fig. 2. Comparison of transmission line simulation in ADS (lines) and Cadence (markers) at 60 GHz

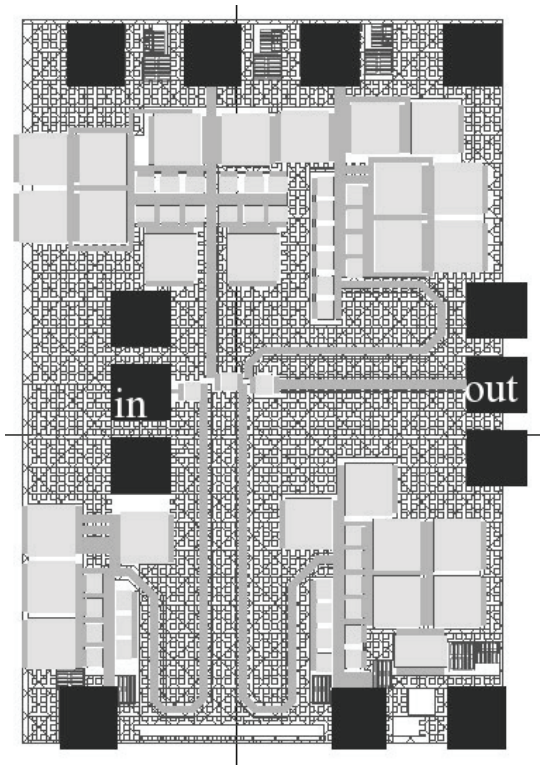

Fig. 3. Layout of the single-ended input power amplifier

sisting of 3 nH series inductance with Q=10 and a 50 fF shunting capacitance has been used for the bond wires. The circuit is stable under these conditions indicating that the decoupling is sufficient[1].

In Fig. 3 a view of the single-ended input layout is shown. The chequered ground plane is present under the whole chip, providing a low-ohmic and well distributed ground. Under the TL a return path for the ground current is provided as a 20 μm wide wire in the ground plane, thus minimizing current loops.

To be able to measure the differential input amplifier a differential probe has to be used. The spacing between the RF pads is then at least 200 μm for a SGS probe. To route the signal from the pads to the first stage approximately 70 μm long wires are used. This routing has to be included in the simulations as well.

III. Simulation Results

The amplifiers are simulated in a Cadence environment with SpectreRF. All simulations are performed with as much of the circuits as possible in extracted view, e. i. post-layout. As source and load 50 Ω ports are used to emulate a measurement environment.

In Fig. 4 the output power versus frequency is plotted, with 0 dBm input power. As can be seen the difference between the two topologies is very small. The maximum output power is 3.7 dBm and 5.0 dBm for the SI and DI (Fig. 5), respectively. These power amplifiers can be driven by 30 GHz amplifiers to achieve the feeding signal. High power gain is easier to attain at lower frequencies, [7], [8] show two designs at about 30 GHz having gains of 7-8 dB. Other published 60 GHz power amplifiers in CMOS show about 2-4 dB gain per stage [9]–[11], which our amplifiers also have in the last stage. The 3-dB bandwidth is 5.9 GHz and 6.8 GHz, for the SI and DI. A 7-GHz bandwidth is enough to cover the the 57-64 GHz frequency band opened up by FCC.

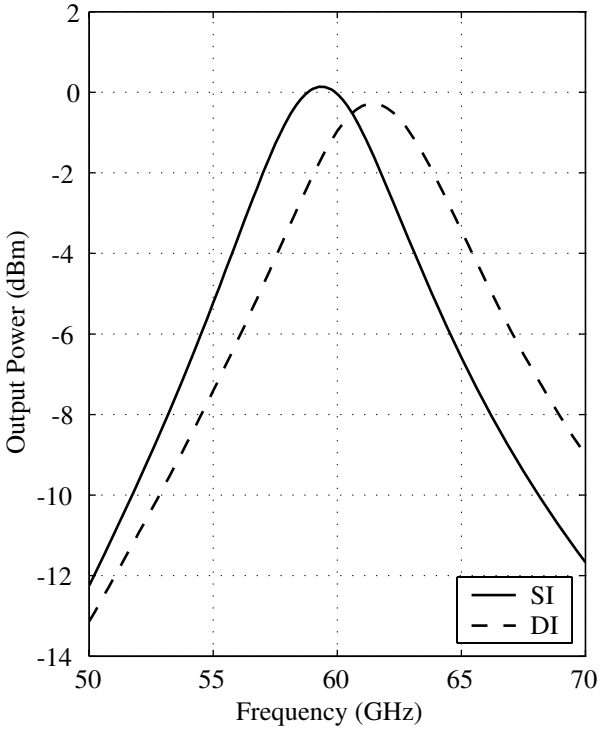

Fig. 4. Comparison of the two power amplifier topologies with 0 dBm input power

A power sweep was also simulated (Fig. 5) achieving an output 1 dB compression point of -10 dBm and -11 dBm, respectively. Note that the slope of the asymptotes is equal to 2, since the amplifiers uses the 2:nd harmonic.

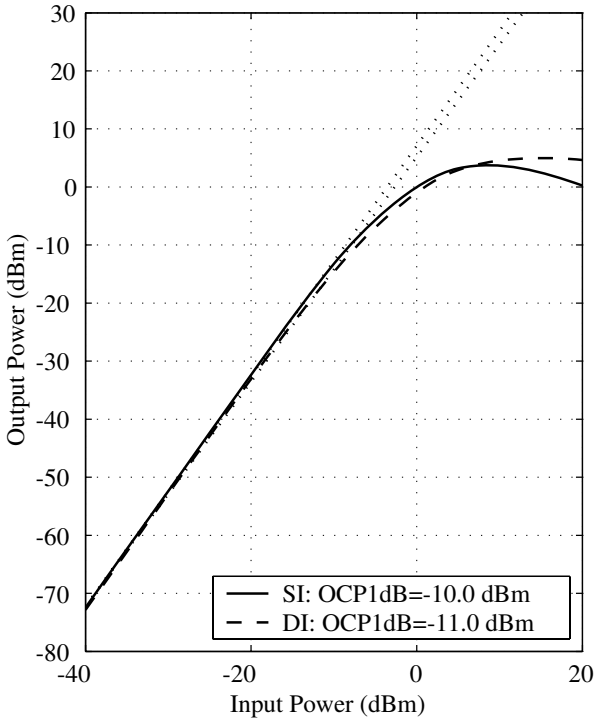

Fig. 5. Power sweep of the two topologies at 60 GHz output frequency, notice the slope of 2 on the asymptotes

A. Summary

Table I is a summary of the simulated results for the two topologies. The performance of the two topologies are rather equal with a somewhat higher output power and wider bandwidth for the differential one. The area is roughly 40% larger because two TL are needed to tune the gates of the input stage. The suppression of the fundamental tone is significantly improved by the DI topology as expected.

IV. Conclusion

Two 60 GHz topologies have been simulated, one with single-ended input the other with differential input. The power amplifiers have internal frequency doubling, converting a 30 GHz input signal.

[1]Which have been investigated by observing the response of a input step, while the load was open and 50 Ω.

TABLE I

COMPARISON BETWEEN SINGLE INPUT AND DIFFERENTIAL INPUT TOPOLOGIES

	SI	DI
V_{DD} (V)	1.2	1.2
I_{DC} (mA)	27.0	27.7
Max. Output Power (dBm)	3.7	5.0
Drain efficiency (%)	7.3	9.5
OCP1dB (dBm)	-10.0	-11.0
Power Gain (dB)[2]	0.9	0.4
Bandwidth (GHz)	5.9	6.8
Fundamental Tone Suppression (dB)	14.1	82.8
Total Area (mm^2)	0.90	1.26

[2] With 0 dBm input power.

The single-ended input amplifier relies on the nonlinearity of the transistor to do the conversion from 30 GHz to 60 GHz. The differential input amplifier makes use of the fact that the second harmonics are in phase in the differential signal, thus connecting the drains together (Fig. 1(b)) effectively produces a frequency doubling. A cancellation of the fundamental and the odd harmonics is also achieved by this connection.

A maximum output power of 5.0 dBm is achieved from the differential input amplifier taking 28 mA from a 1.2 V supply. The 3-dB bandwidth is 6.8 GHz covering the FCC frequency band from 57-64 GHz. The 1 dB output referred compression point for this amplifier is -11 dBm.

V. ACKNOWLEDGMENT

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