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Embedded Tutorial IV

Fault management in an IEEE P1687 (IJTAG) environment

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To meet the constant demand for performance, it is increasingly common with multi-processor system-on-chips (MPSoCs). As these integrated circuits (ICs) may contain billions of transistors squeezed on a few square centimeters, it is difficult to ensure that they are correct. Defects may escape manufacturing test or develop during operation and, further, ICs manufactured in later semiconductor technologies are increasingly sensitive to environmental disturbances. These defects may be permanent (hard) or transient (soft).

To enable graceful degradation, fault management can be applied to handle eventual defects. Fault management include collection of error statuses from each of the processors, classify the defects, fault mark defective processors, schedule jobs on non-defective processors.

This tutorial consists of three parts. First, we will discuss the need of IEEE P1687 (IJTAG), a standardized mechanism to access embedded features. Second, we will discuss how to make use of IEEE P1697 for fault management. And, third, we will make a demonstration of a fault management solution that makes use of IEEE P1687.