Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si

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***Abstract*—**We use a self-aligned, gate-last process providing n-type (InAs) and p-type (GaSb) MOSFET co-integration with a common gate-stack and demonstrate balanced drive current capability at about 100 µA/µm. By utilizing HSQ-spacers, control of gate-alignment allows to fabricate both n- and p-type devices based on the same type of vertical heterostructure InAs/GaSb nanowire with short gate-lengths down to 60 nm. Refined digital etch techniques, compatible with both sensitive antimonide structures and InAs, enable channel region diameters down to 16 nm for GaSb and 10 nm for InAs. Balanced performance is showcased for both n- and p-type MOSFETs with I_{on} = 156 µA/µm, at I_{off} = 100 nA/µm, and 98 µA/µm, at $|V_{DS}|$ = 0.5, respectively.

I. Introduction

High mobility materials such as narrow band gap III-V compounds offer a possibility to increase the MOSFET performance for both logic and high-frequency devices. Specifically InAs and GaSb material options present high bulk mobility for electrons and holes, respectively, which makes the combination attractive for CMOS implementation. GaSb based transistor performance is currently limited by the gate-stacks and the reactive nature of the antimony-compounds imposes challenges in both material growth as well as device fabrication. [1]

The continuation of the traditional down-scaling of MOSFETs for digital circuits has led to short channel effects due to deteriorated electrostatics [2]. 3D gate architectures are therefore proposed, and implemented, with gate-all-around (GAA) structures utilizing vertical nanowires as a strong candidate. Fundamentally, vertical nanowire MOSFETs presents a seamless way to decouple gate-length and contact geometry from the device footprint area. The small footprint also allows larger lattice mismatch without propagating defects, which simplifies integration of high mobility materials on top of Si substrates. [3]

In this work, we demonstrate a streamlined co-integration process for p- and n-type MOSFETs, with a common gate-stack, using a self-aligned, gate-last process. State-of-the-art vertical p-type GaSb MOSFET performance is demonstrated, with g_m = 230 µS/µm, co-integrated with a strong InAs n-type device showcasing good off-state with I_{on}=156 µA/µm at I_{off} = 100 nA/µm, all at $|V_{DS}|$ = 0.5 V (**Table 1**). The data includes 5x drive current improvement for the GaSb MOSFET combined with a 3x increase in g_m as well as a decreased SS_{min} as compared to previous results [4]. The improvement is attributed to adjustment in the aspect ratio (Diameter:L_g) for the n-type and p-type devices, from 2:5 and 2:4 to 2:30 and 2:6, respectively, in order to achieve balanced drive currents. For the n-type device this has resulted in improved off-state characteristics reaching the I_{off} = 100 nA/µm limit and simultaneously the p-type current has been improved with a 5 times higher I_{on} of 98 µA/µm (**Table 2**).

II. Device Fabrication

The processed MOSFETs are based on vapor-liquid-solid (VLS) grown InAs-GaSb heterostructure nanowires overgrown with, a highly n-doped InAs shell. The implementation of an overgrown shell protects the GaSb, which circumvents issues regarding etch selectivity and enables processing with hydrogen silsesquioxane (HSQ) allowing development of a self-aligned, gate-last process. Optimization of alcohol based digital etching, in conjunction with the gate last implementation, has enabled scaled diameters and selective digital etch of the channel region. Therefore, GaSb devices with diameters down to 16 nm have been achieved, which has proven crucial for improved performance.

Fig. 1 represents the critical fabrication steps for the co-integration process. The devices are based on 260 nm epitaxial InAs layer grown on p-type silicon (111) substrates. Subsequently, InAs-GaSb nanowires are grown by VLS from EBL defined 32 nm diameter Au discs. The top of the InAs segment and GaSb segment is doped by Sn and Zn, respectively. The nanowires are also overgrown with an InAs shell for improved etch selectivity (**Fig 1-a**).

After nanowire growth, an HSQ mask is applied whose thickness is controlled by the EBL exposure dose. The thickness control allows for varied gate-position along the nanowire, enabling p- and n-type devices to be fabricated from the same type of nanowires. The spacer is used as a template to align the top metal, which is applied by 200 nm sputtered W and 3 nm ALD TiN (**Fig. 1-b**). Prior to metal deposition, a citric acid dip is performed followed by HCL:IPA to remove the protruding InAs shell and restore the core-material. The applied metal is selectively removed from the planar surfaces by reactive ion etching leaving the finished top contact.

The HSQ mask, previously used for top contact alignment, is thinned by diluted HF 1:400 to form the bottom spacer and to expose the nanowire channel-region. The channel region is selectively digitally etched by 4 cycles of short ozone exposure followed by HCL:IPA 1:30 wet etch. The digital etch removes the InAs shell and further serves to trim the channel down to sub 25 nm diameters. A bilayer high-k is applied consisting of

6 cycles of Al_2O_3 and 36 cycles of HfO_2, corresponding to an EOT of 0.85 nm (**Fig. 1-c**). The result after high-k deposition is shown in **Fig 2**, presenting before and after SEM images of a single nanowire p-type device.

Finally, 60 nm sputtered tungsten is used as gate metal and the top edge aligned vertically by a back etched S1813 resist as etch mask for an SF_6 dry etch. Afterwards an organic top spacer is defined followed by sputtering of the top contact consisting of Ni/Au (15/200 nm), see **Fig. 1-d**.

III. Measurements

Fig. 3 and **Fig. 4** represent combined output and transfer characteristics for InAs (L_G = 150 nm, diameter = 10 nm) and GaSb (L_G = 60 nm, diameter 22 nm) channel devices, co-integrated on the same Si substrate. The data are showcasing well behaved characteristics with maximum g_m = 405 and 230 µS/µm, respectively, normalized to the total circumference, see **Table 1**. A high I_{on} = 156 µA/µm (at I_{off} = 100 nA/µm) is also achieved for the n-type device, representing a 14% improvement compared to previous vertical InAs MOSFETs [5]. Both the n- and p-type devices showcase good electrostatics with SS_{lin} = 72 and 175 mV/dec, attributed to the aggressive diameter scaling (**Fig. 5** and **Fig. 6**) and high-quality semiconductor/high-*k* interfaces. Also, the minimum subthreshold slope is maintained over a wide bias range for the n-type device (**Fig. 6**), demonstrated that the co-integration process does not introduce a drastic increase in D_{it} for InAs. Notice that the InAs transistor is fabricated from a 200 nm long InAs segment, which introduces significant constraint on contact formation contributing to a comparably high R_{on} = 1.4 kΩ·µm for the n-type MOSFET. For the p-type device, contributions to the contact resistance from rapid re-oxidation of GaSb and injection via a, not optimized, broken bandgap source serves to further limit the on-state performance. The limited off-state can be attributed to background doping in the GaSb channel (**Fig. 7**). [6]

To demonstrate the improved digital etch technique and technology scalability, a p-type device with diameter down to 16 nm, although with longer gate-length of 150 nm is shown in **Fig. 8**. Alcohol based digital etch techniques enable the aggressive diameter scaling. Notice the large difference between top contact diameter with respect to the channel region, which improves resistance originating from the drain contact. The device transfer characteristics is presented in **Fig. 9**, showing that a high transconductance of 87 µS/µm can be maintained also when the diameter is scaled. Notably, the performance of GaSb p-MOSFETs strongly depends on the gate length. Also the off-state performance is improved, quantified by SS_{sat} = 257 mV/dec (**Fig. 10**). The output characteristics for this device (**Fig. 11**) showcase an exponential behavior that indicates the presence of a potential barrier (**Fig. 12**) which can be resolved by further contact optimization.

To visualize the performance improvements as compared to previous GaSb, as well as InGaSb, devices a g_m versus SS_{sat} plot is presented in **Fig 12**. Here, importance of scaling the gate-length and diameter is clearly emphasized. With a balance between *SS* and g_m metrics also at scaled gate lengths, this work shows improved performance over state-of the-art GaSb MOSFETs, including InGaSb fin-FETs. [1]

IV. CMOS Implementations

Many alternative co-integration strategies have been proposed and implemented utilizing the same material combination, namely InAs and GaSb, see **Table 2**. One approach is to use nano-ribbons with a two-step transfer technique. [7] The same technique, utilizing nano-ribbons, with a single transfer step has also been developed and demonstrated. [8] Another method is to use grown periodic InAs-GaSb planar structure with selectively etched segments enabling fabrication of separate lateral GAA InAs and GaSb devices. [9] The CMOS implementation presented in this work, based on vertical InAs-GaSb heterostructure nanowires, on top of Si, [10] has the potential to include heterostructure InAs-InGaAs segments [11] to reduce the off-state leakage and to further increase the transconductance. [4] In fact, we show a technology that can merge high transconductance n-type MOSFETs [11] with balanced CMOS implementation for high-speed logic and mixed applications.

From the benchmarking of various all-III-V CMOS implementations in **Table 2,** we note that the implementation presented in this work, represents the best set of combined metrics including g_m vs SS_{sat}. We show that competitive device performance can be achieved within a co-integrated process, challenging other state-of-the-art III-V devices.

V. Conclusions

We present an all-III-V co-integration process aggressively scaled to gate-lengths (L_G = 60 nm) and diameters (D_{InAs} = 10 nm, D_{GaSb} = 16 nm). This has served to reach balanced drive-currents for the III-V CMOS at 156 and 98 µA/µm for the n- and p-type devices respectively (**Table 1**) as well as demonstration of competitive transistor performance.

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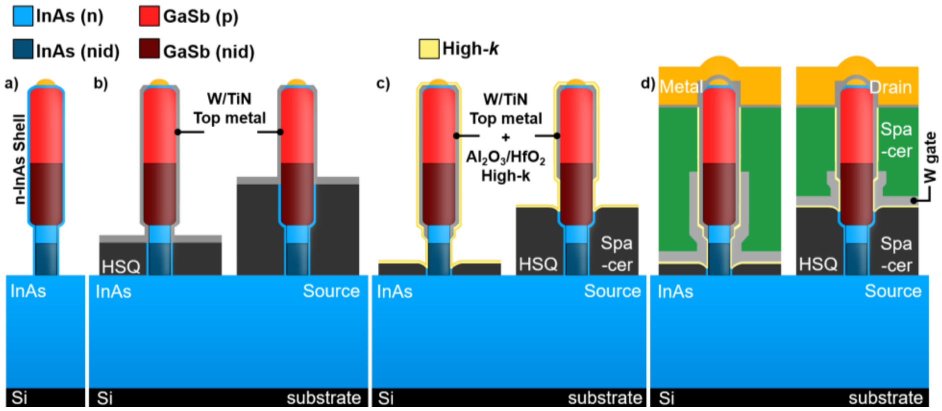

Fig. 1. Schematics of process flow, showing a) nanowire after VLS growth, b) top metal alignment, c) first spacer and high-k deposition, and d) final structure with contacts.

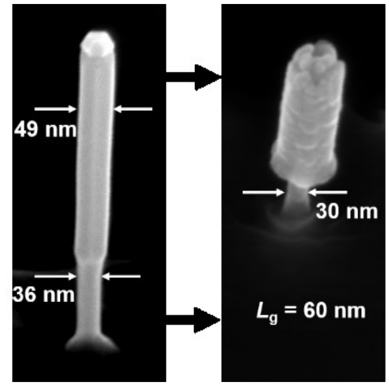

Fig. 2. SEM-image of a nanowire prior to processing and after first spacer and high-k deposition, see Fig. 1-c.

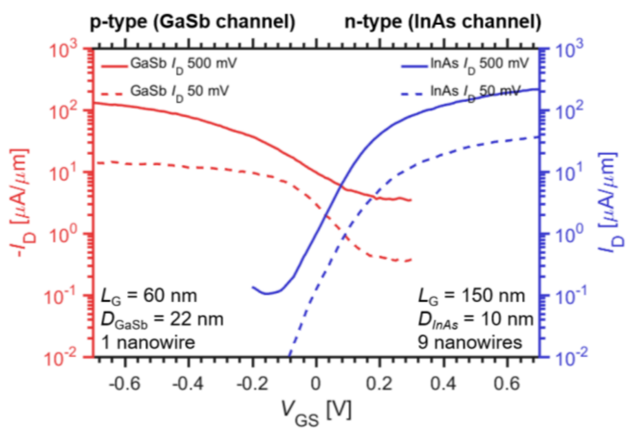

Fig. 3. Combined transfer characteristics for p-type single nanowire GaSb device (L_G = 60 nm, diameter 22 nm) and 9 nanowire n-type InAs device (L_G = 150, diameter 10 nm).

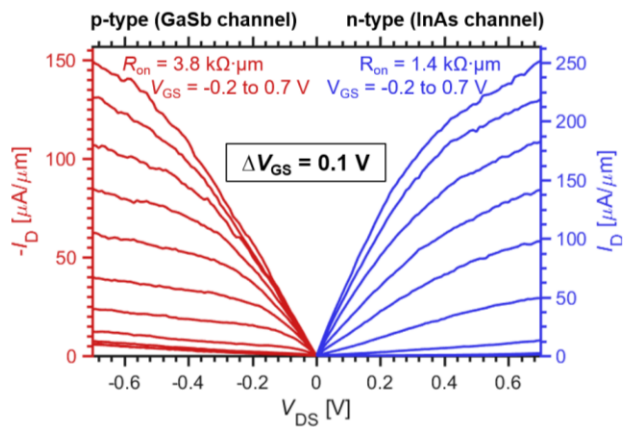

Fig. 4. Combined output characteristics for p-type single nanowire GaSb device (L_G = 60 nm, diameter 22 nm) and 9 nanowire n-type InAs device (L_G = 150, diameter 10 nm).

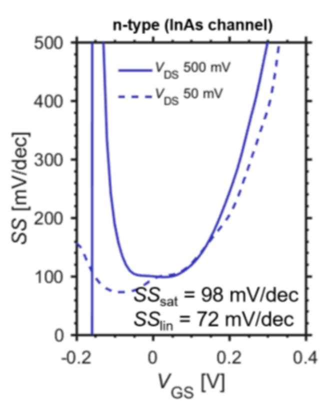

Fig. 5. SS_{sat} and SS_{lin} for the device consisting of 9 nanowires, with L_G = 150 nm and diameter 10 nm.

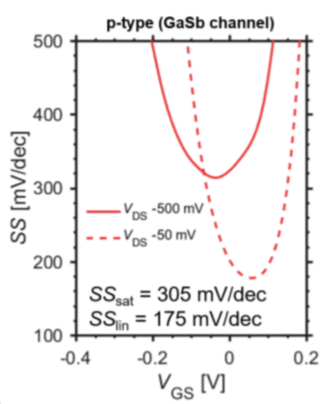

Fig. 6. SS_{sat} and SS_{lin} for the single nanowire device, with L_G = 60 nm and diameter 22 nm.

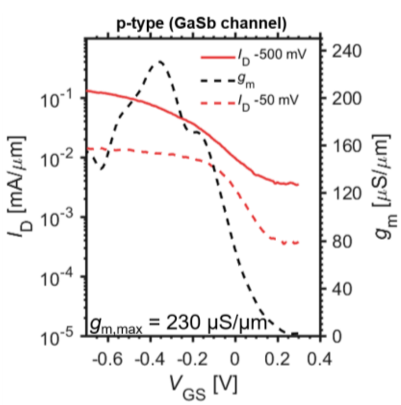

Fig. 7. Transfer characteristics and transconductance g_m for the single nanowire device with L_G = 60 nm and diameter 22 nm. A $g_{m,max}$ of 230 μS/μm is demonstrated.

	n-type	p-type
***I*on** [μA/μm]	156	98
***g*m** [μS/μm]	405	230
***L*G** [nm]	150	60
***SS*sat** [mV/dec]	98	305
***SS*lin** [mV/dec]	72	175

Table 1. Summary of DC-metrics for the all-III-V CMOS process. I_{on} defined at I_{off} = 100 nA/um for the n-type device and at V_{DS} = -0.5 V for the p-type device.

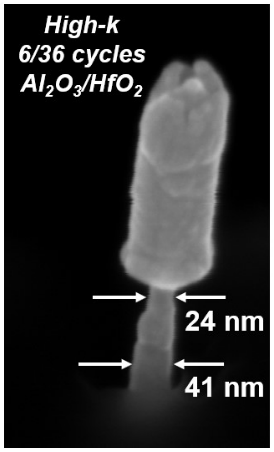

Fig. 8. SEM-image showcasing a diameter of 16 nm (+ 8 nm high-k) inside a 2-nanowire p-type device.

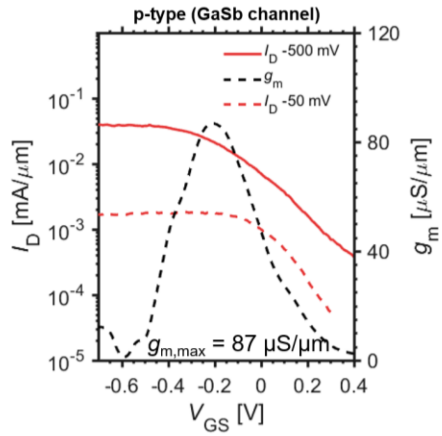

Fig. 9. Transfer characteristics for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

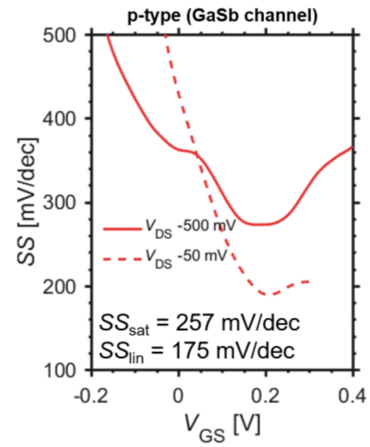

Fig. 10. SS_{sat} and SS_{lin} for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

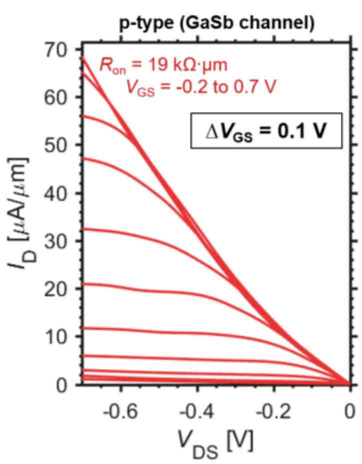

Fig. 11. Output characteristics for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

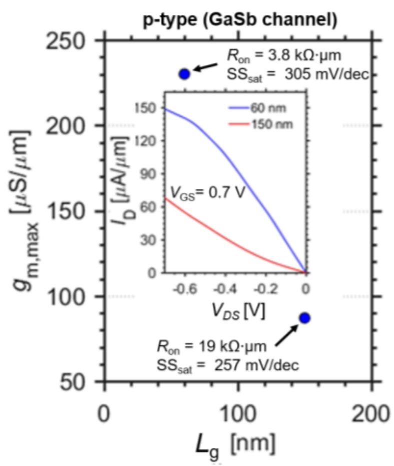

Fig. 12. The $g_{m,max}$ dependence of L_G for the single nanowire and the 2-nanowire p-type device. The inset highlights the difference at the on-state.

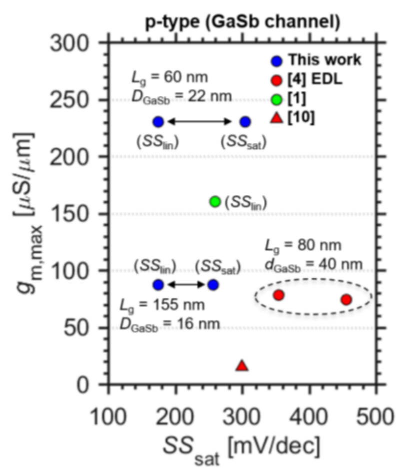

Fig. 13. Benchmarking with respect to GaSb and InGaSb p-type devices.

	III-V CMOS						III-V CMOS					
	n-type [This work]	n-type EDL [4]	n-type [9]	n-type [7]	n-type [8]	n-type [5]	p-type [This work]	p-type EDL [4]	p-type [9]	p-type [7]	p-type [8]	p-type InGaSb [1]
I_{on} [µA/µm]	156			80	4	140	98	17	10	22	2.4	~100
g_m [µS/µm]	405	1200				640	230	74				160
L_G [nm] /Crit.Dim	150 /10	50 /20	500 /20	/13	/2.5	50 /28	60 /22	80 /40	500 /20	/7	/20	20 /10
SS_{sat} [mV/dec]	98	158	185	84		158	305	355		156		
SS_{lin} [mV/dec]	72	76					175	273				260

Table 2. Benchmarking table with devices from other III-V CMOS processes as well as key p- and n-type standalone processes. I_{on} for InAs devices defined at I_{off} = 100 nA/um limit and for GaSb/InGaSb p-type devices is defined at V_{DS} = -0.5 V. Blank spaces are due to incomplete data.