Vertical, High-Performance 12 nm diameter InAs Nanowire MOSFETs on Si using an all III-V CMOS process

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High mobility materials such as narrow band gap III-V compounds offers an option to increase the MOSFET performance. Specifically, InAs and GaSb presents high bulk mobility for electrons and holes, respectively, making this material combination well suited for CMOS implementation. A continuation of the traditional down-scaling of MOSFETs for digital circuits has led to short channel effects due to deteriorated electrostatics. Therefore, new gate architectures are proposed, and implemented, with gate-all-around (GAA) structures utilizing vertical nanowires as a strong contender. Vertical nanowire MOSFETs presents an attractive way to decouple gate-length and contact geometry from the device footprint area.

Here, we present a streamlined process for co-integration of InAs(n-type) and GaSb(p-type) MOSFETs, utilizing a common gate-stack, Fig 1. Sub-100 nm gate-length devices with g_m vales up to 2.7 mS/um where fabricated, Fig 2. A detailed evaluation of series resistance originating from the source contact is enabled via utilization of thin hydrogen silsequioxane (HSQ) based spacers for the InAs devices. The process is optimized for strong n-type performance, co-integrated with a functional p-type device. The processed MOSFETs are based on, gold seeded, vapor-liquid-solid (VLS) grown InAs-GaSb heterojunction nanowires[1] with a, highly doped, overgrown InAs shell for improving etch selectivity and reducing contact resistance. The shell is later removed at the gate position to restore the proper channel material, namely InAs or GaSb core material, respectively.

The HSQ-spacer is controlled via electron beam lithography (EBL) exposure followed by wet etching (citric acid + $(NH_4)_2S$ 1:100) and deposition of a top contact (W sputtering and TiN ALD). The metal is selectively removed from the planar surfaces via an ICP-RIE process leaving the finished top contact present at the nanowire sidewalls. The same HSQ spacer is thinned down with highly diluted HF to expose the channel segment of the nanowire. This enables control of gate-position along the nanowire for the respective devices. Fig 2 presents statistical data for, 12 nm diameter, n-type devices with respect to gate position quantified by the spacer thickness. As compared to our earlier transistors[2], the metal-semiconductor drain contact is improved and the device performance is clearly influenced by added resistance at the source.

R_{on} (absolute value) dependence of the HSQ spacer thickness is illustrated in Fig. 3. The developed process enables variation of gate placement along the vertical nanowire with similar gate-lengths for all n-type devices (L_g = 40 and 50 nm). With the top contact as drain the source resistance showcases good accordance to the calculated value of 0. Ω/nm, that is calculated based on measured values in vertical TLM structures.[3] The same variation is observed as the electrodes are reversed. The top ohmic contact resistance behavior is expected to be constant since the contact transfer length is substantially shorter than the physical contact length. A linear fit in the top grounded case gives a resistance value of 0.20 Ω/nm, which demonstrates symmetrical resistance behavior of the contacts.

We have presented a streamlined process utilizing advanced VLS growth for co-integration of n- and p-type III-V MOSFETs with a common gate stack on top of Si. Strong n-type (InAs) performance is demonstrated due to greatly improved contacts. The enhanced top contact and control of gate-placement has enabled evaluation of the bottom epitaxial InAs contact.

1. J. Svensson *et al.*, Nano Letters, 15, 2898-7904 (2015) **2.** M. Berg *et al.*, Appl. Phys. Lett. 107 (2015) **3.** M. Berg *et al.*, IEEE Electron Device Letters, 37 (2016).

Figures

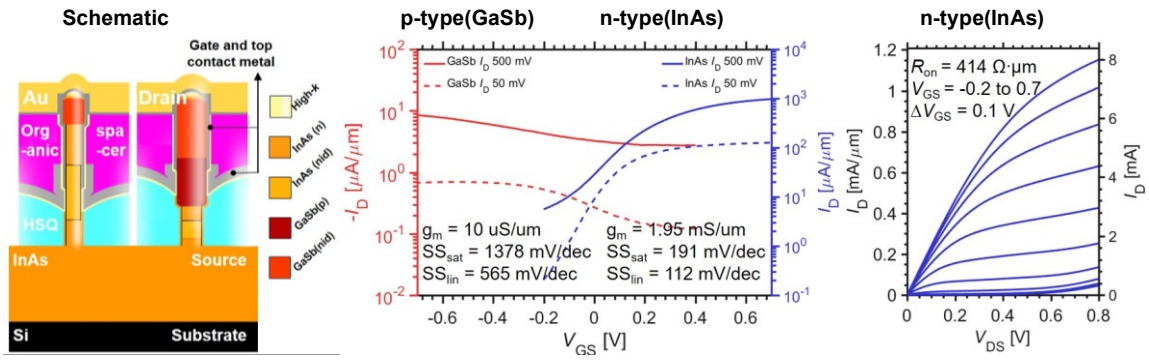

Fig. 1: Output and transfer characteristics for co-integrated n-type (InAs) and p-type (GaSb) devices. N-type: 12 nm diameter, Lg = 50 nm, 184 nanowire array. P-type: 35 nm diameter, Lg = 70 nm, 184 nanowire array.

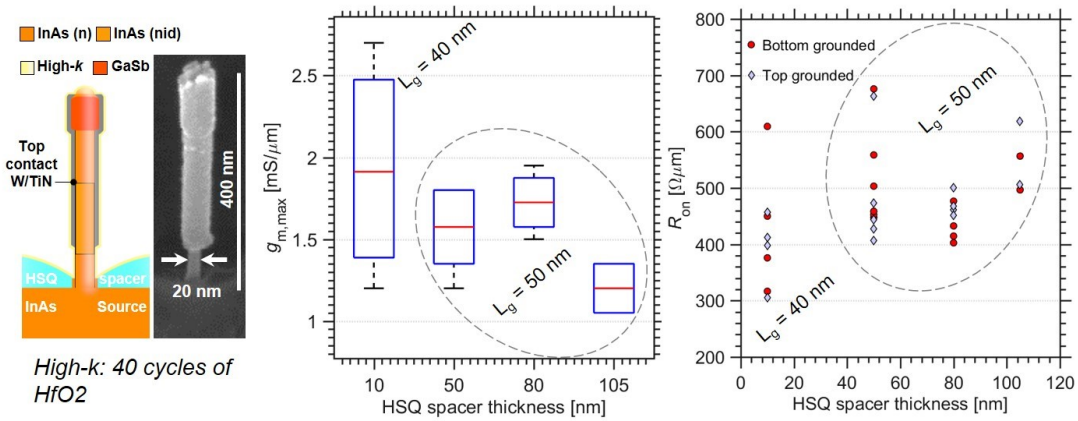

Fig. 2: Schematic of an n-type(InAs) transistor with corresponding SEM-image. Transconductance and Ron is presented with respect to HSQ spacer thickness, present at the bottom contact.

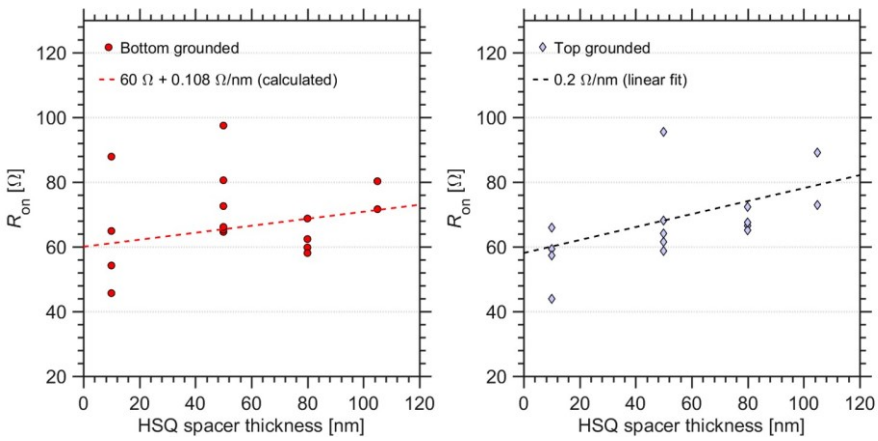

Fig. 3: Absolute R_{on} value for n-type devices with respect to HSQ spacer thickness. Resistance is evaluated in bottom and top grounded configuration. The dashed line represents a resistance trend calculated based on vertical TLM data for doped InAs nanowires (bottom grounded) with a 60 Ω offset. In the top grounded configuration the dashed line instead represents a linear regression based on measurements.