DC Distributed Power Systems - Analysis, Design and Control for a Renewable Energy System

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Abstract

Renewable energy systems are likely to become wide spread in the future due to environmental demands. As a consequence of the dispersed nature of renewable energy systems, this implies that there will be a distributed generation of electric power. Since most of the distributed electrical energy sources do not provide their electric power at line frequency and voltage, a DC bus is a useful common connection for several such sources. Due to the differences in output voltage among the sources, depending on both the type of source and their actual operating point, the sources are connected to the DC power system via power electronic converters. The intention behind the presented work is not to replace the existing AC power system, but to include local DC power systems. The AC and DC power systems are connected at some points in the network. The renewable energy sources are weak compared to the present hydro power and nuclear power plants, resulting in a need of power conditioning before the renewable energy is fed to the transmission lines. The benefit of such an approach is that power conditioning is applied on a central level, i.e. at the interface between the AC and DC power systems.

The thesis starts with an overview of related work. Present DC transmission systems are discussed and investigated in simulations. Then, different methods for load sharing and voltage control are discussed. Especially, the voltage droop control scheme is examined thoroughly. Since the droop control method does not require any high-speed communication between sources and loads, this is considered the most suitable for DC distributed power systems. The voltage feed back design of the controller also results in a specification of the DC bus capacitors (equivalents to DC link capacitors of single converters) needed for filtering. If the converters in the DC distribution system are equipped with capacitors selected from this design criterion and if the DC bus impedance is neglected, the source converters share the total load equally in per unit.

The same DC distribution bus configuration is studied in a wind power application. Especially the dynamic properties of load-source interactions are highlighted. They are interesting since the sources are considered weak for a distributed power system. This is illustrated with simulations where the power is fed from wind turbines only and constant power loads are controlled at the same time as the DC bus voltage level. The wind power generators are modeled as permanent-magnet synchronous machines. The controller needed for the machines, including position estimation and field weakening, is discussed. To control the DC bus voltage, the available wind power must be higher than the power consumed by the loads and the excess power removed by pitch angle control. Pitch angle control is a comparably slow process and, therefore, the DC bus voltage controller must handle the transient power distribution.

Personal safety and prevention of property damage are important factors of conventional AC power systems. For the investigated DC power system this is maybe even more important due to the fact that the star point of the sources and loads is left ungrounded or grounded through high impedance. The difficulty of detecting ground faults arises from the fact that the AC sources and loads are ungrounded or have high impedance to ground in order to effectively block zero-sequence currents flowing between the AC systems. A grounding scheme for the DC distribution system together with algorithms for detection of ground faults, are presented. The proposed method detects ground faults on both the AC and DC sides and is extended to cover short circuit faults with a minor work effort.

Two schemes for high voltage interconnection of DC systems are studied. One of them provides galvanic isolation, which is an advantage since elevated voltage might appear in the DC systems otherwise, in the case of a ground fault in the high voltage interconnection.

Experimental verifications follow the theoretical investigations introduced above. First, dynamic properties are studied and the behaviour predicted from theoretical analysis and simulations is verified. Then, load sharing is investigated. Also in this investigation, the experimental results agree with the simulated.

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Per Karlsson

Contents

Chapter 1

Introduction

In this chapter DC distributed power systems (DPS) are introduced together with a review of the DC DPS state of the art technology. Renewable energy systems are likely to become wide spread in the future, due to environmental demands, for example, regarding pollution. This implies that there will be a distributed generation of electric power. Since several of the distributed electrical energy sources provide DC voltage, several such sources might be connected. Due to the differences in output voltage among the sources, depending on both the type of source and their actual operating point, the sources are connected to the DC power system via power electronic converters.

It should be clear that the intention is not to replace the existing AC power system, but to include local DC systems [14]. These AC and DC systems are connected at some points in the network. The benefit of such an approach arises from the fact that renewable energy sources are weak compared to present fossil fuel, hydro power and nuclear power plants, resulting in a need of power conditioning before being fed to the transmission lines. With a DC distributed system, conditioning can be applied at a central level of the AC distribution system, close to the DC system connection points. Also, several consumer loads operate on DC (rectified AC). Therefore, DC distribution could be used to omit the need for transformers and rectifiers in every single load.

The DC distributed power system has various kinds of energy storage added, which means that it can support nearby customers during AC power system failure or emergency situations. Also, sensitive equipment likely to be installed in future intelligent buildings also needs energy backup, i.e. uninterruptable

power supply (UPS) properties. This is already in use, for example, in telecommunication sub-stations where backup batteries are usually installed. Another example is given in [63] where a battery powered DC system is supplying the AC system circuit breaker control system. Of course, reliable operation of such systems is necessary.

A larger part of the power transmission network is likely to use high voltage direct current (HVDC) transmission technology in the future [14]. Also, the recently introduced medium voltage DC (MVDC) technology is likely to be used in DC distributed power systems [14]. This implies that future electric power systems constitute a mixture between AC and DC technology.

A distributed power system with as much as several hundred power electronic converters, call for new methods and technologies, both on the operator and system level. Not only an increased control effort is required, but also the complexity of protection systems will increase in the case of dispersed generation [31]. This is true especially if autonomous operation of the distributed power system is intended.

This work addresses control and stability issues of DC distributed power systems together with their connections to surrounding AC power systems, sources and loads. Also grounding and issues on fault detection and clearance are considered.

1.1 Objectives

The main objective of this work is to study the consequences of large-scale incorporation of power electronic converters in DC distributed power systems. The main objective is split into several sub-objectives, all imperative for a large-scale system. The first issue to treat is selection of a suitable system voltage, at least at the consumer level. Stability and dynamic properties of DC voltage control are of great concern. Requirements on hardware and software should be stated so that the system could grow, i.e. additional converters installed in an existing system, without system degradation. Voltage control in the case of weak sources should also be investigated, since several of the renewable energy sources possess low inertia. Suitable grounding and fault detection schemes should be investigated. Connection of several DC systems should be investigated. One important objective is that the need of communication should be studied.

1.2 Contributions

The contributions of this work are given in Chapters 3 to 7 and concluded in Chapter 8. The main results are summarised here. Suitable voltage levels are not explicitly discussed in the thesis. Instead, a DC bus voltage level suitable for 400 V AC sources and loads is adopted. This is due to the fact that by doing so, the proposed system voltage covers existing consumer loads. Future apparatus might require a different load voltage level. To compensate this shortcoming, a large portion of the investigation is made on a per unit (p.u.) basis. Therefore, the results can be used for any DC bus voltage level.

The converters are first specified with focus on interaction between the AC and DC sides. Then a DC bus voltage droop controller is adopted. The demands on interaction together with droop requirements give a specification of the relation between rated power and converter DC side filter, i.e. DC bus capacitance, for each converter. The dynamic properties are investigated, both by means of stability analysis, in terms of root-locus, and large-signal simulations. It is found that for reasonable DC bus cable parameters, stability is of minor concern, for the selected DC side filter. In other words, the requirements on interaction between input and output of the converters is stronger than the stability requirement. Voltage droop control provides autonomous load sharing, implying that communication is not needed. The selected implementation of the droop algorithm and the controller parameters allow an arbitrary number of converters in the DC system. Furthermore, the already inserted units are not altered if additional units are incorporated.

A wind powered DC system is adopted to investigate voltage control and load sharing in the case of renewable energy sources. In this case a speed droop algorithm is developed. The dynamic properties of speed and voltage droop control are investigated. It is concluded that low-speed communication is beneficial for non-dispatchable sources. A fault detection algorithm is developed. The algorithm is studied for different levels of communication, ranging from none to point-to-point communication. An existing converter topology is adopted for interconnection of DC systems. The same converter topology is also used for power transmission. Voltage droop control is adopted also here. Thus, high-speed communication is not necessary. However, when low-bandwidth communication is utilised, the system operator has the ability to control power flow. A laboratory set-up is designed to verify voltage control, load sharing and fault detection.

1.3 Outline of the thesis

This chapter contains a brief introduction to the thesis and the academic work presented. A survey of previous work is also given. Chapter 2 reviews classical HVDC and Voltage Source Converter (VSC) based HVDC transmission systems. The study includes simulations, where especially the harmonic content of the currents is compared.

In Chapter 3, voltage and power control methods for the investigated distributed power system are developed. This analysis also results in a method for selection of DC bus filter capacitors. The steady state and dynamic properties of the selected control scheme are investigated for varying cable parameters. Load sharing is investigated for different voltage control methods.

In Chapter 4, the same system but with weak sources is investigated. Here, the DC power system is fed only with wind power and still constant power loads can be supplied and the DC bus voltage controlled. Personal safety and protection of equipment are important issues for any power system and Chapter 5 is devoted to these topics. The chapter starts with a presentation of the grounding scheme and typical fault conditions. Then the methods of fault detection and localisation are presented and verified in simulations.

In Chapter 6, connection of DC distributed systems is considered. The proposed scheme contains a transformer, providing galvanic separation between different DC systems. In Chapter 7, measurement results verifying dynamic properties, load sharing and fault detection are presented. The work is concluded in Chapter 8.

MATLAB™ Power System Blockset is utilised for the time-domain simulations of Chapter 2 where thyristor based converters are considered. DYMOLA™ is utilised for the time-domain simulations including transistor based converters, i.e. for the simulation of VSC based HVDC transmission in Chapter 2 and all time-domain simulations in Chapters 3 to 7. Large-signal converter models are used for simulations investigating two-converter systems and DC transmission systems. Average converter models are utilised for simulations where load sharing or fault detection is investigated. Discrete-time controllers are utilised for both the large-signal and the average converter models. MATLAB™ is used in Chapter 3 for investigation of stability for different cable parameters in terms of root-locus of the poles. The simulations in the appendixes are all carried out in MATLAB™-SIMULINK™.

1.4 Publications

The results presented in this thesis regard DC bus voltage control and fault detection and clearance, found in Chapters 3, 4, 5 and 7. The main results of these chapters are also presented in

P. Karlsson and J. Svensson, "DC Bus Voltage Control for Renewable Energy Distributed Power Systems", IASTED Power and Energy Systems Conference, PES 2002 Conf. Proc., Marina del Rey, CA, USA, May 13-15, 2002, pp. 333-338.

P. Karlsson and J. Svensson, "Fault Detection and Clearance in DC Distributed Power Systems", IEEE Nordic Workshop on Power and Industrial Electronics, NORPIE 2002 workshop proc., Stockholm, Sweden, Aug. 12-14, 2002, CD-ROM pages 6.

P. Karlsson and J. Svensson, "DC Bus Voltage Control for a Distributed Power System", provisionally accepted for publication in IEEE transactions on power electronics, paper no. 2001-834-LP.

P. Karlsson and J. Svensson, "Voltage Control and Load Sharing in DC Distribution Systems", submitted to European Conference on Power Electronics and Applications, EPE 2003, Toulouse, France, Sept. 2-4, 2003.

The thesis author has also authored the publication

J. Svensson and P. Karlsson, "Wind Farm Control Software Structure", International Workshop on Transmission Networks for Offshore Wind Farms, workshop proc., Stockholm, Sweden, Apr. 11-12, 2002, proceeding pages 15.

in the same research project. The contribution made by the thesis author in the last paper is minor.

The previous work on off-board battery chargers for electric vehicles, also part of the research work, is reported in

P. Karlsson, M. Bojrup, M. Alaküla and L. Gertmar, "Efficiency of Off-Board, High Power, Electric Vehicle Battery Chargers with Active Power Line Conditioning Capabilities", European Conference on Power Electronics and Applications, EPE '97 Conf. Rec., Trondheim, Norway, Sept. 8-10, 1997, vol. 4, pp. 4688-4692.

M. Bojrup, P. Karlsson, B. Simonsson and M. Alaküla, "A Dual Purpose Battery Charger for Electric Vehicles", IEEE Power Electronics Specialists Conference, PESC '98 Conf. Rec., Fukuoka, Japan, May 17-22, 1998, vol. 1, pp. 565-570.

M. Bojrup, P. Karlsson, M. Alaküla and L. Gertmar, "A Multiple Rotating Integrator Controller for Active Filters", European Conference on Power Electronics and Applications, EPE '99 Conf. Rec., Lausanne, Switzerland, Sept. 7-9, 1999, CD-ROM pages 9.

P. Karlsson, M. Bojrup, M. Alaküla and L. Gertmar, "Zero Voltage Switching Converters", IEEE Nordic Workshop on Power and Industrial Electronics, NORPIE 2000 workshop proc., Aalborg, Denmark, Jun. 13-16, 2000, pp. 84-88.

P. Karlsson, M. Bojrup, M. Alaküla and L. Gertmar, "Design and Implementation of a Quasi-Resonant DC Link Converter", European Conference on Power Electronics and Applications, EPE 2001 Conf. Rec., Graz, Austria, Aug. 27-29, 2001, CD-ROM pages 10.

Only minor parts of the work reported in the second and third publications above are attributed the author of this thesis. The work on resonant converters reported in the other publications above is also the basis of the Licentiate's thesis

P. Karlsson, "Quasi Resonant DC Link Converters - Analysis and Design for a Battery Charger Application", Licentiate thesis, Department of Industrial Electrical Engineering and Automation, Lund Institute of Technology, Lund, Sweden, November 1999.

This work was evaluated by Professor Frede Blaabjerg at the Department of Energy Technology, Aalborg University, Denmark.

Besides the publications within the research projects, another publication related to power electronics education has been presented

A. Nilsson, P. Karlsson and L. Gertmar, "Environmental Engineering in the Power Electronics Education", European Conference on Power Electronics and Applications, EPE 2001 Conf. Rec., Graz, Austria, Aug. 27-29, 2001, CD-ROM pages 10.

Less than half of the work of this paper is attributed the thesis author.

1.5 Previous work

This section provides a literature survey of previous work on renewable energy sources and distributed power systems in which the most relevant previous work is discussed. A classification of the papers is made based on the nature of the references even though several of them cover more than one topic. However, the references are sorted under the topic, which the thesis author find most interesting in the context of the rest of the thesis.

Distributed energy systems

Several arguments for distributed power systems are listed in [31]. Among these, transmission capability saturation of centralised power systems and related stability problems seem most important. The additional intelligence needed to control, protect and maintain distributed power systems is focused in [31]. The future market of (DC) distributed power systems is discussed in [33], where it is concluded that the growing market includes computer, military/aerospace and communication applications. It is also stated that distributed power systems are more costly than centralised. Note that in [31], the distributed system is part of a nation wide power transmission/distribution system including dispersed generation. In [33], the distributed system intended is restricted to supply power to electronic equipment like inside a single computer.

Power electronics for use in renewable energy applications are discussed in [14]. Also some benefits and drawbacks associated with renewable energy sources are discussed. Photovoltaic, fuel cell and wind energy systems are reviewed briefly. Small-scale hydro pump stations or battery banks for electric energy storage are, however, not discussed in [14]. Still, they are included in the principal scheme of a distributed power system, together with flywheel and superconducting magnetic energy storages.

DC distributed power systems

Some of the literature studied does not fit into the study, though interesting. For example, [39][40][41][42][66] investigate a high current, low voltage DC mesh with thyristor based converters. In [39][40][42], a superconducting power system is considered, whereas an industrial power distribution system with inherent UPS properties is considered in [41][66]. The intended system

might contain several hundred thyristor based sources (rectifiers) and loads (inverters), but the simulated systems are of considerably lower complexity. In [39], a DC power system formed by one rectifier and three inverters is studied. In [40][41][42][66], three rectifiers are used as sources. Since three sources are present, load sharing has to be considered. In all these cases, DC voltage droop control is used to give appropriate load sharing. This means that a voltage droop characteristic is assigned to each source. In [40][66], the LVDC mesh is simplified to a ring bus and in [42] a superconducting energy storage (SMES) is added to the system. The paper [41] focuses on investigation of the droop scheme. It is stated that this works well for superconducting networks. However, the performance of a non-superconducting network is questioned.

In the literature the term power electronic building block (PEBB) is sometimes used as a term for generic building blocks for power conversion, control and distribution with control intelligence and autonomy. The work presented in [11] proposes a distributed digital controller for PEBBs. The main requirements and desired features of such a controller is discussed in [11]. The proposed controller is based on components presently available and used in other applications.

A 600 W front-end source converter module and a 300 W load converter module are designed in [36]. The source converter is designed for zero voltage transition (ZVT) technique and the load converter utilises zero voltage switching (ZVS) technique. The source converter is formed by a single-phase rectifier, equipped with a power factor corrector (PFC), i.e. followed by a boost converter. The DC system voltage equals 48 V. Experimental results are included in [36]. In [46], converter topologies suitable for DC distributed power systems are evaluated. Especially, source side front-end boost rectifier candidates are investigated but also load side converter modules.

Voltage control and load sharing

There are basically two different methods to achieve load sharing. One of the methods is referred to as the droop concept and the other as the master/slave concept.

For the droop concept, a finite loop gain for the DC voltage controller is adopted. A droop characteristic is obtained from the transfer function slope in the *P-V* plane at the desired DC bus voltage. Since this droop characteristic appears as a negative slope in the *P-V* plane, load sharing is obtained. The

quality of load sharing is determined by the negative slope of the droop characteristic, i.e. for a steep slope, load sharing is good but voltage regulation is poor. On the other hand, for a shallow slope, load sharing is poor but voltage regulation is good. Therefore, a trade-off between voltage regulation and load sharing has to be made for the droop concept.

In the master/slave concept, only one of the source converters is controlling the DC bus voltage. The other source converters are current controlled. This results in a stiff DC bus voltage regulation and a fully controllable load sharing.

The papers [38][52][58] give an overview of these paralleling methods. According to [52], five different droop schemes exist. The first is based on the use of converters with inherent droop feature. The second scheme is based on voltage droop due to series resistors. The third scheme is called voltage droop via output current feedback. The fourth scheme is referred to as current mode with low DC gain. The fifth is scheduling control via a non-linear gain. The benefits of the droop schemes are the ease of implementation and expansion and that no communication between the converters (i.e. supervisory control) is needed. This gives high modularity and reliability. The main disadvantages are that the voltage regulation is degraded to achieve the droop characteristic and that the current sharing is poor due to open loop control of the entire system.

The next large group identified in [52] is referred to as active current sharing schemes. Common to these schemes, is that an additional control loop is used to provide current sharing. According to [52], three different active current sharing control structures are used for parallel converter systems. The first control structure is called inner loop regulation (ILR). The second control structure is referred to as outer loop regulation (OLR). The third structure relies on an external controller (EC). EC implies a large number of interconnections between the converters. This means that both the modularity and reliability might be degraded. It is, however, stated in [52] that the rapid development of distributed power systems implies that this technique should be examined in a new light. The high level supervisory controller can be redundant, and the converter cells are only responsible for gating and fault indication. This method is likely to yield the highest performance because of its possibility of interleaving [52].

Also six current programming (CP) methods for active current sharing schemes are reviewed in [52]. Of these six, three are average and three are

master/slave current programming methods. Seven methods to operate multiple DC-DC converters in parallel are given in [38]. In [58], four methods to achieve load sharing in parallel converter systems are given.

In [29], load sharing properties are studied by examining the output plane (output current versus voltage). A small-signal model is developed for the investigation. Simulations and experiments verify the theoretical results. The output plane is derived from equations for current programmed converters in [13]. The output plane is verified in large-signal simulations and experiments. Droop load sharing is evaluated in [37]. One of the important conclusions made in [37] is that the droop method requires precise control of the initial output voltage. It is also stated that the main advantages of the droop control method compared to other converter paralleling schemes, are the ease of implementation and that communication by means of control-wire connection is not required.

A droop function with a programmed droop resistance equal to the equivalent series resistance (ESR) of the output capacitor is proposed in [16]. Load sharing with the selected droop function is investigated by means of simulations and experiments.

A paralleling scheme called central-limit control, closely related to master/slave control, is presented in [64] and reviewed in [58]. The main difference between master/slave and central-limit control is that for the latter all the sources regulate the load converter DC bus voltage.

Autonomous master/slave current sharing is used in [62] for two source converters connected in parallel. A small-signal model for the two source converters together with their controllers is derived. A current sharing algorithm is also presented. Current sharing control is necessary since otherwise small differences in the source converter parameters would cause severe load imbalance. Also, the voltage loop is investigated. Design of the compensators is discussed but only a few actual results are concluded.

In a situation where several converters connected to the DC distribution bus that all control the voltage precisely to the reference at their respective connection point, load sharing among sources is not controlled. Instead, load sharing is entirely determined by the distribution bus impedance [75].

In [76], it is stated that distributed power systems have better performance than centralised. Moreover, it is stated that the sources connected in parallel to the DC bus (front-end boost rectifiers), should share the load to ensure proper

operation. In [76], the droop method is used together with gain scheduling, which is said to give a robust design in terms of source-load interaction, i.e. good load sharing and good voltage regulation for a modular design approach.

According to [76], the main problems of master/slave load sharing are that fast communication is required and that a single point failure can disable the entire system. Also, all modules are control dependent. Six important issues are addressed in [76]. The first is stability, for example, in terms of interactions between parallel converters (especially in the case of three-phase sources due to the appearance of zero-sequence currents). The second important issue is load sharing when several sources are connected in parallel to the DC distribution bus. The third issue is modularity, i.e. the ability to manufacture and maintain the DC system. The fourth issue is autonomous control enhancing modularity and providing increased system reliability and redundancy. The fifth issue is DC bus voltage control, which is imperative. The sixth and last issue identified in [76], is the source output impedance which indeed affect several of the other issues, for example, the interaction between converters connected to the DC system.

The gain-scheduling method utilised in [76] is based on a modified droop method where the voltage loop gain is increased for increasing output power in such a way that the voltage error decreases compared to the case with a constant gain droop function. According to [76], both DC bus voltage control and load sharing show better performance compared to master/slave control. An interesting option not discussed in [76] is to use an adaptive controller for the DC bus voltage control.

In [44], a droop load sharing scheme is investigated where the DC bus voltage reference is adaptively controlled for each converter, in order to improve voltage regulation and load sharing.

Small-signal stability based on impedance specification

A system with an arbitrary number of DC-DC source converters paralleled using master/slave control, is investigated in [61]. Small-signal stability and dynamic performance are investigated. Also, a current sharing compensator is developed. The compensator is designed in the frequency-domain and verified through time-domain simulations.

A small-signal model for a parallel rectifier system is derived in [12]. Dynamic properties in the case of long inductive and resistive cables are investigated. It

is found that the cable parameters do not affect the dynamic properties extensively. Load sharing is investigated for both droop and master/slave methods. It is found that a system with parallel rectifiers is stable provided that each individual rectifier is stable when the droop method is applied. This is not true in the case of master/slave control, which should be designed carefully.

Small-signal stability criteria for DC-DC converter systems often end up in an impedance specification, where the relation between source converter output impedance Z_o and total load converter input impedance Z_i is given by

$$|Z_o| << |Z_i| = 1 \Big/ \left| \sum_k \left(1 \Big/ Z_{i,k} \right) \right| \tag{1.1}$$

where $Z_{i,k}$ is the input impedance for converter k. This impedance criterion was first established in the paper "Input Filter Considerations in Design and Application of Switching Regulators" written by Middlebrook in 1976 [55].

Some of the more recent impedance specifications for stable operation of DC distribution systems instead specify a "forbidden" region in the complex frequency plane [20][21][28][70]. In [70], a forbidden region for the total loop gain is specified so that a minimum phase margin is ensured. This is further developed in [20][21] where the individual load converter impedance is specified so that the forbidden region is avoided by applying

$$\mathrm{Re}\left(\frac{Z_o}{Z_{i,k}} \right) < -\frac{1}{2} \cdot \frac{P_{load,k}}{P_{source}} \tag{1.2}$$

and

$$-90^\circ - \Phi_k < \left(\angle Z_o - \angle Z_{i,k} \right) < 90^\circ + \Phi_k \tag{1.3}$$

where

$$\Phi_k = \arcsin \left| \frac{1}{2} \cdot \frac{Z_{i,k}}{Z_o} \cdot \frac{P_{load,k}}{P_{source}} \right| \tag{1.4}$$

The results obtained in [20][21] are applied for the power supply of a Pentium processor in [71]. The power system of the investigated PC provides the voltage levels 3.3 V, 5 V and 12 V. The interactions between source and

load are found to be strong but no instability occurs. However, it is found that conditional stability problems might occur. It is stated that conditional stability problems cannot be solved by the application of the impedance criterion. According to [71], there are two possible solutions to check for conditional stability. The first is to derive the system transfer function with different loads, which is generally very complicated. The second is to include gain information in the impedance criterion, giving a set of impedance curves for the source converter output impedance. There are also two methods reducing the risk for occurrence of conditional stability. The first is to increase the source converter DC side capacitance. The second is to apply a current feedback loop. The work in [20][21] together with the stability margin monitoring method presented in [22][23][24][50] is concluded in [25].

In the paper [65], the relationship between stability and DC bus capacitance is studied. Also fault propagation is investigated. The main objective of the investigation is to minimise the DC bus capacitance.

In [28], large DC power systems for space applications are investigated. Here, equation (1.1) is used for small-signal stability analysis. It is also pointed out that large-signal or transient stability issues are of great concern. The methods suggested for large-signal analysis are computer analysis involving Bode plots, Nyquist curves and transient responses. Also, hardware testing, both for validation and model development, are used in the stability analysis.

Input filter design is discussed in [27]. Here, all the DC-DC converters are equipped with an input filter. Initially, the effect of the input filter on the DC-DC converter transfer function is investigated. Then, the extra element theorem [56] is used to investigate the effect caused by the impedance seen from the filter input terminals. This impedance is divided into two parts: the source (series) impedance and the cumulative (shunt) impedance, i.e. the collective regulator input impedance resulting from the input filters of the other power modules. If

$$\begin{aligned} |Z_s| &<< |Z_n| \\ |Z_s| &<< |Z_d| \end{aligned} \tag{1.5}$$

hold, where Z_s is the filter output impedance, Z_n and Z_d are the DC-DC converter input impedances with the output nulled and shorted, respectively, then the DC-DC converter transfer function is in principle unaltered by the input filter [27]. Furthermore, this means that the negative impedance

resulting from a constant power load is decoupled from the DC distribution bus. It is found that if several DC-DC converters, equipped with filters designed from this rule are connected to a common DC distribution bus, then the cumulative impedance is positive and decrease as the number of power modules increase. This means that the stability margin increases as the number of connected power modules increases.

In [51], power buffering is utilised to enhance stability of a DC distributed power system during transients. This is achieved by reducing the loop gain, and consequently, the negative incremental input impedance of the converters so that the sum of the source output impedance and the negative incremental input impedance is positive. This yields a stable system. Another possibility is also discussed in [51], where the power buffer is controlled to a certain input impedance during the transients.

Large-signal stability

Large-signal stability is treated in [2], where the distributed power system is formed by one single DC source with several load converters connected. Each load converter is equipped with an input *LC*-filter. The *LC*-filters are modeled as ideal except for a resistor *R* connected in series with the inductor. The large-signal stability constraints are expressed as boundaries on *R*. The upper limit for *R* is formed by application of the equilibrium point condition, i.e. by investigation of the maximum *R* yielding an intersection between the source and the load characteristics. According to [2], this gives

$$R < \frac{1}{4} \cdot \frac{V_{dc}^2}{P_o} \tag{1.6}$$

where V_{dc} is the DC source voltage and P_o is the load converter output power. The lower limit for *R* is found from the mixed potential criterion. In [2], lower limits on *R* are established for the cases with one, two and *n* load converters connected to a single DC source. However, computational problems appear for larger systems. Therefore, approximations are used in the case of multiple constant power loads. In the case of *n* constant power loads it is also assumed that these are equal in terms of filter component values and output power. For this case, an approximate lower bound is given by [2]

$$R > \sqrt{\frac{L}{C}} \sqrt{2n^2 - n} \tag{1.7}$$

For high n, the resistance R has to be high, which implies high power dissipation. In [2], it is found that the approximation of the lower bound for R gives an error between the approximated maximum singular value and the exact approaching 11% as n increases.

Robustness against parameter uncertainty

In [47], DC power system stability is investigated with focus on robustness against parameter uncertainty. Robust control theories are applied to DC power systems. According to [47], this is done to cope with the sensitivity to parameter and load variation resulting in DC power systems prone to instability. The stability robustness is investigated by computing the multivariable stability margin, k_m, and the structured singular value, μ. Calculating these quantities exactly is cumbersome. Therefore, different approximation methods are investigated in [47].

The inherent instability of DC distribution systems originates from the fact that constant power loads appear as negative resistances to the regulators (source converters). The equivalent resistance seen from the regulator is [47]

$$R_{eq} = \frac{\partial v}{\partial i} = -\frac{v_{bus}^2}{P} \tag{1.8}$$

In [47], Middlebrook's Criterion [55] is regarded as the normal way to handle this problem, i.e. to use an isolation concept. Two problems arise from using Middlebrook's Criterion according to [47]. Firstly, parameter variations are not covered by the criterion and, secondly, it is intended for a two-port system. For the multiloop case considered in [47], a multiple input multiple output (MIMO) system should instead be investigated, which is not covered by Middlebrook's Criterion. In [47], expressing the electrical system as a MIMO system and then use the convex hull algorithm to calculate the stability margin is instead emphasised. This method is compared to other.

Converter modeling and control

Modeling and control issues for front-end three-phase boost rectifiers are discussed in [34]. An average model is developed and the stability with different loads connected across the DC side is investigated. Since an average model is used, a constant power load is modeled as a resistor with negative resistance. A non-linear controller, e.g. with feed forward of the load current, gives the best performance.

Modeling of a four-leg inverter, i.e. a neutral connected inverter, used in a PEBB based DC distributed power system, is investigated in [67]. The four-leg converter is presented in [78]. As in [34], the converter model in [67] is averaged. The converter input filter is of *LC*-type but with an *RC*-circuit connected across the capacitor to increase the shunt impedance at high frequencies. The impedance overlap between the filter input and output impedances is investigated, to fulfil equation (1.1). As expected, the interaction between input and output decreases as the damper resistance increases, i.e. the phase margin increases. In [67], a single source converter formed by a transistor front-end rectifier is considered. The DC side filter of the transistor rectifier is formed by a capacitor. Interaction between the rectifier output filter and the inverter input filter is also investigated. As in the previous case, the phase margin increases with increasing damper resistance. The same result is achieved by increasing the rectifier DC side capacitance. A more interesting solution exists according to [67]: if the controller bandwidth is reduced, the phase margin is increased. The interesting characteristic about this feature is that it can be tuned online, whereas the system has to be shut down for the other two methods.

In [75], two source converters connected to the same DC distribution bus are modeled simultaneously to investigate their interaction. Here, master/slave control is used and it is claimed that the same control strategy as in the single source case applies. However, it is stated that for long distribution distances with several sources and loads, other control strategies are probably required.

A switch model for large-signal modeling of distributed power systems is studied in [10]. It is found that the simulation with the proposed model shows good agreement with device level simulations. It is also found that the simulation time is reduced significantly.

The zero-sequence current in distributed power systems

The fact that grid connected converters might give rise to high common mode currents is well known. This causes problems like bearing currents and insulation problems in electrical machines [48]. The common mode current results from the variations in voltage potential of the DC side supply rails, depending on the actual switch state. Consequently, the fundamental of the common mode current appears at switching frequency. The capacitive coupling between the supply rails and ground provides a path for the common mode current. Due to the capacitive nature of the current path, the common mode current magnitude increases with increasing switching frequency.

In [72], the supply rail voltage shift is analysed. First, the neutral to ground voltage variation for a diode rectifier/three-phase converter combination is investigated. The neutral is in this case the star-point of the load at the converter output, which for example could be the star-point of an electrical machine. It is shown that the neutral to ground voltage varies as the negative supply rail to neutral voltage for the rectifier with the converter switching superimposed. Both simulations and measurements are shown. Second, the same investigation is made for a controlled rectifier/converter combination, connected back-to-back. In this case the situation is even worse, at least in terms of high frequency content, since the negative supply rail to ground voltage variation is determined by the switching frequency of the rectifier. According to [72], one way to partly reduce the problem is to synchronise the modulation carriers of the rectifier and converter. Note that synchronisation should be avoided if modularity and autonomous control is desired. Also a third case is investigated, where two generators feed the same DC distribution bus via transistor rectifiers. In this case it is complicated to synchronise the switching patterns since it is likely that the generators operate at different load conditions. Furthermore, there might be extremely high zero-sequence currents if both generators are grounded to the same physical ground potential. Three methods are proposed to reduce the problems related with common mode currents. First the alleviation method, which includes installing electromagnetic interference (EMI) suppressing chokes, filtering and the use of soft-switching techniques. The second method is referred to as a tolerant method, where EMI currents are allowed but shielding is used in the motor to reduce the bearing currents and insulation stress. The third method addresses new converter topologies, where the four-leg VSC [67][78] is mentioned as an example. In [1], high impedance grounding is investigated to manage problems associated with neutral voltage shift.

In [74], two transistor rectifiers are connected to the same generator (or equivalently AC power system) and the rectifiers feed the same DC distribution bus. It is found that in the average simulation model, in *dq*-coordinates (Appendix B), the zero-sequence current does not appear. Instead, a *dq0* simulation model has to be adopted. In this simulation model, a high zero-sequence current appears. This problem is especially obvious when one of the rectifiers has the switch state 000 and the other 111 (Appendix A), which means that the DC distribution bus voltage is applied across the sum of the generator stator inductances for each phase. In [74], this is solved by adopting a modulation strategy where the zero voltage vectors, 000 and 111, are not utilised for the source rectifiers. In [77], a non-isolated system of one front–

end boost rectifier and one inverter is studied, from a converter modulation point of view. It is found that the proposed modulation scheme (interleaving) reduces the common mode current. In [75], ground loop interactions between two generators with a common ground, is also discussed.

An active filter for the DC bus is discussed in [73]. The active filter is formed by a transistor half-bridge and a DC link capacitor. The DC distribution bus side filter is purely inductive. The active filter is required to reduce AC current components injected from three-phase voltage source converters. These AC components result from negative-sequence or harmonic currents on the AC side of the three-phase converters. In [73], the switching frequency of the active filter is selected considerably higher than the one of the other converters of the DC distribution bus. The high switching frequency implies that interactions between the other converters can be suppressed, resulting in a stabilising effect. Consequently, the DC distribution bus impedance is tuned for best performance, thus, enhancing the stability. Note that the DC link capacitor voltage must be higher than the DC bus voltage, for the active filter.

Electromagnetic interference

In the paper [8], EMI problems related to switch mode power supplies connected to a DC distribution bus of long length are investigated. The load converter switching appears as a variable load, which generates reflections. The high rise and fall times generate high frequency signals radiated by the long power system conductors.

In [15], high frequency interaction in terms of disturbance propagation from DC distribution bus voltage to load converter output voltage is addressed. The problem is investigated from an analytical point of view and with simulations and experiments. The key result is that the switching frequencies of the converters should be as equal as possible to reduce load converter output oscillations.

Load flow and short circuit calculations

DC power system analysis in terms of load flow and short circuit calculations is investigated in [26]. Numerous source models (i.e. battery charger, rectifier and generator models) are given. Also connector models for load flow and short circuit calculations are investigated. Loads and branches are modeled. According to [26], the present standards (in the year 1996) are not complete and need further work.

In [3], the methods of the IEC draft standard "Calculation of short circuit-currents in dc auxiliary installations in power plants and substations" are investigated. The calculations are intended to determine appropriate fusing for the system. Four different loads are investigated in [3]. These are the (thyristor) converter in 50 or 60 Hz AC systems, stationary lead-acid batteries, smoothing capacitors and DC motors. The straightforward methods given in the standard are compared with EMTP simulations. The standard gives conservative estimates of the short circuit currents (25% overestimated). Also, the time constants estimated according to the standard are longer than the simulated. The standard was not applicable (in the year 1996) to large DC systems, such as railway traction systems, HVDC transmission systems and photovoltaic systems. According to [3], the reason is that the models developed for the standard do not cover the set of electrical parameters appearing for these systems.

A detailed model of an *RL*-fed bridge converter for use in a Newton-Raphson power flow program for industrial AC/DC power systems is derived in [68]. This is done since bridge models in simulation packages are generally only valid in, for example, HVDC applications where the commutation resistance is negligible. Two systems are simulated to demonstrate the accuracy, a coal mine electrical power system and a railway power system. It is found that the developed model yields a considerably higher accuracy for systems with high commutation resistance.

Due to the differences between load-flow studies of AC and DC power systems, a new algorithm and a DC simulation package are developed in [79]. The load flow algorithm is based on the Newton–Raphson method. DC load flow simulation models are developed for constant DC voltage power sources, batteries, AC/DC rectifiers, constant power load, constant current load, constant resistance load and time-varying load. Several case studies are simulated, and their voltage profiles are shown.

Grounding

According to [72], the best ground point is the mid-potential between the positive and negative conductors of the DC distribution bus. This means that the voltage shift is localised to each sub-system. In [17], grounding issues for drive systems in general are discussed. A thorough analysis is presented and it is found that high impedance grounding is expected to be used in the future as fault detection systems become more accurate and reliable.

1.6 Specification of a distributed power system

This section contains the main requirements put on a future DC distributed power system. The requirements are based on the previously addressed objectives of this work.

- The power system should be well adapted to operate with present sources and loads, in terms of voltage and frequency. It should also provide a high degree of load and source power controllability.
- The system should be expandable, i.e. new load and source units should be possible to add, without altering units already connected.
- Communication between individual converters should be avoided since adding new units will be more complicated. Also, the system could suffer from reliability problems. On the other hand, communication at a low bandwidth is considered necessary for supervisory control. Therefore, single converters are allowed to rely on low bandwidth communication but should be able to operate as stand-alone units.
- The degree of personal safety should be equal to or better than in the present power system.

The basic requirements above lead to other, more technical, requirements. For example, high bandwidth source and load side current controllers should be adopted to provide load and source power controllability. Also, the high bandwidth of the current controllers together with the desire to not rely on (high-speed) communication result in a demand of long equivalent time constants of the DC bus voltage control. This also makes the DC bus robust against disturbances on converter load and source sides, for example, negative-sequence disturbances.

Chapter 2

Existing DC power systems

There are few systems utilising DC to transmit or distribute electrical power by means of DC today. Most power is transmitted and distributed by means of AC. The AC grid frequency is thereby the most essential control parameter and after that generation and distribution of reactive power to keep the voltage within specified limits. The stability of an AC power system is strongly dependent on its electro-magnetic characteristics and to a minor extent on power electronics because power systems expanded over wide areas during half a century when DC based high-voltage transmission was non-competitive. During the latter half of the last century, HVDC transmission became cost effective, especially as a way to connect asynchronous grids.

For the last decades, the feasibility of low-voltage self-commutated inverters connected to a common DC bus has increased, resulting in LVDC distribution systems feeding industrial adjustable-speed drives. Converters similar to the ones utilised in VSC based HVDC and in industrial drives are also used on-board electrical railway vehicles equipped with a common low-voltage, LV, or medium-voltage, MV, DC bus. The main aspect of those, so-called, traction drives is that the converters connected to the propulsion drives are normally handling the same power levels but split into parallel drives due to redundancy and/or rating reasons. There is usually also an auxiliary power converter connected to the common DC bus.

In this chapter, HVDC transmission systems are discussed since these are judged to have relevance as a background to the DC distributed power systems to be studied. First, the classical HVDC link is investigated. Second, the recently introduced VSC based HVDC concept, utilising insulated gate bipolar transistor (IGBT) technology, is discussed.

2.1 HVDC

The principal structure of a classical HVDC transmission link consists of two three-phase thyristor converters connected via an intermediate inductive DC bus. However, in real installations, more complicated converter structures are utilised. Also, shunt reactive compensators and passive filters for suppression of harmonics are used. This is further discussed at the end of this section. Figure 2.1 shows a principal schematic of an HVDC transmission system.

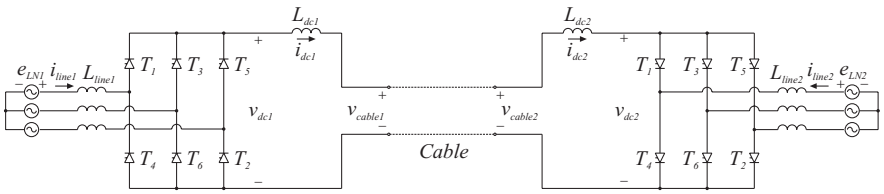

Figure 2.1: Principal schematic of an HVDC power transmission system.

The leftmost converter in Figure 2.1 operates as rectifier and the rightmost as inverter. The average DC bus voltage for control angle α is calculated from

$$V_{dc} = \frac{1}{T/6}\int_{T/6}\hat{e}_{LL}\cos(\omega_1 t)dt = 6\frac{\hat{e}_{LL}}{2\pi}\int_{-\pi/6+\alpha}^{\pi/6+\alpha}\cos(\omega_1 t)d(\omega_1 t) = \frac{3}{\pi}\hat{e}_{LL}\cos(\alpha) = \\ = \frac{3\sqrt{2}}{\pi}E_{LL}\cos(\alpha) = V_{dc0}\cos(\alpha) \tag{2.1}$$

where E_{LL} is the RMS grid voltage and V_{dc0} is the average DC bus voltage in the case of a three-phase diode rectifier. Note that α is defined as the angular displacement from the angle where the corresponding diode rectifier would have experienced a commutation, to the angle where it takes place. For a single-phase diode rectifier this angle coincides with the zero crossing of the phase voltage. For a three-phase rectifier this angle is where two line-to-line voltages e_{LL} intersect.

The rectifier operates at control angles between 0° and 90° and therefore its thyristors are connected so that the power is positive flowing into the DC cable. The inverter operates at control angles between 90° and 180° and therefore its thyristors are connected in such a way that the power is positive flowing out of the DC cable.

Figure 2.2 shows the line-to-line voltages, DC side voltage and control angle for the rectifier and inverter, respectively.

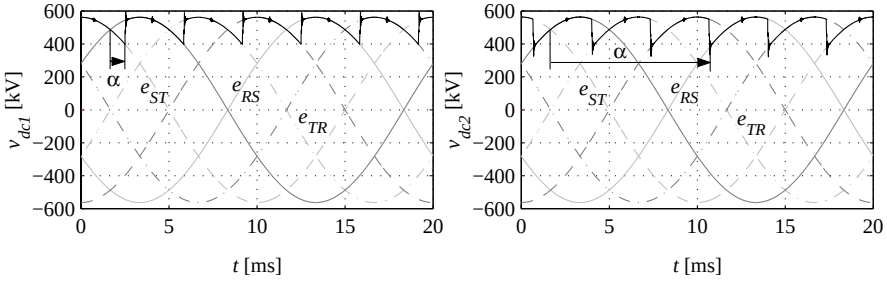

Figure 2.2: Line-to-line voltages, DC side voltage and control angles for the rectifier (*left*) and inverter (*right*) of an HVDC transmission system.

In Figure 2.3 and Figure 2.4, the *R*-phase line current and its spectrum are shown for the rectifier and inverter, respectively.

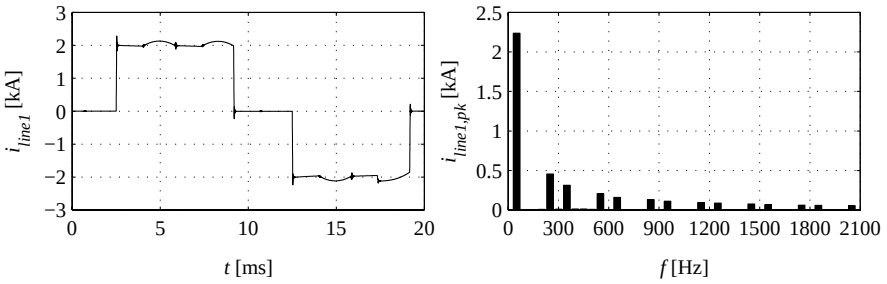

Figure 2.3: *R*-phase line current (*left*) and its spectrum (*right*) for the rectifier of an HVDC transmission system.

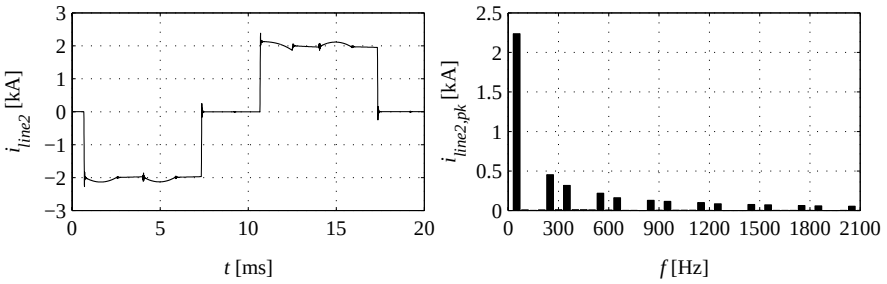

Figure 2.4: *R*-phase line current (*left*) and its spectrum (*right*) for the inverter of an HVDC transmission system.

The only major difference between the line currents in Figure 2.3 and Figure 2.4 is the phase lag of slightly less than 180° for currents flowing out from the AC grids. Consequently, the spectrums for rectifier and inverter operation are similar. The center of the line current pulse is displaced, by an angle equal to the control angle, relative to the line voltage. This means that the line current exhibits a phase lag $\varphi=\alpha$. Therefore, the active P and reactive power Q are

$$\begin{cases} P=\sqrt{3}E_{LL}I_{line,1}\cos(\alpha) \\ Q=\sqrt{3}E_{LL}I_{line,1}\sin(\alpha) \end{cases} \tag{2.2}$$

where E_{LL} and $I_{line,1}$ are the RMS grid voltage and fundamental line current, respectively. Assuming a constant DC side current I_{dc}, the average DC power is given by

$$P=V_{dc}I_{dc}=\frac{3\sqrt{2}}{\pi}E_{LL}I_{dc}\cos(\alpha) \tag{2.3}$$

If the losses are neglected this implies that

$$P=\sqrt{3}E_{LL}I_{line,1}\cos(\alpha)=\frac{3\sqrt{2}}{\pi}E_{LL}I_{dc}\cos(\alpha) \;\Leftrightarrow I_{line,1}=\frac{\sqrt{6}}{\pi}I_{dc} \tag{2.4}$$

The line currents are in principle square for a high DC inductance, $L_{dc1}+L_{dc2}$. For a square line current (60° conduction interval), the harmonics are

$$I_{line,k}=\frac{2\sqrt{2}}{k\pi}I_{dc}\sin\left(\frac{k\pi}{3}\right) \tag{2.5}$$

for k=1,5,7,11,13, etc. This is an important feature of three-phase diode and thyristor rectifiers with inductive DC links.

Classical HVDC utilises an inductive DC bus, as shown in Figure 2.1. Since the overhead lines are also inductive, the commutations take a finite time. This time is termed commutation overlap. Note that the commutation overlap affects the spectrum of a thyristor based current source converter (CSC), since the edges are slightly smoother due to the finite current derivatives. However, the reduction in harmonic content is negligible, at least for low order harmonics. Therefore, it is still a good approximation to assume that the amplitude of the harmonics fall of as $1/k$ where k is the harmonic order.

Practical HVDC installations

Several modifications are made for practical HVDC installations, Figure 2.5, compared to the principal discussed previously.

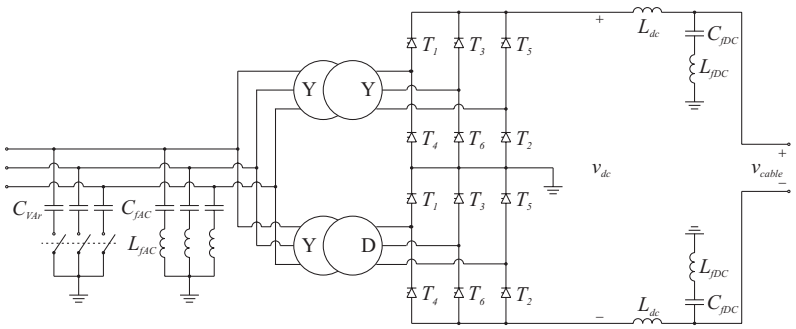

Figure 2.5: Realistic schematic of an HVDC power station.

The main reasons for these modifications are related to the shape of the line currents, shown in Figure 2.3 and Figure 2.4. First, the centers of the current pulses are displaced compared to the centers of the sinusoidal pulses of the line voltages. This corresponds to a phase lag $\varphi=\alpha$ and yields that reactive power is consumed. To circumvent this, switched shunt capacitor banks are installed on the AC line sides of the HVDC transmission. A switched capacitor bank is formed by several capacitors connected to the line through circuit breakers in such a way that the reactive power delivered can be varied in steps. This is required since the reactive power consumed by a thyristor rectifier is

$$Q=\sqrt{3}E_{LL}I_{line,1}\sin(\alpha) \tag{2.6}$$

which means that the reactive power consumed is dependent both on the RMS value of the line current fundamental and the control angle. The second issue regarding the AC line currents relates to their harmonic content. Two methods are used to reduce the harmonics. First, twelve pulse thyristor converter structures are used instead of the basic six-pulse thyristor converter discussed here. A twelve-pulse converter consists of two six-pulse bridges with the DC sides connected in series. The six-pulse bridges are connected to the same AC grid via a three-winding three-phase transformer. One of the thyristor converters is connected to a delta (Δ) winding and the other to a wye (Y) winding. This means that there is a 30° phase shift between the AC voltages feeding the two converters. This implies that there is a 30° phase shift between the currents fed to the converters also. Since the transformer

connected to the converters has a common primary side for both secondary windings, the line current on the primary side will exhibit its lowest harmonic around the 12th harmonic, i.e. the 11th and 13th order harmonics are the lowest appearing. The next pair of current harmonics appearing, are of the 23rd and 25th order. Passive shunt filters tuned to these specific harmonics are also included to further reduce the harmonic content of the AC line currents.

Traditional line-commutated, thyristor based HVDC transmission systems are difficult to build and operate cost-effectively with larger complexity than those two-terminal ones discussed above. The recently introduced VSC based HVDC transmission systems are more feasible to use as multi-terminal systems. By adopting VSCs, the problems associated with reactive power consumption and harmonics production are circumvented to a large extent.

2.2 VSC based HVDC

HVDC Light (trademark of ABB) [19] and HVDC Plus (trademark of Siemens) are basically extensions of the IGBT back-to-back converter, operating at higher power and voltage levels and with an intermediate cable between the converters. Even though this might seem as small step from a development point of view it has resulted in numerous new patents. The main reason is that the development of VSC based HVDC has forced the limits of power electronic converter technology. For example, IGBT valves withstanding more than 100 kV (through series connection) have been developed, light triggered gate or drive circuits have been developed, new cable technologies have emerged and so on. Of course, this introduction cannot provide all the details but instead focuses on the basic operation. Figure 2.6 shows a principal scheme of a VSC based HVDC transmission system.

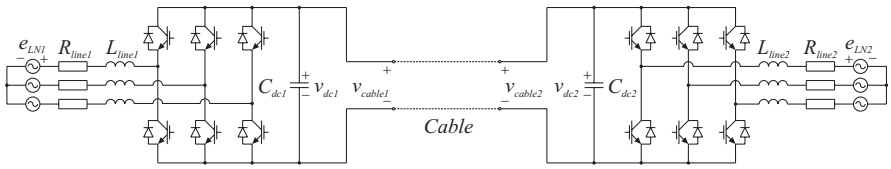

Figure 2.6: Basic VSC HVDC power transmission interconnection.

From Figure 2.6 it is clear that transistor based VSCs are used for this new type of HVDC transmission system. Three-phase VSCs inherently provide the possibility of bidirectional power flow. Both the sending and receiving end converters are current controlled on the AC side, since these sides are

inductive. The current controllers operate in the *dq*-frame as described in Appendix B. The sending end converter is responsible for controlling the DC bus voltage. To enhance the dynamic performance of DC bus voltage control, information on the output power of the receiving end converter should be fed forward to the DC bus voltage controller. The DC bus voltage controller for the converter operated as rectifier is shown in Figure 2.7.

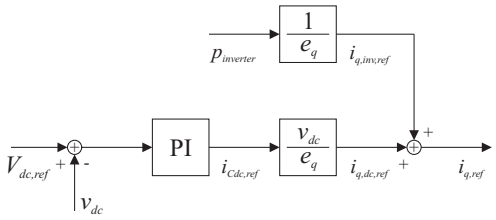

Figure 2.7: DC bus voltage controller for VSC based HVDC.

Figure 2.8 shows a more realistic VSC based HVDC scheme where additional AC side filters are included. This is required due to the fact that both sides of each converter are grounded and still third order injection modulation (Appendix A) is used, resulting in a zero-sequence voltage. To attenuate the current harmonics, shunt filters tuned to switching frequency are inserted between the converter AC side interface and the transformer. Figure 2.8 also shows high frequency filters (100 kHz and above) inserted at the DC side of the converter. These are required to avoid disturbances transmitted from the cable, which could interfere with broadcasting and other radio frequency equipment. Following the high frequency DC side filter, a common mode choke is inserted.

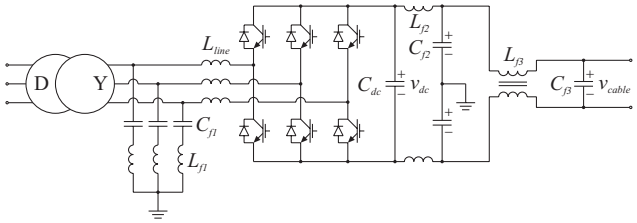

Figure 2.8: Realistic VSC based HVDC converter station.

A VSC based HVDC transmission system consisting of two converters according to Figure 2.8 and a T-model of an HVDC cable (similar to the π-link shown in Figure 3.3) is investigated in simulations. The converters have a rated power of 330 MVA each and the nominal DC cable voltage is 300 kV

(±150 kV). The reactance of the inductive line filters equal 0.14 p.u. and the equivalent time constant of each converter including DC link capacitor is 2 ms. The rated power is the same as the one given in [19] and the other data are typical for an HVDC Light system. For the simulations, the rated line-to-line voltage is set to 150 kV. The shunt filter is tuned to switching frequency (1950 Hz) so that the fundamental current component equals 0.01 p.u., which yields appropriate values for both L_{f1} and C_{f1}. The high frequency filter on the DC side is based on a characteristic frequency of 100 kHz and $C_{f2}=C_{f1}/10$. If the capacitance of C_{f2} is higher, it will affect the characteristic frequency of the shunt harmonic filter. The mutual inductance of the common mode choke is set to the same value as L_{f2} and the magnetic coupling factor is set to 0.99. The capacitance of C_{f3} is set to $C_{f3}=2\cdot C_{f2}$. These component values most likely defer from the ones intended for the real installation. Also the DC bus voltage controller and the converter current controllers are not equal to the ones used in the real installation. Probably the current controllers used here have higher gain than the ones in the real installation.

Figure 2.9 and Figure 2.10 show the converter power and DC bus voltage, respectively, for a time-domain simulation starting at no-load. The inverter receives an output power command equal to 165 MW (half rated power) at time t=20.0 ms. The current controller becomes aware of the increased power reference at time 20.25 ms, and calculates the desired AC side voltage reference which is applied one sample later, at time 20.5 ms. The current immediately starts to increase, but this is not noticed by the current controller before the next sample instant, at 20.75 ms. At this time, the current controller of the inverter sends a power reference to the converter acting as a rectifier, which increases its power demand. Due to the time required to establish a rectifier input power corresponding to the inverter output power, the DC bus voltage is somewhat reduced, see Figure 2.10.

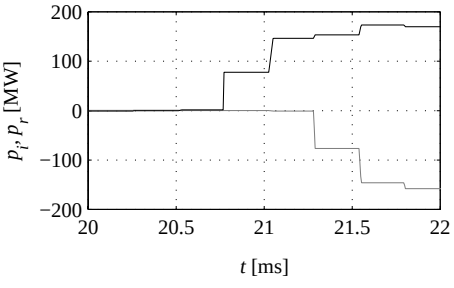

Figure 2.9: Inverter AC side power (*black*) and rectifier AC side power (*grey*).

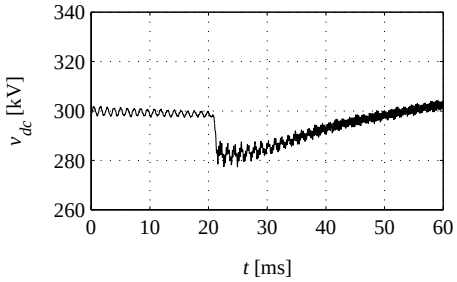

Figure 2.10: Rectifier DC side voltage.

Figure 2.11 shows the line and converter currents for both the rectifier and inverter. It is seen that the currents contain a rather high ripple, originating from switching. Especially, the converter currents exhibit a high ripple at the power increase. These ripple currents are mainly zero-sequence switching frequency components. The ripple is not so pronounced in the line currents, due to the shunt harmonic filter. The high gain of the current controllers makes this problem worse. Figure 2.12 shows the stationary line and converter currents for the inverter, together with the corresponding harmonic spectrums in the vicinity of switching frequency. The shunt filter tuned to switching frequency attenuates this component effectively.

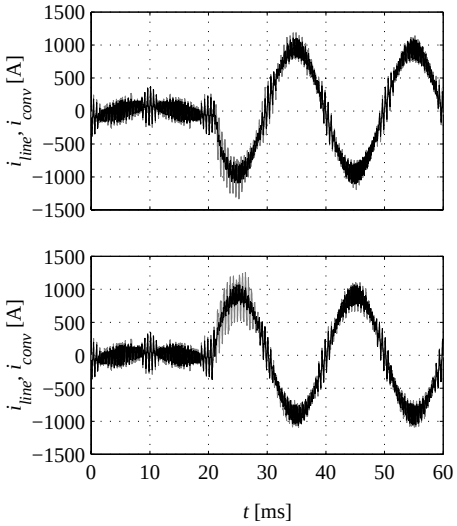

Figure 2.11: Line current (*black*) and converter current (*grey*) for the rectifier (*top*) and inverter (*bottom*) for a load power increase. The currents are positive flowing into the AC grids.

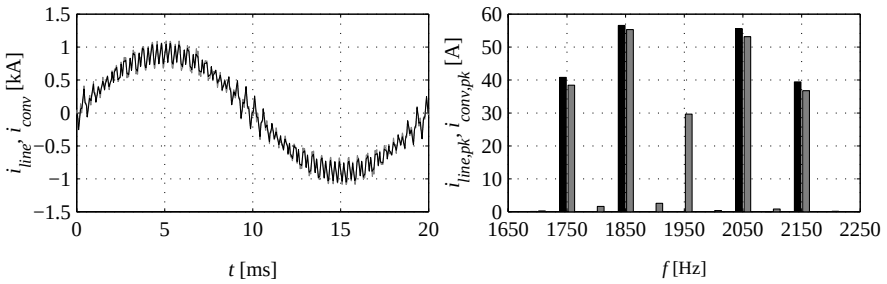

Figure 2.12: Line current (*black*) and converter current (*grey*) for the inverter (*left*) and line current spectrum (*black*) and converter current spectrum (*grey*) for the inverter at frequencies close to switching frequency (*right*).

In practical HVDC Light installations, resistors are connected in parallel to the inductors of the shunt filter. As a consequence, harmonics in a broader frequency spectrum are attenuated. Therefore, the harmonics around switching frequency in Figure 2.12 are attenuated more effectively in a real installation.

Feed forward of the output power of the inverter for DC bus voltage control is not used in real installations. Due to the low equivalent time constant of the converters, only low rate of change of the inverter output power is allowed.

The HVDC Light installations of comparably low rating, approximately 50 MW, are based on two-level converter technology (Figure 2.8). To achieve higher power ratings (300 MW), three-level VSCs are utilised [19].

Self-commutated two-level converters of the same type as used in the study of VSC based HVDC form, thus, a basis for the investigated multi-terminal DC distribution system. Some experience could also be found from industry and traction as mentioned in the introduction to this chapter.

Chapter 3

DC bus voltage control

Two different DC bus voltage control schemes are investigated. One of the methods, referred to as the communication or master/slave method, strongly relies on fast communication between the source and load converters. The output power, with sign, is calculated for each of the converters. Information on total output power is fed forward to the converters. One of the converters, the master, is responsible for controlling the DC bus voltage. Feed forward of the total output power allows for high bandwidth DC bus voltage control. The DC bus voltage controller is, however, still required during transients and to compensate for losses in the DC power system. Due to the resistive voltage drop, a proportional-integral (PI) controller is adopted in order to avoid stationary DC bus voltage error.

The other method is referred to as voltage droop control. Droop control does not require any communication at all between the converters. Instead, the DC bus voltage is measured at the source converter terminals. All the source converters contribute to balance the total power consumed by the loads and the losses of the DC power system. In common voltage droop control, the DC bus voltage decreases linearly as the output power for the converter increases, in order to give stable operation. This, of course, yields a stationary error in the DC bus voltage. Therefore, a restoration process to reduce the stationary DC bus voltage error is also discussed.

The chapter begins with an overview of the investigated system. Then the DC bus model used for the analysis is introduced. The controller structures are investigated and appropriate controller parameters are derived. The dynamic properties in the case of droop control are investigated. Last, the investigated DC bus voltage control schemes are compared in terms of load sharing.

3.1 Investigated system

The investigated DC distribution network model consists of five converters: three are operated as sources and two are feeding power to loads. The converters are connected to galvanically separated AC power sources or loads. The sources and loads are modeled as three-phase grids. The grids are galvanically separated, i.e. without common reference, to avoid a low-impedance path for the zero-sequence and third order harmonic currents [72].

To investigate the transient response of the DC bus voltage controllers, the power references for the power fed to the loads are changed in steps. Therefore, the dynamics of the generators, wind turbines, etc. might interfere with the dynamics of the voltage control. This is further discussed in Chapter 4, where a distributed system operated only with wind power is investigated. Figure 3.1 shows a five-converter DC power system configuration, representative for the power systems considered in the analysis.

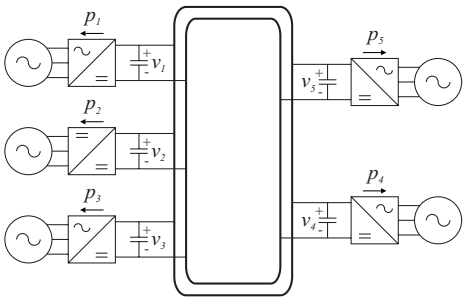

Figure 3.1: The investigated DC power system configuration.

Each converter has a front interface with an inductive connection to the source. Therefore, the end interface connected to the DC bus is capacitive. Consequently, the front side of the converter is current controlled and the end side is voltage controlled. In Figure 3.2, the i^{th} converter sub-system of the five included in the DC network is shown.

From Figure 3.2 it is clear that the considered converters are self-commutated, three-phase full-bridges. The DC bus capacitor is used to partly decouple the AC and DC systems so that a disturbance on one side is not reflected on the other side of the converter. A similar system is investigated in [66] but instead of transistor equipped VSCs, thyristor based CSCs are considered.

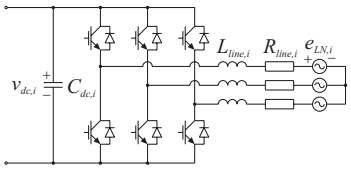

Figure 3.2: The converter forming the interface between the DC bus and the i^{th} three-phase AC network, source or load.

3.2 DC bus model

There are two DC bus models discussed in this chapter. The DC bus voltage controllers are designed based on the assumption that the DC bus is purely capacitive. Therefore, a purely capacitive DC bus, with capacitance equal to the total converter DC bus capacitance, is analysed first. Then, a more accurate DC bus network with the cable segments modeled as resistive, inductive and capacitive π-links, according to Figure 3.3, is analysed.

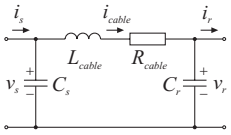

Figure 3.3: The two-converter DC bus π-link model.

In the investigation of dynamic properties, C_s and C_r in Figure 3.3 denote the total bus capacitance, i.e. cable and converter DC bus capacitance, for the sending and receiving ends, respectively. The cable capacitance is split in two equal parts, which are then added to the DC bus capacitances to give the total sending and receiving end capacitances. In the investigation on load sharing, the cable and DC bus capacitances are modeled separately.

Large-signal stability in the case of distributed converters supplying constant power loads is investigated in [2]. The result is an input *LC*-filter specification for the load converters, based on the maximum output power for the load converters and the total source converter output resistance. An equilibrium point criterion is used to formulate an upper limit for the source converter output resistance, which results in an intuitively understandable criterion stating that: *The equivalent load resistance must be higher than the source converter output resistance.* Mathematically, this is expressed as [2]

$$R_{cable} < \frac{v_r^2}{4P_r} \tag{3.1}$$

with notations according to Figure 3.3. The load or receiving end power is denoted P_r. A lower bound for the source output resistance is also given in [2]. For a single output converter with a constant power load, the lower bound in the case of an ideal source is given by

$$R_{cable} > \sqrt{\frac{L_{cable}}{C_r}} \tag{3.2}$$

Modifications made to the latter expression to include the case with several constant power load converters are shown in [2]. However, the derived expressions are based on the assumption that the resistance R_{cable} is common for all the paralleled converters. In a distributed power system this is not likely. The resistance is instead distributed along the cables. Furthermore, the inductance is also a property of the cables and not inserted on purpose for filtering action. Here, only capacitors are inserted as voltage stabilisers and filters, close to both source and load converters. The stability problem therefore merely becomes a problem of selecting converter DC bus capacitors.

3.3 Controller structure

Several different DC bus voltage control schemes exist [52], of which especially two seem commonly used: master/slave and droop control. In master/slave control, active load sharing is performed and the master controller distributes power references to the other converter controllers operated as sources, e.g. the slave converters. In droop control, each source converter delivers power to the DC bus determined by the actual DC bus voltage error at the converter. Therefore, droop control does not require any communication.

Even though master/slave and droop DC bus voltage controllers operate in a different manner, the controller structures are essentially equal, which is apparent from [49]. The main difference is that in master/slave DC bus control the actual output power of the slave and load converters is also fed forward to the master, which in turn generates power references for the slave converters acting as sources. Since communication is used for the master/slave scheme, the bandwidth of the DC bus voltage control can be increased if the

communication bandwidth is sufficiently high. Thus, less energy needs to be stored in the DC bus, which implies that the DC bus capacitance can be decreased [49]. However, the system becomes more prone to interactions between the two sides of the converters when the energy storage is reduced [6]. In [73], grid interactions are handled by an active power line conditioner connected to the DC bus. This means that the DC bus capacitance can be kept low and, still, undesired interaction between the converter sides is attenuated.

DC bus voltage droop control

In common voltage droop control, the bus voltage decreases linearly as the output current, or in some cases power, for the converter increases, in order to give stable operation (Figure 3.4). This, of course, results in a stationary error in the voltage level.

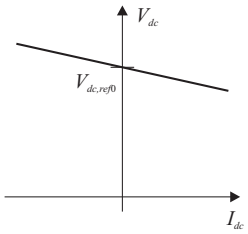

Figure 3.4: Steady state droop characteristic.

The controller structure for DC bus voltage control is shown in Figure 3.5. A proportional (P) controller is used for the droop scheme, similar to the PI-controller derived in [6] for back-to-back converter DC link voltage control. This controller structure is implemented in all converters, intended for power flow into the DC bus. The reason for this is to be able to distribute the total load between the sources when droop control is used. Note that several converters are used to support the power flow, which is not evident from Figure 3.5.

To simplify the investigation, a simple system with only one source and one load converter is considered. This is extended to cover the case with several source and load converters. The measured DC bus voltage is low-pass filtered (Figure 3.5) to attenuate interactions between the negative-sequence current of the AC side and the DC bus voltage control discussed in [67], and to facilitate controller pole-placement design [6].

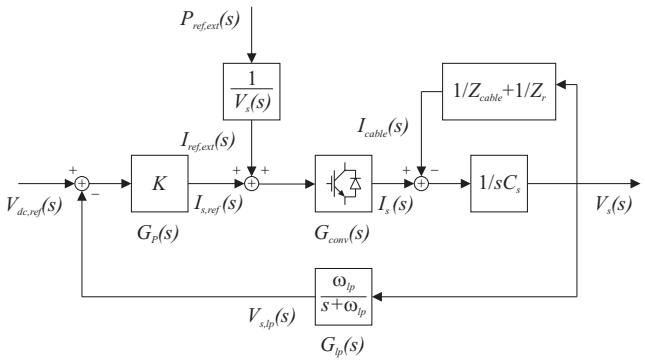

Figure 3.5: Structure of the DC bus voltage droop controller. The source converter current is denoted I_s and the cable current I_{cable}.

The DC bus voltage controller for the droop scheme is written

$$i_{s,ref} = K\left(V_{dc,ref} - v_{s,lp}\right) \tag{3.3}$$

In the case of a purely capacitive DC distribution system, i.e. when L_{cable}=0 H, R_{cable}=0 Ω and $C_{dc}=C_r+C_s$ (Figure 3.3), the closed loop transfer function from DC bus voltage reference to actual voltage is written

$$G_{cl}(s)=\frac{\left(K/C_{dc}\right)\left(s+\omega_{lp}\right)}{s^2+\omega_{lp}s+\omega_{lp}\left(K/C_{dc}\right)} \tag{3.4}$$

The effects of non-zero cable impedance are shown in the next section, where dynamic properties are examined. In the case of a purely capacitive DC distribution system, the current at the receiving end is expressed as

$$i_r = i_s - i_{Cdc} \tag{3.5}$$

which in the case of a single source gives a droop function according to

$$V_s(s)=\frac{\left(K/C_{dc}\right)\left(s+\omega_{lp}\right)}{s^2+\omega_{lp}s+\omega_{lp}\left(K/C_{dc}\right)}V_{dc,ref}(s)-\frac{\left(1/C_{dc}\right)\left(s+\omega_{lp}\right)}{s^2+\omega_{lp}s+\omega_{lp}\left(K/C_{dc}\right)}I_r(s) \tag{3.6}$$

The steady state droop impedance or resistance is, thus, written

$$R_{droop}=\frac{1}{K} \tag{3.7}$$

The characteristic polynomial of the closed loop transfer function is given by

$$p(s) = s^2 + \omega_{lp} s + \omega_{lp}\left(K/C_{dc}\right) \tag{3.8}$$

The desired characteristic polynomial can be expressed as

$$p(s) = s^2 + 2\zeta_n \omega_n s + \omega_n^2 \tag{3.9}$$

and is fulfilled for

$$K = \frac{1}{(2\zeta_n)^2}\omega_{lp} C_{dc} \tag{3.10}$$

The closed loop bandwidth is given by

$$\omega_n = \frac{1}{2\zeta_n}\omega_{lp} \tag{3.11}$$

It is apparent that a high damping of the poles of the closed loop transfer function requires a high DC distribution bus capacitance. Here, the poles are chosen to obtain a performance corresponding to the one of a Butterworth filter, which means that the damping is selected as

$$\zeta_n = \frac{1}{\sqrt{2}} \tag{3.12}$$

This choice of damping requires a rather moderate DC distribution bus capacitance without making the system oscillatory. The last point is important since the DC distribution bus is not purely capacitive. This implies that it is not advisory to make the simplified system oscillatory and then introduce non-idealities into the system.

From the equations above, the gain is expressed as

$$K = \frac{1}{2}\omega_{lp} C_{dc} \tag{3.13}$$

Assume that each converter corresponds to a virtual resistance, with a base value equal to

$$R_n = \frac{V_{dc,ref}^2}{P_n} \tag{3.14}$$

In the case of droop control, the DC current at rated load for rectifier operation increases due to the decreased DC bus voltage caused by the droop characteristic

$$I'_{dc,n} = \frac{P_n}{V_{dc,ref}(1-\delta_n)} = \frac{I_{dc,n}}{(1-\delta_n)} \tag{3.15}$$

where δ_n is the relative converter output voltage droop at rated power. Since the voltage droop corresponds to the gain, it is found that

$$R_{droop} = \frac{1}{K} = \frac{(2\zeta_n)^2}{\omega_{lp} C_{dc}} = \frac{V_{dc,ref}\delta_n}{\frac{I_{dc,n}}{(1-\delta_n)}} = R_n(1-\delta_n)\delta_n \tag{3.16}$$

This is rewritten to

$$(1-\delta_n)\delta_n = \frac{(2\zeta_n)^2}{\omega_{lp}} \cdot \frac{1}{R_n C_{dc}} = \frac{(2\zeta_n)^2}{\omega_{lp}} \cdot \frac{1}{\tau_{n,system}} \tag{3.17}$$

where $\tau_{n,system}$ is the time constant of the system. Now, it is assumed that only half the DC bus capacitance required is located at the source converter. The other half is located at the receiver or load converter. This means that

$$C_s = C_r = C_{dc,converter} = \frac{C_{dc}}{2} \tag{3.18}$$

and the converter time constant is

$$\tau_{n,converter} = R_n C_{dc,converter} = \frac{R_n C_{dc}}{2} = \frac{\tau_{n,system}}{2} \tag{3.19}$$

This gives the following specification for each converter, both source and load

$$\tau_{n,converter} = \frac{2\zeta_n^2}{\omega_{lp}} \cdot \frac{1}{(1-\delta_n)\delta_n} \tag{3.20}$$

This implies that all converters connected to the DC distribution system should be equipped with DC bus capacitors selected according to

$$C_{dc,converter} = \frac{P_n}{V_{dc,ref}^2} \cdot \frac{2\zeta_n^2}{\omega_{lp}} \cdot \frac{1}{(1-\delta_n)\delta_n} \tag{3.21}$$

Note that for a multi-converter system all the source converters should have the same stationary characteristic to obtain proper, i.e. democratic, load sharing. If the DC side capacitor of each converter is selected according to the expression above, this is fulfilled. Furthermore, for an ideal cable, i.e. without any impedance other than the DC side capacitors, the system transfer function is the same as for the two-converter system when the total rated power of the sources equal the one of the loads. For converters with the following data

$$\begin{cases} V_{dc,ref} = 750 \text{ V} \\ \omega_{lp} = 2\pi 30 \text{ rad/s} \approx 188 \text{ rad/s} \\ \zeta_n = 1/\sqrt{2} \\ \delta_n = 0.05 \end{cases} \tag{3.22}$$

it is found that each converter, source and load, should have a DC side capacitance to rated power ratio given by

$$\frac{C_{dc,converter}}{P_{n,converter}} = 199 \,\mu\text{F/kW} \tag{3.23}$$

Note that the rated power is given for inverter operation at a DC link voltage equal to $V_{dc,ref}$. According to [4], the converter losses decrease for rectifier operation compared to inverter operation (Appendix C). This implies that the maximum allowable rectifier power is higher than the maximum inverter power based on the assumption that the converter losses are equal in the two cases. It is shown in a later section that for the IGBT module Semikron SKM300GB123D, the rectifier power resulting in the same amount of converter losses as inverter operation at rated load, is around 17% higher for droop control than the rated power for inverter operation. The higher rated power at rectifier operation is used to compensate for DC bus losses.

The DC bus capacitance required for each converter by applying this method is higher compared to what has been reported in other work on the same topic [67]. Therefore, the converter proposed here is more bulky. However, the DC

link capacitance for each converter is lower than twice the one of a regular three-phase converter, e.g. for motor drive applications. Furthermore, the magnitude of the DC bus voltage oscillations observed for an unbalanced AC load [67] is inversely proportional to the DC bus capacitance [6]. The oscillation appears at twice the fundamental frequency of the unbalanced AC network [6][67], which means that introducing a low-pass filter with break-over frequency lower than the oscillation frequency effectively attenuates the problem. For the 75 kW DUAL battery charger [5], a DC bus variation of 5% of the rated DC link voltage of 750 V is allowed in the specification. This requires a DC link capacitance of 2.45 mF, according to Appendix D. The sinusoidal 100 Hz component has an amplitude of 58 A (41 A RMS). Furthermore, two 450 V capacitors has to be connected in series, which implies that DC link capacitors of 4.7 mF should be sufficient. However, the RIFA PEH 4.7 mF capacitors only sustain between 13.5 and 15.9 A RMS at 100 Hz. Therefore, at least three such branches are required to avoid thermal overloading of the capacitors, which corresponds to 7.05 mF. In the implemented DUAL battery chargers, five such branches are used to provide margin to the absolute maximum temperature, which yields a total DC link capacitance of 11.75 mF. This should be compared to the 15 mF required for a 75 kW DC distribution converter according to the selection method proposed here.

DC bus voltage control with droop error restoration

There have been attempts to include error restoration in droop control [7]. This could be done by, for example, using DC bus voltage PI-control instead of the P-controller shown in Figure 3.5. If a PI-controller is adopted in the scheme in Figure 3.5, the closed loop transfer function from DC bus voltage reference to actual voltage for each converter operated as a source, i.e. supporting the DC bus voltage, is written

$$G_{cl}(s)=\frac{\frac{K}{T_i C_{dc}}(sT_i+1)(s+\omega_{lp})}{s^3+\omega_{lp}s^2+\frac{K\omega_{lp}}{C_{dc}}s+\frac{K\omega_{lp}}{T_i C_{dc}}} \tag{3.24}$$

where T_i is the time constant of the integral part. The controller parameters are selected in a similar way as for the regular droop scheme to compare the controller action. Therefore, the closed loop transfer function should have a characteristic polynomial given by

$$p(s)=s^3+\omega_{lp}s^2+\frac{K\omega_{lp}}{C_{dc}}s+\frac{K\omega_{lp}}{T_iC_{dc}}=\left(s^2+2\zeta_n\omega_n s+\omega_n^2\right)(s+\omega_n) \tag{3.25}$$

This gives the following controller parameters

$$\begin{cases}\omega_n=\dfrac{1}{1+2\zeta_n}\omega_{lp}\\ K=\dfrac{1}{1+2\zeta_n}C_{dc}\omega_{lp}\\ T_i=\dfrac{(1+2\zeta_n)^2}{\omega_{lp}}\end{cases} \tag{3.26}$$

For poles located according to a corresponding third order Butterworth filter, a relative damping

$$\zeta_n=1/2 \tag{3.27}$$

is required. This gives the following controller parameters

$$\begin{cases}\omega_n=\dfrac{1}{2}\omega_{lp}\\ K=\dfrac{1}{2}C_{dc}\omega_{lp}\\ T_i=\dfrac{4}{\omega_{lp}}\end{cases} \tag{3.28}$$

Note that the gain is the same as for the P-controller used for regular droop control. Thus, the same controller can be used in both cases and the only difference is whether the integral part should be added or not. For PI-control, the source converter output voltage is written

$$\begin{aligned}V_s(s)=&\frac{(K/C_{dc})(s+\omega_{lp})(s+(1/T_i))}{s^3+\omega_{lp}s^2+(K/C_{dc})\omega_{lp}s+\left(K\omega_{lp}/C_{dc}T_i\right)}\cdot V_{dc,ref}(s)-\\ &-\frac{(1/C_{dc})s(s+\omega_{lp})}{s^3+\omega_{lp}s^2+(K/C_{dc})\omega_{lp}s+\left(K\omega_{lp}/C_{dc}T_i\right)}\cdot I_r(s)\end{aligned} \tag{3.29}$$

Note that the steady state source impedance is equal to zero, which is the main advantage gained by the use of PI-control. One major drawback exists with decentralised PI DC bus voltage control, resulting from the fact that several sources equipped with integral parts control the same quantity, the DC bus voltage. In automatic control terms this results in that both observability and controllability are lost [80]. This implies that any non-ideal feature of the DC distribution network, for example the bus resistance, will force the sources to exhibit poor load sharing.

One way of partly circumvent this problem is to inhibit updating of the controller integral part when the DC bus voltage at the particular source is inside a specified dead-band [7]. The dead-band ought to be proportional to the voltage drop along the DC bus between the source converter in question and a predetermined point in the DC network common to all source converters. Also the transient behaviour is affected by the DC bus impedance and since an integrator corresponds to a dynamical state, the imbalance during the transients remains in stationary conditions. This is partly solved by applying a load dependent integral time constant, so that a converter connected to a source with high relative loading will have a weak integral part. Consequently, it is only updated to a limited extent for a new load situation. This has been successfully utilised for wind power farms operating directly on the three-phase AC grid [7]. Simulations of a DC distributed power system with source converters with integral parts given by

$$T_i = \frac{4}{\omega_{lp}}\left(1 - \frac{P}{2P_n}\right) \tag{3.30}$$

are shown in the section on load sharing. Note that the power is considered as positive flowing out of the converter AC side. Therefore, the time constant above increases the more power the source delivers to the DC system.

Master/slave DC bus voltage control

In the master/slave DC bus voltage control scheme investigated here, only the master is responsible for voltage control. The voltage controller for the master converter is shown in Figure 3.6. Information on actual power for all the other converters is fed forward to the master, where appropriate power references for the slaves, i.e. the other converters operated as sources, are calculated. Even if not used here, the voltage controller output could be included in the slave power references.

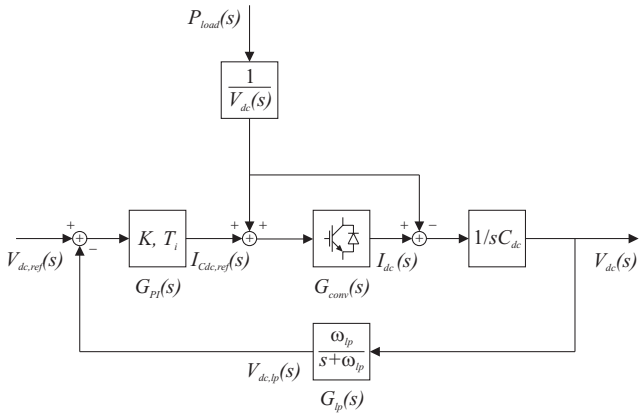

Figure 3.6: Structure of the master/slave DC bus voltage controller. The source converter current is denoted I_{dc}.

In Figure 3.6, a PI-controller is adopted for master/slave DC bus voltage control. The closed loop transfer function from DC bus voltage reference to actual voltage is equal to the one for droop control with voltage error restoration, i.e.

$$G_{cl}(s)=\frac{\frac{K}{T_i C_{dc}}(sT_i+1)(s+\omega_{lp})}{s^3+\omega_{lp}s^2+\frac{K\omega_{lp}}{C_{dc}}s+\frac{K\omega_{lp}}{T_i C_{dc}}} \tag{3.31}$$

Note that for this master/slave scheme, only one converter serves to control the DC bus voltage. Still, several converters are used to support the power flow but their power reference is provided by the over-lying controller structure. The load power fed forward in Figure 3.6 is, thus, the sum of the output power of all the other converters in the DC system.

Also for master/slave DC bus voltage control, the closed loop transfer function has poles located as a corresponding third order Butterworth filter, to obtain similar dynamic properties. Consequently, the controller parameters are given by (3.28) for the master/slave scheme. However, note that the gain is based on the total DC bus capacitance in the case of master/slave control. For droop control, the gain is calculated based on $C_{dc}=2\cdot C_{dc,converter}$ for each source converter. For master/slave control, the source converter output voltage is written

$$V_{dc}(s)=\frac{(\omega_{lp}/2)(s+\omega_{lp})(s+(\omega_{lp}/4))}{(s^2+(\omega_{lp}/2)s+(\omega_{lp}/2)^2)(s+(\omega_{lp}/2))}\cdot V_{dc,ref}(s) \qquad (3.32)$$

if the power fed forward is accurate and the DC bus is purely capacitive.

3.4 Cable impedance

In this section the effect of cable impedance on voltage droop control is studied. The investigation focuses on regular droop control, i.e. without voltage error restoration.

Steady state characteristics

For simplicity, assume a network consisting of only one source and one load, operating in steady state. The latter assumption implies that the network can be regarded as purely resistive and that only the steady state droop characteristic has to be considered, see Figure 3.7.

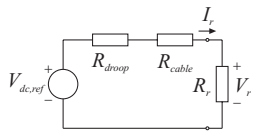

Figure 3.7: The simplified Thevenin equivalent for steady state analysis.

The current supplied to the load, with reference to Figure 3.7, is written

$$I_r=\frac{V_{dc,ref}-V_r}{R_{droop}+R_{cable}}=\frac{P_r}{V_r} \qquad (3.33)$$

This is rewritten to form a second order algebraic equation

$$V_r^2-V_{dc,ref}V_r+(R_{droop}+R_{cable})P_r=0 \qquad (3.34)$$

If this is expressed in one common p.u. system, e.g. the one of the source, it is found that

$$(1-\delta_r)^2-(1-\delta_r)+((1-\delta_n)\delta_n+r_{cable})p_r=0 \qquad (3.35)$$

where (1-δ_r) and p_r are the p.u. receiving end voltage and power, respectively. The p.u. cable resistance is denoted r_{cable}. The p.u. base is given in Appendix D. The stable solution to this equation is written

$$\delta_r = \frac{1}{2} - \sqrt{\frac{1}{4} - \left((1-\delta_n)\delta_n + r_{cable}\right)p_r} \tag{3.36}$$

Since the resistors form a voltage-dividing network, the source voltage is

$$V_s = V_{dc,ref} - \frac{R_{droop}}{R_{droop} + R_{cable}} \cdot \left(V_{dc,ref} - V_r\right) \tag{3.37}$$

The relative voltage reduction at the sending end is thus

$$\begin{aligned} \delta_s &= \frac{(1-\delta_n)\delta_n}{(1-\delta_n)\delta_n + r_{cable}}\delta_r = \\ &= \frac{(1-\delta_n)\delta_n}{(1-\delta_n)\delta_n + r_{cable}} \cdot \left(\frac{1}{2} - \sqrt{\frac{1}{4} - \left((1-\delta_n)\delta_n + r_{cable}\right)p_r} \right) \end{aligned} \tag{3.38}$$

The risk of encountering converter over-modulation due to a too low DC bus voltage is the main reason for investigating the DC bus voltages at different points in the network. The minimum DC link voltage is determined from the required load voltage at the converter output terminals, including the voltage drop across the output filter. For a three-phase AC load expressed in rotating reference *dq*-coordinates (Appendix A, Appendix B), the stationary converter output voltage is written

$$\begin{cases} u_d = R_{line} i_d - \omega_1 L_{line} i_q + e_d = R_{line} \dfrac{Q}{e_q} - \omega_1 L_{line} \dfrac{P}{e_q} \\ u_q = R_{line} i_q + \omega_1 L_{line} i_d + e_q = R_{line} \dfrac{P}{e_q} + \omega_1 L_{line} \dfrac{Q}{e_q} + e_q \end{cases} \tag{3.39}$$

In the expression above, P and Q denote active and reactive power, positive flowing from the converter into the AC system. The AC grid angular frequency is denoted $\omega_1 = 2\pi f_1$ and the voltage vector $\vec{e}^{\,dq} = e_d + j e_q$. According to Appendix A, $e_d = 0$. The AC line filter inductance and resistance are denoted L_{line} and R_{line} (Figure 3.2). The output voltage and current of the

converter are denoted, $\vec{u}^{dq} = u_d + ju_q$ and $\vec{i}^{dq} = i_d + ji_q$, respectively. Neglecting the resistive voltage drop gives

$$\begin{cases} u_d \approx -\omega_1 L_{line} i_q = -\omega_1 L_{line} \dfrac{P}{e_q} \\ u_q \approx \omega_1 L_{line} i_d + e_q = \omega_1 L_{line} \dfrac{Q}{e_q} + e_q \end{cases} \tag{3.40}$$

The converter output voltage magnitude is given by

$$\left|\vec{u}\right|^2 = \left|u_d + ju_q\right|^2 \approx \left(\omega_1 L_{line} \frac{P}{e_q} \right)^2 + \left(\omega_1 L_{line} \frac{Q}{e_q} + e_q \right)^2 \tag{3.41}$$

If this is expressed in line-to-neutral RMS voltages, it is found that

$$U^2 \approx \left(\omega_1 L_{line} \frac{P/3}{E_{LN}} \right)^2 + \left(\omega_1 L_{line} \frac{Q/3}{E_{LN}} + E_{LN} \right)^2 \tag{3.42}$$

The maximum allowable RMS line-to-neutral voltage to avoid over-modulation in stationary operation is given by

$$U_{max} = \frac{V_{dc}}{\sqrt{6}} \tag{3.43}$$

for symmetrical voltage references, i.e. when space vector pulse width modulation (SVPWM) [35] is used, see Appendix A. If it is assumed that the reactive power Q equals zero, the limiting case is written

$$\frac{V_{dc}^2}{6} = \left(\omega_1 L_{line} \frac{P/3}{E_{LN}} \right)^2 + E_{LN}^2 \tag{3.44}$$

which is valid when the converter is operating as inverter as well as for rectifier operation. Thus, for the receiving end converter (index r) of the DC network the limiting case is

$$\frac{V_r^2}{6} = \left(\omega_{1,r} L_{line,r} \frac{P_r/3}{E_{LN,r}} \right)^2 + E_{LN,r}^2 \tag{3.45}$$

Consequently, the receiving end DC bus voltage in p.u. is given by

$$(1-\delta_r) \geq \sqrt{2} \cdot \sqrt{\left(\frac{x_{line,r}}{e_{LL,r}} p_r \right)^2 + e_{LL,r}^2} \tag{3.46}$$

where $e_{LL,r}$ and $x_{line,r}$ are p.u. values of the line-to-line voltage and line reactance of the receiving end, respectively. The p.u. base is given in Appendix D. Rearranging the terms yields

$$\delta_r \leq 1-\sqrt{2} \cdot \sqrt{\left(\frac{x_{line,r}}{e_{LL,r}} p_r \right)^2 + e_{LL,r}^2} \tag{3.47}$$

Rearranging (3.36) gives the cable resistance

$$r_{cable} = \frac{1}{p_r}\left(\frac{1}{4} - \left(\frac{1}{2} - \delta_r \right)^2 \right) - (1-\delta_n)\delta_n \tag{3.48}$$

The maximum cable resistance allowed, is found from combining the last two expressions

$$r_{cable} \leq \frac{1}{p_r}\left(\frac{1}{4} - \left(\sqrt{2} \cdot \sqrt{\left(\frac{x_{line,r}}{e_{LL,r}} p_r \right)^2 + e_{LL,r}^2} - \frac{1}{2} \right)^2 \right) - (1-\delta_n)\delta_n \tag{3.49}$$

The p.u. line reactance used in [6] is approximately equal to

$$x_{line} = 0.0838 \tag{3.50}$$

which is required to fulfil the standard IEC 1000-3-2, if E_{LN}=230 V and $V_{dc,ref}$=750 V at a switching frequency of 4.95 kHz. Assuming operation at rated power, i.e. p_r=1, gives

$$\delta_r \leq 0.214 \tag{3.51}$$

and the maximum allowable cable resistance in p.u.

$$r_{cable} \leq 0.120 \tag{3.52}$$

Furthermore, this corresponds to a source voltage given by the droop

$$\delta_s = \frac{(1-\delta_n)\delta_n}{(1-\delta_n)\delta_n + r_{cable}}\delta_r = 0.06 \tag{3.53}$$

This means that the p.u. power supplied from the source equals

$$p_s = \frac{(1-\delta_s)\delta_s}{(1-\delta_n)\delta_n} = 1.196 \tag{3.54}$$

which implies that the 17% higher rated power possible at rectifier operation for the same amount of losses as for rated inverter operation is not sufficient. On the other hand, a DC network design without margins to avoid over-modulation, is not likely. Also, cable losses approximately equal to 0.2 p.u. seems high. The p.u. droop characteristic for a three-phase converter based on Semikron SKM300GB123D modules, including over-modulation and loss limits, is shown as a function of current in Figure 3.8 and of power in Figure 3.9.

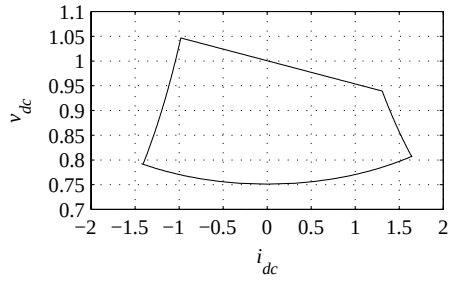

Figure 3.8: Per unit *iv* droop characteristic, including over-modulation and loss limits.

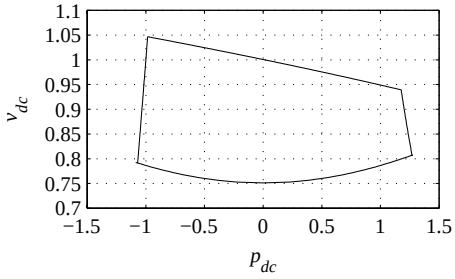

Figure 3.9: Per unit *pv* droop characteristic, including over-modulation and loss limits.

Figure 3.8 and Figure 3.9 are based on the following converter data: S_n=75 kW, $V_{dc,ref}$=750 V, E_{LN}=230 V, 50 Hz and L_{line}=2 mH, according to (3.50). Furthermore, the converter operates in such a way that unity power factor is obtained for the AC network. The loss limits are calculated from the method given in Appendix C and the over-modulation limit is calculated from (3.44).

From Figure 3.9, the increased power handling capability for rectifier operation at a semiconductor loss level equal to the rated appears to be close to 17%, as previously mentioned.

Dynamic properties

An impedance specification for individual loads of DC distribution systems, based on the small-signal stability criterion, is presented in [21]. Here, stability is studied in terms of location of the closed loop poles and the root-locus [51] as a function of the cable parameters. Therefore, the cables are from now on modeled as resistive and inductive, with the cable capacitance neglected or lumped with the converter DC side capacitance, i.e. with

$$Z_{cable} = sL_{cable} + R_{cable} = R_{cable} \cdot (s\tau_{cable} + 1) \tag{3.55}$$

The equivalent impedance of the receiving end is expressed as

$$Z_r = \frac{R_r}{sR_rC_r + 1} = \frac{R_r}{s\tau_r + 1} \tag{3.56}$$

The impedance seen from the source converter (including its DC side capacitor) is written

$$Z = Z_{cable} + Z_r = R_{cable} \cdot (s\tau_{cable} + 1) + \frac{R_r}{s\tau_r + 1} \tag{3.57}$$

Here, the cable and the equivalent receiving end resistances are expressed as

$$\begin{cases} R_{cable} = r_{cable} R_n \\ R_r = \dfrac{V_r^2}{P_r} = \dfrac{(1-\delta_r)^2}{p_r} \cdot \dfrac{V_{dc,ref}^2}{P_n} = r_r R_n \end{cases} \tag{3.58}$$

This means that the corresponding time constants are

$$\begin{cases} \tau_{cable} = \tau_{cable(pu)} \cdot \tau_{n,converter} \\ \tau_r = R_r C_r = \dfrac{(1-\delta_r)^2}{p_r} \cdot \tau_{n,converter} = \tau_{r(pu)} \cdot \tau_{n,converter} \end{cases} \tag{3.59}$$

where $\tau_{(pu)}$ denotes p.u. time constant. The impedance is thus written

$$Z_{cable} + Z_r = \frac{R_r}{s\tau_r + 1} \cdot \left((r_{cable} / r_r)(s\tau_{cable} + 1)(s\tau_r + 1) + 1 \right) \tag{3.60}$$

The source converter output voltage is divided between the cable impedance and the equivalent impedance of the receiving end converter, which gives

$$\begin{aligned} \frac{V_R}{V_S} &= \frac{Z_r}{Z_{cable} + Z_r} = \frac{1}{(r_{cable} / r_r)(s\tau_{cable} + 1)(s\tau_r + 1) + 1} \\ &= \frac{1}{\dfrac{r_{cable}}{r_r}\tau_{cable}\tau_r} \cdot \frac{1}{s^2 + \left(\dfrac{1}{\tau_{cable}} + \dfrac{1}{\tau_r} \right) s + \dfrac{1}{\tau_{cable}\tau_r} \left(1 + \dfrac{r_r}{r_{cable}} \right)} \end{aligned} \tag{3.61}$$

Assuming complex poles, the characteristic polynomial is written

$$p(s) = s^2 + 2\zeta_o \omega_o s + \omega_o^2 \tag{3.62}$$

which results in

$$\begin{cases} \omega_o = \dfrac{1}{\tau_{n,converter} \sqrt{\tau_{cable(pu)} \tau_{r(pu)}}} \cdot \sqrt{1 + \dfrac{r_r}{r_{cable}}} \\ \zeta_o = \dfrac{1}{2} \cdot \dfrac{\tau_{cable(pu)} + \tau_{r(pu)}}{\sqrt{\tau_{cable(pu)} \tau_{r(pu)}}} \cdot \sqrt{\dfrac{r_{cable}}{r_{cable} + r_r}} \end{cases} \tag{3.63}$$

Assuming

$$\omega_o = \omega_{o(pu)} \cdot \left(\omega_{lp} \frac{(1-\delta_n)\delta_n}{2\zeta_n^2} \right) = \omega_{o(pu)} \cdot \omega_{base} \tag{3.64}$$

gives a cable constant of

$$\tau_{cable(pu)} = \frac{1}{\omega_{o(pu)}^2 \tau_{r(pu)}} \cdot \left(1 + \frac{r_r}{r_{cable}} \right) \tag{3.65}$$

Since the measured DC bus voltage is low-pass filtered with break-over frequency ω_{lp} at the sending converter terminals, it is desirable that

$$\omega_{o(pu)} \geq \frac{2\zeta_n^2}{(1-\delta_n)\delta_n} \tag{3.66}$$

The main purpose of (3.61)-(3.66) is to provide a numerical base for the further investigation where the limiting case with cable resistance equal to

$$r_{cable} = 0.06 \tag{3.67}$$

is assumed. This gives the receiving end voltage

$$(1-\delta_r) = \frac{1}{2} + \sqrt{\frac{1}{4} - \left((1-\delta_n)\delta_n + r_{cable}\right) p_r} = 0.877 = 658\,\mathrm{V} \tag{3.68}$$

at rated output power. Therefore, the receiving end p.u. resistance is given by

$$r_r = \frac{(1-\delta_r)^2}{p_r} = 0.770 \tag{3.69}$$

Note that the p.u. resistance and time constant of the receiving end are equal if the cable capacitance is neglected, i.e.

$$r_r \equiv \tau_{r(pu)} = \frac{(1-\delta_r)^2}{p_r} \tag{3.70}$$

Therefore, the maximum allowable time constant, according to (3.66), is given by

$$\begin{aligned} \tau_{cable(pu)} &= \frac{1}{\omega_{o(pu)}^2} \cdot \frac{r_{cable} + r_r}{r_{cable} r_r} = \\ &= \left(\frac{(1-\delta_n)\delta_n}{2\zeta_n^2} \right)^2 \cdot \left(\frac{p_r}{(1-\delta_r)^2} + \frac{1}{r_{cable}} \right) = 0.0405 \end{aligned} \tag{3.71}$$

This means that the cable resistance and inductance are

$$\begin{cases} R_{cable} = r_{cable} \cdot R_n = 0.06 R_n \\ L_{cable} = \tau_{cable} \cdot R_{cable} = 2.432 \cdot 10^{-3} \cdot \tau_{n,converter} \cdot R_n \end{cases} \tag{3.72}$$

For a 750 V, 100 kW system, this is equivalent to cable parameters

$$\begin{cases} R_{cable} = 0.3375\,\Omega \\ L_{cable} = 1.528\,\text{mH} \end{cases} \tag{3.73}$$

The simulation result for this case is shown in Figure 3.10. Note that the cable data investigated here correspond to r_{cable}=0.06 p.u. and l_{cable}=0.0024 p.u., i.e. τ_{cable}=0.04 p.u. All time-domain simulations in this section are carried out using DYMOLA™ with switch-mode converter models utilising vector current controllers according to Appendix B and voltage droop controllers according to (3.3). The voltage droop controller gain (3.10) for each source converter is calculated based on C_{dc}=2C_s since a load converter of the same rated power has C_r=C_s (3.18). The AC side current reference for the source converter is calculated from the droop current reference based on the assumption that the converter is loss-less.

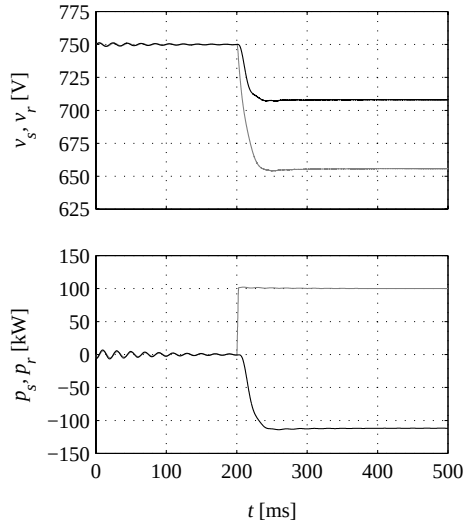

Figure 3.10: DC bus voltage (*top*) and power (*bottom*) of the sending (*black*) and receiving (*grey*) end converters at an output power step from zero to rated power.

In Figure 3.10 it is shown that the stationary voltage is lower than expected (a few Volts). This is due to the fact that rated power is transmitted to the three-phase grid, i.e. the losses in the line side filter have to be added to the power supplied to the DC side of the converter. This also implies that the equivalent load resistance, R_r, is lower than expected from previous calculations.

Now, the system is examined by means of pole-zero plots. The transfer function $V_s/V_{dc,ref}$, according to Figure 3.5, is investigated in MATLAB™ for different cable parameters and receiving end loading. MATLAB™ is used since the transfer function is significantly more complicated than (3.4) when cable parameters are included. The characteristic polynomial for this two-converter system is of the fourth order and analytical expressions for the poles are not possible to derive. Note that (3.61) cannot be used in the stability analysis since the source converter output impedance, including C_s, is not taken into account. Instead, (3.36) is used to calculate the receiving end voltage for the actual loading. An equivalent load resistance is calculated from δ_r and p_r. The transfer function $Z_{cable}+Z_r$, appearing in Figure 3.5, is calculated according to (3.57). The total impedance seen from the converter is calculated as the source converter DC side capacitance C_s in parallel with $Z_{cable}+Z_r$, which also forms the transfer function from I_s to V_s (Figure 3.5). The converter in Figure 3.5 is considered having a transfer function $G_{conv}(s)=1$ for the frequencies of interest and the external power reference $P_{ref,ext}$ is set to zero.

Figure 3.11 shows the pole-zero plot for the system with the same parameters as for Figure 3.10, at no-load (small markings) and at rated load (large markings). It is obvious from Figure 3.11 that the actual loading of the system is of minor importance for stability, which is due to the fact that the equivalent load resistance is considerably higher than the cable impedance.

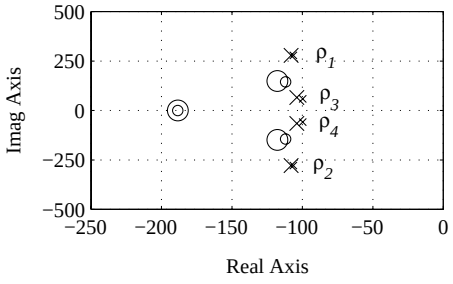

Figure 3.11: Pole-zero map for cable data r_{cable}=0.06 p.u. and l_{cable}=0.0024 p.u., which give τ_{cable}=0.04 p.u. Small markings are used for no-load (p_r=0) and large markings for receiver output power equal to rated sender power (p_r=1.0).

To investigate the robustness against parameter uncertainty, r_{cable} is varied from 0.01 to 0.12 p.u. and the cable time constant is varied from 0.02 to 0.4 p.u. The root-locus is investigated for a case where the receiving end power is approximately equal to rated power of the sending end converter, i.e. p_r is equal to one. This is not a strong limitation since it has been found that the load level affects the pole-zero map to a barely noticeable extent. Figure 3.12 and Figure 3.13 show the resulting root-locus for the poles ρ_1 and ρ_3, respectively (Figure 3.11). The two other poles, ρ_2 and ρ_4, are complex conjugate pairs of the ones in Figure 3.12 and Figure 3.13, and therefore not included.

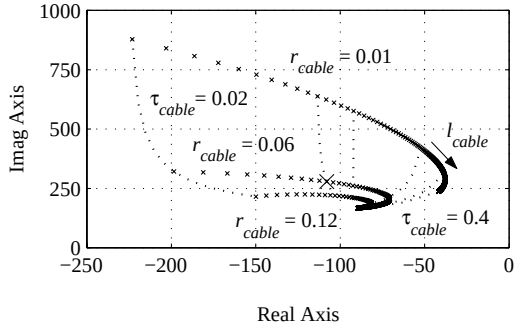

Figure 3.12: Root-locus for pole ρ_1 at p_r=1.0 p.u. The traces are from top to bottom: r_{cable}=0.01, 0.06 and 0.12 p.u. The dotted lines show constant τ_{cable}=0.02, 0.04, 0.05, 0.1, 0.2 and 0.4 p.u. from left to right.

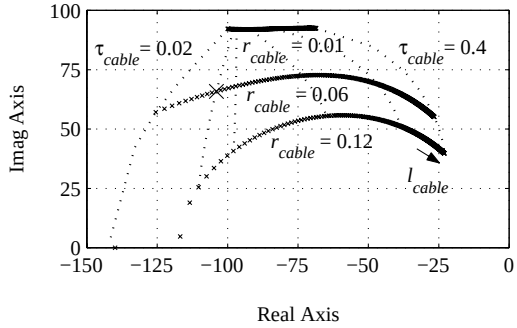

Figure 3.13: Root-locus for pole ρ_3 at p_r=1.0 p.u. The traces are from top to bottom: r_{cable}=0.01, 0.06 and 0.12 p.u. The dotted lines show constant τ_{cable}=0.02, 0.04, 0.05, 0.1, 0.2 and 0.4 p.u. from left to right. Note that the pole is real valued for low l_{cable} when r_{cable}=0.12 p.u.

From Figure 3.12 and Figure 3.13, it is concluded that a low cable resistance results in a moderately damped system, which is also expected. This is further seen from the overshoot appearing in the DC bus voltage response resulting from a load power step at low cable resistance and time constant, see Figure 3.14. The overshoot is due to the ρ_3-ρ_4 pole pair, resulting from the selected damping (3.12).

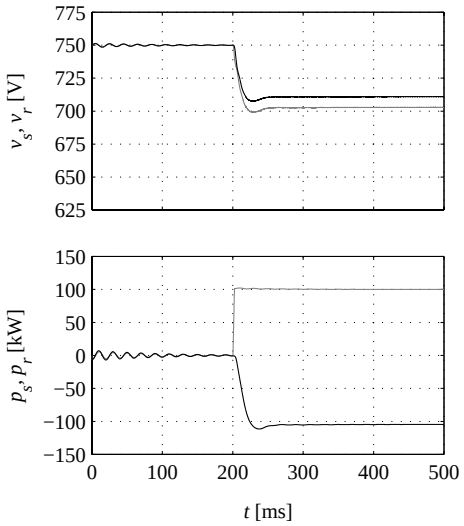

Figure 3.14: DC bus voltage (*top*) and power (*bottom*) of the sending (*black*) and receiving (*grey*) end converters at an output power step from zero to rated power when r_{cable}=0.01 p.u., l_{cable}=0.0002 p.u. and, thus, τ_{cable}=0.02 p.u.

For a long time constant of the cable, the situation is worse with a superimposed oscillation on the overshoot (Figure 3.15). The oscillation frequency is close to 40 Hz, corresponding to the location of ρ_1 (and ρ_2) in Figure 3.12. On the other hand, when r_{cable}=0.12 p.u., the system is well damped but the receiving end converter operates at the limit of over-modulation for rated output power. Furthermore, the cable losses are high, around 20%, as discussed earlier. Therefore, such a high cable resistance is not recommended.

From this investigation it is concluded that the DC bus voltage droop controller operates as intended for practical cable parameters. The cable resistance is limited by the risk of converter over-modulation. The investigated cable inductance most likely covers practical situations.

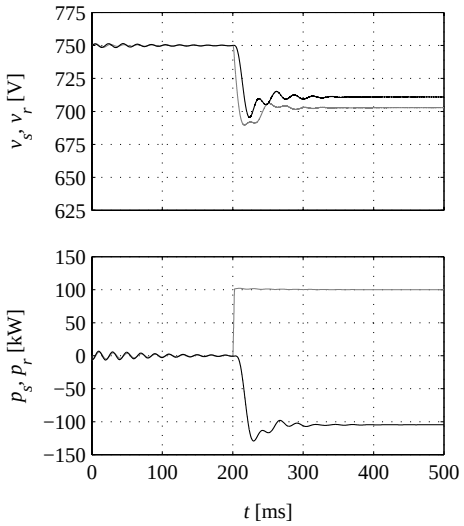

Figure 3.15: DC bus voltage (*top*) and power (*bottom*) of the sending (*black*) and receiving (*grey*) end converters at an output power step from zero to rated power for the case with r_{cable}=0.01 p.u., l_{cable}=0.004 p.u. and, thus, τ_{cable}=0.4 p.u.

3.5 Load sharing

Load sharing for a five-converter DC ring bus (Figure 3.1) is investigated in simulations. The network and converter parameters are given in Table 3.1. Cable segment 1 (Figure 3.3) is connected between converter 1 and 2, segment 2 between converter 2 and 3, etc. Since this is a ring bus, segment 5 is connected between converters 5 and 1. To determine an appropriate cable resistance (R_{cable}, Table 3.1), it is assumed that the cable length of each segment is 100 m and that the maximum current density is 4 A/mm^2 even if the ring bus is broken. The cable inductance (L_{cable}) is calculated assuming a distance between the centers of the conductors equal to twice the conductor diameter. This assumption is also used in the calculation of the cable capacitance (C_{cable}).

Both stationary and transient load sharing are investigated for master/slave and droop DC bus voltage control. Load sharing in the case of droop control with voltage error restoration is also investigated. Three converters, 1, 3 and 5 in Table 3.1, are operated as sources. Converters 2 and 4 are operated as loads. The sources and loads are modeled as three-phase AC grids, which are galvanically separated. Consequently, the dynamics of sources and loads are not taken into account in this investigation.

Table 3.1: Simulation model data.

Converter no.	i	1	2	3	4	5
Rated power	S_n [kVA]	25.0	100.0	50.0	50.0	75.0
Line-to-neutral voltage	E_{LN} [V]	230	230	230	230	230
Line frequency	f_n [Hz]	50	50	50	50	50
Switching frequency	f_{sw} [kHz]	7.5	7.5	4.95	5.0	4.95
Line inductance	L_{line} [mH]	6.0	1.7	3.0	3.40	2.0
Line resistance	R_{line} [Ω]	0.5	0.25	0.5	0.25	0.5
DC bus capacitance	C_{dc} [mF]	5.0	20.0	10.0	10.0	15.0
Cable capacitance	C_{cable} [nF]	5.27	5.27	5.27	5.27	5.27
Cable inductance	L_{cable} [μH]	52.7	52.7	52.7	52.7	52.7
Cable resistance	R_{cable} [mΩ]	64.7	64.7	64.7	64.7	64.7
DC bus voltage reference	$V_{dc,ref}$ [V]	750	750	750	750	750

The investigation starts at a condition where the load converters, 2 and 4 (Table 3.1), operate at no-load. From the initial no-load operating point, the output power of converter 2 increases by 50% of rated power at t=100 ms and the output power of converter 4 increases by 50% of rated power at t=200 ms. This means that for an ideal system, i.e. with zero cable impedance, the source converters should also be loaded to half their rated power at the end of the simulation.

In all the figures shown in this section, black curves denote source converter quantities and grey denote load converter quantities. Therefore, quantities belonging to converter sub-system 1 are solid black, 2 are solid grey, 3 are dashed black, 4 are dashed grey, and 5 are dash-dotted black.

DC bus voltage droop control

Figure 3.16 shows the simulation result for load sharing in the case of DC bus voltage droop control with a P-type controller, i.e. without voltage error restoration. It is seen in Figure 3.16 that load sharing works properly both in stationary and transient conditions. The source converters are loaded to approximately 0.6 p.u. each, on the unit base. The barely noticeable, but present, difference in relative loading is a result of the resistance of the cable segments. As expected, voltage regulation is poor. However, as long as the converters do not operate in over-modulation this is not a problem. As discussed earlier in this chapter, over-modulation is avoided by selecting a distribution bus with a moderate resistance.

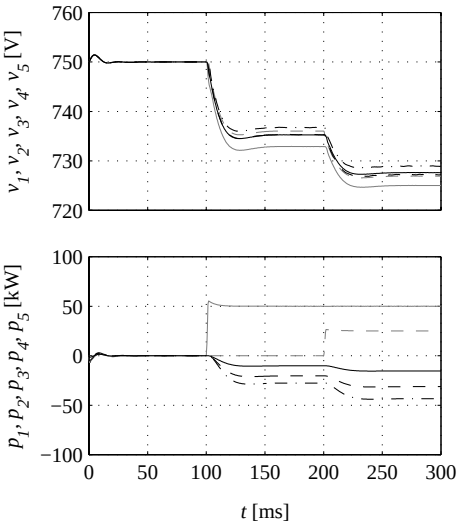

Figure 3.16: DC bus voltage (*top*) and power (*bottom*) for DC bus voltage droop control in the case of an output power increase of 0.5 p.u. of rated load converter power at t=100 ms for converter 2 and t=200 ms for converter 4 starting from 0 p.u. in both cases.

DC bus voltage droop control with error restoration

Figure 3.17 and Figure 3.18 show the simulation results for load sharing in the case of DC bus voltage droop control with a PI-controller, i.e. including voltage error restoration. The simulation result of Figure 3.17 is for a controller equipped with a constant integration time constant and the one of Figure 3.18 with a load dependent integration time constant. The integration is inhibited when the DC bus voltage at each source is inside a dead-band of 5 V located on both sides of the DC bus voltage reference, 750 V.

From Figure 3.17 and Figure 3.18 it is seen that load sharing is poor in both cases. The loading of the source converters in the case of DC bus voltage droop control with error restoration is roughly between 0.5 and 0.7 p.u., on the unit base, according to Figure 3.17 and Figure 3.18. Load sharing might be enhanced if different voltage error dead-bands are specified for each source converter. However, in a mesh network, like the ring bus investigated here, this is a complicated task. On the other hand, voltage regulation is enhanced compared to regular droop control, due to the integral part. Still, appropriate load sharing is considered as being of more concern.

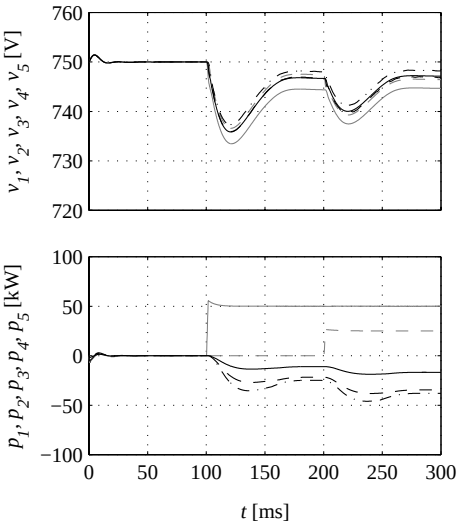

Figure 3.17: DC bus voltage (*top*) and power (*bottom*) for DC bus voltage droop control with error restoration in the case of an output power increase of 0.5 p.u. of rated load converter power at t=100 ms for converter 2 and t=200 ms for converter 4 starting from 0 p.u. in both cases.

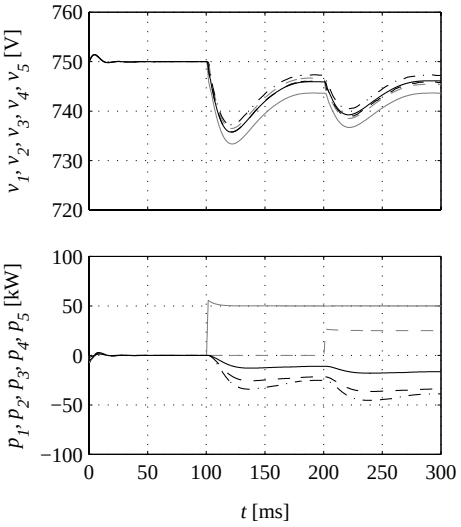

Figure 3.18: DC bus voltage (*top*) and power (*bottom*) for DC bus voltage droop control with error restoration in the case of an output power increase of 0.5 p.u. of rated load converter power at t=100 ms for converter 2 and t=200 ms for converter 4 starting from 0 p.u. in both cases.

Master/slave DC bus voltage control

Figure 3.19 illustrates load sharing in the case of master/slave control. As mentioned earlier, the master receives actual power estimations from all the other units. Then the master distributes power references to the slaves, i.e. the other converters also operated as sources. These power references could also be based on the DC bus voltage controller output. However, in the case investigated here, the power references fed from the master are only calculated from the load converter output power. The power references are scaled in proportion to the rated power of each source, including the master itself. Converter 5 is assigned as master in this case and, therefore, delivers one half of the source converter output power. It should also deliver the power required to control the DC bus voltage. Converters 1 and 3 supply 1/6 and 1/3 of the total power delivered to the loads, respectively. The transients seen in Figure 3.19 are due to DC bus voltage drop, mainly, and sampling delay.

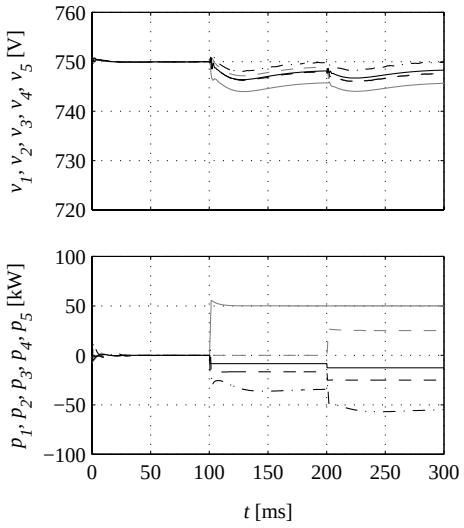

Figure 3.19: DC bus voltage (*top*) and power (*bottom*) for master/slave DC bus voltage control in the case of an output power increase of 0.5 p.u. of rated load converter power at t=100 ms for converter 2 and t=200 ms for converter 4 starting from 0 p.u. in both cases.

From Figure 3.19 it is obvious that converter 5 operates at a relatively higher loading than the other source converters. This is due to the fact that this converter is the only one responsible for DC bus voltage control, since the power references fed forward to the slaves are not based on voltage control.

Master/slave control with a PI DC bus voltage controller gives a stationary voltage error equal to zero at the master DC bus interface. Also, load sharing can be fully controlled. The main disadvantage of master/slave control is the need for communication between the converters. The required bandwidth of the communication is determined by the energy storing devices of the DC bus. If the amount of energy stored in the DC bus capacitors is high, the bandwidth can be low and vice versa. In the simulation result (Figure 3.19), the same DC bus capacitor values as in the previously investigated droop case, are used. At the same time, the communication bandwidth is higher than the converter current controller sampling frequency. Consequently, the voltage control and load sharing show high performance in this case. The communication bandwidth could be reduced in this case and still the performance would be better than for the investigated droop methods. On the other hand, if communication is lost, the system would not work at all.

3.6 Concluding remarks

A method to select the converter DC bus capacitance of each converter connected to the DC distribution bus is presented. The maximum cable resistance is specified upon the margin to over-modulation. Furthermore, the dynamic properties are investigated with aid of the root-locus for varying DC bus cable parameters. The investigated droop control method is simulated, with the converter parameters derived from the analysis, both in a two-converter application and in a five-converter ring bus. From the two-converter analysis it is found that for realistic cable data the system can be modeled without taking the cable inductance into consideration. This means that system specification and investigation can be made using a resistive cable model in a load-flow program. The five-converter DC bus ring bus is simulated with realistic cable parameters for different DC bus voltage control methods. The P-type droop controller is selected for the investigations to follow due to the high performance in terms of load sharing and since communication between converters is not required.

Chapter 4

Wind powered DC bus

Wind power is one of the most promising renewable energy sources. The reasons for this are for example high efficiency also for the present wind power technologies and the fact that wind power turbines can be located both on-shore and off-shore [53] and in both cases produce high power also for rather small installations. This means that the ecological footprint can be kept at acceptable levels. Another benefit is that the rotating mass constitutes an energy storage, which means that small wind variations might not disturb the power transfer extensively. In this chapter it is investigated if a DC distribution system can be operated only with wind powered generators. The investigation focuses on a load case where three wind power generators are fed by a wind speed corresponding to rated power and delivers power approximately equal to half the rated to a DC grid with two converters delivering power to loads. The excess power fed to the wind turbines is removed by pitch angle control. The problem in this case is that the turbine speed might increase beyond the rated, which might result in severe mechanical stress. Another problem is that the increased speed results in an increased back-emf of the generators. In a worst-case scenario, the back-emf might be so high that the controlled voltage source converter looses controllability of the current and instead operates as diode rectifiers due to the freewheeling diodes. Most modern wind power turbines are speed controlled by means of pitch angle control. However, pitch angle control has a rather low bandwidth, with time constants in the range of seconds.

The chapter starts with pitch angle control and then droop offset control follows. The added features of converter control in the case of wind power generators, i.e. speed estimation and field weakening, are discussed. Three different dynamic load conditions are investigated.

4.1 Pitch angle control

In this section it is investigated how the wind power turbines respond to a sudden blocking of the load converters, e.g. before pitch control is fully established. The pitch angle is controlled in such a way that the mechanical power delivered to the generator is expressed as

$$P_{gen} = P_{wind} - P_{pitch} \tag{4.1}$$

where the available wind power is

$$P_{wind} = K_{wind} v_{wind}^3 \tag{4.2}$$

where v_{wind} is the wind speed and K_{wind} a constant. The power lost due to pitch angle control is proportional to the error between the reference and actual mechanical speed and given by

$$P_{pitch} = K_{pitch}\left(\omega_{m,ref} - \omega_m\right) \tag{4.3}$$

The pitch angle controller gain is found from the time constant τ_{pitch} and the moment of inertia J_m

$$K_{pitch} = -\omega_m \frac{J_m}{\tau_{pitch}} \cdot \frac{P_{wind}}{P_n} \tag{4.4}$$

For transients, the following differential equation applies

$$J_m \frac{d\omega_m}{dt} = T_{wind} - T_{pitch} - T_{gen} = \frac{P_{wind} - P_{pitch} - P_{gen}}{\omega_m} \tag{4.5}$$

Assuming the initial conditions

$$\begin{cases} P_{wind}(t_0) = P_0 \\ P_{gen}(t_0^-) = P_0 \end{cases} \quad \text{and} \quad \begin{cases} P_{wind}(t_0) = P_0 \\ P_{gen}(t_0^+) = 0 \end{cases} \tag{4.6}$$

the following expression is approximately valid for the pitch angle controller

$$P_{pitch} = P_0\left(1 - e^{-(t-t_0)/\tau_{pitch}}\right) \tag{4.7}$$

which gives the following differential equation

$$\omega_m \frac{d\omega_m}{dt} = \frac{P_0}{J_m} e^{-(t-t_0)/\tau_{pitch}} \tag{4.8}$$

with the solution

$$\frac{1}{2}\omega_m^2(t) = P_0 \frac{\tau_{pitch}}{J_m}\left(1 - e^{-(t-t_0)/\tau_{pitch}}\right) + \frac{1}{2}\omega_{m0}^2 \tag{4.9}$$

where ω_{m0} is the mechanical speed at time t_0. Thus, the stationary mechanical speed is given by

$$\omega_{m,stat} = \sqrt{2P_0 \frac{\tau_{pitch}}{J_m} + \omega_{m0}^2} \tag{4.10}$$

The worst-case increase is when operating at rated (index *n*) speed and power, i.e.

$$\Delta\omega_{m,max} = \omega_{m,stat,max} - \omega_{m,n} = \sqrt{2P_n \frac{\tau_{pitch}}{J_m} + \omega_{m,n}^2} - \omega_{m,n} \tag{4.11}$$

Note that the maximum speed increase

$$\Delta\omega_{m,max} = \omega_{m,n} \cdot \left(\sqrt{\frac{\tau_{pitch}}{\frac{1}{2}\frac{J_m \omega_{m,n}^2}{P_n}} + 1} - 1 \right) = \omega_{m,n} \cdot \left(\sqrt{\frac{\tau_{pitch}}{H} + 1} - 1 \right) \tag{4.12}$$

is equal in p.u. for different wind turbines if

$$\frac{\tau_{pitch}}{H} = \text{constant} \tag{4.13}$$

is the same for all the wind turbines. To obtain similar behavior in the case of power variations, this ratio should be equal for the wind power aggregates. It is likely that the inertia constant H is approximately equal for the aggregates. Therefore, the pitch angle controller time constant should also be equal.

4.2 Droop offset control

Droop offset control (Figure 4.1) is introduced to handle wind speed variations. There are two ways to introduce this offset. Firstly, an external power reference could be added which is transferred to a current reference, see Figure 3.5. This is used when the supervisory controller orders that one source should supply a certain amount of power when the rest operate at idle conditions. Secondly, the DC bus voltage reference could be altered in such a way that a source is more lightly or heavily loaded. This section covers the second method applied to wind power turbines where the turbine speed is used as a measure on the actual power delivering capability.

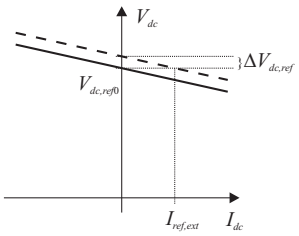

Figure 4.1: Droop offset control.

From the results of the previous section, a droop offset controller gain used to divide the actual available wind power equally (in p.u.) between the source converters is established according to

$$K_\omega = -\frac{\Delta V_{dc,ref,max}}{\Delta \omega_{el,max}} = -\frac{(1-\delta_n)\delta_n V_{dc}}{\sqrt{2P_n \frac{\tau_{pitch}}{J_m} z_p^2 + \omega_{el,n}^2} - \omega_{el,n}} \tag{4.14}$$

where z_p is the number of pole pairs for the electric machine and ω_{el} is the electrical angular frequency. A new DC bus voltage reference is formed from

$$V_{dc,ref} = V_{dc,ref\,0} + \Delta V_{dc,ref} = V_{dc,ref\,0} + K_\omega \left(z_p \omega_{m,ref} - \hat{\omega}_{el} \right) \tag{4.15}$$

where $V_{dc,ref0}$ is the initial reference which is equal to the no-load DC bus voltage. This means that the droop characteristic is shifted up- or downwards, depending on the difference between the speed reference and the estimated electrical speed. Thus, a speed droop is formed.

4.3 Speed estimation

A permanent-magnet synchronous machine (PMSM) is suitable for wind power applications for two reasons correlated to each other. Firstly, if a multiple pole generator, i.e. a machine with low mechanical base speed, is used the mechanical gearbox can be omitted reducing the weight and the need for maintenance. Secondly, the most suitable machine for low base speed is the synchronous machine, at least compared to other three-phase machines, e.g. the induction machine. However, it should be kept in mind that the weight of a multiple pole machine is higher than the weight of a machine with a low pole number but lower if the gearbox is taken into account. It should also be noticed that a PMSM is more expensive than an induction machine.

A current controller similar to the one used for AC network connected converters (Appendix B) is required also for the control of a PMSM. However, the PMSM of a single wind turbine cannot be regarded as a stiff power source, which means that the frequency is not even near constant. The speed and position need to be estimated to fix the rotating (*dq*) coordinate system and to calculate the reactive voltage drop fed forward in the current controller. To track the speed variations, a speed and position estimator is needed. The one utilised here is based on the results obtained in [32]. First the *d*-direction back-emf e_d, which should be close to zero, is estimated

$$e_{d,k} = u_{d,k} - R_s i_{d,ref,k} - \hat{\omega}_{el,k-1} L_q i_{q,ref,k} \tag{4.16}$$

where R_s is the stator resistance and L_q the stator inductance in the *q*-direction. The angular frequency is estimated from

$$\hat{\omega}_{el,k} = \hat{\omega}_{el,k-1} - T_s \gamma_1 (\omega_{f,k}) e_{d,k} \tag{4.17}$$

where T_s is the duration of each sampling interval. The angular position is estimated from

$$\hat{\theta}_k = \left[\hat{\theta}_{k-1} + T_s \hat{\omega}_{el,k-1} - T_s \gamma_2 (\omega_{f,k}) e_{d,k} \right]_0^{2\pi} \tag{4.18}$$

The estimated speed is low-pass filtered according to

$$\omega_{f,k} = \omega_{f,k-1} + T_s \rho_s (\hat{\omega}_{el,k-1} - \omega_{f,k-1}) \tag{4.19}$$

which is then used to calculate suitable adaptation gains for the estimator [32]

$$\begin{cases} \gamma_1 = \dfrac{\rho_0^2}{\omega_f \Psi_m} \cdot z_p \\ \gamma_2 = \dfrac{2\rho_0}{\omega_f \Psi_m} \cdot z_p \end{cases} \tag{4.20}$$

where Ψ_m is the flux-linkage and ρ_0 is the real valued double pole of the estimator. According to [32], a proper choice for the pole is

$$\rho_0 = \sqrt{\rho_s 0.2 \cdot \omega_{el,n} / \sin\left(5^\circ\right)} \tag{4.21}$$

where ρ_s is the bandwidth of the speed control loop. In this application, the speed is not actually controlled but instead an internal droop offset is created from the speed deviation. Since the speed varies slowly in a wind power application, a bandwidth of 10 Hz should be sufficient. This gives

$$\rho_s = 2\pi 10 \text{ rad/s} \tag{4.22}$$

Details on the derivation of the speed and position estimator are given in [32].

4.4 Field weakening

During abnormal operation, for example when the load converters are blocked, the speed might increase to a level considerably higher than base speed. This means that the induced back-emf

$$e_q = \omega_m \Psi_m \tag{4.23}$$

might reach levels so high that the controlled transistor converter starts to act as a non-controlled diode rectifier, formed by the freewheeling diodes. To circumvent this potential risk, resulting in lost control of the DC bus voltage, field weakening is introduced. In field weakening, reactive power is consumed so that the machine terminal voltage is kept at the average level

$$u_q = R_s i_q + \omega_{el} L_d i_d + e_q \tag{4.24}$$

where L_d is the stator inductance in the *d*-direction. A control law could be formed directly from this expression. However, this implies a high gain and

since the speed is estimated this could result in an oscillatory behaviour. To reduce this kind of problem, the *d*-component of the current is filtered with a first order filter with

$$\omega_{lp,id} = \rho_s / 10 \tag{4.25}$$

Then the difference between the back-emf at rated speed and the actual back-emf minus the actual field weakening component is fed to a PI-controller, see Figure 4.2.

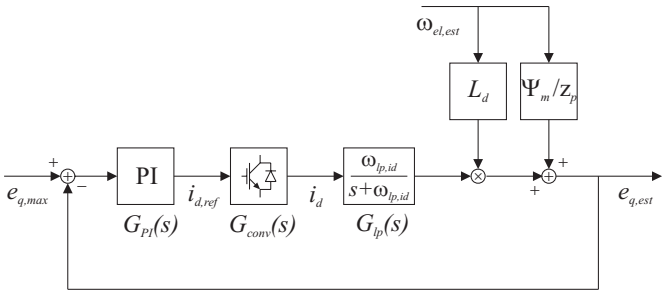

Figure 4.2: Controller structure for generation of the *d*-current reference used for field weakening action. Note that the machine back-emf is estimated.

The gain and integrator time constant of this PI-controller is selected in such a way that the closed loop poles of the field weakening sub-system, with the assumption that the estimated speed is correct, are given by

$$\lambda_{1,2} = -(2\alpha_{id} - 1)\omega_{lp,id} \tag{4.26}$$

where α_{id} is a weighting factor to reduce the gain of the field weakening sub-system. A suitable value for this factor is

$$\alpha_{id} = 0.55 \tag{4.27}$$

The gain and integrator time constant used to generate the *d*-current reference required for field weakening are given by

$$\begin{cases} K_{fw} = (2\alpha_{id} - 1) \cdot \dfrac{1}{L_d} \cdot \left(\dfrac{\Psi_m}{z_p} + \dfrac{1}{|\omega_{el}|} \right) \\ T_{fw} = \dfrac{1}{\omega_{lp,id}} \cdot \dfrac{2\alpha_{id} - 1}{\alpha_{id}^2} \end{cases} \tag{4.28}$$

for a continuous time controller. For the simulation, a sampled controller is used and, therefore, backward Euler transformation [81] is applied.

4.5 Simulations

Three main issues are investigated in simulations: wind speed variations, load sharing and load converter blocking. A ring bus network configuration (Chapter 3) is studied. The network and converter parameters are given in Table 4.1. The *d*- and *q*-direction inductances, L_d and L_q found in Table 4.1, approximately corresponds to the ones given in [30] for a PMSM with a nominal electrical frequency of 26.5 Hz (x_a=0.95 p.u. on the machine base according to [30]), which is recalculated to fit a machine with nominal electrical frequency equal to 50 Hz (x_a=0.52 p.u. on the machine base according to [30]).

Table 4.1: Simulation model data.

Converter no.	i	1	2	3	4	5
Rated power	S_n [kVA]	25.0	100.0	50.0	50.0	75.0
Line-to-neutral voltage	E_{LN} [V]	230	230	230	230	230
Line/PMSM rated frequency	f_n [Hz]	50	50	50	50	50
Switching frequency	f_{sw} [kHz]	7.5	7.5	4.95	5.0	4.95
PMSM *d*-direction inductance	L_d [mH]	9.78	-	4.89	-	3.26
PMSM *q*-direction inductance	L_q [mH]	9.17	-	4.58	-	3.06
PMSM Stator resistance	R_s [Ω]	0.5	-	0.5	-	0.5
Line inductance	L_{line} [mH]	-	1.70	-	3.40	-
Line resistance	R_{line} [Ω]	-	0.25	-	0.25	-
DC bus capacitance	C_{dc} [mF]	5.0	20.0	10.0	10.0	15.0
Cable capacitance	C_{cable} [nF]	5.27	5.27	5.27	5.27	5.27
Cable inductance	L_{cable} [μH]	52.7	52.7	52.7	52.7	52.7
Cable resistance	R_{cable} [mΩ]	64.7	64.7	64.7	64.7	64.7
DC bus voltage reference	$V_{dc,ref}$ [V]	750	750	750	750	750

The DC ring bus and the cable segments are arranged and have the same data as in Chapter 3. For the wind power aggregates the parameters are

$$\begin{cases} J_m = 40\,\text{kgm}^2/\text{kW},\, z_p = 40 \;\Leftrightarrow\; H = 1.2\,\text{s} \\ \tau_{pitch} = 1\,\text{s} \end{cases} \tag{4.29}$$

where H is the inertia constant.

The speed reference is maintained at $\omega_{m,ref}$=6.23 rad/s throughout all the simulations. The moment of inertia is fairly low compared to what present wind turbines exhibit. In the power range considered, a turbine moment of inertia approximately five times higher can be expected. The internal droop offset control is not affected by this fact since its gain is calculated based on an estimation of the moment of inertia. The only way that the reduced moment of inertia affects the simulation results is, therefore, in terms of the magnitude of the increase or decrease in the response of the mechanical speed due to power variations. The system has been simulated with five times higher moment of inertia. Consequently, τ_{pitch}/H is five times less and K_ω is slightly less than five times higher. It is found that the resulting waveforms are similar in shape. The actual speed variation is determined by the initial speed and the voltage variation is determined by the speed error.

Three cases are studied. First, wind speed variations are considered. Second, load sharing is investigated. Third, a load converter blocking situation is considered. In all three cases, the investigation starts at a condition where the load converters are loaded to half their rated power, respectively. For an ideal system, i.e. with zero cable impedance, the source converters should also be loaded to half their rated power. For a realistic system, including cable impedance, it is cumbersome to determine the maximum allowable load converter output power for a given wind situation by analytical methods. However, the actual loading of each source converter can be calculated with a load flow program, similar to the ones used for AC system analysis, to give the input power required for a certain loading. In all the figures shown in this section, black curves denote source converter quantities and grey denotes load converter quantities. Therefore, quantities belonging to converter sub-system 1 are solid black, 2 are solid grey, 3 are dashed black, 4 are dashed grey, and 5 are dash-dotted black.

Wind disturbance

From the initial operating point, the wind speed of aggregate 1 suddenly drops at t=0.5 s, resulting in a wind turbine input power reduction from rated level (25 kW) to 40% of rated power (10 kW). Consequently, the two other source converters (3 and 5) are more heavily loaded, see Figure 4.3. The increased loading of converters 3 and 5 result in a decreased DC bus voltage, due to voltage droop controller action. The power delivered from converter 1 is reduced since the droop offset control reduces $V_{dc,ref}$ for this converter. Thus, its voltage error decreases and the power delivered via converter 1 is reduced.

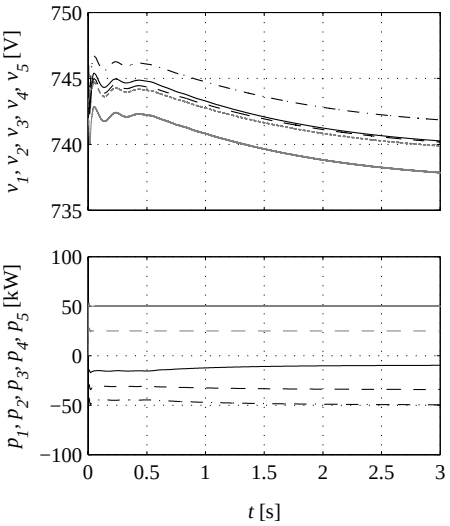

Figure 4.3: Converter DC side voltage (*top*) and power (*bottom*) for converter 1 to 5 at a wind power decrease of 15 kW (60% of rated power) at t=0.5 s for converter 1 starting from 25 kW (rated power).

The power removed by pitch angle control for wind power aggregate 1 is shown in Figure 4.4. Note that the power removed by pitch angle control drops suddenly at t=0.5 s due to the rapid decrease in input power at this instant. Both the droop offset controller and the pitch angle controller rely on an external speed reference. This reference is assumed being supplied from a supervisory controller used for the entire DC distributed power system. The speed reference should be based on actual wind speed and power delivering capability. The communication required is assumed slow, and the speed references are not altered during the simulation.

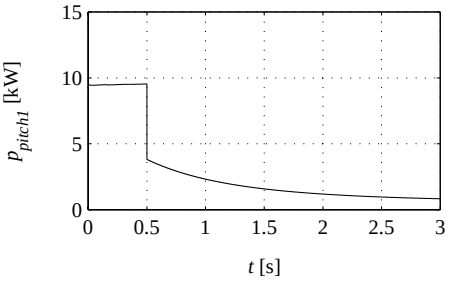

Figure 4.4: The power removed at wind turbine 1 due to pitch angle controller action.

Load sharing

From the initial operating point introduced above, the output power of converter 2 increase by 10% of rated power at t=0.5 s and the output power of converter 4 increase by 10% of rated power at t=1.0 s, see Figure 4.5.

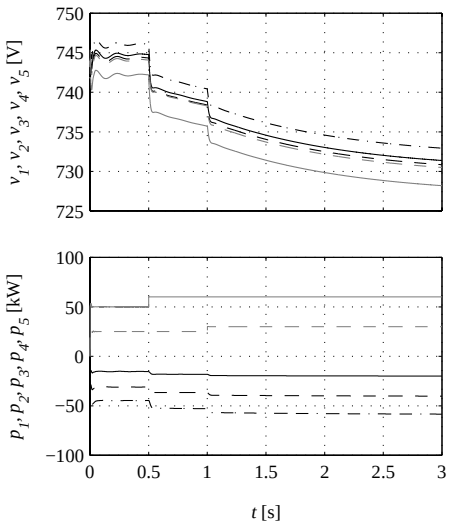

Figure 4.5: Converter DC side voltage (*top*) and power (*bottom*) for an output power increase of 0.1 p.u. of rated load converter power at 0.5 s for converter 2 and 1.0 s for converter 4 starting from 0.5 p.u. in both cases.

In Figure 4.5 it is shown that load sharing works properly both in stationary and transient conditions. Note the rapid steps in the DC bus voltage when the output power is changed, illustrated in Figure 4.5. These are due to voltage droop control action, reducing the voltage because of the increased loading. The slow variation in DC bus voltage is a consequence of internal droop offset-adjustment caused by the speed error resulting from the reduced actual speed. The droop offset also strives to reduce the voltage in order to distribute the total load among the wind power units.

Actual mechanical speed of the wind turbines is shown in Figure 4.6. The mechanical speed is reduced due to the increased loading. Consequently, the speed error increases resulting in a downward shift of the droop characteristic of each source converter. At the same time, the power removed by pitch angle control reduces due to the decreasing speed error. Therefore, a new operating point is established.

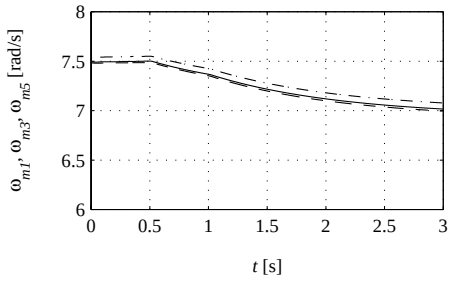

Figure 4.6: Wind power turbine speed.

Load blocking

From the initial operating point introduced above, converter 2 is blocked, i.e. its output power is decreased to 0, at t=0.5 s and converter 4 is blocked at t=1.0 s, see Figure 4.7. The converters could be blocked, for example, because of an emergency situation or due to a fault.

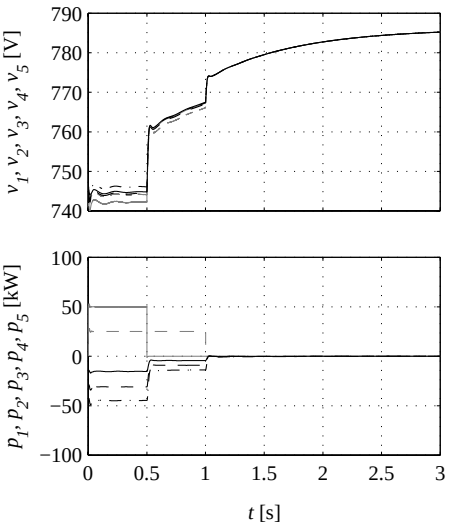

Figure 4.7: Converter DC side voltage (*top*) and power (*bottom*) for an output power decrease of 0.5 p.u. of rated load converter power at 0.5 s for converter 2 and 1.0 s for converter 4 starting from 0.5 p.u. in both cases.

As illustrated in Figure 4.7, load sharing works properly also in this case. Again, the DC bus voltage levels at the converter terminals exhibit both rapid and slow variations. Note that the DC bus voltages approaches each other as

the loading decreases due to the reduced resistive voltage drop experienced at light load. The mechanical speed of the wind turbines is shown in Figure 4.8.

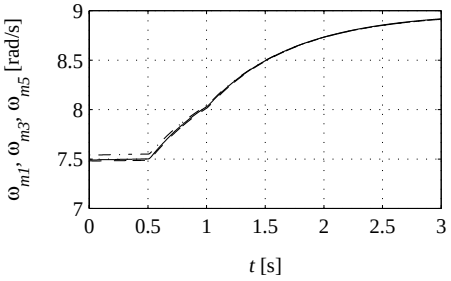

Figure 4.8: Wind power turbine speed. Note that the moment of inertia used for the wind turbine simulation models are approximately five times lower than what can be expected from a real installation.

The speed increase in Figure 4.8 is rather high due to the comparably low moment of inertia assumed for the wind power aggregates. At present, wind power turbines exhibit a moment of inertia approximately 5 times higher than used in the simulation. On the other hand, turbine blade material is becoming stronger, which implies that the weight and thereby the moment of inertia will most likely be reduced for future wind power turbines.

Position and speed estimator

Figure 4.9 shows the actual and estimated electrical speed for unit 1. Note that the bandwidth of the speed estimator is sufficient for the application. The available power could be estimated from the pitch angle and estimated mechanical speed. Therefore, the estimated speed could be used also for other purposes, for example, monitoring and supervisory control.

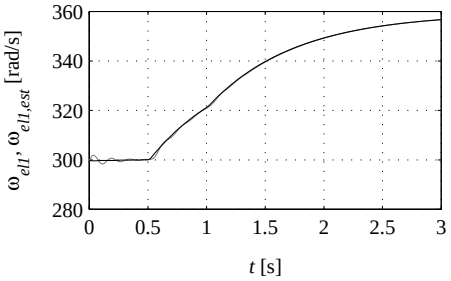

Figure 4.9: Actual (*black*) and estimated (*grey*) electrical speed (angular frequency).

Pitch angle control

The power removed by pitch angle control for wind power aggregate 1 is shown in Figure 4.10. The removed power approaches rated power at the end of the simulation. Both the voltage droop offset controller and the pitch angle controller rely on an external speed reference. This reference is considered as being supplied from a supervisory controller used for the entire wind power system. The speed reference should be based on actual wind speed and total DC bus power demand. Therefore this requires some kind of communication between the supervisory controller and each unit. In the simulations, this communication is considered as being slow, and therefore the speed references are not altered during the simulation run.

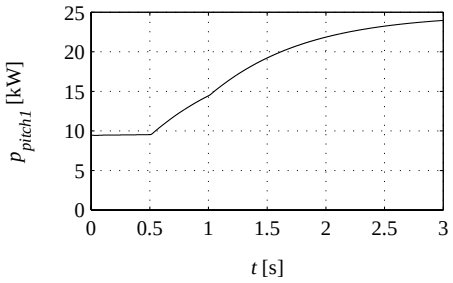

Figure 4.10: The power removed due to pitch angle controller action.

Field weakening

The reference and actual *d*- and *q*-currents for converter sub-system 1 are shown in Figure 4.11 and Figure 4.12, respectively. The *d*-current reference is negative due to the fact that the speed is higher than the base speed. A negative *d*-current implies that reactive power is consumed by the converter.

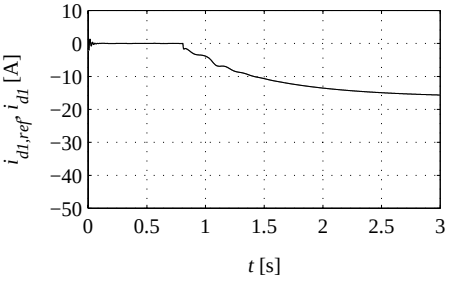

Figure 4.11: The *d*-current (*black*) and its reference (*grey*).

The q-current reference is a measure on the active power delivered from the DC to the AC side of the converter. Since the power is delivered from the AC side of converter sub-system 1, the q-current reference is negative.

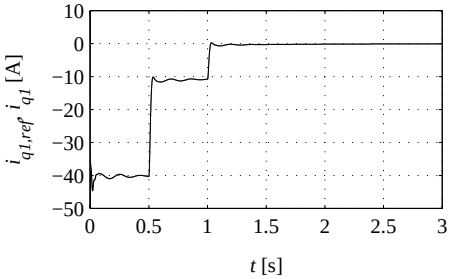

Figure 4.12: The q-current (*black*) and its reference (*grey*).

Chapter 5

Fault detection and clearance

Personal safety and prevention of property damage are important factors of conventional AC power systems. For the investigated DC power system this is maybe even more important, since the star points of the sources and loads are left ungrounded. As discussed in Chapter 3, the star point is not grounded or grounded through high impedance in order to effectively attenuate neutral currents. Otherwise, high amplitude neutral currents could flow between sources and loads since the used converter topologies do not provide any means to control zero-sequence or third order harmonic currents.

Short circuit (conductor-to-conductor) and ground (conductor-to-ground) faults should be detected and cleared to provide personal safety and protection of equipment. The safety requirements on DC distributed power systems should most likely comply with the ones found in [45] for residential photovoltaic systems.

This chapter starts with a presentation of the investigated DC power system grounding scheme together with its fusing. The fuses are intended to act on low impedance faults. The different fault situations are presented through simulations. Since detection and selectivity are important to guarantee proper operation, these issues are also discussed.

5.1 Grounding and fusing

Each converter is connected to the DC ring bus through a cable node. The cable node contains grounding, fuses, circuit breakers and current transducers required for protection (Figure 5.1). The protection capacitors C_p, or more correct, grounding capacitors are selected so that the time constant of ground

fault currents is sufficiently long for proper detection. The idea of the fault detection capacitors is that they should provide a minimum ground fault current, independent of the cable capacitance. Since the fault current is a quantity mainly determined by the cable properties, the capacitance of the fault detection capacitors is determined by the cable impedance and not the rated power and voltage of the converter connected to the cable node. This makes sense, since the same type of cable is used throughout the entire ring bus due to the fact that the cable rating should not limit the power flow in the case of a broken ring bus.

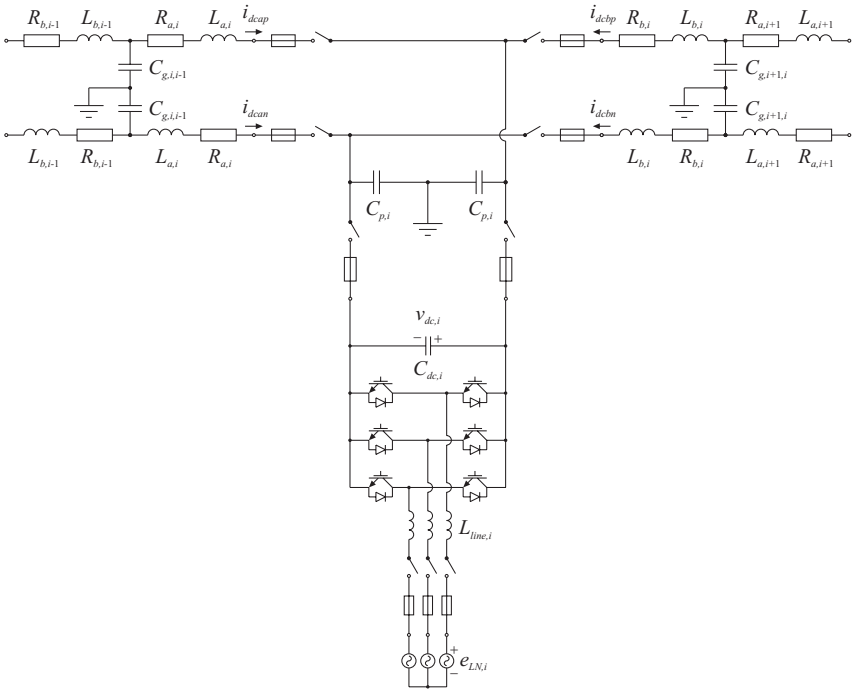

Figure 5.1: Cable node with two T-model cable segments and one converter connected. The interfaces to the cable segments are denoted *A* (*left*) and *B* (*right*).

5.2 Fault situations

To visualise the fault currents, only low impedance faults (1 Ω fault resistance) are investigated. For issues regarding personal safety this is a by far too low fault resistance. Therefore, high impedance faults (3000 Ω fault resistance) are discussed in a later section where fault detection is emphasised. The reason for

dividing the fault situations in this manner is because visualisation of fault currents for high impedance faults is strongly related to the detection method. The investigated five-converter DC distribution system is identical to that of Chapter 3. The protection or fault detection capacitors have a capacitance of C_p=10 μF and an equivalent series resistance of $R_{ESR,Cp}$=100 mΩ. Series resistors are inserted on purpose later on to guarantee a minimum time constant of fault currents. The capacitance is selected based on results obtained in a later section.

Short circuit on the DC side

In the case of a short circuit on the DC side, the DC bus capacitors located at each converter discharge. For low cable impedance, the DC bus voltage decreases with time constants, in principle, equal in all parts of the DC bus. This implies that all converter DC bus capacitors contribute to the fault current and the fault is detected in all cable nodes. Even in the case of low fault resistance, the time constant of the fault current is fairly long due to the high DC bus capacitance of the converters. In Figure 5.2, a short circuit occurs in the middle of cable segment 1, i.e. between converters 1 and 2, at t=1.0 ms. The fault resistance is R_{Fault}=1.0 Ω.

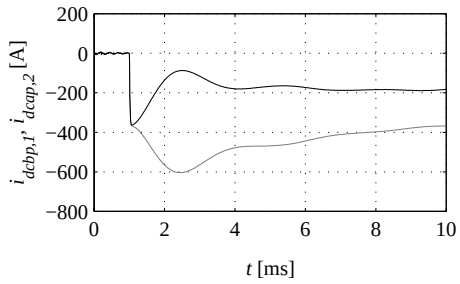

Figure 5.2: Fault currents i_{dcbp} for cable node 1 (*black*) and i_{dcap} for cable node 2 (*grey*) in the case of a short circuit on the DC side between converters 1 and 2 at t=1.0 ms. The fault resistance is R_{Fault}=1.0 Ω.

Note that the time constant of the fault current is not of significant importance for short circuit faults on the DC side when stiff sources or sources possessing high inertia are feeding the system. This is due to the fact that for a DC side short circuit, the bus voltage decreases only to the point where one of the transistor converters starts to operate as diode rectifier. Thus, the source starts to contribute directly to the short circuit current, through the freewheeling diodes of the converter.

Short circuit on the AC side

For a short circuit on the converter AC side, the main fault current contribution flows from the energy source. If the source is stiff, the fault current remains after the transient. This is comparably easy to detect. The fault current is strongly related to the fault location. If the short circuit appears close to the converter, the fault can be detected by the over-current alarm of the converter if the fault impedance is low. If the fault occurs inside the generator or filter windings or between a strong grid and the filter inductors, the fault current might flow almost entirely from the AC source, even in the case of low impedance faults. In such cases, the fault is cleared by the fuses.

Ground fault on the DC side

For a ground fault, all the protection capacitors contribute to the fault current. Assume that the fault resistance between the positive supply rail and ground or common is denoted R_{Fault}, see Figure 5.3.

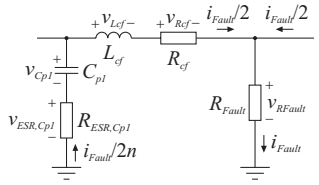

Figure 5.3: Equivalent circuit for ground fault on the DC side.

Figure 5.4 shows the simulation result for a positive supply rail to ground fault between converter 1 and 2. The fault resistance is R_{Fault}=1.0 Ω.

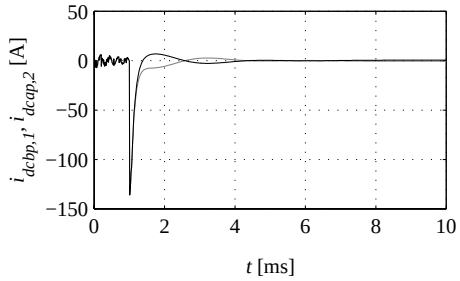

Figure 5.4: Fault currents i_{dcbp} for cable node 1 (*black*) and i_{dcap} for cable node 2 (*grey*) in the case of a low impedance ground fault on the DC side between converters 1 and 2 at t=1.0 ms. The fault resistance is R_{Fault}=1.0 Ω.

Note the short time constant of the fault currents in Figure 5.4. To enhance fault detection, series resistors are connected so that the time constant is not dependent on the ESR of the grounding capacitors. The current flowing through R_{Fault} to ground is denoted i_{Fault}. The fault current divides between the protective capacitors in such a way that

$$\sum_{i=1}^{n}\left(i_{Cp2,i}-i_{Cp1,i}\right)=i_{Fault} \tag{5.1}$$

where n is the number of cable nodes. If the cable resistance is low, the fault current divides approximately equal when the capacitors are of equal capacitance, i.e.

$$\left|\sum_{i=1}^{n}\left(i_{Cp2,i}-i_{Cp1,i}\right)\right|=2n\left|i_{Cp}\right|=i_{Fault} \tag{5.2}$$

If the fault is on the middle of the cable segment, half fault current flows from each side, see Figure 5.3. In this case, the capacitor current is related to the fault current according to

$$i_{Cp1}=-\frac{i_{Fault}}{2n} \tag{5.3}$$

and the current in the equivalent inductor is

$$i_{Lcf}=i_{Rcf}=-\frac{i_{Fault}}{2} \tag{5.4}$$

Since the fault location is in the middle of the cable, R_{cf} and L_{cf} correspond to one quarter of the total resistance and inductance of the cable segment. A differential equation is established from Kirchoff's voltage law applied to the equivalent circuit of Figure 5.3

$$\frac{d^2v_{Cp1}}{dt^2}+\left(\frac{R_{ESR,Cp1}}{nL_{cf}}+\frac{R_{cf}}{L_{cf}}+\frac{2R_{Fault}}{L_{cf}}\right)\cdot\frac{dv_{Cp1}}{dt}+\frac{1}{nL_{cf}C_{p1}}\cdot v_{Cp1}=0 \tag{5.5}$$

Consequently, the equivalent fault resistance is given by

$$R_{Fault,eq}=R_{Fault}+\frac{R_{cf}}{2}+\frac{R_{ESR,Cp1}}{2n} \tag{5.6}$$

The eigenvalues of the differential equation are given by

$$\lambda_{1,2} = -\frac{R_{Fault,eq}}{L_{cf}} \pm \sqrt{\left(\frac{R_{Fault,eq}}{L_{cf}}\right)^2 - \frac{1}{nL_{cf}C_{p1}}} \tag{5.7}$$

The solution to the differential equation is

$$v_{Cp1}(t) = Ae^{\lambda_1 t} + Be^{\lambda_2 t} \tag{5.8}$$

Since $L_l << C_{pl}$, the eigenvalues $\lambda_{1,2}$ are real valued. The capacitor current is

$$i_{Cp1}(t) = C_{p1}\frac{dv_{Cp1}(t)}{dt} = C_{p1}A\lambda_1 e^{\lambda_1 t} + C_{p1}B\lambda_2 e^{\lambda_2 t} \tag{5.9}$$

The initial voltage equals one half of the DC bus voltage and the initial current equals zero due to the inductive part of the cable, i.e.

$$\begin{cases} v_{Cp1}(0) = A + B = V_{dc}/2 \\ i_{Cp1}(0) = C_{p1}A\lambda_1 + C_{p1}B\lambda_2 = 0 \end{cases} \tag{5.10}$$

Therefore, the constants of the solution to the differential equation are

$$\begin{cases} A = \dfrac{\lambda_2}{\lambda_2 - \lambda_1} \cdot \dfrac{V_{dc}}{2} \\ B = -\dfrac{\lambda_1}{\lambda_2 - \lambda_1} \cdot \dfrac{V_{dc}}{2} \end{cases} \tag{5.11}$$

The time instant of maximum current is given by ($\lambda_1 < \lambda_2 < 0$)

$$t_{peak} = \frac{1}{\lambda_2 - \lambda_1} \ln\left(\frac{\lambda_1}{\lambda_2}\right) \tag{5.12}$$

To select appropriate fuses, the resulting I^2t has to be calculated. This is first done for the capacitor current.

$$\int_0^\infty i_{Cp1}^2 \, dt = -\left(C_{p1}\frac{V_{dc}}{2}\right)^2 \cdot \frac{1}{2} \cdot \frac{\lambda_1\lambda_2\left(\lambda_1^2 + \lambda_2^2\right)}{(\lambda_2 - \lambda_1)^2(\lambda_1 + \lambda_2)} \tag{5.13}$$

Since the current flowing through the fuses is n times higher

$$\int_0^\infty i_{Fuse}^2 dt = \int_0^\infty \left(n \cdot i_{Cp1}\right)^2 dt = n^2 \int_0^\infty i_{Cp1}^2 dt =$$

$$= -n^2 \left(C_{p1} \frac{V_{dc}}{2} \right)^2 \cdot \frac{1}{2} \cdot \frac{\lambda_1 \lambda_2 \left(\lambda_1^2 + \lambda_2^2\right)}{(\lambda_2 - \lambda_1)^2 (\lambda_1 + \lambda_2)} = \tag{5.14}$$

$$= \frac{1}{8} \cdot \left(\frac{V_{dc}}{2} \right)^2 \cdot \frac{nC_{p1}}{R_{Fault,eq}} \cdot \left(1 + \frac{nC_{p1} R_{Fault,eq}^2}{nC_{p1} R_{Fault,eq}^2 - L_{cf}} \right) \approx \frac{1}{4} \cdot \left(\frac{V_{dc}}{2} \right)^2 \cdot \frac{nC_{p1}}{R_{Fault,eq}}$$

According to simulations, this expression yields an overestimation of the I^2t the fuse is exposed to by approximately 10%. The main reasons for this deviation are that the peak current is lower than expected and that I^2t is only calculated when the current exceeds the rated current, in the fuse model.

Ground fault on the AC side

A ground fault on the AC side is more complicated to investigate analytically than on the DC side due to the sinusoidal nature of the line voltage and current, resulting in initial conditions dependent on the time instant of the fault occurrence. Still, expressions for the ground fault current are derived. An expression for calculating the stress on fuses, in terms of I^2t, is not derived.

Figure 5.5 shows an equivalent circuit for an AC side phase-to-ground fault.

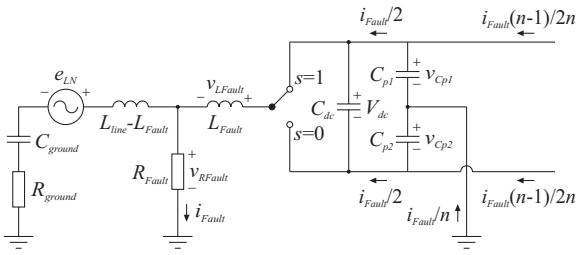

Figure 5.5: Phase-to-ground fault on the AC side.

Due to the high impedance between the neutral (or star) point of the AC side transformer or machine and the ground, the main contribution of the fault current flows from the DC side through the converter to the fault location.

The fault might be located on either side of the AC side inductors or even inside the inductors. Therefore,

$$0 \le L_{Fault} \le L_{line} \tag{5.15}$$

Figure 5.6 shows the simulation result for an *R*-phase-to-ground fault of converter 1. The fault resistance is R_{Fault}=1.0 Ω. The fault is located so that L_{Fault}=L_{line}. Therefore, the fault currents supplied from the converter is comparably low.

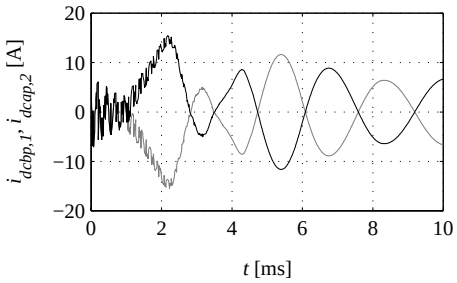

Figure 5.6: Fault currents i_{dcbp} for cable node 1 (*black*) and i_{dcap} for cable node 2 (*grey*) in the case of a low impedance ground fault on the AC side of converter 1 at t=1.0 ms. The fault resistance is R_{Fault}=1.0 Ω.

The fault resistance, i.e. the resistance between the phase conductor and ground at the fault location, is denoted R_{Fault} as before. The voltage across the fault is given by

$$u = s \cdot v_{Cp1} + (s-1) \cdot v_{Cp2} = s \cdot (v_{Cp1} + v_{Cp2}) - v_{Cp2} = s \cdot V_{dc} - v_{Cp2} \tag{5.16}$$

where u is the output voltage of the particular phase of the converter and the corresponding switch state is denoted s=[0,1]. The capacitor currents and fault current are related according to

$$i_{Fault} = -2n \cdot i_{Cp1} = 2n \cdot i_{Cp2} \tag{5.17}$$

This results in a differential equation

$$\frac{d^2 v_{Cp2}}{dt^2} + \frac{R_{Fault}}{L_{Fault}} \cdot \frac{dv_{Cp2}}{dt} + \frac{1}{2nL_{Fault}C_{p2}} \cdot v_{Cp2} = \frac{1}{2nL_{Fault}C_{p2}} \cdot s \cdot V_{dc} \tag{5.18}$$

Note that the ESR of the grounding capacitors is neglected in this case.

The roots to the characteristic polynomial are given by

$$\lambda_{1,2} = -\frac{R_{Fault}}{2L_{Fault}} \pm \sqrt{\left(\frac{R_{Fault}}{2L_{Fault}}\right)^2 - \frac{1}{2nL_{Fault}C_{p2}}} \tag{5.19}$$

For a high fault resistance, the eigenvalues are real and the characteristic solution is given by (5.8). However, also for rather high fault resistance, the poles are complex due to the fact that $L_{Fault} >> C_{p2}$. In this case, the poles are expressed as

$$\lambda_{1,2} = \sigma_0 \pm j\omega_0 \tag{5.20}$$

If the switch state is averaged, the following is valid

$$\bar{s} = d = \frac{1}{2}\left(1 + \frac{\hat{u}}{V_{dc}/2} \cdot \sin\omega_1 t\right) = \frac{1}{2}\left(1 + \hat{d} \cdot \sin\omega_1 t\right) \tag{5.21}$$

which gives the general solution

$$\begin{aligned} v_{Cp2} = &\left(A \cdot \cos\left(\omega_0 (t - t_0)\right) + B \cdot \sin\left(\omega_0 (t - t_0)\right)\right) \cdot e^{\sigma_0 (t - t_0)} + \frac{V_{dc}}{2} + \\ &+ \frac{V_{dc}}{2n} \cdot \frac{\left(1/2n - \omega_1^2 L_{Fault} C_{p2}\right)\sin\omega_1 t - \omega_1 R_{Fault} C_{p2} \cos\omega_1 t}{\left(1/2n - \omega_1^2 L_{Fault} C_{p2}\right)^2 + \left(\omega_1 R_{Fault} C_{p2}\right)^2} \cdot \frac{\hat{d}}{2} \end{aligned} \tag{5.22}$$

The constants A and B are determined by the initial conditions, which are dependent on the time instant when the fault occurs. However, it is also seen that there is a stationary solution, which is not damped, but remains. This solution is obtained also for real eigenvalues. Only this part of the solution is investigated further. The capacitor current in the case of high fault resistance is approximately given by

$$i_{Cp2} = C_{p2}\frac{dv_{Cp2}}{dt} \approx \frac{V_{dc}/2}{2nR_{Fault}} \cdot \hat{d} \cdot \sin\omega_1 t \tag{5.23}$$

Consequently, the fault current is

$$i_{Fault} = 2n \cdot i_{Cp2} \approx \frac{V_{dc}/2}{R_{Fault}} \cdot \hat{d} \cdot \sin\omega_1 t \tag{5.24}$$

5.3 Detection and selectivity

When a ground fault occurs, the fault current at the cable and converter interfaces of the cable nodes flow in the same direction. In other words, a ground fault results in common mode currents. If the fault resistance is low, a high common mode current flows. This is easily detected by subtraction of the cable currents. If the fault resistance is high, simple subtraction is not feasible, due to noise and offset. Therefore, two differential current measurements are made at each converter node (Figure 5.7). The transducers measuring differential currents could be placed so that the common mode current flowing into the cable node, from each cable segment, is measured instead. This is further discussed at the end of the chapter. The voltage across the capacitors could also be measured to detect a ground fault, but not to localise the fault [54].

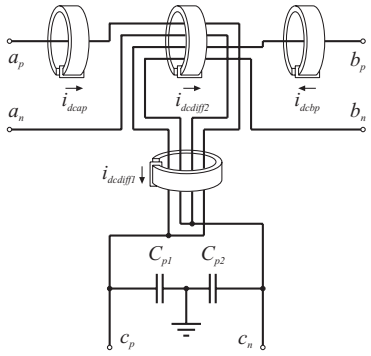

Figure 5.7: Detail of the placement of the current transducers in the cable nodes. The interfaces are denoted *A* (*left*), *B* (*right*) and *C* (*bottom*).

With reference to Figure 5.7, the differential currents $i_{dcdiff1}$ and $i_{dcdiff2}$ are measured so that

$$\begin{cases} i_{dcdiff1} = i_{dcap} + i_{dcan} + i_{dcbp} + i_{dcbn} \\ i_{dcdiff2} = i_{dcap} + i_{dcan} - i_{dcbp} - i_{dcbn} \end{cases} \tag{5.25}$$

To circumvent the problem of calculating the difference between two fault currents resulting in a low difference, the measurements are differential as previously mentioned. The resulting winding schemes for the transducer coils are shown in Figure 5.7.

Short circuit

Short circuit is detected by measuring over-current both for the DC and AC sides. For the DC side, the current in the positive rails of the cable interfaces at the node, i.e. i_{dcap} and i_{dcbp} in Figure 5.7, are measured. When over-current is detected, the direction to the fault is also determined. On the AC side, over-current is detected by the transducers measuring at least two of the phase currents required for vector control (Appendix B). Each cable node is equipped with a controller for decision on appropriate action when a fault is detected. Communication between the cable nodes can also be used to distinguish the location of the fault. The need for communication is further discussed later in this section.

Ground fault on the DC side

Some interesting observations are made for ground faults on the DC side. When the magnitude of $i_{dcdiff2}$ is higher than twice the magnitude of $i_{dcdiff1}$, then the fault is a ground fault on the DC ring bus, and not between the cable node and AC source. If $i_{dcdiff1}$ is negative, the ground fault is between the positive rail of the DC bus and ground. If $i_{dcdiff1}$ is positive, the ground fault is between the negative rail of the DC bus and ground. When $i_{dcdiff1}$ and $i_{dcdiff2}$ have the same sign, i.e. both are positive or both are negative, the ground fault is on the *A*-side of the cable node (Figure 5.1 and Figure 5.7). If $i_{dcdiff1}$ and $i_{dcdiff2}$ have opposite sign, the ground fault is on the *B*-side of the cable node.

When communication with nearby converters is used, the observations above are used to detect that a DC bus ground fault is present and also the location, since one of the cable nodes at the faulted cable segment indicates fault on its *A*-side and the other at the same cable segment indicates fault on its *B*-side.

If communication between nearby converters is not utilised, fault localisation is more complex. In this case, the fault currents $i_{dcdiff1}$ and $i_{dcdiff2}$ are instead integrated when $i_{dcdiff1}$ exceeds a certain threshold level signalling a fault situation. Now, the idea is to create an integral, increasing with the same speed for the cable nodes close to the fault but considerably slower for the cable nodes far from the fault location. There are two reasons why this is important. Firstly, the fault indicator should be significant so the correct cable nodes detect the fault first and disconnects the cable segment. Secondly, the circuit breakers have a rather long operational time, which implies that cable nodes far from the fault location also might detect the fault before it is cleared by the most appropriate cable nodes.

In the case of an unbroken DC ring bus, the fault current flows to the fault location from both ends of the cable segment with approximately the same magnitude but with opposite sign. This means that $i_{dcdiff2}$ will have highest amplitude for the cable nodes close to the fault. If the protection capacitors are of equal capacitance these two currents are given by

$$\left| i_{dcdiff2} \right| = (n-1) \cdot \left| i_{dcdiff1} \right| = 2(n-1) \cdot \left| i_{Cp} \right| \tag{5.26}$$

The corresponding time integral is given by

$$\left| \int_0^\infty i_{dcdiff2}\, dt \right| = (n-1) \cdot 2 \left| \int_0^\infty i_{Cp} dt \right| = (n-1) \cdot 2C_p \frac{V_{dc}}{2} = (n-1) \cdot C_p V_{dc} \tag{5.27}$$

For the cable node next to the faulted cable node away from the fault, the corresponding current is

$$\left| i_{dcdiff2} \right| = (n-3) \cdot \left| i_{dcdiff1} \right| = 2(n-3) \cdot \left| i_{Cp} \right| \tag{5.28}$$

or in more general terms

$$\left| i_{dcdiff2} \right| = (n-(2n_c+1)) \cdot \left| i_{dcdiff1} \right| = 2(n-(2n_c+1)) \cdot \left| i_{Cp} \right| \tag{5.29}$$

where n_c is the number of cable segments between the cable node and the fault. This means that for a low number of cable nodes, $i_{dcdiff2}$ is just integrated and the trip level is determined as

$$(n-3) \cdot C_p V_{dc} < \left| \int i_{dcdiff2}\, dt \right|_{\text{Trip level}} < (n-1) \cdot C_p V_{dc} \tag{5.30}$$

Already from the previous expression, it is clear that this method is complicated to implement in the case of high number of cable nodes. Firstly, the trip current is high for high n and the fault current levels, for the different cable nodes, are close to each other in magnitude. Secondly, the integral for an unfaulted cable node might reach the trip current while the circuit breaker is operated for the faulted cable node due to the long operation time for present circuit breakers.

The situation becomes worse when one fault is already cleared and the ring structure is broken. Now, $i_{dcdiff2}$ is not determined by the total number of cable nodes but by the number of cable nodes at each side of the fault. Therefore, the appropriate trip current level cannot be estimated.

However, if each converter assumes a worst-case scenario, this might be solved. To do this, each $i_{dcdiff2}$ integral is multiplied with a constant so that the circuit breaker is operated when

$$\left| k_i \cdot \int_0^{T_i} i_{dcdiff2,i}\, dt \right| = \left| k_i (2i-1) \int_0^{T_i} i_{dcdiff1}\, dt \right| = I_{Trip} \tag{5.31}$$

where i is the order of the cable node (i=1 for the cable nodes where the bus is already broken), which is dependent on the direction of the fault current since

$$(2i-1) = \frac{\left| \int i_{dcdiff2,i}\, dt \right|}{\left| \int i_{dcdiff1}\, dt \right|} \tag{5.32}$$

and T_i is the trip time. The idea is that the gain k_i should be selected in such a way that the fault conditions are evaluated sequentially. This means that a cable node is not allowed to disconnect a cable segment unless it can guarantee that if the fault should be disconnected by a cable node downstream, it would already have been done and the fault current would not flow anymore. The same trip level I_{Trip} is used for all the cable nodes. Therefore,

$$\left| k_i (2i-1) \int_0^{T_i} i_{dcdiff1}\, dt \right| \geq I_{Trip} \geq \left| k_{i-1} (2(i-1)-1) \int_0^{T_{i-1}} i_{dcdiff1}\, dt \right| \tag{5.33}$$

where

$$T_{i-1} \geq T_i + T_{sc} \tag{5.34}$$

where T_{sc} is the operation time for the circuit breaker. Thus

$$\left(k_i(2i-1) - k_{i-1}(2(i-1)-1)\right) \cdot \left| \int_0^{T_i} i_{dcdiff1}\, dt \right| \geq k_{i-1}(2(i-1)-1) \cdot \left| \int_{T_i}^{T_i+T_{sc}} i_{dcdiff1}\, dt \right| \tag{5.35}$$

If it is assumed that the time constant of the fault current is long compared to the time needed to operate the relay multiplied by the number of cable nodes, i.e.

$$\tau_2 = \frac{1}{-\lambda_2} >> nT_{sc} \tag{5.36}$$

it can be assumed that the fault current is constant during a time interval equal to T_{sc}. This yields

$$\left(k_i(2i-1)-k_{i-1}(2i-3)\right)\cdot(T_i)\geq k_{i-1}(2i-3)\cdot(T_{sc}) \tag{5.37}$$

which implies that the detection time for cable node *i* is determined from

$$T_i \geq \frac{k_{i-1}(2i-3)}{\left(k_i(2i-1)-k_{i-1}(2i-3)\right)}\cdot T_{sc} \tag{5.38}$$

For the cable node most far from the fault location, i.e. the one at the upstream end, the time is given by

$$T_1 \geq T_2 + T_{sc} \geq \frac{k_1}{(3k_2-k_1)}\cdot T_{sc} + T_{sc} = \frac{3k_2}{(3k_2-k_1)}\cdot T_{sc} \tag{5.39}$$

This cable node should detect the fault last. Since there are, at most, *n*-1 cable segments, the time required for detection is

$$T_1 \geq (n-1)T_{sc} \tag{5.40}$$

and assuming equality gives

$$\frac{3k_2}{(3k_2-k_1)} = n-1 \tag{5.41}$$

which yields the constant

$$k_2 = \frac{n-1}{3(n-2)}k_1 \tag{5.42}$$

or

$$k_i = \frac{(2(i-1)-1)}{(2i-1)}\cdot\left(1+\frac{1}{n-i}\right)\cdot k_{i-1} \tag{5.43}$$

for the general case. If it is assumed that k_1=1 then

$$k_i = \prod_{j=1}^{i-1}\frac{(2j-1)}{(2j+1)}\cdot\left(1+\frac{1}{n-j-1}\right) \tag{5.44}$$

The appropriate trip time is found for each cable node by multiplying the gain determined above and the integral of the differential current $i_{dcdiff2}$, when the trip level is the same for all the nodes. As a result, each cable node waits a time period proportional to the number of cable nodes in the direction of the fault current. This functionality could also be implemented as a pure time delay. However, the described method is only applicable if the time constant of the fault current is long compared to the number of cable segments multiplied by the circuit breaker operation time. Otherwise, the fault detector cannot distinguish between fault current removal due to discharged protection capacitors or circuit breaker operation.

The most secure operation to do when a second fault is detected is to shut down the entire ring bus. This might seem like a drastic solution but if one ground fault already has occurred, the system needs service anyway. The other method, relying on communication between nearby converters or cable nodes, do not suffer from this kind of problem and the DC distribution system could be segmented down to converters operating in pairs without any problem. It is likely that the interest for such an option is dependent of the number of converters operating on the DC ring bus as this determines the need for this kind of island operation.

Ground fault on the AC side

Similar to the previous section on ground faults on the DC side, a number of observations are made for ground faults on the AC side. When the magnitude of $i_{dcdiff1}$ is higher than the magnitude of $i_{dcdiff2}$, the fault is a ground fault on the AC side of the particular converter connected to the ring bus. The magnitude of $i_{dcdiff1}$ is time dependent due to the sinusoidal voltage. In the same way as for a DC side fault, the sign combination of $i_{dcdiff1}$ and $i_{dcdiff2}$ determines the direction to fault for each cable node. Therefore, if $i_{dcdiff1}$ and $i_{dcdiff2}$ have the same sign, the fault is located to the left of the cable node, i.e. on its *A*-side. If $i_{dcdiff1}$ and $i_{dcdiff2}$ have opposite sign, the fault is located to the right of the cable node, i.e. on its *B*-side. Selectivity is provided also in this case since the converter with a faulted AC side does not signal a DC fault to other cable nodes. Consequently, only the cable node at the fault location detects the fault accurately as a being an AC side fault. However, the false DC bus ground fault detected by other converters is not acknowledged and no attempts to clear the detected but non-existent DC bus fault is made. This implies that communication yields the same advantage in detection of AC side faults as for DC side faults.

5.4 Simulations

As a result of the previous investigation, communication is utilised in the simulations. Without communication, one ground fault allows further operation. For a second fault, the system should be shut down, because selectivity cannot be guaranteed. When communication is utilised, there is no such limitation. As a matter of fact, the DC network can be segmented down to converters operating in pairs.

The trip limit used for the integrated fault currents is selected as

$$I_{trip} = \frac{1}{2} \cdot C_p V_{dc} = \left| \int_0^\infty i_{Cp}\, dt \right| \tag{5.45}$$

Since the magnitude of the differential fault currents $i_{dcdiff1}$ and $i_{dcdiff2}$ are at least twice the current magnitude of the protection capacitors, the trip level is reached also for n=2. This is important in the case of a heavily segmented DC distribution system. The capacitance of the protection capacitors is determined so that the time to detect a high impedance fault is limited to prevent from personal injury. Furthermore, the time constant should be sufficiently long for proper detection of low impedance faults close to the cable node for a low number of cable nodes. To satisfy both demands, the capacitance should be selected from the time required for detection of a high impedance fault with fault resistance corresponding to the resistance of a human being. Here, this resistance is assumed to equal 3000 Ω. For a high impedance fault

$$\left| i_{dcdiff2} \right| = \frac{2(n-1)}{2n} \cdot i_{Fault} \approx \frac{(n-1)}{n} \cdot \frac{V_{dc}/2}{R_{Fault}} \tag{5.46}$$

for the cable nodes connected to the faulty cable segment. For a heavily segmented DC distribution bus (n=2), the time to detect a fault is

$$t_{detect} = \frac{I_{trip}}{\left| i_{dcdiff2} \right|} = 2 \cdot C_p R_{Fault} \tag{5.47}$$

For C_p=10 μF this implies that t_{detect}=60 ms. The circuit breaker operating time should be added to get the total time to clear the fault. This time is often in the range of 20 ms. Here, 10 ms is used due to the non-inductive

characteristic of cables. The relays are modeled as variable resistors with on-state resistance of 1.0 mΩ, and an off-state resistance of 1.0 MΩ. The transition between these two states is modeled as linear with respect to time.

To ensure that low impedance faults are detected, a resistor is connected in series with each protection capacitor. In this case, 100 Ω is recommended, which yields a minimum time constant of 1 ms for the fault current. In [60], a purely resistive grounding system is used to limit the fault current to prevent humans from electric shock.

The differential fault currents $i_{dcdiff1}$ and $i_{dcdiff2}$ and the positive rail currents i_{dcap} and i_{dcbp}, with reference to Figure 5.7, are measured. Note that the measured fault currents are low-pass filtered with break-over frequency of 500 Hz to attenuate switching frequency disturbances. The differential fault currents are integrated if they exceed a certain limit. The limit is set equal to the maximum offset of the current transducers, which is assumed to be 10 mA. Thus,

$$I_{idcdiff1,k} = \begin{cases} \gamma I_{idcdiff1,k\text{-}1} + t_{sample} \cdot i_{dcdiff1,k} & \text{if} \quad \left| i_{dcdiff1,k} \right| > i_{offset} \\ \gamma I_{idcdiff1,k\text{-}1} & \text{else} \end{cases} \tag{5.48}$$

and

$$I_{idcdiff2,k} = \begin{cases} \gamma I_{idcdiff2,k\text{-}1} + t_{sample} \cdot i_{dcdiff2,k} & \text{if} \quad \left| i_{dcdiff2,k} \right| > i_{offset} \\ \gamma I_{idcdiff2,k\text{-}1} & \text{else} \end{cases} \tag{5.49}$$

where γ is a forgetting factor. The forgetting factor is set based on the fault signal reset time according to

$$\gamma = 1 - \frac{t_{sample}}{t_{reset}} \tag{5.50}$$

A suitable reset time is 1 s. Ground faults are detected through

$$\begin{aligned} GroundFault_A = & \Big(\big(\big(I_{idcdiff1,k} > 0 \big) \text{ and } \big(I_{idcdiff2,k} > I_{trip} \big) \big) \\ & \text{or } \big(\big(I_{idcdiff1,k} < 0 \big) \text{ and } \big(I_{idcdiff2,k} < -I_{trip} \big) \big) \big) \\ & \text{and } \big(\left| I_{idcdiff1,k} \right| < \left| I_{idcdiff2,k} \right| \big) \end{aligned} \tag{5.51}$$

$$\begin{aligned} GroundFault_B = & \left(\left(\left(I_{idcdiff1,k} < 0\right) \text{ and } \left(I_{idcdiff2,k} > I_{trip}\right)\right)\right. \\ & \text{or } \left.\left(\left(I_{idcdiff1,k} > 0\right) \text{ and } \left(I_{idcdiff2,k} < -I_{trip}\right)\right)\right) \\ & \text{and } \left(\left|I_{idcdiff1,k}\right| < \left|I_{idcdiff2,k}\right|\right) \end{aligned} \tag{5.52}$$

In this application there is no distinction between ground fault on the converter DC side (*C*) and the converter line side (*AC*) interfaces. Instead

$$GroundFault_C = \left(\left(I_{idcdiff1,abs,k} > I_{trip}\right) \text{ and } \left(\left|I_{idcdiff1,k}\right| > \left|I_{idcdiff2,k}\right|\right)\right) \tag{5.53}$$

is used for both. The integral of the absolute value of $i_{dcdiff1}$ is calculated according to

$$I_{idcdiff1,abs,k} = \begin{cases} \gamma I_{idcdiff1,k\text{-}1} + t_{sample} \cdot \left|i_{dcdiff1,k}\right| & \text{if } \left|i_{dcdiff1,k}\right| > i_{offset} \\ \gamma I_{idcdiff1,k\text{-}1} & \text{else} \end{cases} \tag{5.54}$$

Short circuit faults are detected by evaluation of

$$ShortCircuit_A = \left(i_{dcap,k} < -i_{Cable,max}\right) \tag{5.55}$$

$$ShortCircuit_B = \left(i_{dcbp,k} < -i_{Cable,max}\right) \tag{5.56}$$

$$ShortCircuit_C = \left(\left(i_{dcap,k} > i_{Cable,max}\right) \text{or } \left(i_{dcbp,k} > i_{Cable,max}\right)\right) \tag{5.57}$$

$$ShortCircuit_{AC} = \left(\left(\left|i_{a,k}\right| > i_{line,max}\right) \text{or } \left(\left|i_{b,k}\right| > i_{line,max}\right)\right) \tag{5.58}$$

For $ShortCircuit_{AC}$ only two phase currents are evaluated since only two are needed for vector control purposes, assuming that the zero-sequence current equals zero. The following logical variables are set if a fault is detected

$$\begin{aligned} & LocalFault_A = \\ & \left(\left(\text{not } Disconnected_A\right) \text{and } \left(GroundFault_A \text{ or } ShortCircuit_A\right)\right) \end{aligned} \tag{5.59}$$

$$\begin{aligned} & LocalFault_B = \\ & \left(\left(\text{not } Disconnected_B\right) \text{and } \left(GroundFault_B \text{ or } ShortCircuit_B\right)\right) \end{aligned} \tag{5.60}$$

$$\begin{aligned} & LocalFault_C = \\ & \left(\left(\text{not } Disconnected_C\right) \text{and } \left(GroundFault_C \text{ or } ShortCircuit_C\right)\right) \end{aligned} \tag{5.61}$$

The variables *Disconnect* are used to start a relay disconnect operation. The variables *Disconnected* are held also after the fault is cleared.

$$Disconnect_A = (LocalFault_A \text{ and } RemoteFault_A) \tag{5.62}$$

$$Disconnected_A = (Disconnect_A \text{ or } Disconnected_A) \tag{5.63}$$

$$Disconnect_B = (LocalFault_B \text{ and } RemoteFault_B) \tag{5.64}$$

$$Disconnected_B = (Disconnect_B \text{ or } Disconnected_B) \tag{5.65}$$

$$Disconnect_C = LocalFault_C \tag{5.66}$$

$$Disconnected_C = (Disconnect_C \text{ or } Disconnected_C) \tag{5.67}$$

$$Disconnect_{AC} = (ShortCircuit_{AC} \text{ or } LocalFault_C) \tag{5.68}$$

$$Disconnected_{AC} = (Disconnect_{AC} \text{ or } Disconnected_{AC}) \tag{5.69}$$

The variables *RemoteFault* are set by the fault detectors in the remote end and transferred to the node in the direction of the fault. In this way, each cable node sends two signals and receives two signals for fault localisation. The relay operates on two signals, the *Disconnected* variable and one variable indicating the status of the fuses termed *FusesOK*.

$$Operate_A = (\text{not } Disconnected_A \text{ and } FusesOK_A) \tag{5.70}$$

$$Operate_B = (\text{not } Disconnected_B \text{ and } FusesOK_B) \tag{5.71}$$

$$Operate_C = (\text{not } Disconnected_C \text{ and } FusesOK_C) \tag{5.72}$$

$$Operate_{AC} = (\text{not } Disconnected_{AC} \text{ and } FusesOK_{AC}) \tag{5.73}$$

This implies that each cable node must collect four additional signals for each set of fuses.

To verify the previous statements several cases are investigated in simulations. First, a case with a 1.0 Ω ground fault between the positive supply rail and ground is simulated. The fault occurs between converter 1 and 2 at t=1.0 ms, see Figure 5.8.

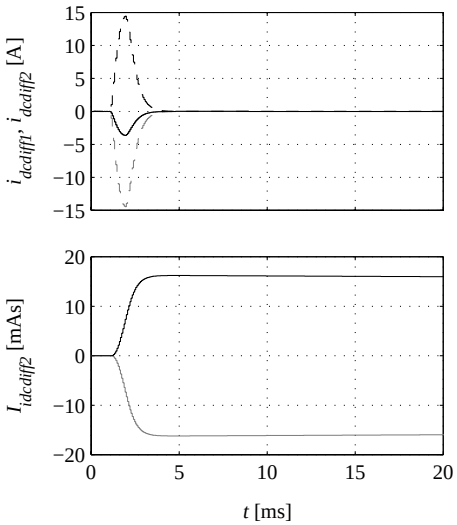

Figure 5.8: *Top*: Fault currents $i_{dcdiff1}$ (*solid*) and $i_{dcdiff2}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a ground fault on the DC side (positive supply rail-to-ground) between converters 1 and 2 at t=1.0 ms. *Bottom*: Integrated fault current $I_{idcdiff2}$ for converters 1 (*black*) and 2 (*grey*). The fault resistance R_{Fault} is equal to 1.0 Ω.

A ground fault on the DC side is detected by the fact that $I_{idcdiff2}$ reaches the trip limit I_{trip}=3.75 mAs, according to (5.45), see Figure 5.8. The integral continues to increase beyond the trip limit due to the comparably long operation time of the relays. The sign determines the direction to the fault location. The result of the same simulation with fault resistance equal to 3.0 kΩ, is shown in Figure 5.9. From both fault situations it is apparent that the sign combination of the differential currents indicates that cable node 1 detects a fault on its *B*-side and cable node 2 on its *A*-side. The fault is detected and localised. If the ring bus is broken due to a previous fault, the differential currents do not have equal magnitude for the two cable nodes, which implies that the fault is not detected simultaneously.

Figure 5.10 shows the differential currents $i_{dcdiff1}$ and $i_{dcdiff2}$ in the case of a low impedance ground fault on the AC side (1.0 Ω between *R*-phase and ground). Note that cable node 2 detects a ground fault on its *A*-side since both $i_{dcdiff1}$ and $i_{dcdiff2}$ are negative and the absolute value of $i_{dcdiff2}$ is higher than the one of $i_{dcdiff1}$. Cable node 1 detects the fault as a ground fault on the AC side and does not send a fault signal to cable node 2. The fault indicator in this case is calculated as the time integral of the absolute value of the differential current $i_{dcdiff1}$.

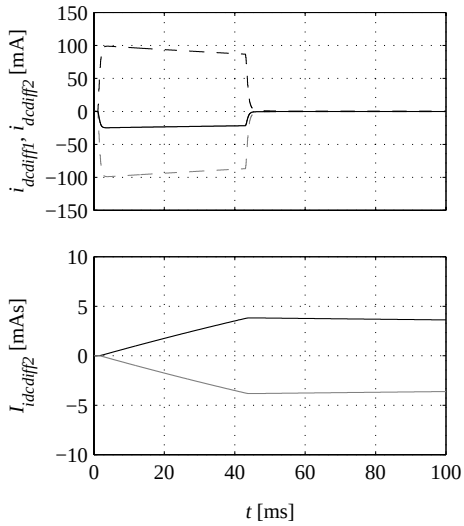

Figure 5.9: *Top*: Fault currents $i_{dcdiff1}$ (*solid*) and $i_{dcdiff2}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a 3.0 kΩ ground fault on the DC side (positive supply rail-to-ground) between converters 1 and 2 at t=1.0 ms. *Bottom*: Integrated fault current $I_{idcdiff2}$ for converters 1 (*black*) and 2 (*grey*).

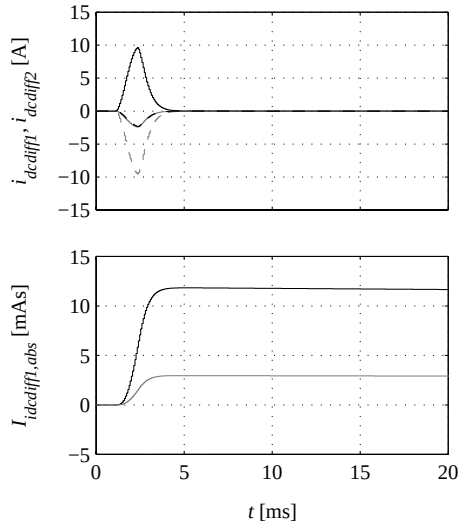

Figure 5.10: *Top*: Fault currents $i_{dcdiff1}$ (*solid*) and $i_{dcdiff2}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a 1.0 Ω ground fault on the AC side (*R*-phase-to-ground) of converter 1 at t=1.0 ms. *Bottom*: Integrated fault current $I_{idcdiff2}$ for converters 1 (*black*) and 2 (*grey*).

The reason for calculating the integral of the absolute differential current, to determine the trip instant, is not obvious in the case of low fault impedance. However, if the same simulation is made with a ground fault impedance of 3.0 kΩ (Figure 5.11), it is found that the differential currents are AC quantities. Therefore, the absolute value is used. The AC component could also be filtered out, which gives the possibility to distinguish between faults on the AC side and the converter-to-cable connection (*C* interface).

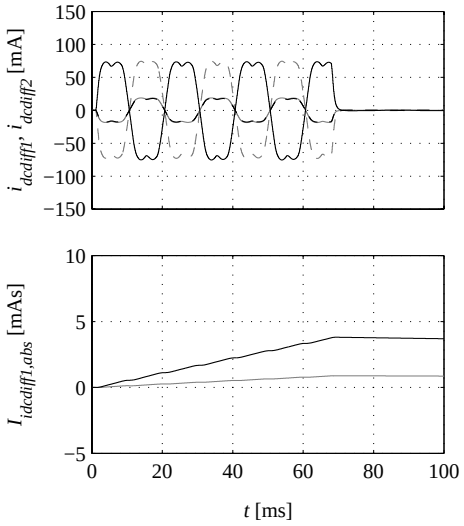

Figure 5.11: *Top*: Fault currents $i_{dcdiff1}$ (*solid*) and $i_{dcdiff2}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a ground fault on the AC side (*R*-phase-to-ground) of converter 1 at t=1.0 ms. *Bottom*: Integrated fault current $I_{idcdiff2}$ for converters 1 (*black*) and 2 (*grey*). The fault resistance R_{Fault} is equal to 3.0 kΩ.

Multiple faults

The ground fault protection scheme should work for multiple faults. Therefore, a case with two low impedance faults (1.0 Ω) is simulated. First, a short circuit occurs on the DC bus between converters 4 and 5 at time t=1.0 ms. Second, at t=11.0 ms, a ground fault occurs between the positive supply rail of the DC bus and ground. The fault currents for converter 1 and 2 are shown in Figure 5.12. It is evident from Figure 5.12 that the magnitude of $i_{dcdiff2}$ is no longer equal for the two cable nodes. This is a consequence of the fact that the ring bus is broken, resulting in an unequal number of cable nodes contributing to the fault current, on each side of the fault.

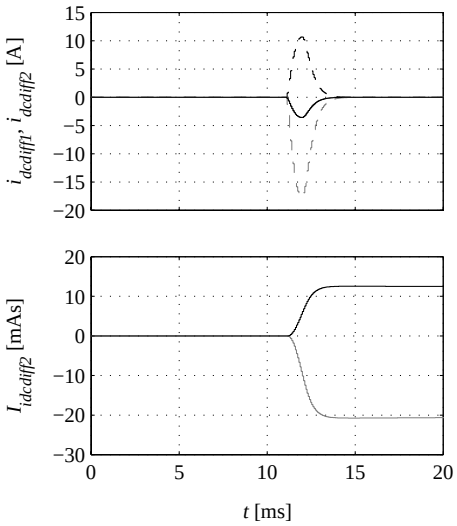

Figure 5.12: *Top*: Fault currents $i_{dcdiff1}$ (*solid*) and $i_{dcdiff2}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a ground fault on the DC side (positive supply rail-to-ground) between converter 1 and 2 at t=11.0 ms. *Bottom*: Integrated fault current $I_{idcdiff2}$ for converters 1 (*black*) and 2 (*grey*). The fault resistance R_{Fault} is equal to 1.0 Ω. Note that the ring bus is broken between converters 4 and 5 due to a short circuit occurring at t=1.0 ms.

Of course, the short circuit fault current does appear in the differential currents of Figure 5.12. The time integrals of the differential fault currents are also shown in Figure 5.12. Because the fault current magnitudes of $i_{dcdiff2}$ differ, the time integrals reach the trip level at different time instants. Consequently, cable node 2 is aware of the fault prior to cable node 1. However, cable node 2 waits until cable node 1 acknowledges the fault situation before the circuit breakers are operated.

Limitations

Note that for large DC distribution systems, i.e. with a high number of cable nodes, the ground current $i_{dcdiff1}$ might be below the offset level of the transducer. This means that the fault is not accurately detected. To circumvent this problem the differential currents $i_{dcdiffa}$ and $i_{dcdiffb}$ according to

$$\begin{cases} i_{dcdiffa} = i_{dcap} + i_{dcan} \\ i_{dcdiffb} = i_{dcbp} + i_{dcbn} \end{cases} \tag{5.74}$$

could be measured instead. The measurement is made differential, i.e. the current transducers are connected to measure the current sum directly in a similar way as for the scheme shown in Figure 5.7. This method also suffers from a problem, although less severe. Consider a case where the ring bus structure is not used or have been broken due to a previous fault and a second fault occurs at the last segment of the bus. The differential current $i_{dcdiffa}$ or $i_{dcdiffb}$ flowing from the end of the bus could be lower than the offset level, in the case of high impedance faults for a large distribution system. Figure 5.13 shows the differential currents $i_{dcdiffa}$ and $i_{dcdiffb}$ for the same simulation as shown in Figure 5.12.

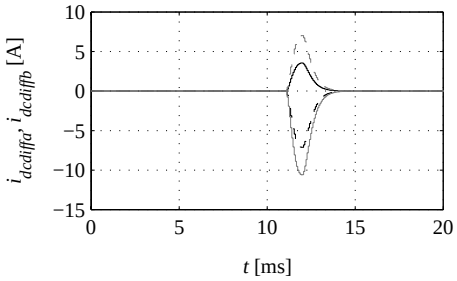

Figure 5.13: Fault currents $i_{dcdiffa}$ (*solid*) and $i_{dcdiffb}$ (*dashed*) for converter 1 (*black*) and converter 2 (*grey*) in the case of a ground fault on the DC side (positive supply rail-to-ground) between converter 1 and 2 at t=11.0 ms. The fault resistance R_{Fault} is equal to 1.0 Ω. Note that the ring bus is broken between converters 4 and 5 due to a previous fault.

The ratio between the trip current levels of the scheme where $i_{dcdiffa}$ and $i_{dcdiffb}$ are used, compared to the scheme where $i_{dcdiff1}$ and $i_{dcdiff2}$ are used, is given by

$$I_{Trip,ratio} = \frac{k}{2(k-0.5)} \tag{5.75}$$

where k is the number of cable nodes on the side with the lowest number of cable nodes at the fault location. For an unbroken ring bus

$$k = \frac{n}{2} \tag{5.76}$$

even if the total number of cable nodes n is odd. In the simulation where $i_{dcdiffa}$ and $i_{dcdiffb}$ are used for a five-converter system, this means that the equivalent trip current level compared to (5.45) is equal to a trip current ratio of 2/3, i.e.

$$I_{trip} = \frac{1}{3} \cdot C_p V_{dc} \tag{5.77}$$

For a very high number of cable nodes, (5.75) approaches 0.5. This means that a suitable trip limit for this scheme is given by

$$I_{trip} = \frac{1}{4} \cdot C_p V_{dc} \tag{5.78}$$

which yields at least the same performance in terms of detection time as the scheme where $i_{dcdiff1}$ and $i_{dcdiff2}$ are used.

Chapter 6

DC transmission

In the same manner as for present AC power transmission systems, DC power transmission should be operated at high voltage levels in order to reduce ohmic losses and this is done in, for example, HVDC. Galvanic separation is required for large DC distribution systems to circumvent the risk of elevated voltage levels occurring in the low voltage parts of a DC distribution system in the case of a ground fault located in high voltage parts. Also, some of the fault detection methods are only applicable for a low number of cable nodes due to the relatively low difference between incoming and outgoing fault current in the case of a large number of cable nodes, which is explained in Chapter 5.

In this chapter, two different schemes for DC power transmission between two DC distribution systems are investigated. One of the schemes is similar to VSC based HVDC and the other is based on the double active bridge (DAB) converter introduced in [18]. The schemes are referred to as the back-to-back and DAB structures, respectively.

6.1 The back-to-back structure

The circuit schematic and control for the back-to-back transmission structure are discussed in this section. Also, simulation results for a system of low complexity are shown.

Circuit schematic

The back-to-back structure is based on technology similar to VSC based HVDC. In this technology the low voltage sides are equipped with inductive filters, whereas the input filter to the DC bus should be capacitive. VSC based

HVDC is intended for an AC low voltage side, whereas a DC side is considered here. Even if bidirectional power flow is required, single half-bridge transistor converters could be used as interface between the different voltage levels. However, this could cause neutral current problems since one terminal of each DC system connected via the transmission bus is common. Since the DC-DC full-bridge converter, Figure 6.1, can be controlled to have an output in principle free of common mode components, it is preferred.

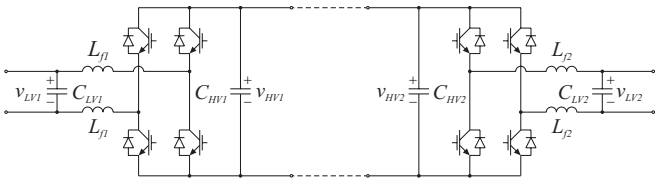

Figure 6.1: The investigated back-to-back converter structure, intended for DC transmission.

Control

The DC-DC converters in this scheme are equipped with basic current controllers similar to the three-phase current controllers derived in Appendix B. Bidirectional DC bus voltage controllers are implemented on top. The power flow direction can be set in two different ways. One way is to set the direction so that only one direction is allowed. The other way, which is implemented here, is by specifying the minimum (negative) and maximum (positive) power transfer limits. Note that either of these two could be set to zero, to force a unidirectional power flow. For normal operation, the power direction is set to flow from the higher (relative to the reference) to the lower (relative to the reference) voltage level. As shown in Chapter 3, a voltage overshoot might occur when the source output power changes, depending on the cable parameters. This implies that for transients, the sending end voltage might become lower than the receiving end voltage. This would cause a change of reference power direction, if no precautions are taken. Also for stationary operation there might be problems due to the resistive voltage drop of the converter stage. To circumvent this, a hysteresis controller with dead-band is employed in the reference direction algorithm. The width of the dead-band is proportional to the actual current flowing in the transmission bus. The low-pass filtered difference in p.u. DC bus voltage for the two sides is compared to a dead-band with limits specified from

$$\Delta v_{dc,limit} = 2R_{eq} i_{dc} \tag{6.1}$$

In this case, the equivalent resistance R_{eq} is given by the voltage drop of the converter and the resistance of the filter inductors, and considered as low. For the back-to-back scheme, this is not important but for the DAB scheme it is of great importance due to the transformer inserted between the converter stages. Figure 6.2 shows the algorithm for determining power flow direction.

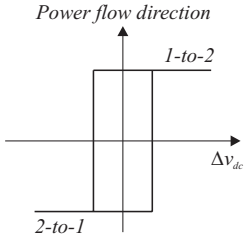

Figure 6.2: Dead-band for determination of power flow direction.

When the power flow direction is determined, the regular droop reference current is calculated in the same way as in Chapter 3. Note that the same type of converter could be used when DC electric energy storage elements, such as batteries or fuel cells, are employed.

Simulation

Figure 6.3 shows a simplified schematic of the simulated transmission system. The transmission bus has a rated power of 100 kW, which yields DC bus capacitors equal to 20 mF for the 750 V sides and 0.31 mF for the 6 kV side, according to (3.21). The filter inductors on each low voltage side have a total inductance of 10 mH and a total series resistance of 50 mΩ.

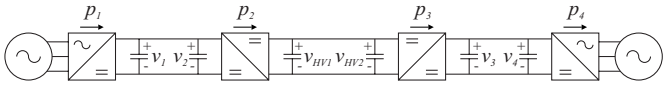

Figure 6.3: Back-to-back transmission system investigated in simulations.

The simulation results for the back-to-back transmission system of Figure 6.3 are shown in Figure 6.4, Figure 6.5 and Figure 6.6. All power references are positive from left to right (Figure 6.3). Solid lines are used for DC-DC converter quantities. For the leftmost AC-DC and DC-DC converters (index 1 and 2) the curves are black and for the rightmost AC-DC and DC-DC converters (index 3 and 4) the curves are grey. The quantities representing unit 1 and 3 are solid and for unit 2 and 4 they are dashed.

Figure 6.4 shows simulated low side voltage and power, in the case of back-to-back transmission.

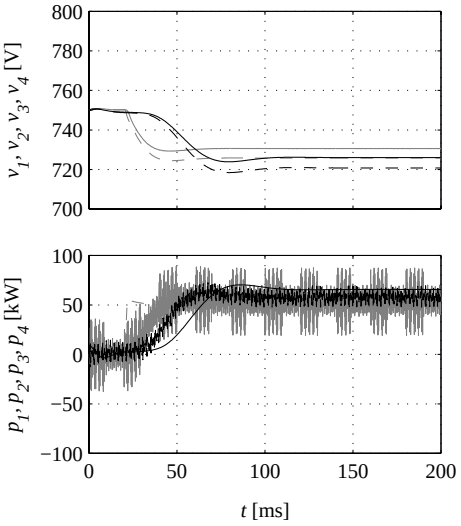

Figure 6.4: Simulated voltage (*top*) and power (*bottom*).

Due to the high current ripple in the inductors, the estimated power in Figure 6.4 also has a high content of switching frequency related harmonics. The variation in the ripple of estimated power p_3 is due to inductor current sampling distortion causing a distortion in the converter voltage reference for the low voltage side of unit 3. The only difference between the back-to-back converters, unit 2 and 3, are the sampling and switching frequencies. For unit 2, f_s=15 kHz and f_{sw}=7.5 kHz. For unit 3, f_s=10 kHz and f_{sw}=5 kHz. Consequently, the back-to-back transmission scheme is sensitive to controller parameters. The low-pass filtered estimated power is shown in Figure 6.5.

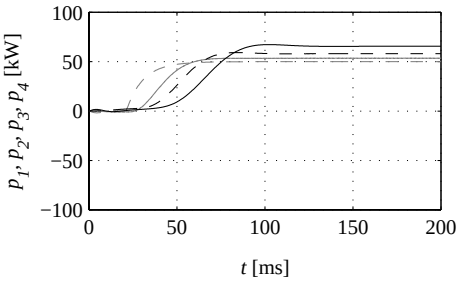

Figure 6.5: Simulated power (low-pass filtered).

Figure 6.6 shows the simulated high side voltage. The voltage drop along the transmission cable is low so the voltages are on top of each other in Figure 6.6.

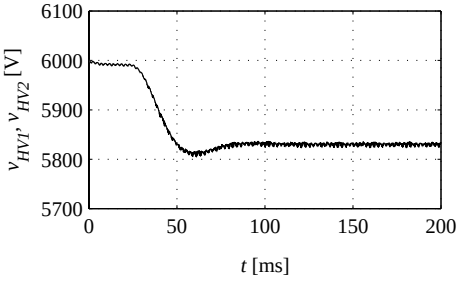

Figure 6.6: Simulated high side voltage.

6.2 The DAB structure

In this section, the schematic and control of the DAB transmission system are discussed. Simulation results for a minimal system are shown in the same way as for the previously investigated back-to-back system.

Circuit schematic

The DAB converter consists of two DC-DC full-bridge converters, connected front-to-front, with a transformer connected in between (Figure 6.7).

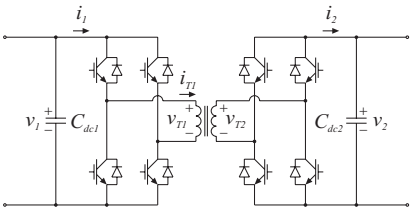

Figure 6.7: The investigated DAB structure, intended for connection of two DC ring buses with galvanic separation.

The DAB converter provides bidirectional power flow and also galvanic separation due to the transformer. The DAB converter is often designed to operate at high frequencies and in some cases also for resonant operation [69]. In this chapter the aim is to show that the DAB converter can be operated for transmission with the proposed voltage control algorithms. Therefore, high frequency and resonant operation are not considered.

To connect two DC power systems with galvanic isolation, only one DAB converter is needed. To connect two such systems with a high voltage DC transmission system, two DAB converters, i.e. four full-bridge converters and two transformers, are required (Figure 6.8).

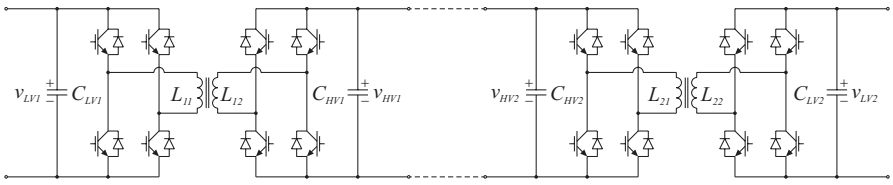

Figure 6.8: The investigated DC transmission structure utilising DAB converters. Both the DC ring bus side and transmission side of each DAB are truly capacitive.

Control

For a DAB, both converters are operated with the same controller. This means that the receiving end converter is not simply operated as an uncontrolled diode rectifier. Instead, the current controller calculates an appropriate phase lag between the gate signals of the two converters. The transistors of each converter are operated in pairs so that the lower or upper transistors of one of the converters of the DAB are not conducting simultaneously. In stationary conditions, the gate pulses of the receiving end lag the ones of the sending end converter. The time lag is used as control parameter in the simulations shown later in this chapter. The ideal waveforms for the DAB converter given in [18] are shown in Figure 6.9, with reference to Figure 6.7, to visualise the basic operation of the converter.

To control the DAB converter in DC transmission, a controller structure similar to the one used for three-phase converters according to Appendix B is employed. Similar to the controller found in [18], the relative delay is used as control variable instead of converter output voltage. The relative delay (with respect to the sampling time interval T_s) is calculated from

$$d = \frac{K'_p \cdot \left(i'_{ref} - i'_{lp}\right) + \frac{1}{T'_i} \cdot \sum \left(i'_{ref} - i'_{lp}\right) + K'_r \cdot i'_{lp} + \left(v'_2 - v'_1\right)}{2v'_2} \tag{6.2}$$

where i'_{lp} is a low-pass filtered version of the current i_{T1} in Figure 6.7. The break-over frequency of the low-pass filter is 500 Hz.

The controller parameters are

$$\begin{cases} K'_p = k_i L'/T_s = 0.25 L'/T_s \\ 1/T'_i = K'_p T_s R'/L' \\ K'_r = R' \end{cases} \tag{6.3}$$

where L' is the total stray and leakage inductance and R' is the total resistance referred to the primary. Note that a positive delay d implies that the primary side transistors should be trigged a time $d \cdot T_s$ before the corresponding transistors of the secondary side. Consequently, a negative delay d implies that the secondary side transistors should be trigged a time $-d \cdot T_s$ before the transistors of the primary side.

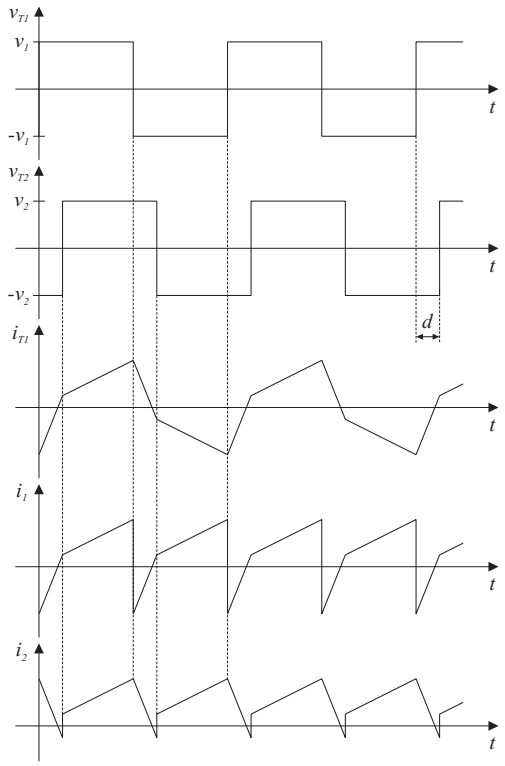

Figure 6.9: Ideal waveforms for the investigated DAB structure, intended for connection of two DC ring buses.

The dead-band is calculated in the same way as for the back-to-back counterpart, i.e.

$$\Delta v'_{dc,limit} = 2R'i'_{dc} \tag{6.4}$$

The dead-band is of great importance for this scheme due to the resistive and inductive voltage drop across the transformer, especially during transients.

Simulation of DAB for HVDC transmission

Figure 6.10 shows the simplified schematic of the simulated HVDC DAB system, which in this schematic form is equal to the back-to-back test system.

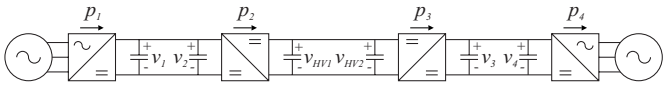

Figure 6.10: DAB transmission system investigated in simulations.

The simulation result for the DAB transmission system of Figure 6.10 is shown in this section. All power references are positive from left to right, see Figure 6.10. The data for the DAB converters are given in Table 6.1. The transformer short circuit resistance R_{sc} and self-inductance L_s are given for both the primary and secondary. The magnetic coupling factor k is assumed to be 0.99, see Table 6.1. The DC bus capacitance is given both for the low and high voltage sides. The cable data is the same as in Chapter 3 and Chapter 4.

Table 6.1: Simulation model data.

DAB no.	i	1	2
Rated power	P_n [kW]	100.0	100.0
Switching frequency	f_{sw} [kHz]	7.5	7.5
Transformer resistance	R_{sc} [Ω]	0.1/6.4	6.4/0.1
Transformer self-inductance	L_s [mH]	5/320	320/5
Magnetic coupling factor	k	0.99	0.99
DC bus capacitance	C_{dc} [mF]	20.0/0.31	0.31/20.0
Cable capacitance	C_{cable} [nF]	5.27	5.27
Cable inductance	L_{cable} [μH]	52.7	52.7
Cable resistance	R_{cable} [mΩ]	64.7	64.7
DC bus voltage reference (LV)	$V_{dc,ref,LV}$ [V]	750	750
DC bus voltage reference (HV)	$V_{dc,ref,HV}$ [V]	6000	6000

Figure 6.11 shows simulated voltage and power for the system in the case of a step in the output power of the load converter equal to 50 kW at t=20 ms. For the leftmost AC-DC and DC-DC converters (index 1 and 2) the curves are black and for the rightmost AC-DC and DC-DC converters (index 3 and 4) the curves for each quantity are grey. The quantities representing unit 1 and 3 are solid and for unit 2 and 4 they are dashed.

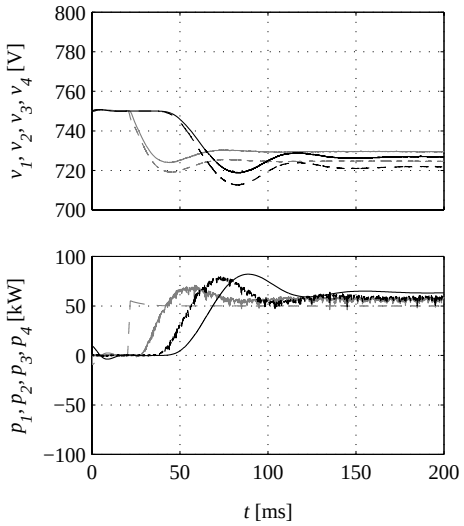

Figure 6.11: Simulated low side voltage (*top*) and power (*bottom*).

Figure 6.12 shows the low-pass filtered power, to be compared with the corresponding simulation result for the back-to-back structure, investigated in the previous section. The high side voltage in the case of DAB transmission is shown in Figure 6.13. Note that the two voltages shown in Figure 6.13 are on top of each other.

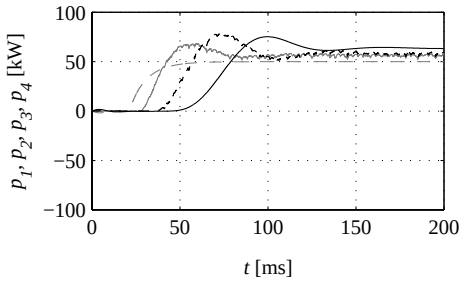

Figure 6.12: Low-pass filtered simulated power.

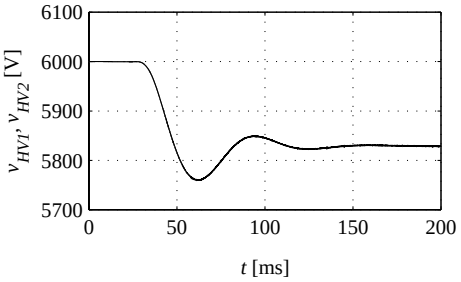

Figure 6.13: Simulated high side voltage.

6.3 Proposed interconnection structure

The DAB transmission structure is selected for the further analysis. This is due to several reasons. The galvanic isolation of the DAB is a desirable property since fault currents should not propagate through the entire DC distribution system. The DAB structure also provides a truly capacitive interface to the DC bus so that the converter input and output impedances, in p.u., are the same for all converters. The current ripple is lower than that of the back-to-back structure. Also, the thermal design of the filter inductor could be cumbersome for the back-to-back scheme. The DAB structure is also suitable for high frequency and resonant implementation [69].

Simulation of a DAB transmission system connecting two DC ring buses

Here, a system with two ring buses and an intermediate DAB transmission bus is investigated, see Figure 6.14. Note that in a realistic application, the transmission system could be radial and consist of more than two converters.

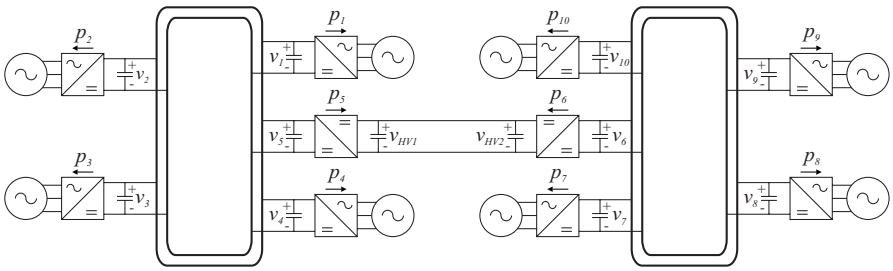

Figure 6.14: Two ring bus DAB transmission system investigated in simulations.

Each ring consists of four grid connected converters (not including the DAB low voltage converter), with data according to Table 6.2. The DAB converter data are found in Table 6.1.

Table 6.2: Simulation model data.

Converter no.	i	1, 2, 4, 7, 9	3, 8, 10
Rated power	S_n [kVA]	100.0	50.0
Line-to-neutral voltage	E_{LN} [V]	230	230
Line frequency	f_n [Hz]	50	50
Switching frequency	f_{sw} [kHz]	7.5	5.0
Line inductance	L_{line} [mH]	1.70	3.40
Line resistance	R_{line} [Ω]	0.25	0.25
DC bus capacitance	C_{dc} [mF]	20.0	10.0
Cable capacitance	C_{cable} [nF]	5.27	5.27
Cable inductance	L_{cable} [μH]	52.7	52.7
Cable resistance	R_{cable} [mΩ]	64.7	64.7
DC bus voltage reference	$V_{dc,ref}$ [V]	750	750

The system is simulated, starting from a no-load condition. The power references for units 1 and 3 are changed stepwise by 0.1 p.u. (unit base) at time equal to 10 and 20 ms, respectively. The power references for units 7 and 8 are changed stepwise by 0.2 p.u. (unit base) at time equal to 100 and 120 ms, respectively.

The magnitudes of the power reference steps are selected in such a way since it is desired to force a change in the direction of the power flow of the transmission bus. The simulation results are shown in Figure 6.15 and Figure 6.16, where the quantities for unit 1 and 6 are solid black, 2 and 7 are solid grey, 3 and 8 are dashed black, 4 and 9 are dashed grey, and 5 and 10 are dash-dotted black.

The simulated voltage and power for the transmission bus are shown in Figure 6.17. Note that the simulated power is low-pass filtered in Figure 6.17, but not in Figure 6.15 and Figure 6.16.

As seen in the simulation result, the DAB transmission system operates as intended. The power flowing through the transmission bus changes direction shortly after t=120 ms due to the applied load, as intended. Note the oscillations in the ring and transmission bus voltages. Due to the hysteresis in the algorithm for determining the direction of power flow it does not change in the simulation.

The transmission bus voltage controller presented here strives to share the total load democratic. To actually control the power flow, external references should be set. This implies that supervisory control and monitoring are needed.

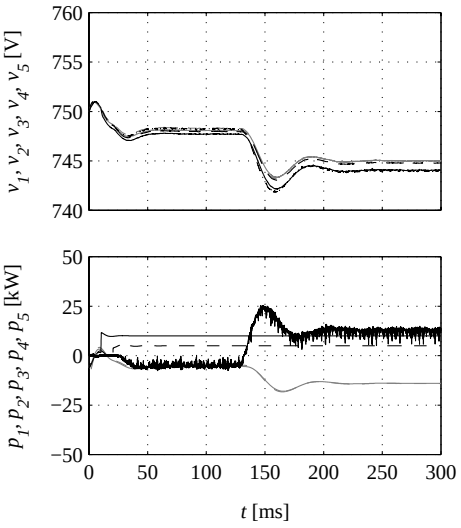

Figure 6.15: Simulated ring bus 1 voltage (*top*) and power (*bottom*).

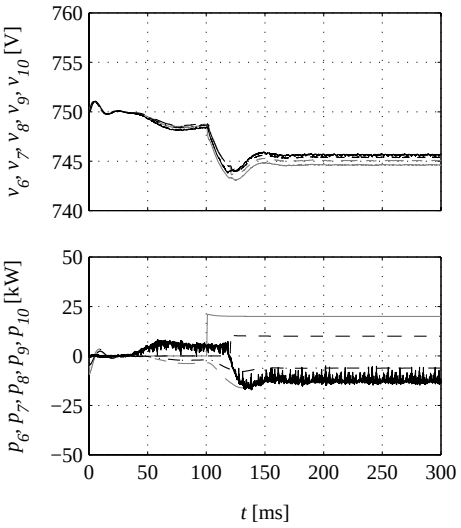

Figure 6.16: Simulated ring bus 2 voltage (*top*) and power (*bottom*).

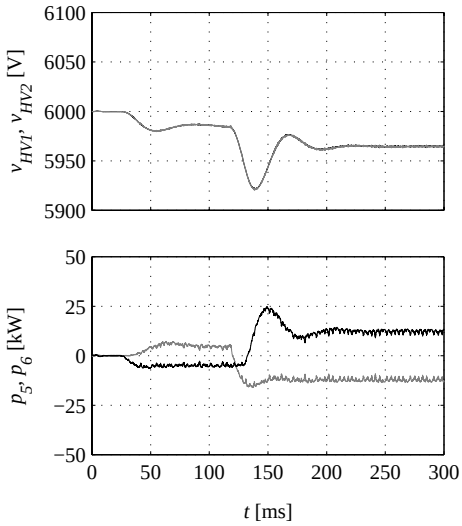

Figure 6.17: *Top*: Simulated DAB transmission bus voltages v_{HV1} (*black*) and v_{HV2} (*grey*). *Bottom*: Simulated low-pass filtered power of the DAB transmission, p_5 (*black*) and p_6 (*grey*).

Chapter 7

Measurements

In this chapter, a small experimental DC distributed power system is implemented based on the results of Chapter 3 and Chapter 5. Parts of the analysis in these chapters are verified in measurements. The experiments focus on dynamic properties of a two-converter system, and load sharing for a three-converter system. Measurement result of fault currents in the case of a high impedance fault for the three-converter system is also shown.

7.1 Experimental set-up

The experimental set-up is formed by three-phase converters connected to a 230 V, 50 Hz three-phase grid. As discussed in the previous chapters, the converters are galvanically separated on the AC line sides and, therefore, each converter is connected to the common three-phase grid through transformers. The transformers are connected *YNy* with a voltage ratio of 230/145. The neutral on the line side is used only for measuring the line voltage, required for the current controller (Appendix B). The reason for selecting such a low converter side voltage is that the maximum allowed DC bus voltage of the converters is equal to 300 V. With the same $V_{dc,ref}/E_{LL}$ ratio as in previous chapters, the DC bus voltage equals 270 V for a converter side line-to-line voltage of 145 V.

The data of the transformers are unfortunately not fully known. To avoid over-modulation (Appendix A) due to a transformer impedance higher than expected, the rated droop is reduced to half compared to the previous chapters, i.e. the rated droop is set to δ_n=0.025. This corresponds to reducing the damping to ζ_n=0.5. This gives the following specification of the voltage controllers

$$\begin{cases} V_{dc,ref} = 270\ \text{V} \\ \omega_{lp} = 2\pi 30\ \text{rad/s} \approx 188\ \text{rad/s} \\ \zeta_n = 1/2 \\ \delta_n = 0.025 \end{cases} \tag{7.1}$$

According to (3.21), the corresponding DC side capacitance to rated power ratio is given by

$$\frac{C_{dc,converter}}{P_{n,converter}} = 1536\ \mu\text{F/kW} \tag{7.2}$$

The DC bus voltage controller gain for each source converter is, thus, given by

$$K = 2\omega_{lp} C_{dc,converter} \tag{7.3}$$

The *R*- and *S*-phase currents flowing out from each converter are measured together with the DC bus voltage at each converter-to-DC bus interface. The converters are mounted in racks with two converters in each rack. Since only two AC voltage measurement transducer cards (giving voltage vectors in the stationary $\alpha\beta$-frame) are available, both converters of each rack must utilise the same voltage measurement to create the reference for the rotating *dq*-frame. This measurement is made on the line side of the transformers, to avoid the voltage drop of the transformer short circuit impedance.

Line side filter inductors of 3 mH each are inserted between each converter and transformer. The short circuit inductance of the transformer is estimated to 8 mH. The resistances of the filter inductors and transformers are estimated to 0.25 and 0.5 Ω per phase, respectively. The transformer stray inductance is not verified. The transformer short circuit resistance seems to be higher than first estimated, approximately equal to 0.9+0.4 Ω, from a DC measurement. The data used for the experimental set-up and simulation model are listed in Table 7.1.

In Table 7.1, both model and controller parameters are given. The parameters used in the controller should be equal in both simulation and experimental set-up. For the experimental set-up, the estimated parameters and the ones the controllers are based on are equal, which is also natural. However, as mentioned above the parameters are measured more thoroughly after the experiment and some deviations found, e.g. in the short circuit resistance.

Table 7.1: Measurement and simulation model data.

System data		Measurement		Simulation	
		Estimated,	Controller	Estimated,	Controller
Line-to-neutral voltage	E_{LN} [V]	84	84	84	84
Line frequency	f_n [Hz]	50	50	50	50
Switching frequency	f_{sw} [kHz]	3.44	3.44	3.44	3.44
Line inductance	L_{line} [mH]	11.0	11.0	11.0	11.0
Line resistance	R_{line} [mΩ]	750	750	1500	750
DC bus voltage reference	$V_{dc,ref}$ [V]	270	270	270	270

According to Table 7.1, the switching frequency (f_{sw}) is somewhat lower than the one used in the investigations in the previous chapters. The switching frequency of the laboratory set-up is set by the controller hardware. However, this is not critical since the switching frequency is still considerably higher than the DC bus voltage controller bandwidth.

All the controller algorithms needed for each converter are implemented in IEA-MIMO control computers [9]. The IEA-MIMO is based on the Texas Instruments TMS320C30 floating-point digital signal processor (DSP). One of the key benefits of the IEA-MIMO is the simultaneous sampling of 16 analogue input channels with 12 bits resolution. Furthermore, it provides 8 analogue output channels. The quantities shown in the figures in this chapter are actually measured from these output channels. A Tektronix TDS 640A oscilloscope is used for all the measurements. The IEA-MIMO is also equipped with a DSPLINK bus for expansion boards, e.g. the PWM board. Triangular carrier wave modulation (Appendix A) is carried out on the PWM board. The sampling instants of the IEA-MIMO are synchronised to the positive and negative peaks of the carrier via the DSPLINK bus. Consequently, the sampling frequency equals twice the switching frequency.

7.2 Dynamic properties

The dynamic properties are investigated in the same way as in Chapter 3. A simplified schematic of the experimental set-up is shown in Figure 7.1.

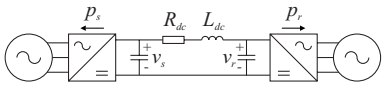

Figure 7.1: Experimental set-up for investigation of dynamic properties.

Both converters are equipped with DC bus capacitors with a total nominal capacitance of 1.1 mF each, which is used for calculation of the voltage droop gain. This gives a rated power for the converters equal to 716 W. The rated power with respect to the semiconductor devices in the converter is considerably higher. As discussed in Chapter 3, the rated power of the converter is determined by the DC bus capacitor and rated voltage. Of course, the semiconductors of the converter are selected in accordance with rated power and DC bus voltage in a practical application.

Since the damping is reduced for the experimental set-up compared to the analysis of Chapter 3, the measurements are assisted with simulations. Ideally, the simulation model should agree with the experimental set-up. Therefore, the DC bus capacitances are measured for the simulations. The measurement indicates that the source DC bus capacitance is 1.128 mF and the load converter DC bus capacitance is 1.123 mF. The controllers used in the simulation are, however, still based on a converter DC bus capacitance of 1.1 mF each.

The experiments on dynamic performance are conducted with a DC bus series resistor, R_{dc} in Figure 7.1, of either 1.0 Ω or 6.0 Ω together with a series inductor L_{dc} of 0.3, 3.0 or 32 mH. The investigated combinations of parameters are listed in Table 7.2. As shown in Table 7.2, the total series resistance is slightly higher due to the inductor winding resistance. This is accounted for in the simulation model.

Table 7.2: Measurement and simulation model data.

Measurement no.	Measurement parameters		Simulation parameters	
	R_{dc} [Ω]	L_{dc} [mH]	R_{dc} [Ω]	L_{dc} [mH]
1	1.0	0.0	1.0	$1.0 \cdot 10^{-6}$
2	1.0	0.3	1.1	0.3
3	1.0	3.0	1.2	3.0
4	1.0	32	1.7	32
5	6.0	32	6.7	32

The investigations on dynamic performance in this section are carried out for a step in the output power reference of the load converter corresponding to nominal power, i.e. 716 W. The root-locus (with reference to Chapter 3) for R_{dc}=1.0 Ω are shown in Figure 7.2 and Figure 7.3. The cases actually investigated, i.e. L_{dc}=0.3, 3.0 and 32 mH, are shown with large markings. The other two cases listed in Table 7.2 are not included in the root-locus since two

poles are real. One of the real valued poles is located at a very high frequency (close to a zero) and therefore, the visibility of the root-locus is lost if these cases are included. Note that there is only a minor difference in the root-locus at no-load and rated load.

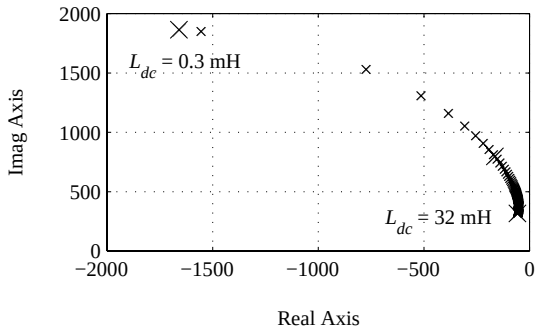

Figure 7.2: Root-locus of pole ρ_1. The difference between rated load and no-load is not visible in this scale.

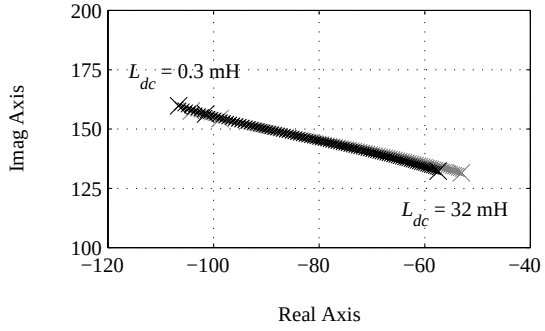

Figure 7.3: Root-locus of pole ρ_3 at rated load (*black*) and no-load (*grey*).

Experimental and simulation results

The measured and simulated voltage and power for the sending and receiving end converters are shown in Figure 7.4 (R_{dc}=1.0 Ω and L_{dc}=0 mH), Figure 7.5 (R_{dc}=1.0 Ω and L_{dc}=0.3 mH), Figure 7.6 (R_{dc}=1.0 Ω and L_{dc}=3.0 mH), Figure 7.7 (R_{dc}=1.0 Ω and L_{dc}=32 mH) and Figure 7.9 (R_{dc}=6.0 Ω and L_{dc}=32 mH). Figure 7.8 shows a ten-run average measurement with the same parameters as for Figure 7.7. In Figure 7.4, Figure 7.5 and Figure 7.6 (case 1-3) there is a good agreement between measurement and simulation results. However, in Figure 7.7, Figure 7.8 and Figure 7.9 (case 4-5) agreement seems to be poor.

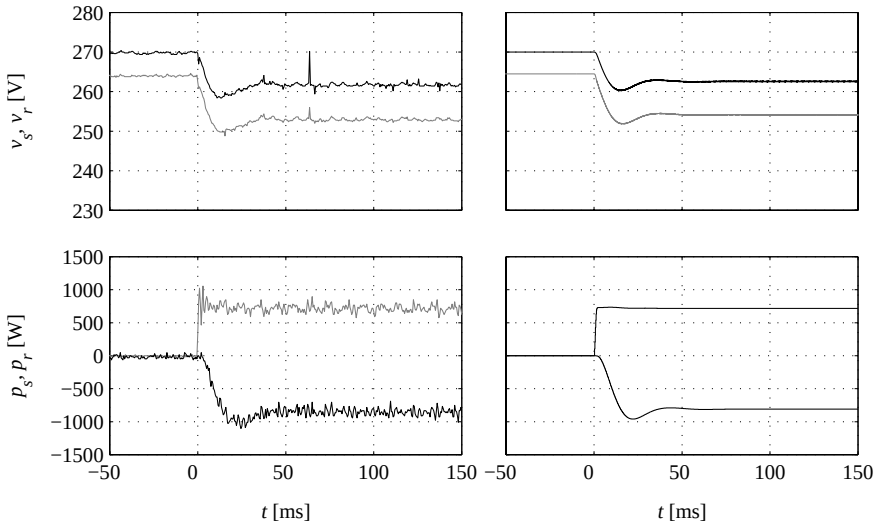

Figure 7.4: Measured (*left*) and simulated (*right*) sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω and L_{dc}=0 mH (L_{dc}=1.0 nH for the simulation model).

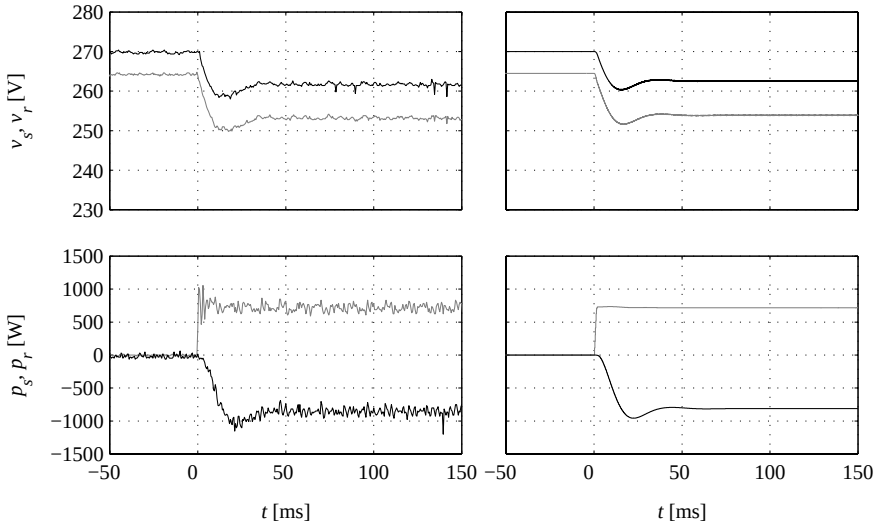

Figure 7.5: Measured (*left*) and simulated (*right*) sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω and L_{dc}=0.3 mH.

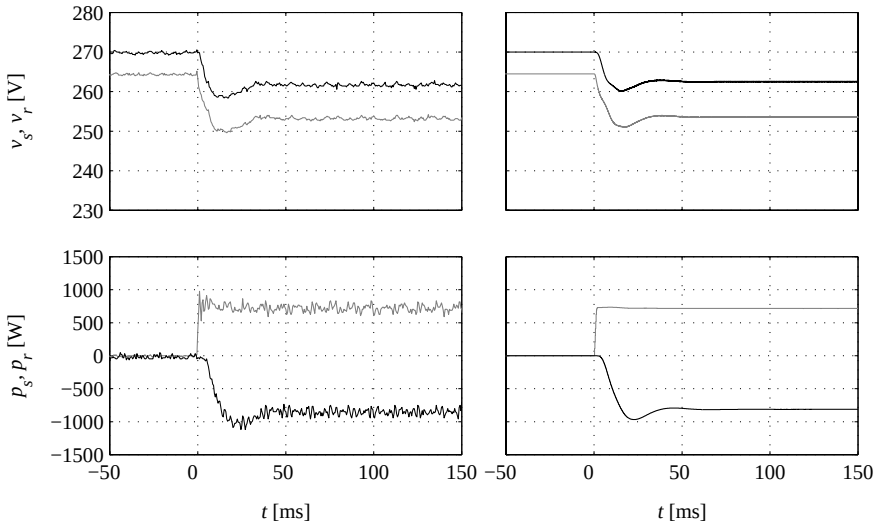

Figure 7.6: Measured (*left*) and simulated (*right*) sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω and L_{dc}=3.0 mH.

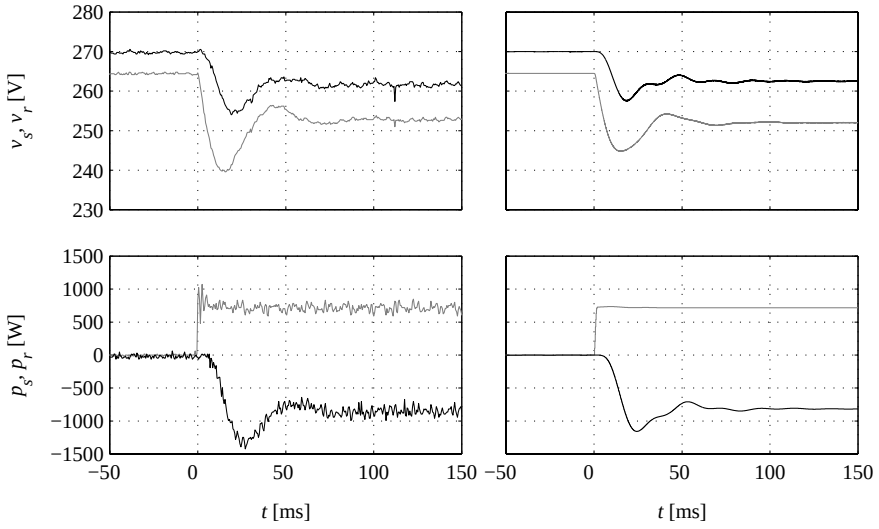

Figure 7.7: Measured (*left*) and simulated (*right*) sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω and L_{dc}=32 mH.

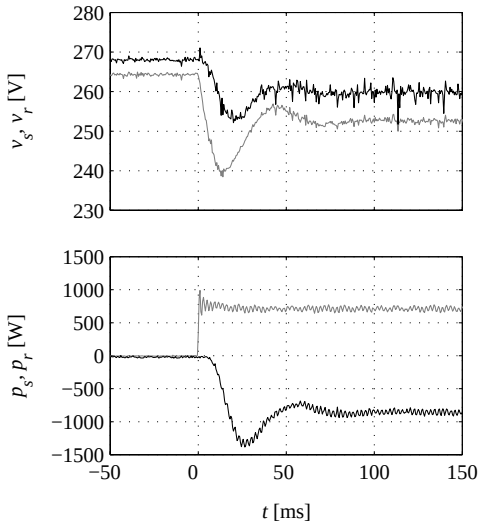

Figure 7.8: Ten-run average measurement of sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), for R_{dc}=1.0 Ω and L_{dc}=32 mH.

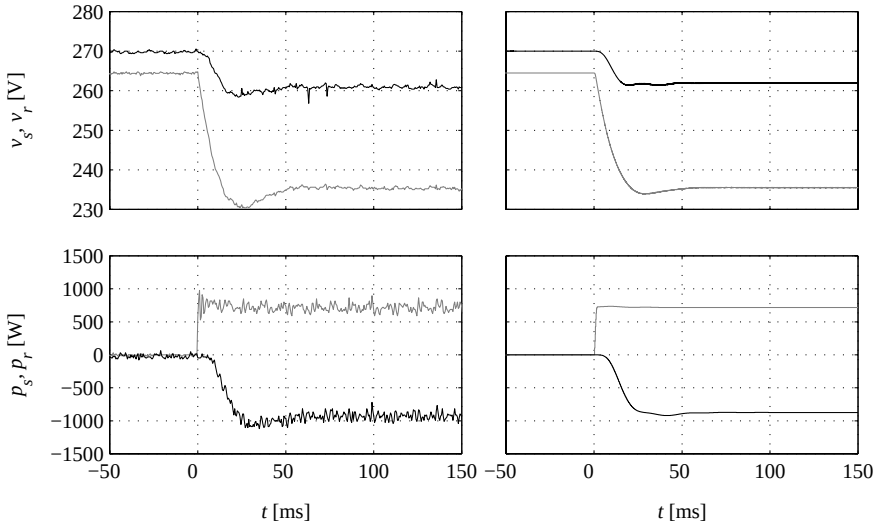

Figure 7.9: Measured (*left*) and simulated (*right*) sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=6.0 Ω and L_{dc}=32 mH.

Comments

Due to the poor agreement between simulation and measurement for case 4 (R_{dc}=1.0 Ω and L_{dc}=32 mH), it is investigated further. Since the DC bus voltage controllers are implemented the same way in both simulations and experiments, it is concluded less likely that the problem originate from the DC bus voltage controller. Therefore, the emphasis of the investigation is put on the AC side and its current controller. The main reason is that it seems like the estimated AC side power appears to have a higher overshoot in the measurements than in the simulations. This implies that the transient DC bus voltage is lower in the measurements than in the simulations. The reasons for the deviations between measurement and simulation results are investigated in the following. The *q*-direction current reference is calculated from

$$i_{q,ref} = \frac{p_{ref}}{e_{q,f}} \tag{7.4}$$

where p_{ref} is the power reference and $e_{q,f}$ is the low-pass filtered grid voltage vector. The first order low-pass filter, with break-over frequency of 5 Hz, is used to attenuate disturbances since it is found that they affect the reference to a large extent. The estimated power, however, is not used for control purposes and disturbances are not considered as a problem. Therefore, it is calculated from

$$p_{est} = e_q i_q \tag{7.5}$$

The problem is that the line impedance is not modeled in the simulation but always present in an experimental set-up. Consequently, e_q is not constant in the measurements as in the simulations. When the output power from the load converter increases, e_q also increases while $e_{q,f}$ remains unaltered initially. Thus, $i_{q,ref}$ is unaltered causing the overshoot in the estimated power.

The experimental set-up is connected to an AC power outlet equipped with 10 A fuses. Consequently, it is likely that the short circuit impedance of the grid is rather high. Therefore, a short circuit impedance of Z_{sc}=0.25+*j*0.25 Ω is used for the following simulations.

Moreover, the power converters are connected to the same outlet via the three-phase transformers. When the load converter responds to the step in its power reference it delivers power to the grid. This means that when the source converter starts to draw power from the same three-phase grid, the loading of

the outlet is lower than expected. However, during the voltage transients the short circuit impedance of the outlet is important. The simulation model used previously in Chapter 3 and in this section is altered to comply more with the experimental set-up, see Figure 7.10.

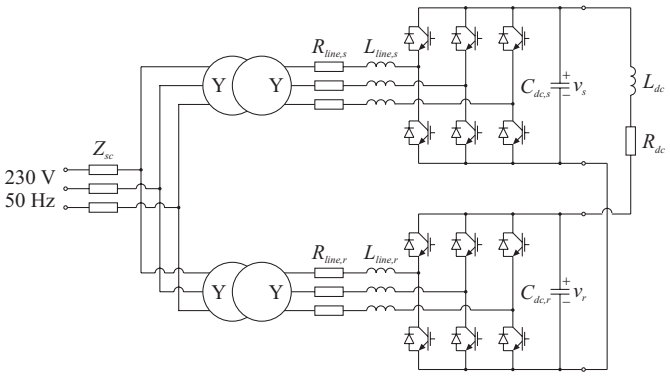

Figure 7.10: Simulation model for investigation of dynamic properties. This model complies more with the experimental set-up than the previously used.

Two simulations are repeated with this line impedance applied to the model in Figure 7.10. In Figure 7.11 the simulation result with R_{dc}=1.0 Ω and L_{dc}=3.0 mH is shown. The measurement and simulation results for this case show a good agreement already in Figure 7.6. The reason for repeating the simulation with the altered model is to verify that it covers all cases and not just the ones with L_{dc}=32 mH.

It is clearly seen that the result corresponds well with the measured result of Figure 7.6. Due to the good agreement between measurement and simulation also for the altered model in this case, the other simulations that already show a high degree of agreement is not repeated.

Figure 7.12 shows the simulation result for the case with R_{dc}=1.0 Ω and L_{dc}=32 mH. The simulation result in Figure 7.12 shows better agreement with the measured result in Figure 7.7 compared to the simulation result of Figure 7.7. Still, the ringing following the voltage overshoot in the simulation is not apparent in the measurement. This is most likely due to the fact that the short circuit impedance Z_{sc} of the three-phase outlet is not accurately estimated and that the distributed impedance in the converter is not modeled but present in the experimental set-up.

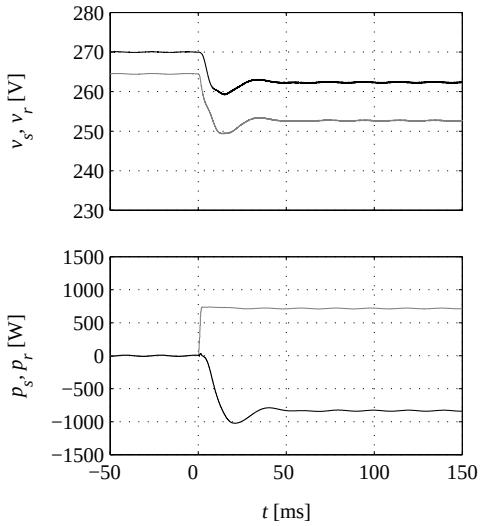

Figure 7.11: Simulated sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω, L_{dc}=3.0 mH and line impedance equal to Z_{sc}=0.25 + *j*0.25 Ω per phase.

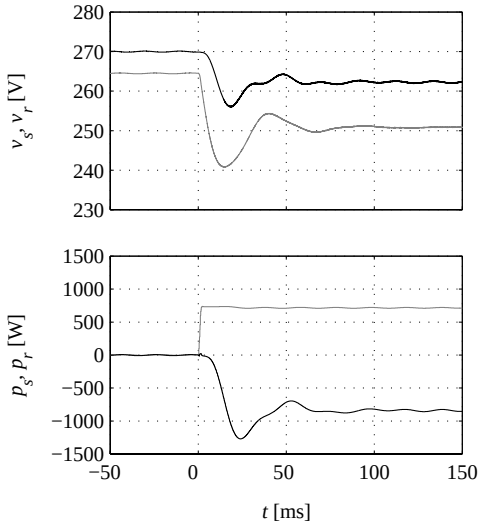

Figure 7.12: Simulated sending end (*black*) and receiving end (*grey*) voltage (*top*) and power (*bottom*), in the case of R_{dc}=1.0 Ω, L_{dc}=32 mH and line impedance equal to Z_{sc}=0.25 + *j*0.25 Ω per phase.

7.3 Load sharing

To investigate load sharing, a DC ring bus with three converters is studied. The system is shown in Figure 7.13.

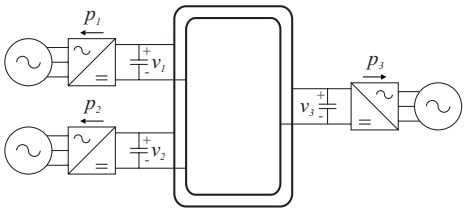

Figure 7.13: Experimental set-up for investigation of load sharing.

Two of the converters, unit 1 and unit 3, are operated as sources. Unit 2 is operated as load. Additional DC bus capacitors are connected at the converters to increase the rated power. Thus, the converters are equipped with DC bus capacitors of 1.6 mF (unit 1, 1041 W), 2.1 mF (unit 2, 1367 W) and 1.1 mF (unit 3, 716 W). Since the gain is calculated based on the DC bus capacitance of the sources, the total DC bus capacitance is overestimated to 2·(1.6+1.1) mF=5.4 mF whereas the actual total DC bus capacitance is 4.8 mF. However, this is not adjusted for, since this is regarded possible also for real installations.

Each converter is connected to the DC ring bus through a cable node with two 10 μF grounding capacitors (Figure 5.1), with 220 kΩ bleeder resistors connected in parallel. Resistors of 100 Ω are connected in series with each grounding capacitor, to obtain a minimum time constant of 1 ms for the fault currents, as described in Chapter 5. Current transducers are not mounted. Instead, current probes are used for measuring the differential fault currents.

Each cable segment is modeled by four 0.1 Ω resistors (Figure 5.1), to introduce a fault on the middle. Note that all the measurements in this section are averaged from ten separate measurements due to the high level of measurement noise. According to the measured transient response shown in Figure 7.7 and Figure 7.8 of the previous section, the ten-run average measurement gives a result consistent with a single measurement. Therefore, it is concluded that ten-run average measurements can be used also when load sharing is investigated, since the network is more ideal in this case and, consequently, the dynamics are less pronounced.

This section is arranged as follows. First, load sharing is examined for a system where the DC bus voltage measurements of the sources are offset-adjusted in such a way that they are loaded proportionally equal. Measurements are made for both an unbroken and broken DC ring bus. The result of a high impedance DC bus ground fault is also examined. Second, load sharing without offset-adjusted DC bus voltage measurements are investigated.

The power reference for the load converter (unit 2) is changed in steps in all the experiments on load sharing. The magnitude of the step corresponds to approximately 850 W.

Load sharing for offset-adjusted DC bus voltage measurements

In the first experiment on load sharing, the DC bus voltage measurement of unit 3 is adjusted by subtraction of 3.7 V in the controller to give the same level as for unit 1 at no-load conditions. Figure 7.14 shows the voltage and power for the three units. Both source converters are loaded to approximately 0.6 p.u. (unit base) and, hence, the total load is shared democratic. Note that the load, unit 2, has no offset-adjustment of the DC bus voltage measurement (Figure 7.14), which is also the case in the previous section.

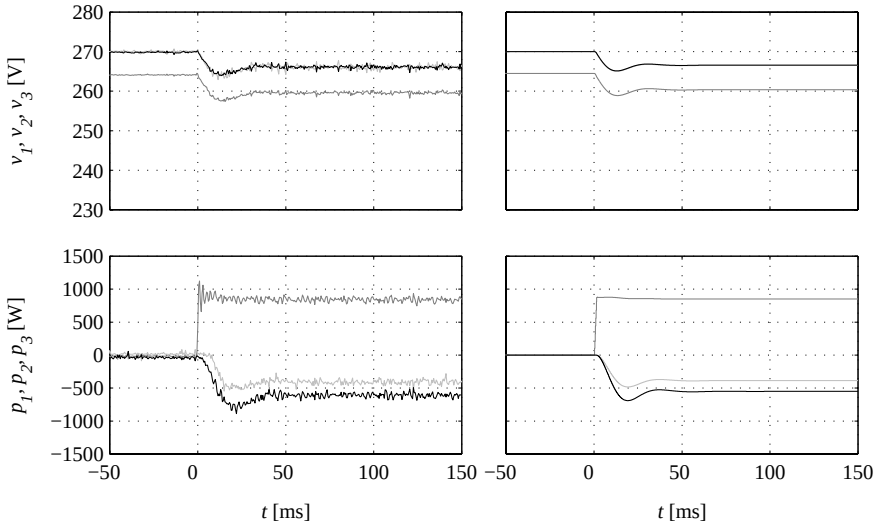

Figure 7.14: Measured (*left*) and simulated (*right*) unit 1 (*black*), unit 2 (*grey*) and unit 3 (*light-grey*) DC bus voltage (*top*) and power (*bottom*), in the case of offset-adjusted DC bus voltage measurements for the source converters.

High impedance DC bus ground fault

The differential fault currents in the case of a 1.0 kΩ DC bus ground fault between unit 1 and 2 of the three-converter system, are investigated. Current probes with a transfer ratio of 100 mV/A are used for the differential current measurements. The measurement noise due to switching has a higher magnitude than the fault currents in this case. Therefore, the fault currents are measured for a case where the converters are not operated. Consequently, the DC bus voltage equals the peak AC line-to-line voltage, i.e. 205 V. The differential current measurements are shown in Figure 7.15.

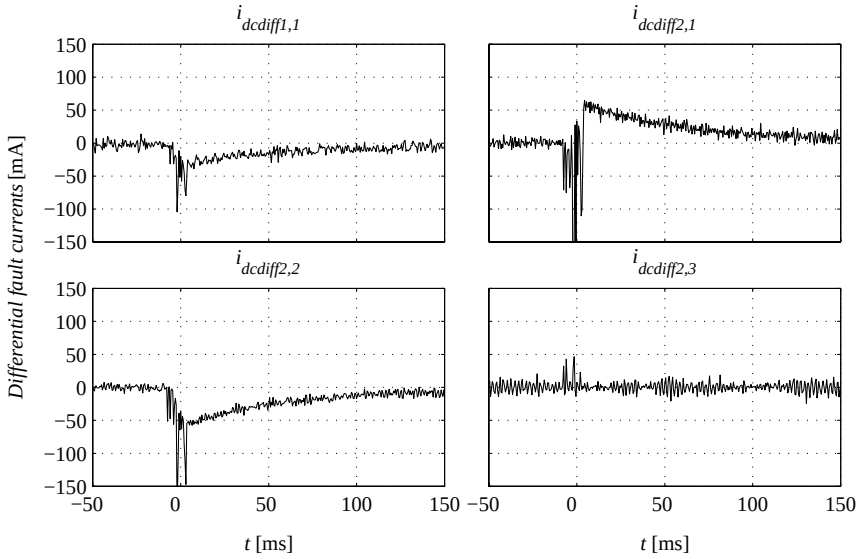

Figure 7.15: Measured unit 1 differential current $i_{dcdiff1}$ (*top*, *left*), unit 1 differential current $i_{dcdiff2}$ (*top*, *right*), unit 2 differential current $i_{dcdiff2}$ (*bottom*, *left*) and unit 3 differential current $i_{dcdiff2}$ (*bottom*, *right*).

The peak fault current at the fault location should equal 205 mA, which means that the peak differential fault current $i_{dcdiff2}$ equals 68 mA for units 1 and 2, according to (5.46). The peak value of the differential fault current $i_{dcdiff1}$ equals 34 mA, according to (5.26). The levels of the fault currents are, thus, in agreement of the results of Chapter 5. Since $i_{dcdiff1}$ is negative, the fault is located between the positive DC bus conductor and ground. The sign combinations of $i_{dcdiff1}$ and $i_{dcdiff2}$ for units 1 and 2 reveal that the fault is located between these units. For unit 3, $i_{dcdiff2}$ is essentially unaffected by the fault since the common mode current flows into both cable segments for this cable node.

Note that the switching noise problem discussed earlier in this section indicates that the transducers for the differential current measurement should have a higher transfer ratio, for example 1 V/A to accurately detect high impedance ground faults. They should also be saturable to avoid excessive voltages for low impedance faults.

Load sharing for broken DC bus

In the next experiment, load sharing in the case of a broken DC ring bus, for example following a fault, is investigated. Figure 7.16 shows the measured DC bus voltage and estimated power in the case that the ring bus is broken between converters 1 and 2. Load sharing is only slightly degraded compared to the case with an unbroken DC bus. This is due to the low equivalent cable resistance compared to the equivalent resistance of the droop controllers R_{droop}.

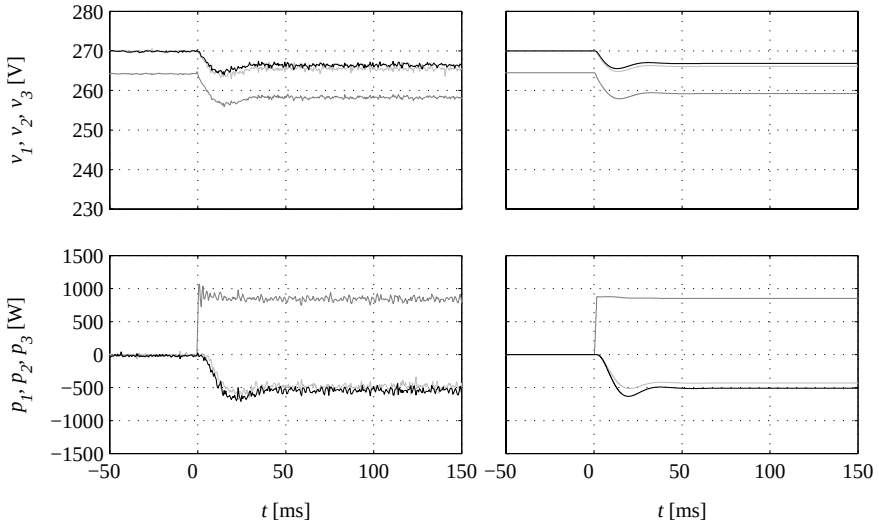

Figure 7.16: Measured (*left*) and simulated (*right*) unit 1 (*black*), unit 2 (*grey*) and unit 3 (*light-grey*) DC bus voltage (*top*) and power (*bottom*), in the case of a DC bus broken between units 1 and 2.

Load sharing for non-offset-adjusted bus voltage measurements

In the last experiment on load sharing, the performance is investigated for a case where the DC bus voltage measurement of unit 3 is not offset-adjusted. As seen in Figure 7.17, unit 1 delivers power to the DC bus and unit 3 draws power from the DC bus when unit 2 operates at no-load.

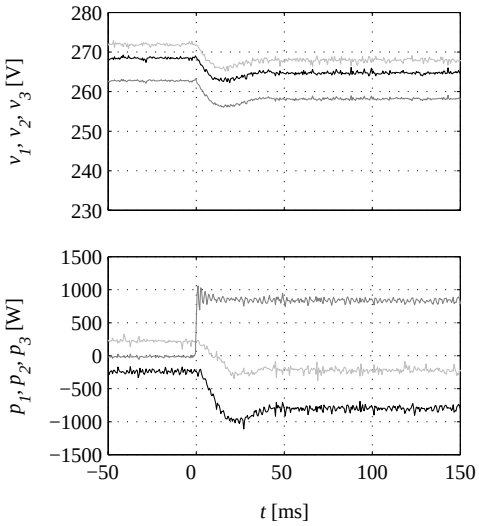

Figure 7.17: Measured unit 1 (*black*), unit 2 (*grey*) and unit 3 (*light-grey*) DC bus voltage (*top*) and power (*bottom*), in the case of non-offset-adjusted DC bus voltage measurements for the source converters.

Figure 7.17 clearly demonstrates that one of the key problems of converter design is that the DC bus voltage measurement must be accurate to yield proper load sharing. On the other hand, it also indicates that DC bus voltage offset control, like the one used in the wind power application of Chapter 4 is possible.

Chapter 8

Conclusions

This thesis presents a possible solution for incorporation of renewable energy sources in the power system. Here, local DC distribution systems are proposed, which might also provide inherent UPS properties if energy storage elements or local generating units are employed. A DC distribution system similar to the one used for renewable energy systems presented here, can also be used for example for telecommunication systems and industrial multi-converter systems for drives. Moreover, DC distribution systems could also be implemented for propulsion and traction applications. First, a summary of the obtained results is given. Second, some future research topics for DC distributed power systems are provided.

8.1 Summary of results

The investigation on DC distributed power systems has provided results summarised in this section.

Voltage control and load sharing

Several different methods to achieve voltage control and load sharing are investigated. The DC bus voltage droop controllers employed, do not inherently require communication between source and load converters to achieve voltage control and load sharing. Therefore, the droop method is selected for the further investigations. However, in applications where the available power could be lower than the requested, some kind of supervisory control or monitoring action is needed to give priorities for load shedding schedules, when required.

The stationary and dynamic properties of a two-converter system are investigated. One of the converters is operated as a constant power load and the other as a source, utilising DC bus voltage droop control. The analysis provides a method to select DC bus capacitance of each converter connected to the power system. This DC bus capacitance is selected based on the droop voltage error and desired attenuation of the interaction between AC and DC sides of the converter. It is found that stability is not the main limiting factor for reasonable cable impedance. The cable resistance is limited by the risk of converter over-modulation. The cable inductance can be equal to, or even higher than the AC side filter inductance, without compromising stability. Then, the investigated DC bus voltage controllers are compared in terms of load sharing for a five converter system. In this investigation, it is found that the source converters share the total load democratic for the implemented droop controller.

Load sharing in the case of renewable energy sources

DC bus voltage control and load sharing in the case of non-dispatchable sources, like wind power, are also investigated. In this study, the available input power must exceed the desired output power since constant power loads are supplied. Most likely, non-dispatchable sources require low bandwidth communication, to ensure that more power than available is not delivered to the loads.

A system supplied only by wind power is considered to study load sharing in the case of non-dispatchable sources. To achieve steady state power balance, the wind power aggregates are equipped with pitch angle control. The investigated voltage droop control scheme is further developed to include voltage droop offset, i.e. speed droop control, to handle transient power variations and to obtain democratic loading of the wind power aggregates. The droop offset controller acts to reduce the power drawn from wind turbines operating with lower available power than expected. The sources and loads operate as autonomous units, which means that high-speed communication is not needed. The externally calculated turbine speed references are not updated during the simulations. Consequently, the bandwidth of the communication required for the investigated system could be considerably lower than the sampling frequency of the current controllers (at least four orders of magnitude in the investigated system). The simulation results verify that disturbances are handled properly.

Fault detection

Fault detection and clearance are important for any electrical distribution system. For the investigated DC power distribution system, grounding capacitors are required due to the fact that the converter AC sides should be galvanically separated to avoid ground current flowing between the converters through protective earth and the DC bus.

A grounding scheme and an algorithm for detection of ground faults and short circuits in DC distributed power systems, are presented for a system of sources and loads with high impedance or no connection to ground. A grounded system is preferable due to reasons of personal safety and protection of equipment. For DC distributed power systems operated with power electronic converters, the common reference between sources and loads provides a path for the common mode or neutral current. The neutral current appears since the converters have no AC side terminal connected to ground, which means that ground currents cannot be controlled. Also, zero-sequence currents, in the form of third order harmonics, are often included in the modulation signals to utilise the DC side voltage more effectively and reduce the harmonic content (positive- and negative-sequence) of the AC side currents.

The scheme presented here detects ground faults both on the AC and DC sides of the distributed power system. In the investigation, ground faults are focused, but a similar algorithm can be used to detect short circuits by measuring two of the currents flowing into the cable node. The selected detection method relies on communication between nearby cable nodes for fault localisation, since this gives possibility to operate the DC distributed power system even if it is highly segmented due to multiple faults.

DC system interconnection

The ground fault detection algorithm not utilising communication to locate the fault is sensitive to transducer offset and linearity when there is a high number of cable nodes in the DC distribution system. Therefore, galvanically separated connection of DC distribution systems are investigated. Also, connection of DC distribution systems with DC transmission links is investigated. Galvanic separation is of great concern in the latter case also, since a ground fault on the transmission link would otherwise impose a high voltage potential in the low voltage parts of the system. An existing DC-DC converter topology with galvanic separation is therefore adopted for DC transmission purposes. This is studied in simulations.

Experimental results

A laboratory set-up is implemented based on the results obtained from the theoretical analysis. First, the dynamic properties are investigated for a two-converter system for several combinations of DC bus series resistance and inductance. The measurements are assisted with simulations of an equivalent system. The good agreement between simulation and measurement results verify the dynamic properties. Second, load sharing is verified in measurements and simulations of a three-converter DC ring bus system. The importance of an accurate DC bus voltage measurement is highlighted. Third, the algorithm to detect high impedance ground faults is verified in experiments. The importance of measurement noise immunity is highlighted.

8.2 Future work

One of the benefits of the adopted voltage control method, i.e. DC bus voltage droop control, is that communication is not required. However, the method proposed for selection of DC bus capacitor together with the adopted requirements result in a high capacitance of the DC bus capacitors. If the requirements are less strict, the required capacitance is reduced. For example, if the rated droop is maintained at 0.05, as in Chapter 3, and the rated closed loop damping is reduced to 0.5, as in Chapter 7, the required DC bus capacitance for each converter is reduced to 100 μF/kW for a 750 V system. Furthermore, the break-over frequency of the DC bus voltage filters might be increased from the proposed 30 Hz, especially if the source frequency is higher than 50 Hz, which also results in a reduced DC bus capacitance. This should be investigated both in simulations and experiments. Load sharing in the case of non-dispatchable sources should also be investigated in experiments.

There are however some obstacles remaining before local DC distribution system might become widely accepted. Firstly, the need of galvanic isolation to prevent from zero-sequence disturbances results in a considerable cost. Secondly, the fusing required to protect this kind of system at short circuit faults and the transducers required to detect ground faults are also costly. Therefore, the system should be investigated from an economical point of view. Another safety issue also needs further investigation. This issue is related to the fact that there might be loads that are only fed from the DC system. If these are connected via a transformer, to reduce zero-sequence currents, there is a potential risk that faults on the load side are not cleared by the fuses and not detected by the cable nodes if the energy stored in the load is low.

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Appendix A

Modulation

Modulation means bring in order or agreement with. For power electronic switch mode converters this is interpreted as the creation of a pulse pattern where the average voltage (in the case of voltage source converters) equals the desired output voltage. Here, only carrier wave modulation [35] is discussed. Other methods exists, mainly tolerance or dead-band control, but are left out here. Another limitation made is that only triangular carrier based modulation is discussed and saw-tooth carrier modulation left out.

First, different types of reference waveforms for the sub-oscillation and modified sub-oscillation methods [35] are discussed. These are: the sinusoidal, symmetrical and bus-clamped reference waveforms. The main differences between these are, firstly, to what extent they are able to utilise the DC link voltage and, secondly, the harmonic current spectrum they produce. Both the differential mode and common mode spectrums for the output voltages are investigated and compared. Also, typical current spectrums are investigated. Second, examples of the switching pattern for each modulation reference are examined in detail by means of current space vectors. Here, it is found that the only difference between the carrier references is how long each zero voltage vector is applied.

A.1 Modulation methods

As previously mentioned, three different carrier wave modulation methods are investigated. Tolerance band control, where the current is allowed to vary in a band $\pm\Delta i$, around the current reference is not discussed here. However, it should be clear that tolerance band control, of course, gives a high dynamic performance at the expense of a varying switching frequency. A varying

switching frequency is not desirable since this makes semiconductor switching loss approximation cumbersome. Also, the high frequency harmonic current content strongly affects the design of the output filter inductors. Especially the losses due to iron core eddy currents are complicated to estimate if the harmonic content is varying.

In the case of carrier wave modulation, on the other hand, the switching frequency is well determined since it equals the fundamental frequency of the carrier. Still, the amplitude of the current harmonics varies with the loading of the converter but the frequencies at which the harmonics appear are fixed.

The only difference between the investigated carrier wave modulation schemes is the reference waveforms. To be more correct, the only difference is whether a zero-sequence signal is added or not, and if added, what the zero-sequence looks like [35]. A zero-sequence component in the references does not show up in the output voltage since the converter is not connected to the neutral. Therefore, the converter cannot produce any voltage affecting the neutral. A zero-sequence voltage per definition results in a zero-sequence current and since no neutral is connected there is no path for the zero-sequence (or sometimes called neutral) current to flow through.

This means that all the reference waveforms considered can be treated as being originally sinusoidal but later altered with a zero-sequence component. The reference waveforms are altered to affect the harmonic current spectrum or to increase the utilisation of the converter by increasing the maximum allowable modulation index for which linear modulation is obtained. The modulation index m_a is defined as

$$m_a = \frac{u_{i,ref}}{V_{dc}/2} \quad \text{where} \quad i = a,b,c \tag{A.1}$$

where u is the converter output phase potential and V_{dc} the DC bus voltage. The reason why m_a is calculated using $V_{dc}/2$ is that in most cases the triangular carrier has a DC level equal to zero and amplitude proportional to $V_{dc}/2$. Here, the amplitude is equal to $V_{dc}/2$. This is because, otherwise, the reference signals should be scaled by the same factor as the carrier peak-to-peak level in order to get an accurate modulation. Note that for full-bridge converters, the carrier DC level is not critical since the output voltages are differential, i.e. line-to-line voltages.

When m_a higher than 1 occurs, the switching of the particular phase is inhibited, since no crossings between the carrier and the reference waveforms occur. This situation is termed over-modulation. Over-modulation is equal to actuator saturation and should be avoided at least for stationary operation. The problem is not only that the controller command signals are not obeyed by the power electronic converter, but also that the output current harmonic content increases strongly [35][57].

The most important issue for all the investigated modulation methods is that the line-to-line output voltage should be equal for the different reference signals. As mentioned earlier, the voltage references are modified by a zero-sequence signal, in such a way that the maximum m_a is altered. The different voltage references are shown in Figure A.1 for a time equal to one period of the fundamental.

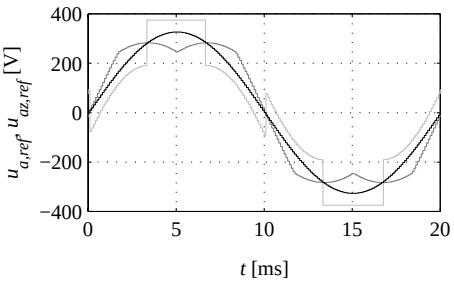

Figure A.1: Carrier wave modulation: sinusoidal (*black*), symmetrical (*grey*) and bus-clamped (*light-grey*) voltage references.

The line-to-line output voltage resulting from these references equals 400 V, 50 Hz in all the cases. For sinusoidal modulation, the references are kept as they are, i.e. as sinusoidal phase potentials. For symmetrical references, the references are altered in such a way that the most positive and most negative reference is made equal but with opposite sign. For bus-clamped modulation the reference with the highest instantaneous value (positive or negative) is clamped to $\pm V_{dc}/2$, dependent on which is the closest.

For sinusoidal references it is clear that over-modulation, i.e. m_a=1, occurs when the reference peak equals half the DC link voltage. Therefore,

$$u_{i,ref,max} = \frac{V_{dc}}{2} \quad \text{where} \quad i = a,b,c \tag{A.2}$$

for sinusoidal modulation. For symmetrical modulation the zero-sequence signal is calculated from

$$u_z = \frac{1}{2}\left(\max\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right) + \min\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right)\right) \tag{A.3}$$

For 1/6th of the fundamental period where $u_{a,ref}$ is the most positive and $u_{b,ref}$ is the most negative reference in stationary conditions, the resulting reference for the half-bridge connected to the *a*-phase is written

$$u_{az,ref} = u_{a,ref} - u_z = \frac{\sqrt{3}}{2} \cdot \hat{u} \cdot \cos\left(\omega_1 t - \frac{\pi}{6}\right) \tag{A.4}$$

As in the previous case, over-modulation occurs when the reference equals half the DC link voltage, which gives

$$u_{iz,ref,max} = \frac{1}{\sqrt{3}} \cdot V_{dc} \quad \text{where} \quad i = a,b,c \tag{A.5}$$

For bus-clamped modulation, the transition between two bus-clamped references is investigated. Assume that the *b*-phase has been clamped to $-V_{dc}/2$ and that the *a*-phase is going to be clamped to $+V_{dc}/2$. When this occurs

$$u_{a,ref} = \frac{\sqrt{3}}{2} \cdot \hat{u} \quad \text{and} \quad u_{b,ref} = -\frac{\sqrt{3}}{2} \cdot \hat{u} \tag{A.6}$$

This means that the zero-sequence voltage to be set equals

$$u_z = \frac{\sqrt{3}}{2} \cdot \hat{u} - \frac{V_{dc}}{2} < 0 \tag{A.7}$$

This gives

$$u_{az,ref} = \frac{\sqrt{3}}{2} \cdot \hat{u} - \left(\frac{\sqrt{3}}{2} \cdot \hat{u} - \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} \tag{A.8}$$

and

$$u_{bz,ref} = -\frac{\sqrt{3}}{2}\cdot\hat{u} - \left(\frac{\sqrt{3}}{2}\cdot\hat{u} - \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} - \sqrt{3}\cdot\hat{u} \tag{A.9}$$

The limit for over-modulation is given by

$$u_{bz,ref} = \frac{V_{dc}}{2} - \sqrt{3}\cdot\hat{u} \geq -\frac{V_{dc}}{2} \tag{A.10}$$

which gives

$$u_{iz,ref,max} = \frac{1}{\sqrt{3}}\cdot V_{dc} \quad \text{where} \quad i = a,b,c \tag{A.11}$$

This means that modulation with symmetrical or bus-clamped references provides a 15 % higher margin to over-modulation compared to modulation with sinusoidal references. The harmonic content of the output voltage depends on the waveform of the reference voltage. Both the differential mode (DM) harmonics, i.e. the harmonic content in

$$u_{ij} = u_{iz} - u_{jz} \quad \text{where} \quad i, j = a,b,c \tag{A.12}$$

and the common mode (CM) harmonic content, i.e. the harmonic content in u_z, are of great importance. For example, the DM harmonics result in losses in filter inductors etc. The CM harmonics can also result in parasitic current through capacitive coupling between conductors and ground. In turn, this results in malfunction of earth protectors and the occurrence of bearing currents in motors. The DM and CM harmonic content for the different modulation references in Figure A.1 are shown in Figure A.2 and Figure A.3, respectively.

For a purely inductive filter, the damping is proportional to the frequency, since the impedance is given by

$$Z_L = j\omega_1 L \tag{A.13}$$

The resulting harmonic content in the output currents is shown in Figure A.4, in the case of L=L_{line}=1.7 mH. This filter inductance is suitable for a 100 kW converter with 750 V DC bus voltage connected to a 400 V three-phase AC grid [6]. Note that the harmonic current content is calculated from the DM spectrum of the output voltage.

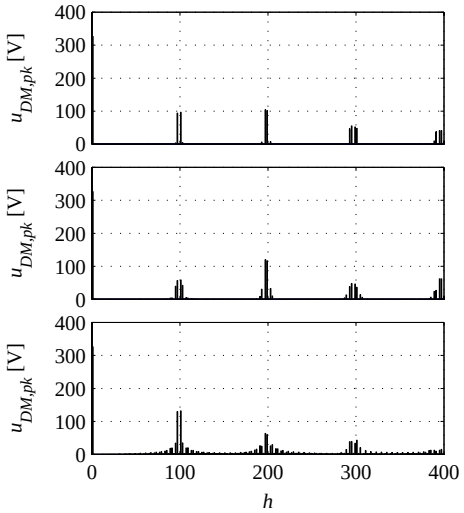

Figure A.2: Differential mode output voltage spectrum for sinusoidal (*top*), symmetrical (*middle*) and bus-clamped modulation (*bottom*). The fundamental frequency is 50 Hz and the spectrums are shown as a function of harmonic order h, where 1 denotes the fundamental.

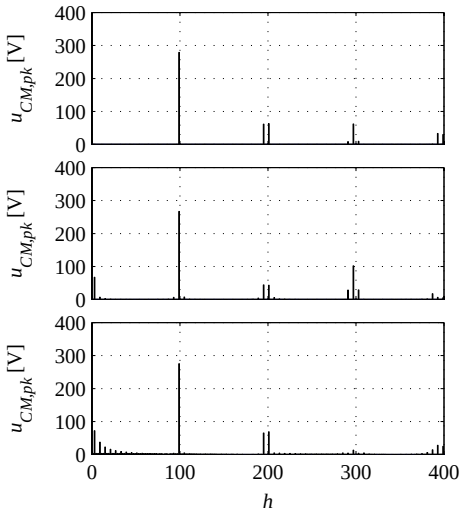

Figure A.3: Common mode output voltage spectrum for sinusoidal (*top*), symmetrical (*middle*) and bus-clamped modulation (*bottom*). The fundamental frequency is 50 Hz and the spectrums are shown as a function of harmonic order h, where 1 denotes the fundamental.

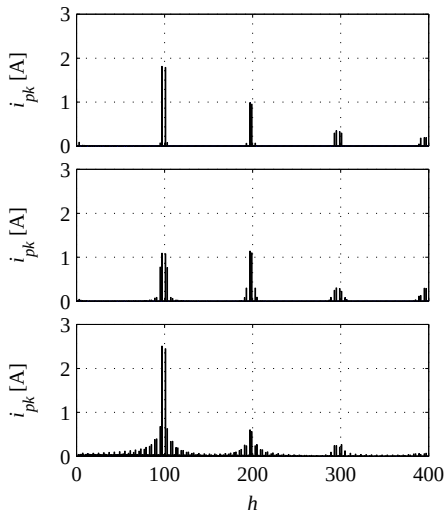

Figure A.4: Output current spectrum for sinusoidal (*top*), symmetrical (*middle*) and bus-clamped modulation (*bottom*). The fundamental frequency is 50 Hz and the spectrums are shown as a function of harmonic order h, where 1 denotes the fundamental.

A.2 Vector representation

A space vector $\vec{s}^{\alpha\beta}$ is defined from instantaneous three-phase values s_a, s_b and s_c according to

$$\vec{s}^{\alpha\beta} = s_a \cdot e^{j0} + s_b \cdot e^{j\frac{2\pi}{3}} + s_c \cdot e^{j\frac{4\pi}{3}} = s_\alpha + j s_\beta \tag{A.14}$$

For symmetrical three-phase quantities, i.e. if

$$\begin{cases} s_a = \hat{s} \cdot \cos(\omega_1 t) \\ s_b = \hat{s} \cdot \cos\left(\omega_1 t - \dfrac{2\pi}{3}\right) \\ s_c = \hat{s} \cdot \cos\left(\omega_1 t - \dfrac{4\pi}{3}\right) \end{cases} \tag{A.15}$$

the power-invariant transformation is given by

$$\begin{cases} s_\alpha = \sqrt{\frac{3}{2}} \cdot s_a \\ s_\beta = \frac{1}{\sqrt{2}}(s_b - s_c) \end{cases} \tag{A.16}$$

It is important to understand that the last expression cannot be used for switched quantities since these are not symmetrical. In the stationary $\alpha\beta$-frame, the same calculation methods as used for regular three-phase calculations can be used. Kirchoff's voltage law in space coordinates applied to a three-phase converter with inductive filter connected to a three-phase grid gives

$$\vec{u}^{\alpha\beta} - L\frac{d}{dt}\vec{i}^{\alpha\beta} - R\vec{i}^{\alpha\beta} - \vec{e}^{\alpha\beta} \approx \vec{u}^{\alpha\beta} - L\frac{d}{dt}\vec{i}^{\alpha\beta} - \vec{e}^{\alpha\beta} = 0 \tag{A.17}$$

This means that the current derivatives are expressed as

$$\begin{cases} \frac{di_\alpha}{dt} = \frac{1}{L}(u_\alpha - e_\alpha) \\ \frac{di_\beta}{dt} = \frac{1}{L}(u_\beta - e_\beta) \end{cases} \tag{A.18}$$

Assuming that the switching frequency period time T_{sw} is much longer than the time constant of the inductive filter, i.e. $T_{sw} = 1/f_{sw} << \tau_{el} = L/R$, implies that the current derivatives can be approximated according to

$$\begin{cases} \frac{\Delta i_\alpha}{\Delta t} = \frac{1}{L}(u_\alpha - e_\alpha) \\ \frac{\Delta i_\beta}{\Delta t} = \frac{1}{L}(u_\beta - e_\beta) \end{cases} \Leftrightarrow \begin{cases} \Delta i_\alpha = \frac{1}{L}(u_\alpha - e_\alpha)\Delta t \\ \Delta i_\beta = \frac{1}{L}(u_\beta - e_\beta)\Delta t \end{cases} \tag{A.19}$$

Since triangular carrier modulation is utilised, the duration of each interval can be calculated from their carrier crossings. For one half period (negative slope) of the carrier, the following expression is valid

$$u_{i,ref} = \frac{V_{dc}}{2} - \frac{V_{dc}}{T_s} \cdot t_i \quad \Leftrightarrow \quad t_i = \left(\frac{1}{2} - \frac{u_{i,ref}}{V_{dc}}\right) \cdot T_s \tag{A.20}$$

Note that Δt is the time duration for which a certain voltage vector is applied, in other words the distance between two consecutive carrier crossings for the different reference voltages. Actually, for the investigated carrier wave modulation strategies, the only difference is the time duration for which each different voltage vector is applied.

The sampling time T_s is selected as half the switching frequency time period, i.e. $T_s = T_{sw}/2$. Furthermore, the sampling instants are synchronised with the carrier in such a way that the sampling instants coincide with the carrier peaks. This is done in order to perform the samplings when the currents pass their average to avoid sampling distortion.

The grid is considered as being symmetrical, i.e.

$$\begin{cases} e_a = \hat{e} \cdot \cos(\omega_1 t) \\ e_b = \hat{e} \cdot \cos\left(\omega_1 t - \dfrac{2\pi}{3}\right) \\ e_c = \hat{e} \cdot \cos\left(\omega_1 t - \dfrac{4\pi}{3}\right) \end{cases} \tag{A.21}$$

The instantaneous grid voltages for $\omega_1 t = \pi/4$ are given by

$$\begin{cases} e_a = \dfrac{1}{\sqrt{2}}\hat{e} \\ e_b = \dfrac{\sqrt{3}-1}{2\sqrt{2}}\hat{e} \\ e_c = -\dfrac{\sqrt{3}+1}{2\sqrt{2}}\hat{e} \end{cases} \tag{A.22}$$

This gives

$$\begin{cases} e_\alpha = \sqrt{\dfrac{3}{2}} \cdot e_a = \dfrac{\sqrt{3}}{2} \cdot \hat{e} \\ e_\beta = \dfrac{1}{\sqrt{2}}(e_b - e_c) = \dfrac{\sqrt{3}}{2} \cdot \hat{e} \end{cases} \tag{A.23}$$

To calculate the converter output voltage (which is not a symmetrical three-phase quantity) equation (A.14) has to be used. The switches are considered as being ideal, i.e. the output voltage assumes the two discrete levels $\pm V_{dc}/2$. The voltage vectors applied for $\omega_1 t = \pi/4$ are shown in Figure A.5.

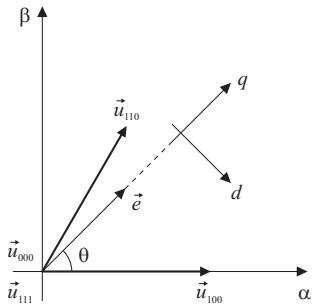

Figure A.5: The grid voltage vector $\vec{e}$ and the converter output voltage vectors applied at $\omega_1 t = \pi/4$.

The voltage vectors are calculated in Table A.1.

Table A.1: Voltage vectors used at $\omega_1 t = \pi/4$.

Switch state	u_α	u_β
000	0	0
100	$\sqrt{2/3} \cdot V_{dc}$	0
110	$1/\sqrt{6} \cdot V_{dc}$	$1/\sqrt{2} \cdot V_{dc}$
111	0	0

In the following sections the switching behavior is investigated for the different modulation strategies. As in the previous section, the investigation is performed under the conditions listed in Table A.2.

Table A.2: Converter specification.

DC link voltage	V_{dc}	750 V
Grid peak voltage	$\hat{e}$	325 V
Grid frequency	f_1	50 Hz
Switching frequency	f_{sw}	5000 Hz
Line filter inductance	L	1.7 mH

Sinusoidal modulation

In the case of sinusoidal references in no-load condition, the stationary voltage reference for each phase is given by the instantaneous grid voltage. At $\omega_1 t = \pi/4$ this means that

$$\begin{cases} u_{a,ref} = \dfrac{1}{\sqrt{2}}\hat{e} = 229.8\,\text{V} \\ u_{b,ref} = \dfrac{\sqrt{3}-1}{2\sqrt{2}}\hat{e} = 84.1\,\text{V} \\ u_{c,ref} = -\dfrac{\sqrt{3}+1}{2\sqrt{2}}\hat{e} = -313.9\,\text{V} \end{cases} \tag{A.24}$$

The carrier and the converter output voltage references in the case of sinusoidal modulation are shown in Figure A.6. Figure A.6 also shows the switching states applied. Note that only the vectors depicted in Figure A.5 are used, as expected.

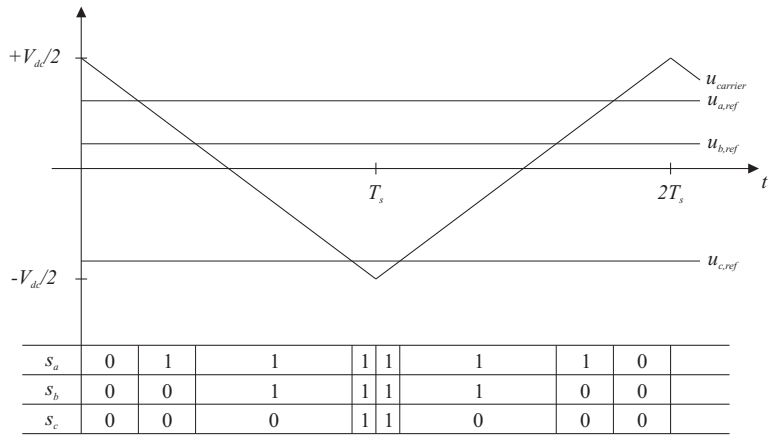

Figure A.6: The modulation carrier and the voltage references at $\omega_1 t = \pi/4$ in the case of modulation with sinusoidal references. The lower part shows the applied switch states.

The corresponding carrier wave crossings occur at (calculated for the negative slope)

$$\begin{cases} t_a = \left(\frac{1}{2} - \frac{u_{a,ref}}{V_{dc}}\right) \cdot T_s = 0.194 \cdot T_s = 19.4\,\mu s \\ t_b = \left(\frac{1}{2} - \frac{u_{b,ref}}{V_{dc}}\right) \cdot T_s = 0.388 \cdot T_s = 38.8\,\mu s \\ t_c = \left(\frac{1}{2} - \frac{u_{c,ref}}{V_{dc}}\right) \cdot T_s = 0.919 \cdot T_s = 91.9\,\mu s \end{cases} \quad \text{(A.25)}$$

The corresponding duration of each voltage vector (during the negative slope of the carrier) are, thus, equal to

$$\begin{cases} \Delta t_{000} = t_a - 0 = \left(\frac{1}{2} - \frac{u_{a,ref}}{V_{dc}}\right) \cdot T_s = 19.4\,\mu s \\ \Delta t_{100} = t_b - t_a = \left(\frac{u_{a,ref}}{V_{dc}} - \frac{u_{b,ref}}{V_{dc}}\right) \cdot T_s = 19.4\,\mu s \\ \Delta t_{110} = t_c - t_b = \left(\frac{u_{b,ref}}{V_{dc}} - \frac{u_{c,ref}}{V_{dc}}\right) \cdot T_s = 53.1\,\mu s \\ \Delta t_{111} = T_s - t_c = \left(\frac{1}{2} + \frac{u_{c,ref}}{V_{dc}}\right) \cdot T_s = 8.1\,\mu s \end{cases} \quad \text{(A.26)}$$

Applying this to equation (A.19) gives current vector variation according to Table A.3.

Table A.3: Current vector increase.

Switch state	Δi_α [A]	Δi_β [A]
000	-3.21	-3.21
100	3.78	-3.21
110	0.77	7.77
111	-1.34	-1.34

Note that the sum of the variations equals zero. This is approximately true if the pulse number m_f, i.e. the ratio between switching frequency and fundamental of the output voltage, is high. Also, if m_f is high, the grid voltage vector does not change much during the following carrier half period since the

sampled grid voltages are almost unaltered. This yields that the same converter output voltage vectors appear in the opposite order for approximately the same duration as for the previous sampling interval. The space vector current trajectory for one switching interval is shown in Figure A.7.

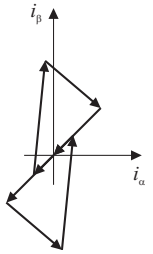

Figure A.7: Current vectors for modulation with sinusoidal references at $\omega_1 t=\pi/4$.

Symmetrical modulation

For symmetrical references, in no-load operation, the stationary voltage reference for each phase is not given by the instantaneous grid voltage. Instead, the most positive reference and the most negative reference are altered to have the same magnitude. This is done in the following manner and gives for $\omega_1 t=\pi/4$

$$\begin{aligned} u_z &= \frac{1}{2}\left(\max\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right)+\min\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right)\right)= \\ &= \frac{1}{2}\left(u_{a,ref}+u_{c,ref}\right)=\frac{1}{2}\left(229.8-313.9\right)\mathrm{V}=-42.05\ \mathrm{V} \end{aligned} \tag{A.27}$$

This gives the voltage references

$$\begin{cases} u_{az,ref} = u_{a,ref} - u_z = 271.85\ \mathrm{V} \\ u_{bz,ref} = u_{b,ref} - u_z = 126.15\ \mathrm{V} \\ u_{cz,ref} = u_{c,ref} - u_z = -271.85\ \mathrm{V} \end{cases} \tag{A.28}$$

The corresponding switching times (calculated for the negative slope of the carrier) are

$$\begin{cases} t_a = \left(\frac{1}{2} - \frac{u_{az,ref}}{V_{dc}}\right) \cdot T_s = 0.138 \cdot T_s = 13.8\,\mu s \\ t_b = \left(\frac{1}{2} - \frac{u_{bz,ref}}{V_{dc}}\right) \cdot T_s = 0.332 \cdot T_s = 33.2\,\mu s \\ t_c = \left(\frac{1}{2} - \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 0.863 \cdot T_s = 86.3\,\mu s \end{cases} \tag{A.29}$$

The corresponding duration of each voltage vector (during the negative slope of the carrier) is, thus, equal to

$$\begin{cases} \Delta t_{000} = t_a - 0 = \left(\frac{1}{2} - \frac{u_{az,ref}}{V_{dc}}\right) \cdot T_s = 13.8\,\mu s \\ \Delta t_{100} = t_b - t_a = \left(\frac{u_{az,ref}}{V_{dc}} - \frac{u_{bz,ref}}{V_{dc}}\right) \cdot T_s = 19.4\,\mu s \\ \Delta t_{110} = t_c - t_b = \left(\frac{u_{bz,ref}}{V_{dc}} - \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 53.1\,\mu s \\ \Delta t_{111} = T_s - t_c = \left(\frac{1}{2} + \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 13.8\,\mu s \end{cases} \tag{A.30}$$

Applying this to equation (A.19) gives current variation according to Table A.4.

Table A.4: Current vector increase.

Switch state	Δi_α [A]	Δi_β [A]
000	-2.28	-2.28
100	3.78	-3.21
110	0.77	7.77
111	-2.28	-2.28

Also in this case the sum of the variations equals zero. The space vector current trajectory for one switching interval, i.e. both the positive and the negative slope of the carrier, is shown in Figure A.8.

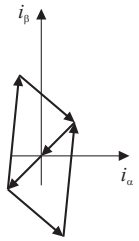

Figure A.8: Current vectors for modulation with symmetrical references at $\omega_1 t=\pi/4$.

Bus-clamping modulation

For bus-clamped references, in no-load condition, the stationary voltage reference for each phase is not given by the instantaneous grid voltage. Instead, the reference with the most positive or negative instantaneous voltage is clamped to a level equal plus or minus half the DC link voltage, i.e. $\pm V_{dc}/2$. As for symmetrical modulation, this is equal to calculating a neutral point voltage differing from zero. This is done in the following manner

$$u_z = \begin{cases} \max\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right) - \dfrac{V_{dc}}{2} & \text{if} \quad \max\left(u_{i,ref}\right) > -\min\left(u_{i,ref}\right) \\ \min\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right) + \dfrac{V_{dc}}{2} & \text{if} \quad \max\left(u_{i,ref}\right) < -\min\left(u_{i,ref}\right) \end{cases} \tag{A.31}$$

For $\omega_1 t = \pi/4$ this yields

$$u_z = \min\left(u_{a,ref}, u_{b,ref}, u_{c,ref}\right) + \frac{V_{dc}}{2} = u_{c,ref} + \frac{V_{dc}}{2} = 61.1\,\text{V} \tag{A.32}$$

The resulting voltage references are calculated according to

$$\begin{cases} u_{az,ref} = u_{a,ref} - u_z = 168.7\,\text{V} \\ u_{bz,ref} = u_{b,ref} - u_z = 23.0\,\text{V} \\ u_{cz,ref} = u_{c,ref} - u_z = -375.0\,\text{V} \end{cases} \tag{A.33}$$

The corresponding switching times (calculated for the negative slope of the carrier):

$$\begin{cases} t_a = \left(\frac{1}{2} - \frac{u_{az,ref}}{V_{dc}}\right) \cdot T_s = 0.275 \cdot T_s = 27.5\,\mu s \\ t_b = \left(\frac{1}{2} - \frac{u_{bz,ref}}{V_{dc}}\right) \cdot T_s = 0.469 \cdot T_s = 46.9\,\mu s \\ t_c = \left(\frac{1}{2} - \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 1.000 \cdot T_s = 100.0\,\mu s \end{cases} \tag{A.34}$$

The corresponding duration of each voltage vector (during the negative slope of the carrier) is equal to

$$\begin{cases} \Delta t_{000} = t_a - 0 = \left(\frac{1}{2} - \frac{u_{az,ref}}{V_{dc}}\right) \cdot T_s = 27.5\,\mu s \\ \Delta t_{100} = t_b - t_a = \left(\frac{u_{az,ref}}{V_{dc}} - \frac{u_{bz,ref}}{V_{dc}}\right) \cdot T_s = 19.4\,\mu s \\ \Delta t_{110} = t_c - t_b = \left(\frac{u_{bz,ref}}{V_{dc}} - \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 53.1\,\mu s \\ \Delta t_{111} = T_s - t_c = \left(\frac{1}{2} + \frac{u_{cz,ref}}{V_{dc}}\right) \cdot T_s = 0.0\,\mu s \end{cases} \tag{A.35}$$

Applying this to equation (A.19) gives current increase according to Table A.5.

Table A.5: Current vector increase.

Switch state	Δi_α [A]	Δi_β [A]
000	-4.55	-4.55
100	3.78	-3.21
110	0.77	7.77
111	0.0	0.0

As before, the sum of the variations equals zero. The space vector current trajectory for one switching interval, i.e. both the positive and the negative slope of the carrier, is shown in Figure A.9.

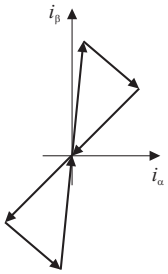

Figure A.9: Current vectors for modulation with bus-clamped references at $\omega_1 t=\pi/4$.

Appendix B

Vector control

A model-based controller is derived for a grid connected voltage source converter. The controller is model-based in the sense that the controller parameters are dependent on the grid parameters, i.e. L (L_{line}) and R (R_{line}). The current controller for three-phase converters discussed here is based on the synchronously rotating (dq) reference frame. Synchronously rotating refers to that the reference frame is rotating with the same speed as the grid voltage vector $\vec{e}^{\,\alpha\beta}$. The rotating reference system has two axes denoted d and q. The grid voltage vector $\vec{e}^{\,\alpha\beta}$ coincides with the q-axis in this case, which means that $e_d = 0$ (Figure A.5). The transformation expressions are written

$$\vec{s}^{\,dq} = \vec{s}^{\,\alpha\beta} \cdot e^{-j\omega_1 t} \quad \text{and} \quad \vec{s}^{\,\alpha\beta} = \vec{s}^{\,dq} \cdot e^{j\omega_1 t} \tag{B.1}$$

The controller is based on a model of the grid together with the converter output filter

$$\vec{u}^{\,\alpha\beta} - L\frac{d}{dt}\vec{i}^{\,\alpha\beta} - R\vec{i}^{\,\alpha\beta} - \vec{e}^{\,\alpha\beta} = 0 \tag{B.2}$$

This is transformed to dq-coordinates by use of the transformation above, i.e.

$$\vec{u}^{\,dq} \cdot e^{j\omega_1 t} - L\frac{d}{dt}\left(\vec{i}^{\,dq} \cdot e^{j\omega_1 t}\right) - R\vec{i}^{\,dq} \cdot e^{j\omega_1 t} - \vec{e}^{\,dq} \cdot e^{j\omega_1 t} = 0 \tag{B.3}$$

which gives

$$\vec{u}^{\,dq} \cdot e^{j\omega_1 t} - L\frac{d}{dt}\vec{i}^{\,dq} \cdot e^{j\omega_1 t} - j\omega_1 L\vec{i}^{\,dq} \cdot e^{j\omega_1 t} - R\vec{i}^{\,dq} \cdot e^{j\omega_1 t} - \vec{e}^{\,dq} \cdot e^{j\omega_1 t} = 0 \tag{B.4}$$

Simplifying the last expression gives

$$\vec{u}^{dq} - L\frac{d}{dt}\vec{i}^{dq} - j\omega_1 L\vec{i}^{dq} - R\vec{i}^{dq} - \vec{e}^{dq} = 0 \tag{B.5}$$

If this is divided into its components, i.e. real and imaginary parts, the resulting expressions are

$$\begin{cases} u_d = L\dfrac{d}{dt}i_d + Ri_d - \omega_1 Li_q + e_d \\ u_q = L\dfrac{d}{dt}i_q + Ri_q + \omega_1 Li_d + e_q \end{cases} \tag{B.6}$$

Note the cross-coupling terms. A discrete-time, dead-beat PI-controller is designed for each component based on the last two expressions. The output from the controller is two voltage references, one in *d*- and one in *q*-direction. The first step is to use backward Euler approximation [81] for the current derivatives. This gives

$$\begin{cases} \dfrac{di_d}{dt} \approx \dfrac{i_{d,k} - i_{d,k-1}}{T_s} \\ \dfrac{di_q}{dt} \approx \dfrac{i_{q,k} - i_{q,k-1}}{T_s} \end{cases} \tag{B.7}$$

Furthermore, it is assumed that the currents can be approximated with their average values, in the particular sampling interval

$$\begin{cases} i_d \approx \dfrac{i_{d,k} + i_{d,k-1}}{2} \\ i_q \approx \dfrac{i_{q,k} + i_{q,k-1}}{2} \end{cases} \tag{B.8}$$

It is also assumed that the grid voltage does not change between two samples. Consequently,

$$\begin{cases} e_{d,k} \approx e_{d,k-1} \\ e_{q,k} \approx e_{q,k-1} \end{cases} \tag{B.9}$$

This gives the following result

$$\begin{cases} u_{d,k} = L\dfrac{i_{d,k} - i_{d,k-1}}{T_s} + R\dfrac{i_{d,k} + i_{d,k-1}}{2} - \omega_1 L\dfrac{i_{q,k} + i_{q,k-1}}{2} + e_{d,k-1} \\ u_{q,k} = L\dfrac{i_{q,k} - i_{q,k-1}}{T_s} + R\dfrac{i_{q,k} + i_{q,k-1}}{2} + \omega_1 L\dfrac{i_{d,k} + i_{d,k-1}}{2} + e_{q,k-1} \end{cases} \tag{B.10}$$

Since a dead-beat controller is considered, it is assumed that

$$\begin{cases} i_{d,k} = i_{d,ref,k-1} \\ i_{q,k} = i_{q,ref,k-1} \end{cases} \tag{B.11}$$

giving

$$\begin{cases} u_{d,k} = L\dfrac{i_{d,ref,k} - i_{d,k}}{T_s} + R\dfrac{i_{d,ref,k} + i_{d,k}}{2} - \omega_1 L\dfrac{i_{q,ref,k} + i_{q,k}}{2} + e_{d,k} \\ u_{q,k} = L\dfrac{i_{q,ref,k} - i_{q,k}}{T_s} + R\dfrac{i_{q,ref,k} + i_{q,k}}{2} + \omega_1 L\dfrac{i_{d,ref,k} + i_{d,k}}{2} + e_{q,k} \end{cases} \tag{B.12}$$

This gives a P-controller according to

$$\begin{cases} u_{d,ref,k} = \left(\dfrac{L}{T_s} + \dfrac{R}{2}\right)\cdot\left(i_{d,ref,k} - i_{d,k}\right) + R\cdot i_{d,k} - \omega_1 L\dfrac{i_{q,ref,k} + i_{q,k}}{2} + e_{d,k} \\ u_{q,ref,k} = \left(\dfrac{L}{T_s} + \dfrac{R}{2}\right)\cdot\left(i_{q,ref,k} - i_{q,k}\right) + R\cdot i_{q,k} + \omega_1 L\dfrac{i_{d,ref,k} + i_{d,k}}{2} + e_{q,k} \end{cases} \tag{B.13}$$

The resistive voltage drop term can be interpreted as an integral part assuming that the current equals the sum of all the previous current errors, i.e.

$$\begin{cases} i_{d,k} = \sum_{n=0}^{k-1}\left(i_{d,ref,n} - i_{d,n}\right) \\ i_{q,n} = \sum_{n=0}^{k-1}\left(i_{q,ref,n} - i_{q,n}\right) \end{cases} \tag{B.14}$$

This gives a PI-controller

$$\begin{cases} u_{d,ref,k} = K \cdot \left(\left(i_{d,ref,k} - i_{d,k} \right) + \frac{1}{T_i} \cdot \sum_{n=0}^{k-1} \left(i_{d,ref,n} - i_{d,n} \right) \right) - K_c \cdot \frac{i_{q,ref,k} + i_{q,k}}{2} + e_{d,k} \\ u_{q,ref,k} = K \cdot \left(\left(i_{q,ref,k} - i_{q,k} \right) + \frac{1}{T_i} \cdot \sum_{n=0}^{k-1} \left(i_{q,ref,n} - i_{q,n} \right) \right) + K_c \cdot \frac{i_{d,ref,k} + i_{d,k}}{2} + e_{q,k} \end{cases} \quad \text{(B.15)}$$

where

$$\begin{cases} K = \left(\frac{L}{T_s} + \frac{R}{2} \right) \\ T_i = R \Big/ \left(\frac{L}{T_s} + \frac{R}{2} \right) = 1 \Big/ \left(\frac{L}{RT_s} + \frac{1}{2} \right) \\ K_c = \frac{\omega_1 L}{2} \end{cases} \quad \text{(B.16)}$$

The impact of the one-sample delay introduced by DSP-control (Chapter 2) is reduced by application of a Smith-predictor [6]. The Smith predictor calculates current references according to [6]

$$\begin{cases} i_{smith,d,k} = \frac{RT_s}{L} \cdot s_{d,k-1} - \omega_1 T_s \cdot s_{q,k-1} - \frac{T_s}{L} \cdot u_{d,k-1} \\ i_{smith,q,k} = \frac{RT_s}{L} \cdot s_{q,k-1} + \omega_1 T_s \cdot s_{d,k-1} - \frac{T_s}{L} \cdot u_{q,k-1} \end{cases} \quad \text{(B.17)}$$

$$\begin{cases} s_{d,k} = \left(1 - \frac{RT_s}{L} \right) \cdot s_{d,k-1} + \omega_1 T_s \cdot s_{q,k-1} + \frac{T_s}{L} \cdot u_{d,k-1} \\ s_{q,k} = \left(1 - \frac{RT_s}{L} \right) \cdot s_{q,k-1} - \omega_1 T_s \cdot s_{d,k-1} + \frac{T_s}{L} \cdot u_{q,k-1} \end{cases} \quad \text{(B.18)}$$

The current references above are added to the current references based on desired output power. The resulting voltage references, in *dq*–coordinates, are transformed to the fixed $\alpha\beta$-frame. Then the $\alpha\beta$-references are transformed to three-phase reference voltages. If the modulation is based on sinusoidal references the three-phase voltage references are used as they are. Otherwise, they are manipulated, for example to become symmetrical or bus-clamped, and then passed on to the modulator.

Appendix C

Converter losses

In this appendix an analytical method for estimation of the semiconductor losses of a self-commutated three-phase VSC is described. A similar method is found in [59]. The calculations are made for a single half-bridge, see Figure C.1. Since the output from a three-phase VSC is a line-to-line voltage, the corresponding line-to-neutral voltage has to be calculated if only a single half-bridge is considered. The original sinusoidal voltage references are used even though they are phase potentials. This is applicable since the average losses are calculated only for the fundamental current component, i.e. neglecting the ripple.

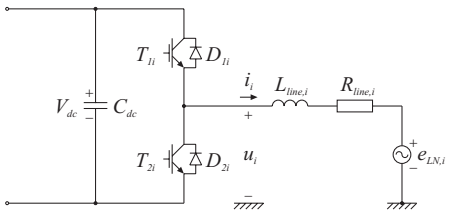

Figure C.1: One half-bridge of a three-phase voltage source converter.

The calculations are based on data sheet information, which is usually only valid for inductive load currents. For a VSC utilising hard-switching, this is not a limitation since the AC side filters are inductive in this case. Furthermore, the calculations only take the fundamental current into account, i.e. the current ripple is not considered.

Figure C.2 shows the fundamental components of the output voltage and current, for one half-bridge of the converter. The converter output current lags the voltage with an angle φ.

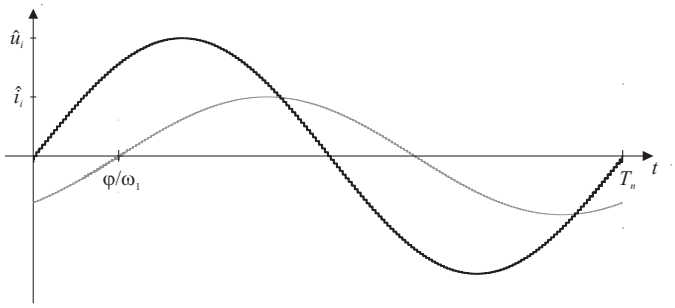

Figure C.2: Converter output voltage and current. The current is displaced by an angle φ relative to the voltage.

For the IGBTs of one half-bridge, the switching losses are estimated from

$$\begin{aligned}\overline{P}_{Ti,sw} &= \frac{1}{T_n}\int_{T_n}\left(P_{on}+P_{off}\right)dt = \frac{f_{sw}}{T_n}\int_{T_n}\left(E_{on}+E_{off}\right)dt = \\ &= \frac{E_{on,n}+E_{off,n}}{V_{dc,n}\cdot I_n}\cdot\frac{V_{dc}\,f_{sw}}{T_n}\int_{T_n}\left|\hat{i}_i\sin(\omega_1 t-\varphi)\right|dt = \\ &= \frac{2\sqrt{2}}{\pi}\cdot\frac{E_{on,n}+E_{off,n}}{V_{dc,n}\cdot I_n}\cdot V_{dc}I_i\,f_{sw}\end{aligned} \tag{C.1}$$

where $E_{on,n}$ and $E_{off,n}$ are the turn-on and turn-off energy loss per switching cycle, specified in data sheets for DC link voltage $V_{dc,n}$ and inductively clamped output current I_n. The switching losses for the freewheeling diodes of a half-bridge are calculated in a similar manner. The turn-on loss for a switching diode is usually negligible whereas the turn-off losses are almost completely due to reverse recovery (E_{Drr}). This gives

$$\begin{aligned}\overline{P}_{Di,sw} &= \frac{1}{T_n}\int_{T_n}\left(P_{on}+P_{off}\right)dt = \frac{f_{sw}}{T_n}\int_{T_n}\left(E_{on}+E_{off}\right)dt = \\ &= \frac{2\sqrt{2}}{\pi}\cdot\frac{E_{off,n}}{V_{dc,n}\cdot I_n}\cdot V_{dc}I_i\,f_{sw} = \frac{2\sqrt{2}}{\pi}\cdot\frac{E_{Drr,n}}{V_{dc,n}\cdot I_n}\cdot V_{dc}I_i\,f_{sw}\end{aligned} \tag{C.2}$$

The conduction losses are more complicated to calculate. The forward voltage drop of an IGBT and a freewheeling diode are given by

$$\begin{cases} V_{T(on)} = V_{T0} + R_{T(on)} i_T \\ V_{D(on)} = V_{D0} + R_{D(on)} i_D \end{cases} \tag{C.3}$$

For the half period where the current is positive, i.e. in the interval $\omega_1 t = [\varphi..\pi+\varphi]$ of Figure C.2, the transistor T_{1i} and the freewheeling diode D_{2i} are conducting. The duty cycle d_{T1i} for T_{1i} in this interval is given by

$$d_{T1i} = \frac{1}{2} + \frac{u_i}{V_{dc}} = \frac{1}{2} + \frac{\hat{u}_i \sin(\omega_1 t)}{V_{dc}} \tag{C.4}$$

The corresponding duty cycle for D_{2i} is

$$d_{D2i} = 1 - d_{T1i} = \frac{1}{2} - \frac{\hat{u}_i \sin(\omega_1 t)}{V_{dc}} \tag{C.5}$$

The conduction losses for one IGBT and freewheeling diode are written

$$\begin{cases} P_{T1i,cond} = V_{T(on)} i_i d_{T1i} \\ P_{D2i,cond} = V_{D(on)} i_i d_{D2i} \end{cases} \tag{C.6}$$

The average losses for one period of the output fundamental are found by integration. Note that T_{1i} and D_{2i} are only conducting when the output current is positive, i.e. in the interval $\omega_1 t = [\varphi..\pi+\varphi]$. This gives

$$\begin{aligned} \overline{P}_{T1i,cond} = &\left(\frac{1}{2\pi} \cdot V_{T0} \hat{i}_i + \frac{1}{8} \cdot R_{T(on)} \hat{i}_i^2 \right) + \\ &+ \left(\frac{1}{4} \cdot V_{T0} \hat{i}_i + \frac{1}{3\pi} \cdot R_{T(on)} \hat{i}_i^2 \right) \cdot \frac{\hat{u}_i \cos(\varphi)}{V_{dc}} \end{aligned} \tag{C.7}$$

and

$$\begin{aligned} \overline{P}_{D2i,cond} = &\left(\frac{1}{2\pi} \cdot V_{D0} \hat{i}_i + \frac{1}{8} \cdot R_{D(on)} \hat{i}_i^2 \right) - \\ &- \left(\frac{1}{4} \cdot V_{D0} \hat{i}_i + \frac{1}{3\pi} \cdot R_{D(on)} \hat{i}_i^2 \right) \cdot \frac{\hat{u}_i \cos(\varphi)}{V_{dc}} \end{aligned} \tag{C.8}$$

For one half-bridge, the conduction losses are twice the losses of a single IGBT and diode, i.e.

$$\begin{aligned}\overline{P}_{Ti,cond} = &\left(\frac{\sqrt{2}}{\pi}\cdot V_{T0}I_i + \frac{1}{2}\cdot R_{T(on)}I_i^2\right) + \\ &+\left(V_{T0}I_i + \frac{4\sqrt{2}}{3\pi}\cdot R_{T(on)}I_i^2\right)\cdot\frac{U_i\cos(\varphi)}{V_{dc}}\end{aligned} \tag{C.9}$$

and

$$\begin{aligned}\overline{P}_{Di,cond} = &\left(\frac{\sqrt{2}}{\pi}\cdot V_{D0}I_i + \frac{1}{2}\cdot R_{D(on)}I_i^2\right) - \\ &-\left(V_{D0}I_i + \frac{4\sqrt{2}}{3\pi}\cdot R_{D(on)}I_i^2\right)\cdot\frac{U_i\cos(\varphi)}{V_{dc}}\end{aligned} \tag{C.10}$$

Note that the converter output RMS voltage U and current I for phase i are used in the two last expressions.

In stationary conditions, the RMS single line equation

$$U - j\omega_1 LI - E_{LN} = 0 \tag{C.11}$$

applies. By separation of the real and imaginary parts

$$\begin{cases}\omega_1 LI\cos(\varphi) = E_{LN}\sin(\delta_{load}) \\ U - \omega_1 LI\sin(\varphi) = E_{LN}\cos(\delta_{load})\end{cases} \tag{C.12}$$

is obtained. By putting the load angle equal to the phase lag, i.e.

$$\delta_{load} = \varphi \tag{C.13}$$

equivalent to unity power factor for the source or load, it is found that

$$\varphi = \arctan\left(\frac{\omega_1 LI}{E_{LN}}\right) \tag{C.14}$$

for inverter operation. For rectifier operation the same expression is valid but with negative line current. The converter output voltage is given by

$$U = E_{LN}\cos(\delta_{load}) + \omega_1 LI\sin(\varphi) = \frac{E_{LN}^2 + (\omega_1 LI)^2}{E_{LN}}\cos(\varphi) \quad \text{(C.15)}$$

which means that the RMS output voltage of the converter is equal in both cases. The phase displacement is also equal but with opposite sign.

This is compared to measurement results of [43], where the losses of a battery charger consisting of four half-bridges are measured. The fourth half-bridge operates as a step-down converter with the output connected to the batteries via an inductive filter. The losses of the battery side half-bridge are given by

$$\overline{P}_T = \left(V_{T0} I_{batt} + R_{T(on)} I_{batt}^2\right) \cdot \frac{V_{batt}}{V_{dc}} + \frac{E_{on,n} + E_{off,n}}{V_{dc,n} \cdot I_n} \cdot V_{dc} I_{batt} f_{sw} \quad \text{(C.16)}$$

for the IGBT and

$$\overline{P}_D = \left(V_{D0} I_{batt} + R_{D(on)} I_{batt}^2\right) \cdot \left(1 - \frac{V_{batt}}{V_{dc}}\right) + \frac{E_{Drr,n}}{V_{dc,n} \cdot I_n} \cdot V_{dc} I_{batt} f_{sw} \quad \text{(C.17)}$$

for the freewheeling diode. All the half-bridges of the battery charger are Semikron SKM50GB123D modules, with approximate data according to Table C.1.

Table C.1: Semikron SKM50GB123D data.

V_{T0}	2.0 V	*Data valid for:*
$R_{T(on)}$	27 mΩ	$T_{junction}$=125 °C
$E_{on,n}+E_{off,n}$	11.5 mWs	$V_{dc,n}$=600 V
V_{D0}	1.2 V	I_n=40 A
$R_{D(on)}$	11.7 mΩ	R_{Gate}=22 Ω
$E_{Drr,n}$	1.9 mWs	

The battery charger operates at V_{dc}=650 V. The input and output power, neglecting the filters, are P_{in}=5765 W and P_{out}=5581 W. The input and output power are measured simultaneously with a four-channel Norma 6100 wide band power analyzer. The three-phase boost rectifier is connected to a 400 V, 50 Hz grid. Consequently, U=233 V. The step down converter is connected

to a battery with V_{batt}=243 V. The calculated losses equal 159 W, whereas the measured are 184 W. Note that the losses of DC link bleeder resistors, with a total resistance of 22 kΩ, and the resistors in series with the LEM LV50P DC bus voltage transducer, with a resistance of 75 kΩ, are not included. The total power loss in these resistors equals 25 W, which is also equal to the difference between the calculated and measured losses. Note that the losses in the DC bus capacitors are not included in the calculation. In [43], the simulated DC link capacitor losses for a 10 kW hard-switched battery charger is found to be approximately 5 W, or 0.05% of the output power. In this case this corresponds to approximately 3 W. Thus, the estimated converter losses equal 187 W.

Appendix D

Normalisation

In this appendix, the normalisation bases used in the thesis are given. Also, the impact on converter DC bus voltage caused by unbalanced AC side loading is investigated. This method can be applied to select appropriate DC link capacitors [6].

D.1 Base system for a single converter

This section gives two per unit base systems. The one used mostly in the thesis is based on converter DC side data. There is however another based on AC data which is used for two purposes in this thesis, namely to calculate appropriate line side filter inductance for VSC based HVDC and generator inductance for wind power generators.

Normalisation based on DC side data

$$V_{base} = V_{dc,ref} \tag{D.1}$$

$$I_{base} = I_{dc,n} = \frac{P_n}{V_{dc,ref}} \tag{D.2}$$

$$R_{base} = R_n = \frac{V_{dc,ref}^2}{P_n} \tag{D.3}$$

$$C_{base} = C_n = \frac{P_n}{V_{dc,ref}^2} \cdot \frac{2\zeta_n^2}{\omega_{lp}} \cdot \frac{1}{(1-\delta_n)\delta_n} \tag{D.4}$$

$$\tau_{base} = R_{base} C_{base} = \frac{2\zeta_n^2}{\omega_{lp}} \cdot \frac{1}{(1-\delta_n)\delta_n} \tag{D.5}$$

$$\omega_{base} = \frac{1}{\tau_{base}} = \omega_{lp} \cdot \frac{(1-\delta_n)\delta_n}{2\zeta_n^2} \tag{D.6}$$

$$L_{base} = \frac{R_{base}}{\omega_{base}} = \frac{V_{dc,ref}^2}{P_n} \cdot \frac{2\zeta_n^2}{\omega_{lp}} \cdot \frac{1}{(1-\delta_n)\delta_n} \tag{D.7}$$

Normalisation based on AC side data

$$S_{base} = S_n \tag{D.8}$$

$$P_{base} = S_n \tag{D.9}$$

$$V_{base} = E_n = E_{LL,n} \tag{D.10}$$

$$I_{base} = \frac{S_{base}}{\sqrt{3} V_{base}} = \frac{S_n}{\sqrt{3} E_n} = I_n \tag{D.11}$$

$$X_{base} = Z_{base} = \frac{V_{base}}{\sqrt{3} I_{base}} \frac{V_{base}^2}{S_{base}} = \frac{S_{base}}{3 I_{base}^2} \tag{D.12}$$

$$\omega_{base} = \omega_{1,n} = 2\pi f_{1,n} \tag{D.13}$$

$$L_{base} = \frac{X_{base}}{\omega_{base}} \tag{D.14}$$

D.2 Converter data expressed in per unit

The DC link capacitor can be specified from the rated power and the allowed disturbance for non-symmetrical loading [6]. The DC link capacitor is selected based on the requirement that the DC link voltage must not vary with amplitude higher than $\pm 0.05 V_{dc,n}$ for single-phase operation at rated AC side current. The rated power determines the minimum converter DC side equivalent resistance.

Selection of converter DC side capacitor

Assume that the three-phase converter is connected to an AC power system with the grid voltages given by

$$\begin{cases} e_a = \hat{e}\cos(\omega_1 t) \\ e_b = \hat{e}\cos(\omega_1 t - 2\pi/3) \\ e_c = \hat{e}\cos(\omega_1 t - 4\pi/3) \end{cases} \tag{D.15}$$

This gives the power-invariant transformation into the stationary $\alpha\beta$-reference frame according to

$$\vec{e}^{\,\alpha\beta} = e_\alpha + je_\beta = \sqrt{\frac{3}{2}}\hat{e}(\cos(\omega_1 t) + j\sin(\omega_1 t)) \tag{D.16}$$

This is transferred into the rotating *dq*-reference frame by

$$\begin{aligned} \vec{e}^{\,dq} &= e^{-j\theta}\cdot\vec{e}^{\,\alpha\beta} = (\cos\theta - j\sin\theta)\cdot(e_\alpha + je_\beta) = \\ &= (e_\alpha\cos\theta + e_\beta\sin\theta) + j(-e_\alpha\sin\theta + e_\beta\cos\theta) = e_d + je_q \end{aligned} \tag{D.17}$$

If the definition

$$\begin{cases} e_d = 0 \\ e_q > 0 \end{cases} \tag{D.18}$$

is used it is found that

$$\theta = \omega_1 t - \pi/2 \tag{D.19}$$

which specifies the rotating coordinate system (Figure A.5).

Now it is assumed that the converter is operating with current flowing only in two phases. This can be the case if for example one of the AC side fuses has failed. This implies that the current on the AC side is written

$$\begin{cases} i_a = \hat{i}\cos(\omega_1 t - \varphi) \\ i_b = -i_a = -\hat{i}\cos(\omega_1 t - \varphi) \\ i_c = 0 \end{cases} \tag{D.20}$$

In the stationary $\alpha\beta$-coordinate system the current vector is expressed as (power invariance)

$$\vec{i}^{\,\alpha\beta} = i_\alpha + j i_\beta = \sqrt{\frac{3}{2}}\hat{i}\cos(\omega_1 t - \varphi) - j\frac{1}{\sqrt{2}}\hat{i}\cos(\omega_1 t - \varphi) \tag{D.21}$$

which for the rotating *dq*-reference system gives

$$\vec{i}^{\,dq} = e^{-j\theta}\cdot\vec{i}^{\,\alpha\beta} = i_d + j i_q \tag{D.22}$$

where

$$\begin{cases} i_d = \frac{\hat{i}}{\sqrt{2}}\left(\sin(\varphi + \pi/6) + \sin(2\omega_1 t - \varphi + \pi/6)\right) \\ i_q = \frac{\hat{i}}{\sqrt{2}}\left(\cos(\varphi + \pi/6) + \cos(2\omega_1 t - \varphi + \pi/6)\right) \end{cases} \tag{D.23}$$

From the expression above it is found that if the line-to-line voltage

$$e_{ab} = e_a - e_b = \sqrt{3}\hat{e}\cos(\varphi + \pi/6) \tag{D.24}$$

is in phase with the corresponding current, i.e. if

$$\varphi = -\pi/6 \tag{D.25}$$

The current components are given by

$$\begin{cases} i_d = \frac{\hat{i}}{\sqrt{2}}\sin(2\omega_1 t + \pi/3) \\ i_q = \frac{\hat{i}}{\sqrt{2}}\left(1 + \cos(2\omega_1 t + \pi/3)\right) \end{cases} \tag{D.26}$$

The input power is written

$$p = e_q i_q = \sqrt{\frac{3}{2}}\hat{e} \cdot \frac{\hat{i}}{\sqrt{2}}\left(1+\cos\left(2\omega_1 t+\pi/3\right)\right) = \sqrt{3}E_{LN} I\left(1+\cos\left(2\omega_1 t+\pi/3\right)\right) \quad \text{(D.27)}$$

If the current in the *a*- and *b*-phases has a magnitude corresponding to rated conditions, the power is thus written

$$p = E_{LL,n} I_n \left(1+\cos\left(2\omega_1 t+\pi/3\right)\right) \quad \text{(D.28)}$$

Note that for rated conditions with equal current in all three phases, the power is written

$$P_n = e_{q,n} i_{q,n} = \sqrt{\frac{3}{2}}\hat{e} \cdot \sqrt{\frac{3}{2}}\hat{i} = \sqrt{3}E_{LL,n} I_n \quad \text{(D.29)}$$

For the case with the *c*-phase current equal to zero, the constant term of the input power is transferred to the DC network. The time dependent term of the power results in an oscillation in the DC bus voltage, at least close to the DC bus capacitor of the converter drawing an unsymmetrical current. The power fed to the DC link capacitor is written

$$p_{Cdc} = v_{Cdc} \cdot i_{Cdc} = v_{Cdc} \cdot C_{dc} \frac{dv_{Cdc}}{dt} = \sqrt{3}E_{LN} I \cos\left(2\omega_1 t+\pi/3\right) \quad \text{(D.30)}$$

Assuming a DC bus voltage equal to

$$v_{Cdc} = V_{dc} + \Delta v_{Cdc} \sin\left(2\omega_1 t+\pi/3\right) \quad \text{(D.31)}$$

gives

$$\begin{aligned} p_{Cdc} = v_{Cdc} \cdot C_{dc} \frac{dv_{Cdc}}{dt} &\approx 2\omega_1 C_{dc} V_{dc} \Delta v_{Cdc} \cos\left(2\omega_1 t+\pi/3\right) \approx \\ &\approx \sqrt{3}E_{LN} I \cos\left(2\omega_1 t+\pi/3\right) \end{aligned} \quad \text{(D.32)}$$

For an *a*- and *b*-phase converter current and a grid voltage corresponding to rated conditions, a criterion giving the maximum DC bus voltage variation can be formulated according to

$$C_{dc} \geq \frac{P_n}{2\sqrt{3} \cdot \omega_1 V_{dc,n} \Delta V_{dc,\max}} \quad \text{(D.33)}$$

which is rewritten as

$$C_{dc} \geq \frac{1}{2\sqrt{3}\cdot\omega_1\left(\frac{\Delta V_{dc}}{V_{dc,n}}\right)_{\max}}\cdot\frac{P_n}{V_{dc,n}^2}=\frac{1}{2\sqrt{3}\cdot\omega_1\left(\frac{\Delta V_{dc}}{V_{dc,n}}\right)_{\max}}\cdot\frac{1}{Z_{base}}= \\ =\frac{C_{base}}{2\sqrt{3}\cdot\left(\frac{\Delta V_{dc}}{V_{dc,n}}\right)_{\max}} \tag{D.34}$$

In p.u. this is, thus, expressed as

$$C_{dc(pu)} \geq \frac{1}{2\sqrt{3}\cdot\left(\Delta v_{dc}\right)_{\max}} \tag{D.35}$$

For a given converter the equivalent resistance for a certain load is written

$$R_{eq}=\frac{V_{dc}^2}{P}=\frac{V_{dc,n}^2}{P_n}\cdot\frac{v_{dc}^2}{p}=Z_{base}\cdot r_{eq} \tag{D.36}$$

Note that this quantity is not constant, since it depends on the DC bus voltage, which is a dynamical state, and the output power, which is an input signal. The time constant this corresponds to is given by

$$\tau_{dc(pu)}=\frac{r_{eq}}{2\sqrt{3}\cdot\left(\Delta v_{dc}\right)_{\max}} \tag{D.37}$$

Note that the time constant is load dependent, which implies that it must be treated with care. For rated conditions

$$\tau_{dc(pu)}=\frac{1}{2\sqrt{3}\cdot\left(\Delta v_{dc}\right)_{\max}} \tag{D.38}$$

is valid.

Appendix E

Nomenclature

Abbreviations

CM	Common mode
CSC	Current source converter
DAB	Double active bridge
DM	Differential mode
DPS	Distributed power system
EMC	Electro magnetic compatibility
EMI	Electro magnetic interference
ESR	Equivalent series resistance
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
LVDC	Low voltage direct current
MVDC	Medium voltage direct current
PEBB	Power electronic building block
PFC	Power factor corrector
PMSM	Permanent-magnet synchronous machine
SMPS	Switch mode power supply
UPS	Uninteruptable power supply
VSC	Voltage source converter
ZVS	Zero voltage switching
ZVT	Zero voltage transition

Symbols

a, b, c	Converter phase order
C_{base}	Per unit base capacitance
C_{cable}	DC side capacitance of cable segment
C_{dc}	DC side capacitance
C_{fAC}	AC side harmonic filter capacitance of an HVDC converter
C_{fDC}	DC side differential mode filter capacitance of an HVDC converter
C_{fVAr}	AC side shunt reactive power compensation capacitance of an HVDC converter
C_{f1}	AC side shunt harmonic filter capacitance for VSC based HVDC converters
C_{f2}	DC side differential mode filter capacitance for VSC based HVDC converters
C_{f3}	DC side common mode filter capacitance for VSC based HVDC converters
C_{p}	Grounding capacitors
C_{r}	DC side capacitance of the receiving end converter
C_{s}	DC side capacitance of the sending end converter
d	Instantaneous duty cycle or relative delay between DAB converters
d_{D2i}	Instantaneous duty cycle for the lower freewheeling diode of the half-bridge connected to phase i
d_{T1i}	Instantaneous duty cycle for the upper transistor of the half-bridge connected to phase i
E_{LL}	AC grid line-to-line RMS voltage in general
E_{LN}	AC grid line-to-neutral RMS voltage in general
E_{n}	Rated AC grid line-to-line voltage
E_{Drr}	Freewheeling diode reverse recovery energy loss
E_{off}	IGBT turn-off energy loss
E_{on}	IGBT turn-on energy loss
e_{LL}	Instantaneous or p.u. AC grid line-to-line voltage
e_{LN}	Instantaneous or p.u. AC grid line-to-neutral voltage

e_d	Instantaneous converter AC grid voltage in the *d*-direction
e_q	Instantaneous converter AC grid voltage in the *q*-direction
e_α	Instantaneous converter AC grid voltage in the α-direction
e_β	Instantaneous converter AC grid voltage in the β-direction
f	Frequency in general
f_n	Rated AC grid or machine frequency
f_{sw}	Switching frequency
f_1	Fundamental frequency
$G_{cl}(s)$	Voltage closed loop transfer function $V_s/V_{dc,ref}$
H	Wind power aggregate inertia constant
I_{base}	Per unit base current
$I_{Cdc}(s)$	Laplace transform of the total DC bus capacitor current
$I_{Cdc,ref}(s)$	Laplace transform of DC bus capacitor current reference from DC bus voltage controller
I_{dc}	Steady state DC side current
$I_{dc,n}$	Nominal steady state DC side current
$I_{dc,ref,ext}$	External DC side current reference
I_i	Converter AC side RMS current for phase *i*
$I_{idcdiff1}$, $I_{idcdiff2}$	Integral of differential currents for ground fault detection
$I_{line,i}$	Line side RMS current component of harmonic of order *i*
I_n	Nominal AC side RMS current
I_r	Steady state DC side current of the receiving end
$I_r(s)$	Laplace transform of DC side current of the receiving end
I_s	Steady state DC side current of the sending end
$I_s(s)$	Laplace transform of DC side current of the sending end
I_{Trip}	Trip level for integrated differential fault currents
I^2t	Fuse current-time withstanding capability
i_{Cdc}	Instantaneous total DC bus capacitor current
$i_{Cdc,ref}$	Instantaneous DC bus capacitor current reference from DC bus voltage controller
i_{Cp}	Grounding capacitor current

i_D	Instantaneous diode current
i_d	Instantaneous converter AC side current in the *d*-direction
i_{dc}	Instantaneous DC side current
i_{dcap}	Instantaneous current in the positive rail of the *A*-interface of a cable node
i_{dcan}	Instantaneous current in the negative rail of the *A*-interface of a cable node
i_{dcbp}	Instantaneous current in the positive rail of the *B*-interface of a cable node
i_{dcbn}	Instantaneous current in the negative rail of the *B*-interface of a cable node
$i_{dcdiff1}$, $i_{dcdiff2}$	Differential currents for ground fault detection
$i_{dcdiffa}$, $i_{dcdiffb}$	Differential currents of the *A*- and *B*-interfaces of cable node *I*
i_{Fault}	Fault current
i_i	Instantaneous converter AC side current for phase *i*
i_q	Instantaneous converter AC side current in the *q*-direction
$i_{q,dc,ref}$	Instantaneous DC bus current reference from DC bus voltage controller and transferred to AC side *dq*-references
$i_{q,inv,ref}$	Instantaneous rectifier current reference based on inverter output power for a VSC based HVDC transmission system
$i_{q,\,ref}$	Instantaneous AC side current reference in the *q*-direction
i_r	Instantaneous DC side current of the receiving end
i_s	Instantaneous DC side current of the sending end
i_T	Instantaneous transistor current
i_{T1}	Instantaneous primary current of DAB transformer
i_1, i_2	Instantaneous DAB converter currents
i_α	Instantaneous converter AC side current in the α-direction
i_β	Instantaneous converter AC side current in the β-direction
J_m	Wind power aggregate moment of inertia
K	Controller gain in general
K_{fw}	Field weakening controller gain
K_{pitch}	Pitch angle controller gain

K_{wind}	Proportionality constant between wind speed and power
K_{ω}	Speed droop gain
k_i	Current controller gain factor or fault current factor
L	AC side filter inductance (used only in Appendixes)
L_{base}	Per unit base inductance
L_{cable}	DC side cable inductance
L_{cf}	DC side cable inductance in the fault current path
L_{dc}	DC side inductance of physical inductor
L_d	PMSM stator inductance in *d*-direction
L_{Fault}	Fault inductance
L_{f1}	AC side shunt harmonic filter inductance for VSC based HVDC converters
L_{f2}	DC side differential mode filter inductance for VSC based HVDC converters
L_{f3}	DC side common mode filter inductance for VSC based HVDC converters
L_{cable}	DC side inductance of cable segment
L_{line}	AC line inductance
L_s	Transformer winding self-inductance
L_q	PMSM stator inductance in *q*-direction
l_{cable}	DC side cable inductance (p.u.)
m_a	Modulation index
m_f	Pulse number
n	Number of cable nodes or nominal conditions (if index)
P	Steady state or Laplace transform of active power in general
P_{base}	Per unit base active power
P_D	Average diode power losses
P_{gen}	Generator power of wind power aggregate
$P_{n,converter}$	Rated power of a converter
P_s	Steady state power of the sending end
$P_s(s)$	Laplace transform of the sending end power

P_n	Nominal active power
P_{pitch}	Power lost due to pitch angle control
P_r	Steady state power of the receiving end
$P_{ref,ext}$	External power reference
$P_r(s)$	Laplace transform of the receiving end power
P_T	Average IGBT power losses
P_{wind}	Available wind power
P_0	Initial power
$p(s)$	Desired characteristic polynomial
p_{Cdc}	Instantaneous power supplied to the total DC bus capacitance
p_{dc}	Instantaneous DC side power
$p_{inverter}$	Instantaneous output power of the converter operated as inverter for a VSC based HVDC transmission system
p_r	Per unit DC side current of the receiving end
p_s	Per unit DC side current of the sending end
p_1-p_{10}	Instantaneous power of DC bus converters
Q	Reactive power in general
R, S, T	AC line phase order
R	AC side filter resistance (used only in Appendixes)
R_{base}	Per unit base resistance
R_{cable}	DC side resistance of cable segment
R_{cf}	DC side cable resistance in the fault current path
R_{dc}	DC side resistance of physical resistor
$R_{D(on)}$	On-state resistance of freewheeling diodes
R_{droop}	Equivalent droop resistance
R_{ESR}	Equivalent series resistance of a capacitor
R_{eq}	Equivalent DC side resistance of load converter
R_{Fault}	Fault resistance
$R_{Fault,eq}$	Equivalent fault resistance
R_{Gate}	Resistance of IGBT gate resistor
R_{line}	AC line resistance of including filter inductor winding resistance

R_n	Equivalent DC side resistance of a converter at nominal load
R_r	Equivalent resistance of the receiving end converter
R_s	PMSM stator winding resistance
R_{sc}	Transformer short circuit resistance
$R_{T(on)}$	On-state resistance of IGBTs
r_{cable}	DC side cable resistance (p.u.)
r_{eq}	Equivalent resistance of load converter (p.u.)
r_r	Equivalent resistance of the receiving end converter (p.u.)
S	Steady state apparent power in general
S_{base}	Per unit base apparent power
S_n	Nominal apparent power
s	Switch state
T	Period time corresponding to the fundamental frequency
T_{fw}	Field weakening controller integration time constant
T_{gen}	Generator mechanical torque for wind power aggregate
T_i	Controller integration time constant in general
T_s	Sampling interval
T_{sw}	Switching interval
T_{pitch}	Mechanical torque lost due to pitch angle control
T_{wind}	Available mechanical torque for wind power aggregate
t	Time in general
t_{detect}	Time required for fault detection
U	Converter AC side RMS line-to-neutral voltage
U_i	Converter AC side RMS line-to-neutral (virtual neutral) voltage for phase *i*
u	Instantaneous converter AC side line-to-neutral voltage
u_{CM}	Converter AC side common mode voltage
u_{DM}	Converter AC side differential mode voltage
u_d	Instantaneous converter AC side voltage in the *d*-direction
u_i	Instantaneous converter AC side voltage for phase *i*

u_{ij}	Instantaneous converter AC side line-to-line voltage between phases *i* and *j*
$u_{i,ref}$	Instantaneous converter AC side reference voltage for phase *i*
u_{iz}	Instantaneous converter AC side line-to-virtual neutral voltage, in the case a zero-sequence signal is added, for phase *i*
$u_{iz,ref}$	Instantaneous converter AC side reference voltage, with zero-sequence signal added, for phase *i*
u_q	Instantaneous converter AC side voltage in the *q*-direction
u_z	Instantaneous converter AC side zero-sequence voltage
u_α	Instantaneous converter AC side voltage in the α-direction
u_β	Instantaneous converter AC side voltage in the β-direction
V_{base}	Per unit base voltage
V_{D0}	On-state freewheeling diode forward voltage for zero current
V_{dc}	Steady state DC side voltage
$V_{dc}(s)$	Laplace transform of DC side voltage in general
$V_{dc,ref}$	DC side reference voltage
$V_{dc,ref0}$	Initial DC side reference voltage
$V_{dc,ref,HV}$	High voltage side DC reference voltage
$V_{dc,ref,LV}$	Low voltage side DC reference voltage
V_r	Steady state DC side voltage of the receiving end converter
$V_r(s)$	Laplace transform of DC side voltage of the receiving end converter
V_s	Steady state DC side voltage of the sending end converter
$V_s(s)$	Laplace transform of DC side voltage of the sending end converter
V_{T0}	On-state IGBT forward voltage for current equal to zero
v_{Cp}	Grounding capacitor voltages
v_{cable}	Instantaneous cable voltage of HVDC converter in general
v_{dc}	Instantaneous DC side voltage of converters in general
v_{HV}	Instantaneous transmission bus voltage at a converter
v_{T1}, v_{T2}	Instantaneous primary and secondary side voltages of a DAB transformer

v_{wind}	Wind speed
v_1-v_{10}	Instantaneous converter DC side voltage
X_{base}	Per unit base reactance
x_{line}	Line filter reactance (p.u.)
Z	Impedance in general
Z_{base}	Per unit base impedance
Z_{cable}	Cable impedance
Z_L	Inductive filter impedance
Z_r	Equivalent impedance of the receiving end converter
Z_{sc}	Short circuit impedance
z_p	PMSM number of pole pairs

Greek symbols

α	Thyristor converter control angle
α_{id}	Weighting factor for the field weakening controller gain
Δi_α	Converter AC side current ripple in the α-direction
Δi_β	Converter AC side current ripple in the β-direction
ΔV_{dc}	Converter DC bus voltage variation
$\Delta V_{dc,ref}$	DC bus voltage droop reference offset
Δv_{dc}	Converter DC bus voltage variation (p.u.)
$\Delta\omega_{el}$	PMSM electrical angular frequency variation
$\Delta\omega_m$	PMSM mechanical angular frequency variation
δ	Voltage droop in general
δ_r	Voltage droop of the receiving end
δ_s	Voltage droop of the sending end
δ_{load}	AC system load angle
γ	Fault detector forgetting factor
γ_1, γ_2	PMSM speed estimator adaptation gains
φ	AC system phase lag between voltage and current
λ_1, λ_2	Eigenvalues for both closed loop field weakening and fault currents

θ	Rotational angle between the rotating (dq) and the fixed ($\alpha\beta$) reference systems
ρ_0	PMSM speed estimator bandwidth
ρ_1-ρ_4	Closed loop poles of two-converter systems including cable
ρ_s	PMSM speed controller bandwidth
τ_{base}	Per unit base time constant
τ_{cable}	Time constant of the cable
$\tau_{cable(pu)}$	Time constant of the cable (p.u.)
$\tau_{dc(pu)}$	Equivalent time constant of converter DC side (p.u.)
$\tau_{n,converter}$	Nominal equivalent time constant of converter
$\tau_{n,system}$	Nominal equivalent time constant of converter system
τ_{pitch}	Equivalent time constant of pitch angle controller
τ_r	Equivalent time constant of the receiving end converter
$\tau_{r(pu)}$	Equivalent p.u. time constant of the receiving end converter
ω_{base}	Per unit base angular frequency
ω_{el}	PMSM electrical angular frequency
ω_f	PMSM low-pass filtered electrical angular frequency
ω_{lp}	DC bus low-pass filter break-over frequency
$\omega_{lp,id}$	Field weakening low-pass filter break-over frequency
ω_m	PMSM mechanical angular frequency
$\omega_{m,ref}$	PMSM mechanical angular frequency reference
ω_n	Closed loop nominal characteristic frequency of DC bus voltage control
ω_o	Characteristic angular frequency of the sum of the cable and the equivalent receiving end impedance
$\omega_{o(pu)}$	Characteristic p.u. angular frequency of the sum of the cable and the equivalent receiving end impedance
ω_1	Fundamental angular frequency of AC system
Ψ_m	PMSM magnetising flux-linkage
ζ_n	Closed loop nominal damping of DC bus voltage control
ζ_o	Damping of the sum of the cable and the equivalent receiving end impedance