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25 GHz and 28 GHz Wide Tuning Range 130 nm CMOS VCOs with Ferroelectric Varactors

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***Abstract* — Two 130nm CMOS VCOs with ferroelectric varactors are presented. The cross-coupled VCO-cores are flip-chip mounted on silicon carriers with integrated inductors and tunable ferroelectric varactors. The output frequency of the first VCO is tunable from 23.4 GHz to 26.1 GHz, corresponding to a tuning range of 11 %. The phase noise of this VCO, tuned to its center frequency, measures -117 dBC/Hz at 1 MHz offset and the power consumption is 18 mW. The second VCO is tunable from 25.8 GHz to 30.5 GHz, corresponding to a tuning range of 17 %. The phase noise at center frequency for this design measures -109 dBc/Hz and the power consumption is 5.3 mW**

***Index Terms* — VCO, ferroelectric, BSTO, varactor.**

I. Introduction

The demand for higher capacity in telecommunication pushes the systems towards higher operating frequencies. This increases the pressure to find ways to fabricate microwave circuits at a lower cost. To realize high performance microwave transceivers, requiring low noise amplifiers and low phase noise VCOs, low loss components are needed. In this paper the possibility to generate signals above 20 GHz with a continuous tuning range in the order of 15 %, while maintaining a low phase noise, is examined. In fully integrated VCOs at these high frequencies the Q-value of the resonator is limited by the losses of the semiconductor varactor, rather than by inductor losses. Further on, the area required by the passive components will not scale down as the lithography is scaled down. The passive components will accordingly occupy a large part of the chip and represent a large cost. An attractive alternative is therefore to place high-Q passive components off-chip. The components may be possible to place on-chip, but this is for many applications not the most cost-effective solution. The designs of this paper use off-chip room-temperature ferroelectric varactors[1], exhibiting Q-values in the order of 50 at 25 GHz. It is shown that the parasitics of the interface between chip and the carrier are low enough to make the co-design possible and that heterogeneous building practice therefore can provide a platform for the next generation of low cost microwave circuits.

II. Circuit Design

The VCO is based on a cross-coupled differential NMOS core with off-chip varactors and inductor, Fig. 1. The gray area represents the inductor. The cross-coupled topology has the advantage of providing negative resistance over a wide frequency range. This provides a large flexibility as the center frequency and tuning range can be changed over a wide range by carrier re-design. The same chip can therefore be reused for many different designs, which is cost effective.

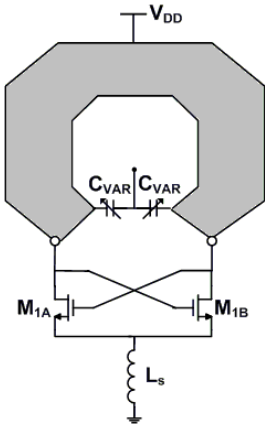

Figure 1. Simplified VCO schematic

A. Chip design

The width of the transistors M_{1A} and M_{1B} in the core are 20 µm. This results in a transconductance large enough to ensure startup of the VCO. Choosing larger devices would increase the capacitive load from the transistors and thereby reduce tuning range. To further reduce the parasitic capacitance, there is no grounded metal shield under the chip pads interfacing the resonator. This results in higher oscillation frequency and larger tuning range.

To isolate the resonator from the 50 Ω load of the measurement system, a 25 fF on-chip capacitor has been used as a passive buffer. The inductor L_s in the source to ground path increases the impedance of the source node at the second harmonic, thereby reducing

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the load of the resonator when the transistors are in the triode region [2].

B. Fabrication of carrier and varactor design

Starting with HR-Si substrates, all processing is carried out in-house at Chalmers. First, a metal layer (M1) consisting of TiO_2 (adhesion layer) and Au is deposited using magnetron sputtering and patterned by ion milling. The BSTO film is subsequently deposited by laser ablation. Next, a layer of SiO_x is introduced in order to prevent DC shorts in large-area decoupling capacitances (via pin-holes in the BSTO film). This layer is removed where the small-sized varactors are formed in order to maximize the tunability of these components. Besides, patterned rings of SiO_2 layer are used as aligning and stop-soldering barriers for mounting of transistor chips. The second metal layer (M2) is deposited by e-beam evaporation and patterned by lift-off. It consists of Ti (improving adhesion to SiO_x) and Au.

The parallel-plate varactors are formed between metal layers M1 and M2. The parallel-plate configuration was chosen because of its high tunability, in comparison to co-planar configuration, at low control voltages. The test varactors sharing substrate with the VCOs have been characterized at 1 MHz. Fig. 2 shows capacitance and loss tangent of a test varactor versus DC bias voltage. The increased loss tangent at positive bottom electrode voltages is caused by increased current through the lowered Ti/BSTO Schottky barrier at the top interface. The small imprint (approximately 0.5 V) is due to asymmetrical top/bottom electrode structure. The capacitance-voltage curve reveals no significant hysteresis. The tunability is 42%. Similar varactors have also been characterized at microwave frequencies, showing a Q-factor higher than 60 and 35 % tunability at frequencies up to 25 GHz [1].

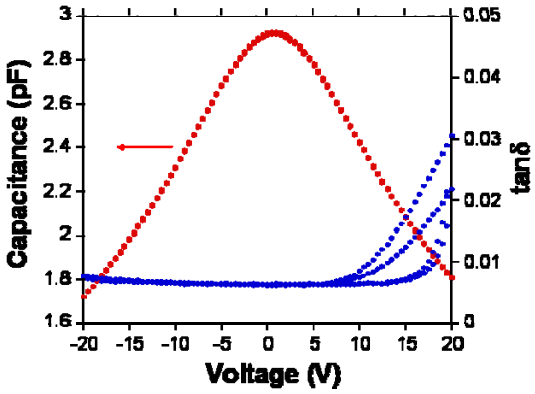

Figure 2. Capacitance and loss tangent of a test varactor versus DC bias voltage.

B. Resonator design

Two different resonators were manufactured, one with a varactor tunable from 50 fF to 90 fF, and one with a 270 fF to 450 fF varactor, Fig. 3. The resonator with the 450 fF varactor has a simulated impedance at resonance of 25 Ω, a Q around 20, and a simulated tuning range 80 % larger than for the other one as the transistor and pad capacitances have less influence when such a large varactor is employed. For the resonator based on the 90 fF varactor the simulated impedance is 40 Ω and the Q is approximately 30.

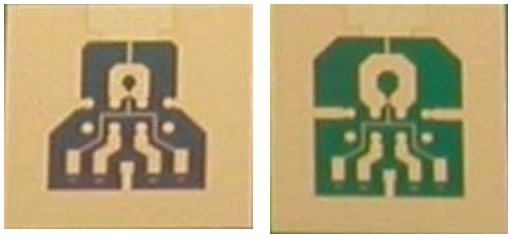

Figure 3. Layouts of the on-carrier resonators. Left: low impedance resonator, Right: high impedance resonator

D. Assembly of module

The flip chip devices have tin-silver-copper bumps manufactured in a high-volume wafer process. Soldering flip chips provides the smoothest process with regards to producibility, self-alignment and repeatability, hence resulting in the lowest cost end-product. The chips were mounted on the carriers using a regular surface mount pick-and-place process. The chip bumps are dipped to a controlled depth in a flux bath, and are then placed on the carrier. The flux is slightly tacky and thus keeps the chip in place while the assembly travels on the conveyor belt through the nitrogen atmosphere soldering oven. The selected flux is a no-clean type, and therefore there was no cleaning step after soldering. The chips are not underfilled at this stage.

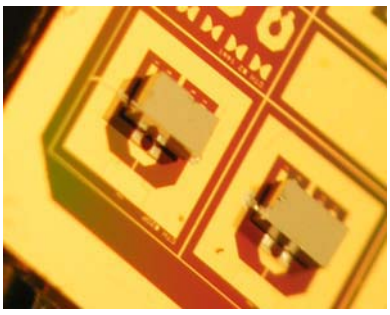

Figure 4. A complete VCO, chip mounted on carrier. The carrier area employed for each design is 1.3x1.4 mm^2

III. Measured Results

The performance of the VCOs is summarized in Table I. The phase noise performance has been measured in a setup based on the delay line technique, whereas frequency characteristics were measured with a spectrum analyzer. Fig. 5 shows the measured tuning characteristics of VCO1 and Fig. 6 the tuning characteristics of VCO2. The output power of the VCOs is depicted in Fig. 7. The measured phase noise over tuning range for VCO1 and VCO2 is shown in Fig. 8 and Fig. 9 respectively.

TABLE I
SUMMARY OF VCO PERFORMANCE

	VCO1	VCO2
Current consumption	6.6mA @ 0.8V	12.8mA @ 1.4V
Varactor size	270-450 fF	50-90 fF
Center frequency	28 GHz	24.8 GHz
Tuning range	25.8 -30.5 GHz	23.4-26.1 GHz
Phase Noise@1MHz offset*	-109 dBc/Hz	-117 dBc/Hz
Phase noise@100kHz offset*	-80 dBc/Hz	-89 dBc/Hz

* Phase noise measured at center frequency

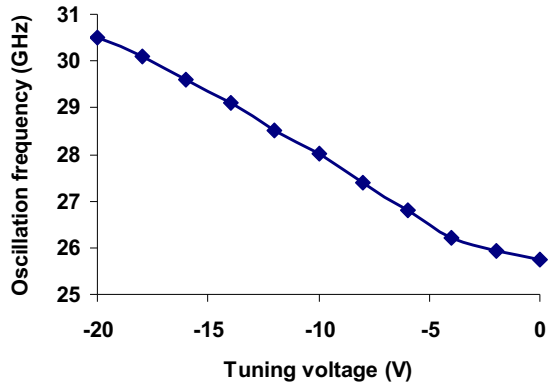

Figure 5. Measured tuning characteristics of VCO1

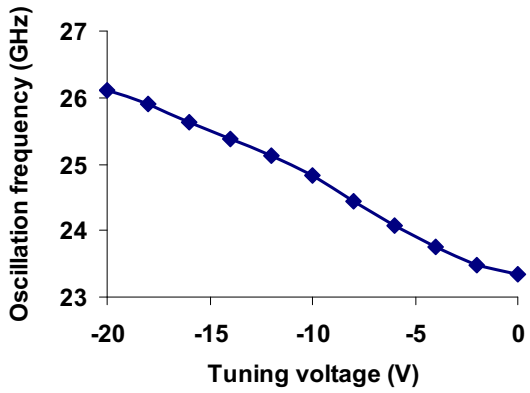

Figure 6. Measured tuning characteristics of VCO2

For VCO2 the phase noise varies less than 2 dB over the tuning range, while it for VCO1 degrades more strongly as the frequency increases. The transition from -30 dB/decade to -20 dB/decade slope at an offset frequency around 1 MHz, indicates a large impact of the CMOS transistors 1/f noise.

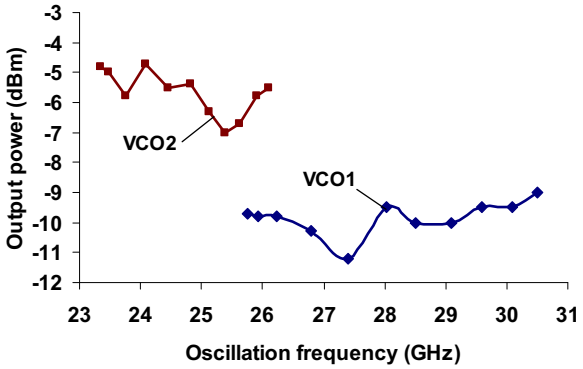

Figure 7. Output power of the VCOs versus frequency.

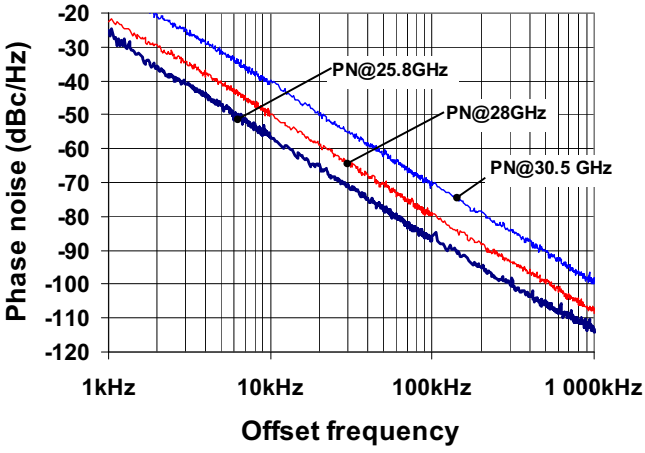

Figure 8. Measured phase noise of VCO1

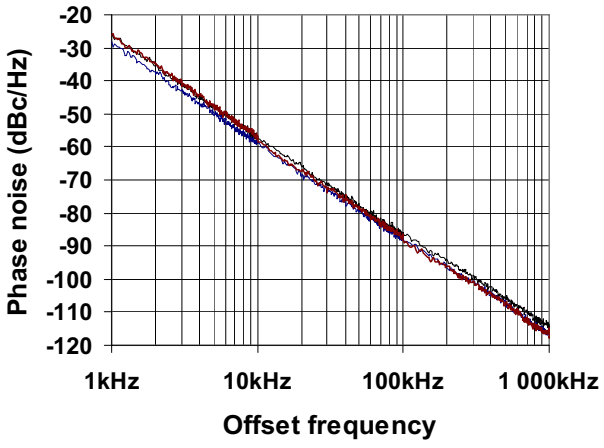

Figure 9. Measured phase noise of VCO2.

TABLE II. SUMMARY OF PUBLISHED VCOS

Ref.	Technology (μm)	F_C (GHz)	Tuning range (%)	V_{DD} (V)	P_{DC}(mW)	PN@1MH offset(dBc/Hz)	FOM(dB)	FOM_T(dB)
This work	CMOS 0.13	24.8	11	1.4	18	-117*	192	193
This work	CMOS 0.13	28	17	0.8	5.3	-109*	191	195
[3]	SiG e	16.5	6.7	3	90	-125*	190	186
[4]	CMOS 0.18	40	20**	1.5	27	-100*	178	184
[5]	CMOS 0.09	18	8.3	0.8	4.2	-120*	199	197
[6]	InGaP-GaAs	25	1.6	9	90	-130*	199	183
[7]	CMOS 0.13	18	5.6	1.2	14	-117*	191	186
[8]	CMOS 0.18	21	10.4	1.8	40	-112*	182	182

* measured at center frequency ** not continuously tuned

$$FOM = -PN + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log\left(P_{DC}(mW)\right) \quad FOM_T = -PN + 20\log\left(\frac{f_0 \cdot tuning(\%)}{\Delta f \cdot 10}\right) - 10\log\left(P_{DC}(mW)\right)$$

IV. Comparison to previously published VCO

A comparison with previous published VCOs, Table II, shows that the performance of the VCOs presented in this paper is very competitive. The 28 GHz VCO shows the largest continuous tuning range, while the 25 GHz VCO demonstrates the possibility to achieve excellent phase noise performance and good tuning range simultaneously.

V. Conclusion

In this paper the potential of heterogeneous building practice is demonstrated by the design of a high performance VCOs utilizing ferroelectric varactors on a carrier. Identical CMOS chips, consisting only of a few transistors, have been flip-chip mounted on carriers with different resonators. The center frequency and the tuning range are mainly set by the carrier design consisting of a resonator structure including a varactor. The carrier is realized in a two metal layer process including a thin BSTO film between the metals to realize ferroelectric varactors. Measurement results are presented for two designs, one were the CMOS chip is mounted on a carrier optimized for high tuning range, and one were the chip is mounted on a carrier optimized for high Q-value and more moderate tuning range. The design for high tuning range consumes 5.3 mW from a 0.8 V power supply, has a tuning range from 25.8 to 30.5 GHz, and a phase noise of -109 dBc/Hz at 1MHz offset. The design optimized for low phase noise consumes 18 mW from a 1.4 V supply, has a tuning range from 23.5 to 25.2 GHz, and a phase noise of -117 dBc/Hz.

Acknowledgement

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