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A 2.4GHz CMOS Power Amplifier using Internal Frequency Doubling

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***Abstract* - A fully integrated 0.18μm 1P6M CMOS power amplifier using internal frequency doubling is presented. Two chips were measured, one stand-alone PA and one PA with a VCO on the same chip. Since the PA and VCO operate at a different frequency, this configuration is suitable for direct-upconversion or low-IF upconversion since oscillator pulling will be reduced. The maximum output power is 15 dBm, and the maximum drain efficiency is 10.7% at an output operating frequency of 2.4 GHz.**

I. Introduction

In recent years, the market of wireless communication has grown significantly. Systems such as GSM have matured, and new systems such as UMTS, Bluetooth and IEEE802.11 are now commercially available. The level of integration has increased, in order to reduce the number of chips per handset as well as the number of external components. In many cases CMOS is the technology of choice for all parts except the power amplifier.

However, for frequencies up to several GHz and low to medium output power, research interest for highly integrated CMOS power amplifiers (PAs) has increased [1-4]. CMOS PAs may be an alternative to stand-alone power amplifiers, offering a possibility for a higher level of integration, generally in exchange for less efficiency and a lower maximum output power.

When having the PA on the same chip as a VCO (voltage controlled oscillator), one of the problems occurring is oscillator pulling, i. e. the VCO oscillation frequency changes due to the PA output signal. This is a problem especially if the PA and VCO are operating at nearly equal frequencies. Several strategies can be used to alleviate this problem, such as composing the LO signal from two VCOs in a direct conversion transmitter or by upconversion in several steps [5]. The approach used in this work is to have a built-in frequency doubler in the power amplifier, cancelling the fundamental signal and utilizing the second harmonic.

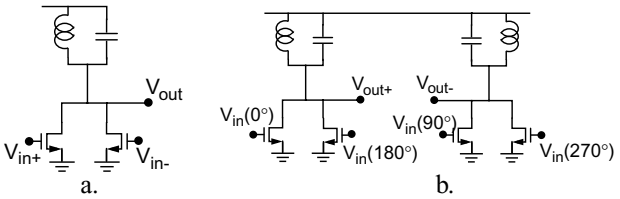

Fig. 1. a). A single-ended PA stage with cancelled odd harmonics, b). differential stage.

In mixers, so-called even-harmonic conversion has been widely used [6], especially for millimeter-wave or receiver applications. With regard to power amplifiers the technique has been described and used previously [7], but has to the authors' knowledge not been used in CMOS integrated PAs.

For fully integrated power amplifiers, which include the output impedance transformation network, the limited quality factor of the integrated passives diminishes the efficiency. An efficiency analysis of the PA with transformation network as presented in this work will be given.

Since many wireless communication systems operate with an output power in the 10 - 20dBm range for the handset, this PA was designed for an output power in that range. Moreover, linearity was not considered to be a critical issue since many wireless systems use a constant envelope modulation scheme.

II. Power Amplifier Analysis

One of the frequency components generated in a PA biased in non-class A is the second-order harmonic. Thus, built-in upconversion may be achieved if this harmonic is large enough compared to other output harmonics. When the drains of two stages are tied together to the same load, as shown in Fig. 1a, the odd harmonics are cancelled if the inputs are driven with a differential signal. This may be referred to as a push-push configuration [7].

If a quasi-differential amplifier is used in order to get a differential output signal, the second stage must be driven

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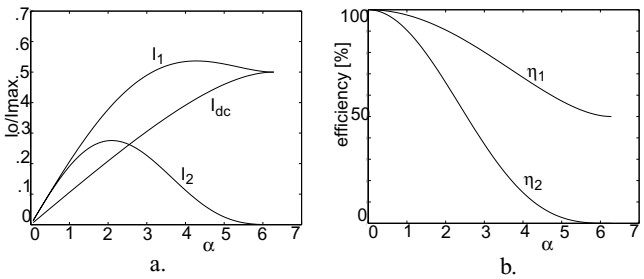

Fig. 2. a). Ideal normalized DC, fundamental and second order output current as function of the conduction angle α, b). drain efficiency for the fundamental and second-order output.

with a 90° phase shift relative to the first stage, as shown in Fig. 1b. Quadrature signals are thus needed to drive the differential PA.

Ideal PA response

Assuming that the output stage of the PA can be modeled as an ideal current source with a maximum voltage swing of $2V_{DD}$ at the drain node, the DC, fundamental and 2nd order response of the PA depend on the conduction angle α or class in which the PA is biased [8].

For this ideal PA both the fundamental and second order responses (output currents normalized to the maximum output current I_{max}), as well as the efficiencies η_1 and η_2 are depicted in Fig. 2, as a function of the conduction angle α. So far it is assumed that the PA does not have a so-called knee voltage V_{knee} [8], that only relevant harmonics are seen at the output, and that the load impedance is always optimized for maximum voltage swing ($2V_{DD}$) with maximum current swing I_{max}.

The impedance transformation network.

The MOSFET DC current is supplied through inductor L_1. The section formed by L_{bw} (the output bondwire inductance) and C_3 in the network shown in Fig. 3 can be seen as a low-pass up-transformation L-section, and the section C_1 and C_2 as a down-transformation stage. In theory this provides us with enough degrees of freedom to ensure sufficient bandwidth while being able to freely choose the transformation ratio. However, both parasitics and size limitations for

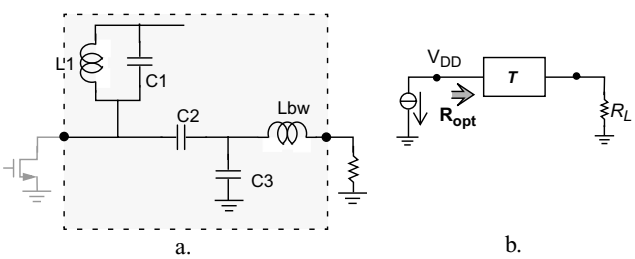

Fig. 3. a). A PA with transformation network (shaded area), b). an ideal model.

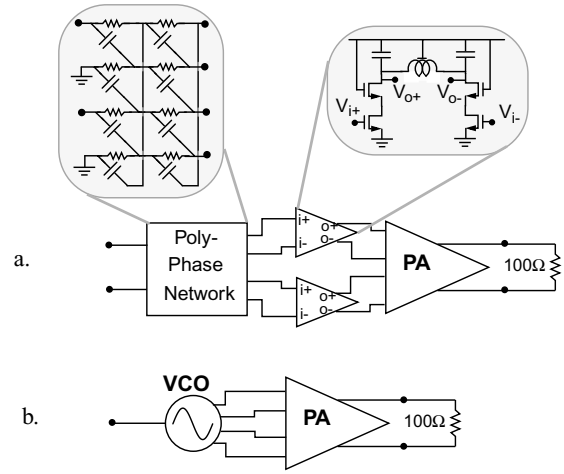

Fig. 4. Block diagrams, a). stand-alone PA, b). PA with VCO.

integrated passive components limit the impedance transformation ratio Parasitic capacitances from the pad may be included in C_3, while parasitic capacitances at the drain are included in C_1. For the PA with internal frequency doubling the network must be tuned so that the desired impedance transformation is achieved at twice the PA input frequency. In the next section we will look more into non-idealities of the transformation network.

III. Implementation

The quasi-differential PA as described in the previous section was implemented in a 0.18µm 1P6M CMOS technology with the option of 3.3V supply. Since we aimed at output powers of 15 - 20 dBm, this supply voltage was chosen, and thus non-minimum length MOSFETs were used in the final stage. One test chip included a passive polyphase filter, a pre-amplifier and the PA, while a second test chip included both a quadrature VCO and the PA. The block diagrams are shown in Fig. 4.

The goal of the circuit in Fig. 4a was to test the concept of internal frequency doubling, as well as the output power and efficiency in the final PA stage. The polyphase network provides the driving stage with *I*- and *Q*- signals, but has a significant signal loss. The PA schematic is shown in Fig. 5.

For the VCO core in the circuit of Fig. 6 PMOSFETs were used, so that the VCO output voltage swings around ground, the desired bias voltage of the PA input. The two

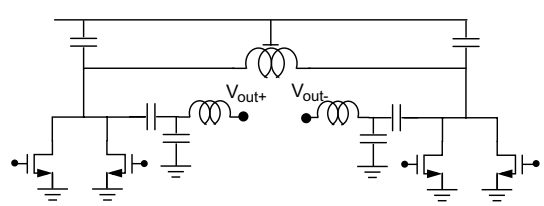

Fig. 5. Simplified schematic of the PA.

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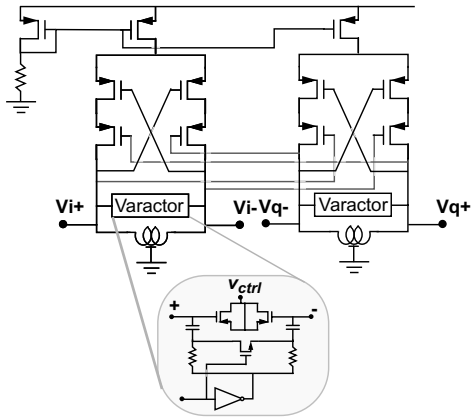

Fig. 6. Schematic of the VCO, including the varactor with continuous and discrete tuning.

blocks can then be connected without buffer or coupling capacitor; a disadvantage is that this more or less fixes the PA input bias voltage, while an advantage is that no signal degradation will take place between the VCO and PA. The switched tuning of the varactor as shown in Fig. 6 has been described earlier [9].

Non-idealities of the PA implementation

One of the most crucial non-idealities in any PA implementation is the knee voltage V_{knee}, i.e. the minimum drain voltage necessary to have the PA operating as an amplifier. V_{knee} will reduce the maximum voltage swing and thus the maximum output power, as well as the efficiency [8].

The integrated passives that make up the impedance transformation network, including "RF choke" inductor, all have a limited quality factor Q. The inductors are differential, saving area and giving a higher Q factor compared to single-ended inductors with similar inductance value. The inductor design and modeling was done in-house [10]. The transformation network was designed to transorm the 50 Ω antenna impedance to 90 Ω at the frequency of operation.

For the transformation network of Fig. 3 with suitable

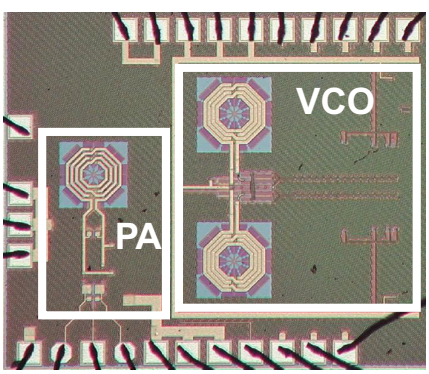

Fig. 7. A chip micrograph of the PA with VCO.

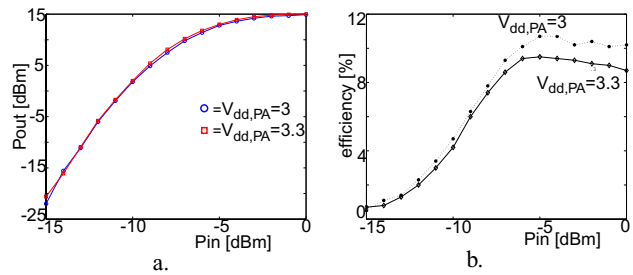

Fig. 8. Measured results for the stand-alone PA for $V_{dd,pa}$=3.3 and 3 V, a). output power, b). drain efficiency.

capacitor and inductor values, including a Q factor of 12 for the inductor L_1, MATLAB simulations showed that the efficiency of the transformation network is about 75%, i.e. the power loss from drain to output will be about 1.2dB. Moreover, in a real impedance transformation network also capacitor non-idealities and interconnect parasitics will cause power losses.

IV. Results

Both the stand-alone PA and the PA with VCO were packaged in an LCC package and attached to a PCB. In Fig. 7 the chip micrograph of the PA with VCO is shown. Parasitics related to the bondwires, package and board were estimated and taken into account in simulations.

The stand-alone PA

The purpose of this circuit was to verify that the internal frequency doubling worked, and to characterize the final stage. Due to the on-chip polyphase network used to generate the quadrature phases the gain is low. In the measurements the circuit was therefore preceded by a Mini-Circuits amplifier. In Fig. 8 measurement results for the stand-alone PA are shown.

The PA with VCO

In Fig. 9 the output power and efficiency as function of $V_{dd,vco}$ is shown. Increasing $V_{dd,vco}$ is equivalent to increasing the input power of the PA stage.

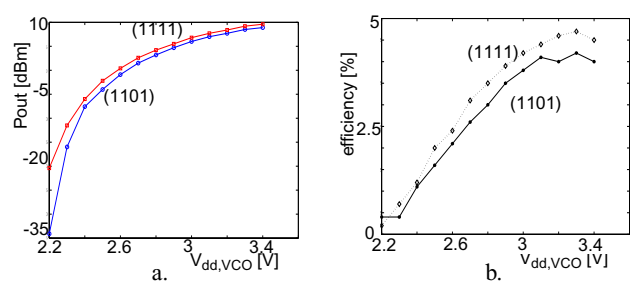

Fig. 9. Measured results for the PA with VCO as a function of $V_{dd,vco}$ for two different VCO control words, a). output power, b). drain efficiency.

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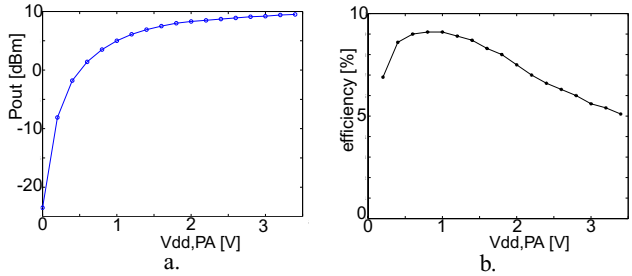

Fig. 10. Results for varying $V_{dd,PA}$, a). output power, b). drain efficiency.

The VCO used in this circuit was not optimized for the purpose. Therefore, it could not drive the PA sufficiently which had a negative impact on the efficiency and output power. For equal VCO supply voltage, the driving power was higher when using the control word (1111) compared to using (1101), thus giving a larger PA output power and a better PA drain efficiency. Moreover, the oscillation frequency was not in agreement with the optimum PA operating frequency. Off-chip components were used to tune the PA to the right frequency.

Fig. 10 shows the output power as function of $V_{dd,PA}$, illustrating the knee effect, and the drain efficiency. The maximum efficiency occurs for relatively low supply voltages; this illustrates the fact that for equal driving power, the PA with low supply voltage has a clipped output voltage waveform, which may be beneficial for the efficiency [8]. For even lower supply voltages ($V_{dd,PA} < 0.6$ V, see Fig. 10b) the MOSFET will be in triode and thus have a lower g_m, resulting in a decreasing efficiency.

Measurements of both circuits showed that the gain in each block is less than expected from simulations. This may be due to a lower transistor g_m or lower inductor Q value. This has a large impact on the total gain, but also on the efficiency of the PA and power consumption of the VCO. In Table 1 the measurement results are summarized.

TABLE 1: SUMMARY OF MEASUREMENT RESULTS

maximum PA output power	15 dBm
maximum PA drain efficiency	10.7%
active area: stand-alone PA	1.44 mm^2
VCO + PA	2.25 mm^2

As was shown in Section II, the efficiency and the output power are degraded since the 2nd harmonic is taken instead of the fundamental.

V. CONCLUSIONS

A fully integrated class-C power amplifier with internal frequency doubler has been designed and measured. A 0.18µm 1P6M CMOS technology was used. The circuit is suitable for a direct-conversion or low-IF transmitter, since the PA and VCO do not operate at the same frequency. Thus, VCO pulling will be reduced. The maximum output power is 15 dBm, with a maximum drain efficiency of 10.7%. The concept of internal frequency doubling was tested both in a stand-alone PA and a PA with VCO on the same chip.

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