LUND UNIVERSITY

A 90 nm CMOS 10 GHz beam forming transmitter

Wernehag, Johan; Sjöland, Henrik

Link to publication

A 90 nm CMOS 10 GHz Beam Forming Transmitter

Johan Wernehag
Department of Electroscience,
Lund University, Box 118, 221 00 Lund, Sweden
Email: Johan.Wernehag@es.lth.se

Henrik Sjöland
Department of Electroscience,
Lund University, Box 118, 221 00 Lund, Sweden
Email: Henrik.Sjoland@es.lth.se

Abstract— **A 10 GHz beam forming transmitter was designed in a 90 nm CMOS process. Two power amplifiers with independently controllable phase enable the beam forming. The controllable phase is accomplished by switching in binary weighted transistors fed by quadrature signals, which are generated by a quadrature voltage controlled oscillator followed by a buffer. The design contains seven differential on-chip inductors, and consumes a total of 44.0 mA from a 1.2 V supply. The desired output power of 5 dBm per power amplifier is delivered at a power added efficiency of 22 % for the power amplifier.**

I. INTRODUCTION

This work is part of a project to find radio transceiver circuit topologies that cope with the trend of scaling CMOS technology towards shorter channel lengths. This leads to lower supply voltages, and thereby less output power for transmitters and less dynamic range for receivers. The benefit of scaling is that it also inherently drives up the transit frequency of the transistors, which enables the use of CMOS technology at higher operating frequencies. New applications for CMOS RF circuitry in the coming five to ten years, could be car radar at 24 and 77 GHz and indoor WLAN at 60 GHz. The project is aimed towards 60 GHz CMOS WLAN.

A 90 nm CMOS 10 GHz beam forming transmitter architecture is presented, consisting of a Quadrature Voltage Controlled Oscillator (QVCO), a buffer, and two Power Amplifiers (PA:s), see Fig. 1. The output phase of each PA is controllable and thus the antenna lobe is steerable. Beam forming is suitable for radar systems and can also be used in WLAN system. In a WLAN system it is beneficial to steer the antenna lobe of the transmitter towards the receiver. Less total output power then needs to be transmitted, saving battery energy and relaxing the requirements on the PA:s. In a system with multiple PA:s and antennas, the output power requirements of each PA can be further relaxed.

A coarse linkbudget was made to find the required output power for an indoor range of about 10 m at 60 GHz. To estimate the propagation loss, measurement results by Hirose [1] have been used. He has measured the attenuation in indoor office environments at 60 GHz with different obstacles in the way of propagation. With a patch antenna array with four elements, and a separate PA feeding each, the output power needed is 5 dBm per PA,
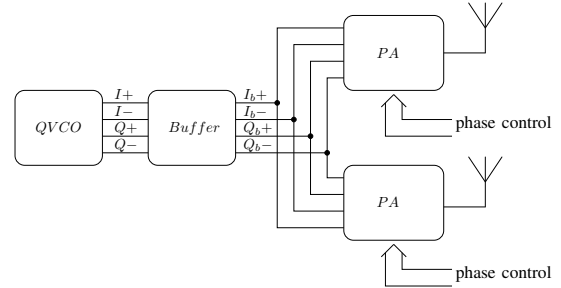

Fig. 1. A block diagram over the transmitter.

which is reasonable for a PA in scaled CMOS technology. At 60 GHz the four antenna elements will occupy just a few millimeters, enabling its integration in the package of the chip.

II. DESIGN AND SIMULATION

First the PA is designed for high efficiency at 5 dBm output power into a 50 Ω load. The input capacitance of the PA can be included in the resonance tank of the buffer, which puts some restrictions on the PA transistor size. To achieve beam forming there are two separate PA:s giving a total differential capacitive load, of 480 fF.

The QVCO and buffer are then designed with the PA:s as load. Due to the different capacitive load of the QVCO and buffer they have on-chip inductors of different sizes. The buffer is needed to ensure that the QVCO has a fixed load impedance. Without the buffer the QVCO would be loaded by the output circuitry of the PA:s, because the large signal swings of the PA:s drive the cascode transistors into triode region for parts of the signal cycle, diminishing the isolation of the cascodes. A changing antenna impedance caused by a changing environment would thus effect the QVCO. Furthermore, the input impedance of a PA change as its phase is changed by a new phase control setting. All this would degrade the accuracy of the quadrature signal generated by the QVCO, and thereby also the accuracy of the beam forming. An even worse problem is that a shifting load would shift the frequency of the QVCO, and the entire transmitter. This effect could however, be significantly suppressed by lock-

ing the frequency of the QVCO to a crystal reference using a PLL frequency synthesizer.

The QVCO is driven at rather high amplitude, 700 mV$_{pk}$. This brings down the phase noise and ensures a reliable start-up. In between each building block there are capacitive taps, which decreases the loading of the previous stage and increases the isolation. The tap consists of the input capacitance of the following stage and an additional series capacitance, which also functions as a DC-block.

A. Power Amplifier

The PA consists of binary weighted transistors for each of the four phases. They can be switched on and off by cascode transistors. The cascode transistors can also be used to select the direction of the signal current, towards the positive or negative differential output, see Fig. 2. By switching on and off and directing the current of the transistors in different combinations the phase of the output is controllable through 360°, and thus the antenna lobe is steerable in any direction. Directing the current of transistor V_{x_y} towards the positive output branch then the current of transistor V_{x+180_y} should be directed towards the negative output branch, see Fig. 2. This switching scheme ensures a differential output of the PA:s.
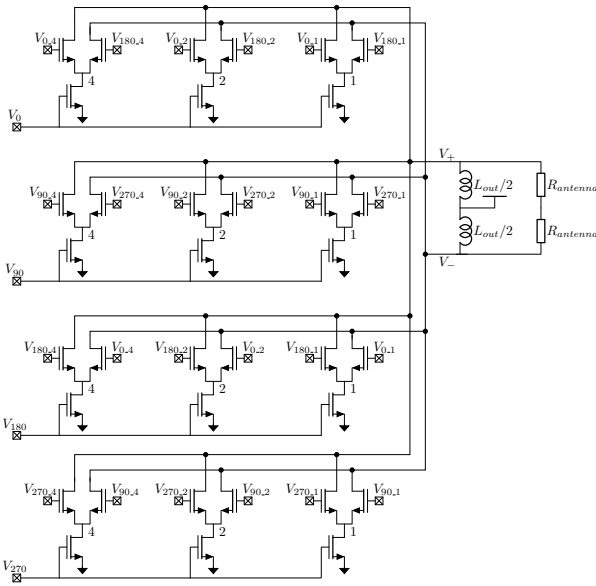

Fig. 2.   A schematic of the power amplifier with three binary weighted transistors per bank.

This circuit has a control word length of three (transistors weighted by 1, 2 and 4) leading to a rather large phase discretisation, see Fig. 3. This is to make it manageable to sweep the phase directly without digital encoding of control words. There is no problem increasing the resolution by adding smaller transistors. As can be seen in Fig. 3 the output power will vary some-

what for different phase settings, and increasing the phase resolution also has the benefit of reducing this power variation.
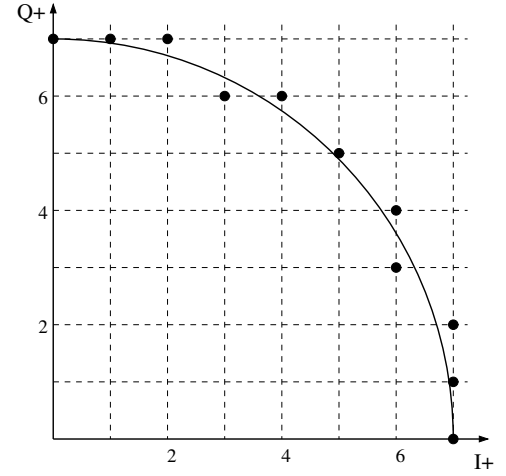

Fig. 3.   Possible phasors over one quadrant.

The output power and phase have been simulated for the phase settings marked with filled circles in Fig. 3, for the PA:s alone and for the complete transmitter. In Fig. 4 the ideal phasors have been plotted over one quadrant, together with simulated values of the PA and the full transmitter. The points + with ideal voltage sources as in-
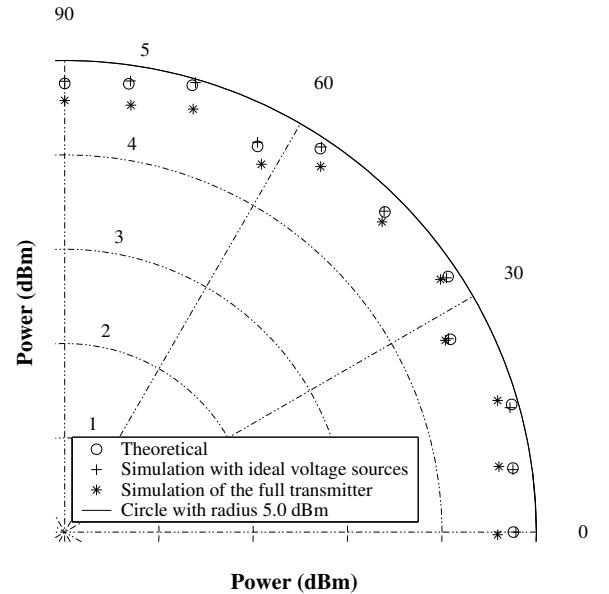

Fig. 4.   Theoretical and simulated phasors over one quadrant.

put to the PA:s agree very well with the ideal case. When the PA:s are fed by the QVCO and buffer, the loading of the PA:s will affect the quadrature of the signals. This will cause some deviation from the ideal pha-

sors, which would have been excessive without the buffer. In this simulation the phase of the other PA is set to 45°.

The desired output power of 5 dBm per PA is achieved with a DC current of 11.7 mA per PA and an associated Power Added Efficiency (PAE) of 22 % for the PA:s and 10 % for the full transmitter. The simulations were performed using SpectreRF, with the BSIM4.2.1 transistor model.

B. Quadrature Voltage Controlled Oscillator and Buffer

The topology of the oscillator and buffer is almost the same as in [2]. This topology, Fig. 5, is chosen because it is robust and has a high quadrature accuracy. The phase noise is also low thanks to the series connected transistors [5], and the inductor tuning the source nodes to twice the frequency of oscillation [4].
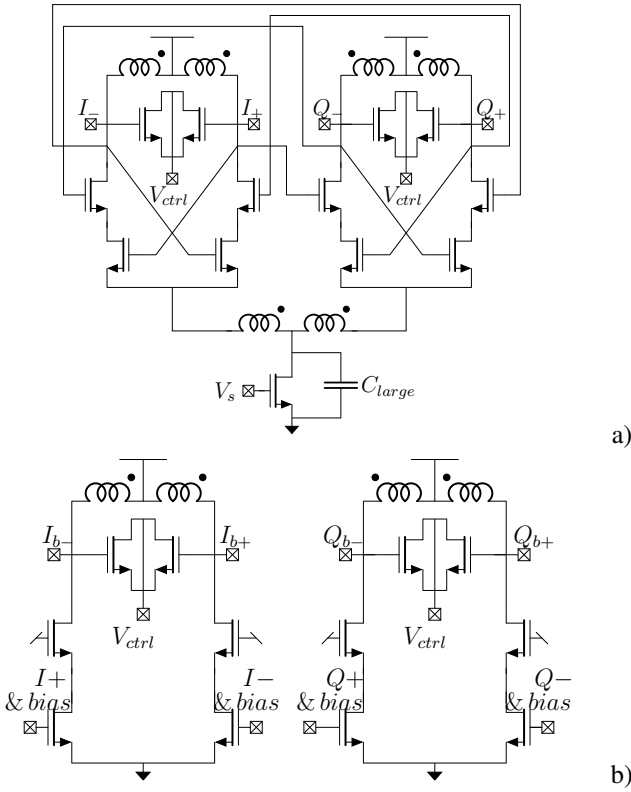
a)

b)

Fig. 5.   a) Topology of the QVCO. b) Topology of the buffer.

A difficulty when designing an oscillator at this high frequency is that the capacitive reactance of the resonance tank is quite low. It is further reduced by the capacitive load of the buffer. The inductance of the resonance tank must therefore be very small. The limit to how small it can be made is set by the parasitic inductance. Since the tank is fully integrated using short wires a 630 pH differential inductor can be used without compromising the robustness. The total differential capacitance must then be 400 fF for 10 GHz operation.

$$C_{diff} = \frac{1}{\omega_0^2 \cdot L_{diff}} \approx 402\,fF \tag{1}$$

This capacitance has to be shared by the switching transistors, the buffer, the varactor, the parasitic capacitances of the routing, and of the inductors. The inductors, switching transistors and buffer capacitance was simulated to 198 fF differential, which leaves 204 fF for the varactor at 10 GHz. An nMOS varactor has a capacitance ratio, η, of 2.5 when the control voltage is varied form ground to supply.

$$\eta = \frac{C_{var,max}}{C_{var,min}} = 2.5 \tag{2}$$

This ratio gives a capacitance variation of 173 fF[1], and a tuning range of 20 %.

The buffer is separately tuned with the PA as load. The inductance is slightly smaller due to the heavy loading of the gate capacitances of the PA:s. A varactor is used also in the buffer to maximize its output voltage swing, and to reduce its current consumption, [2].

The QVCO achieved a phase noise of -120 dBc/Hz at 3 MHz offset, and a tuning range of 20 %, from 9 GHz to 11 GHz. The second harmonic was at -42 dBc at the output of the PA. The current consumption of the QVCO and buffer was 6.7 mA and 14.0 mA, respectively, from a 1.2 V supply. Also these simulations were performed using the SpectreRF simulator.

C. On-Chip Inductors

The process has seven metal layers in copper and one thick top metal layer in aluminum, above a lightly doped substrate. Only differential inductors are used in this circuit, since the design is fully differential. Two inductors at the output of the PA:s form resonance tanks with the parasitic drain-bulk capacitance of the cascode transistors. The drain current to the PA:s is also fed through these inductors, Fig. 2. Two inductors each are used in the QVCO and buffer resonance tanks. Finally one inductor is used at the source node of the switching pair in the QVCO.
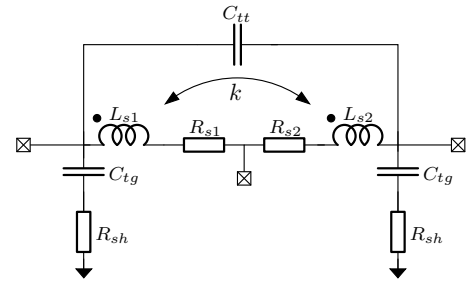
Fig. 6. π-model of the symmetrical inductor.

The Q of the differential inductors is quite high (≈ 25) thanks to the excellent process, resulting in a low power con-

---

[1]$C_{var} = \frac{C_{var,max}+C_{var,min}}{2} = 204fF$
$C_{min}=C_{diff} - C_{var} + C_{var,min} = C_{diff} + C_{var}(\frac{2}{1+\eta} - 1) = 314.6$ fF,
$C_{max}=C_{diff} - C_{var} + C_{var,max} = C_{diff} + C_{var}(\frac{2}{1+1/\eta} - 1) = 489.4$ fF $\Rightarrow \Delta C = C_{max}-C_{min}=174.8$ fF

sumption of the QVCO and buffer. The differential parallel resistance is 1.3 kΩ for the VCO tank. In table I all the lumped elements used to model the different inductors are summarized. The values were extracted using FastHenry, [3].

TABLE I
LUMPED COMPONENTS FOR THE INDUCTORS.

Comp.	Output	QVCO	Buffer
L_{sdiff}/nH	0.94	0.63	0.54
R_{sdiff}/Ω	2.31	1.16	1.43
C_{tg}/fF	68.7	79.2	176.5
C_{tt}/fF	21.2	43.7	0
R_{sh}/Ω	2.5	2.5	2.5
f_{test}/GHz	10	10	10
f_{srf}/GHz	22.04	21.98	22.65
Q	24.64	32.78	21.35
LQ/nH	23	21	12
k	0.606	0.605	-0.062
L_{s1}/nH	0.29	0.20	0.29
L_{s2}/nH	0.29	0.20	0.29
R_{s1}/Ω	1.06	0.53	0.71
R_{s2}/Ω	1.25	0.62	0.71
#-turns	2	2	1

The in-house optimization software, Indentro [6], written by Niklas Troedsson, was used to find the geometry and metal layers to use. It is a very quick solver where one can sweep different parameters and put restrictions on others, e. g. $f_{srf} \geq$20 GHz. After finding a promising geometry an *.ind-file can be exported to FastHenry and simulated there as well. The agreement is quite good, but FastHenry typically gives a somewhat lower Q and L. Since a high resistivity substrate is used the Eddy current in the substrate can be neglected. The capacitively coupled substrate losses are blocked by a patterned ground shield. The substrate does therefore not need to be included in the simulations, and FastHenry gives accurate results. A *.cif-file can also be exported from Indentro for layout in a Cadence environment. The *.cif-file contains all metal traces and all vias for interconnect. The key for all these simulations to be accurate is a correct technology file, where all thicknesses and electrical properties of the different layers of the semiconductor process are specified.

The three to five topmost metal layers were used for the inductors. In Fig. 7 the layout of one of the inductors can be seen. The number of metal layers to use is a trade off between self resonance frequency and series resistance (Q-value). For the small inductors in the buffer the five topmost metal layers are used to bring down the series resistance as much as possible. Since it has just one turn, the self resonance frequency is still high.
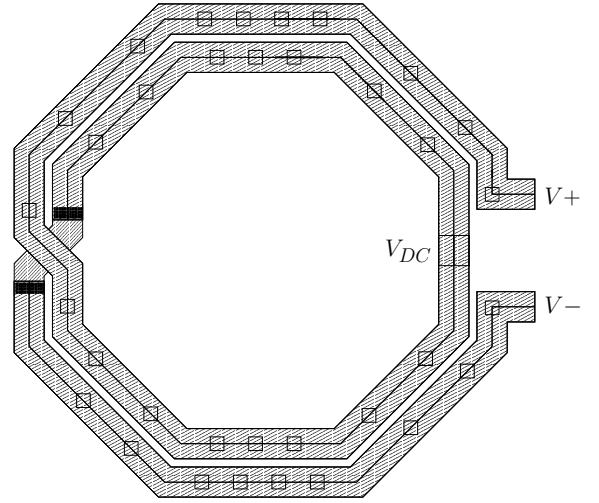

Fig. 7. Layout of a symmetrical inductor, this one is used at the output.

III. CONCLUSION

A 90 nm 10 GHz transmitter circuit is presented, featuring a quadrature oscillator with low phase noise (-120 dBc/Hz at 3 MHz offset) and two phase controlled power amplifiers, each with an output power of 5 dBm. To be able to deliver the amount of power needed to transmit at extreme data rates in an indoor environment, an architecture with multiple power amplifiers is a must in scaled CMOS technology. With multiple antennas and phase controlled power amplifiers beam forming can be used to reduces the output power needed. This work shows how full 360° phase controlled PA:s can be realized in a robust manner.

REFERENCES

[1] T. Hirose, 'Study of mm wave propagation modeling to realize WPANs,' IEEE802.15-03/0365.
[2] N. Troedsson and H. Sjland, 'A Distributed Capacitance Analysis of Co-Planar Inductors for a CMOS QVCO with Varactor Tuned Buffer Stage,' *Analog Integrated Circuits and Signal Processing*, 42, 7-19, 2005.
[3] http://www.fastfieldsolvers.com
[4] E. Hegazi, H. Sjland, and A.A. Abidi. 'Filtering technique to lower LC-oscillator phase noise,' *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921-1930, Dec. 2001.
[5] P. Andreani. 'A low-phase-noise low-phase-error 1.8 GHz quadrature CMOS VCO,' *IEEE Solid-State Circuits Conference*, vol. 2, pp. 228-229 , Dec. 2002.
[6] http://www.indentro.com