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# Vertical III-V/High- $\kappa$ Nanowire MOS Capacitors and Transistors

*Jun Wu*



LUND UNIVERSITY

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Electrical Engineering  
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## Abstract

**T**HE emerging nanowire technology in recent years has attracted an increasing interest for high-speed, low-power electronics due to the possibility of a gate-all-around (GAA) geometry enabling aggressive gate length scaling, together with the ease in incorporating high-mobility narrow band gap III-V semiconductors such as InAs on Si substrates. These benefits make vertical nanowire transistors an attractive alternative to the planar devices. However, huge challenges are also encountered. Apart from the large parasitics associated with the device layout, vertical III-V/high- $\kappa$  nanowire MOSFETs so far are also suffering from a less efficient gate control partially due to the defect states existing in the MOS gate stack. Besides the narrow band gap InAs may result in impact-ionization and band-to-band tunneling at high drain voltages, influencing both the power efficiency and speed of modern integrated circuits (ICs).

In this thesis, results on planar InAs/high- $\kappa$  MOS gate stacks investigated in detail using both the capacitance-voltage (C-V) and the x-ray photoelectron spectroscopy (XPS) techniques are first presented (Paper I and II). The origin of the specific trap state energy distribution is clarified and compared to the well studied InGaAs and GaAs materials. The results highlight the benefit of using InAs, with optimized high- $\kappa$  deposition strategies, as the n-MOSFET channel.

The second focus of the thesis is the improvement of vertical GAA nanowire MOS gate stacks (Paper III and IV). By developing the fabrication scheme and design, conventional C-V technique is successfully applied to extract detailed trap state distributions. A low interface trap state density ( $D_{it}$ ) below  $10^{12}$   $\text{eV}^{-1}\text{cm}^{-2}$  near the MOS semiconductor conduction band edge is achieved. Furthermore, RF C-V measurements, together with the development of a com-

plete small signal equivalent circuit model, for vertical GAA nanowire MOS systems are also presented for the first time, which enables characterizations of border trap density, interface trap density, channel resistivity and quality factor of the nanowire MOSFETs simultaneously.

The third focus is the development of a device structure to reduce detrimental impact-ionization and band-to-band tunneling due to the narrow band gap of InAs (Paper V and VI). An asymmetric InAs/InGaAs vertical nanowire MOSFET with a large band gap drain region is proposed, taking advantage of the efficient strain relaxation of nanowire epitaxial growth. Control of the InGaAs nanowire composition has been successfully demonstrated.

Finally, a vertical integration scheme was developed in the thesis, where track-and-hold circuits, consisting of a MOSFET in series with a metal-insulator-metal capacitor, were successfully fabricated along vertical InAs nanowires (Paper VII).

# Populärvetenskaplig Sammanfattning

**S**INCE 1947 when the first transistor was invented, electronics was transited into an unprecedented era. Different from a resistor that only has two terminals with the applied voltage and flowing current always obeying Ohm's law, a transistor has the third terminal in between, called "gate", which is made by, for metal-oxide-semiconductor field effect transistors (MOSFETs), an oxide layer sandwiched between the metal electrode and the semiconductor channel. This terminal can control the current flowing through the semiconductor by creating an electrical field in the channel when a voltage is applied, hence realizing the switching function between digital 1 (switching on with current flowing) and digital 0 (switching off with current blocked). This is the basis of all digital calculations, and, hence, all modern computers. Besides, a small voltage variation (input signal) sent to the gate node can create a large variation in current in the channel (output signal) under some conditions, which realizes, on the other hand, the signal amplification function. This is the basis of all analogue applications, and, hence, all modern mobile phones.

Based on the transistor technology, the first integrated circuit (IC) was invented in 1960s, which was another revolutionary creation of that century. In an IC, many transistors are integrated in the semiconductor material of silicon to realize different digital and analog functions. The co-founder of Intel, Gordon Moore, predicted in 1965 that the number of transistors per chip would double every 24 months. This prediction later was called Moore's law, and it was accurately followed during the last 50 years via the continuous transistor size downscaling. It also became one of the main goals of the semiconductor industry, since reducing the transistor size not only resulted in an increased packing density of modern ICs and a reduced fabrication cost per transistor, but also an increased circuit speed and a reduced power

consumption as the transistor gate length was reduced continuously.

The transistor size downscaling, however, is not a permanent strategy unfortunately, since as the transistor gate length is reduced below several tens nanometers. The gate will lose control of the channel charges, which is usually termed "short channel effects". After 2002, people began to seek alternative solutions to continuously increase the IC performance. One of the most promising solutions, which is also the main topic of the thesis, was the vertical wrap-gated indium arsenide (InAs)/high-k oxide nanowire MOSFETs. The vertical nanowire geometry enables gate electrode surrounding the nanowire, i.e. wrap-gated, as compared with the conventional planar MOSFET technique. Thus electric field can be applied from all directions, leading to more efficient gate control. Besides the use of InAs provides high mobility charge carriers, which means that the charges can transport faster than those in Si under the same voltage bias. In addition, the use of high-k oxide in the gate leads to larger gate capacitance, which also increases the gate efficiency.

Challenges also exist, however, for the new candidate. From the material's point of view, the interface between the high-k oxide and the semiconductor turns out to be a key to success, since defects at this interface will influence the charge control inside the semiconductor significantly, which is also one of the most severe hindrances of the technology so far.

This work presents the development of a reliable technique to study the vertical wrap-gated nanowire gate stack, understanding and improvement of the gate performance of this type of MOSFETs. Besides, the thesis also presents a new vertical nanowire transistor design with further improved performance. In addition, a vertical integration scheme was developed, where track-and-hold circuits, consisting of a MOSFET in series with a metal-insulator-metal capacitor, were successfully fabricated along vertical InAs nanowires.

## Acknowledgments

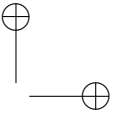
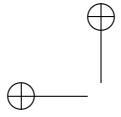
"Do not go gentle into that good night."

- *Dylan Thomas*

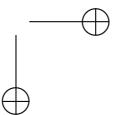
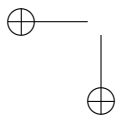
**A**t this end of my expedition to "Dr. Jun Wu", I would like to express my great gratitude to quite a lot of people who helped and accompanied me during these years.

First and foremost, I really appreciate my main supervisor, Lars-Erik, for your continuous inspiration, guidance, encouragement, and numerous fruitful discussions in my researches. I would also like to thank my supervisor, Erik, for sharing your gigantic knowledge about semiconductor physics and devices. Your two's wide-ranging knowledge and deep understanding of the entire field impress me unforgettably. It is really my great honor to have you as my ph.D. supervisors. Besides, I would like to acknowledge all my fantastic colleagues. Especially, I want to thank Johannes who contributed a lot of valuable suggestions in my researches and checked my thesis patiently and carefully. I would also like to thank Elvedin, Olli-Pekka, Kristofer, Aein, Martin, Sofia, Mattias, Anil, Markus for all our enjoyable collaborations. It was great for me also to have Sebastian, Lars, Cezar, Fredrik, Guntrade, Jiongjong during these years. Sebastian, your comment on my personality means a lot to me, and I promise I will keep being a lovely person in the future.

Finally, I would also like to acknowledge Rainer, Martin H., Anders, Jovana, Sofie in synchrotron radiation group; Daniel, Kimberly in FTF for your expertise and contributions in my work. Also thank those engineers who maintains the labs in Lund.



*Jun Wu*  
Lund, April 2016

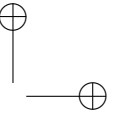
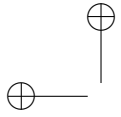


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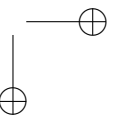
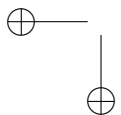


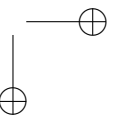
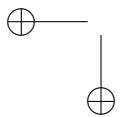
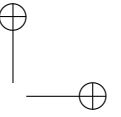
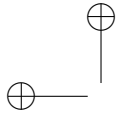
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## PAPERS

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# Preface

*T*his thesis summarizes my academic works of the last four and a half years within the Nanoelectronics group, Lund University, under the supervision of Professor Lars-Erik Wernersson. The thesis focuses on understanding and improving the vertical III-V nanowire based devices and circuits.

## STRUCTURE OF THE THESIS

This thesis is divided into two parts: introduction and included papers

- **INTRODUCTION**

The research field is reviewed and summarized, with emphasis on the papers that are included in the thesis.

- 1: Chapter 1**

- This chapter provides a historical review of the field, which leads to the motivation of the researches performed in the thesis.

- 2: Chapter 2**

- This chapter discusses the optimization of the InAs/high- $\kappa$  metal-oxide-semiconductor (MOS) gate performance. Planar MOS capacitance-voltage (C-V) technique (including the development of a fitting method) and x-ray photoelectron spectroscopy technique are introduced. By combining the electrical and chemical characterizations, the correlation between the trap states across the InAs band gap and different interface chemical species is presented, together with the optimized MOS gate stack fabrication recipes. This chapter is related to Paper I and Paper II.

### 3: Chapter 3

In this chapter, the C-V technique to characterize the vertical wrap-gated InAs/high- $\kappa$  nanowire MOS gate stacks is introduced. The influence of nanowire growth conditions and doping on the MOS gate stack quality is discussed. At the end, RF C-V technique and a complete small signal equivalent circuit model are presented. This chapter is related to Paper III and Paper IV.

### 4: Chapter 4

This chapter presents the development of an asymmetric InAs/InGaAs vertical nanowire MOS field effect transistor (MOSFET) in order to suppress the impact ionization and band-to-band tunneling effects commonly observed in InAs MOSFETs. Band engineering of the new design is presented. Besides, understanding of the ternary InGaAs nanowire growth and control of the Ga incorporation are discussed. This chapter is related to Paper V, Paper VI.

### 5: Chapter 5

This chapter presents an integration scheme to realize track-and-hold circuits along vertical InAs nanowires. This chapter is related to Paper VII

### 6: Chapter 6

This chapter summarizes the conclusions from the thesis and discusses the future of the research field.

#### • PAPERS

The included papers are reproduced in the last part of the thesis. Observe that the copyrights of the papers are owned by the respective publishers.

## INCLUDED PAPERS

The following papers are included in this thesis and the respective published or draft versions are appended at the back of this thesis.

**Paper I:** J. WU, E. LIND, R. TIMM, M. HJORT, A. MIKKELSEN, AND L.-E. WERNERSON, "Al<sub>2</sub>O<sub>3</sub>/InAs metal-oxide-semiconductor capacitors on (100) and (111)B substrates" *Applied Physics Letters*, vol. 100, pp. 132905, Mar. 2012.

► *I performed almost all the works on this paper except for the XPS measurements.*

- Paper II:** E. LIND, J. WU, AND L.-E. WERNERSSON, “High- $\kappa$  oxides on InAs 100 and 111B surfaces” *ECS Transactions*, vol. 45, no. 3, pp. 61–67, Apr. 2012.  
► *In this work, I fabricated the devices, performed the electrical characterization, and participated in the data analysis as well as the result discussions.*
- Paper III:** J. WU, A. S. BABADI, D. JACOBSSON, J. COLVIN, S. YNGMAN, R. TIMM, E. LIND, AND L.-E. WERNERSSON, “Low trap density in InAs/high- $\kappa$  nanowire gate stacks with optimized growth and doping conditions” *Nano Letters*, Manuscript accepted, DOI: 10.1021/acs.nanolett.5b05253.  
► *I performed almost all the works on this paper except for the AFM, TEM and transport measurements.*
- Paper IV:** J. WU, K. JANSSON, A. S. BABADI, M. BERG, E. LIND, AND L.-E. WERNERSSON, “RF characterization of vertical wrap-gated InAs/high- $\kappa$  nanowire capacitors” *IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 584–589, Feb. 2016.  
► *In this work, I developed the techniques of device fabrication and electrical characterization, participated in the data analysis, and wrote the manuscript.*
- Paper V:** K.-M. PERSSON, M. BERG, M. B. BORG, J. WU, S. JOHANSSON, J. SVENSSON, K. JANSSON, E. LIND, AND L.-E. WERNERSSON, “Extrinsic and intrinsic performance of vertical InAs nanowire MOSFETs on Si substrates” *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2761–2767, Sep 2013.  
► *In this work, I grew the nanowires and participated in the result discussions.*
- Paper VI:** J. WU, B. M. BORG, D. JACOBSSON, K. A. DICK, AND L.-E. WERNERSSON, “Control of composition and morphology in InGaAs nanowires grown by metalorganic vapor phase epitaxy” *Journal of Crystal Growth*, vol. 383, pp. 158–165, Aug 2013.  
► *I performed almost all the works on this paper except for the TEM and XEDS measurements.*
- Paper VII:** J. WU, AND L.-E. WERNERSSON, “3D integrated track-and-hold circuit using InAs nanowire MOSFETs and capacitors” *IEEE Electron Device Letters*, Manuscript (to be submitted soon)  
► *I performed all the works on this paper.*

## EXTRANEIOUS PAPERS

The following papers are not included in the thesis, but summarize related work which I have contributed to.

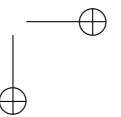
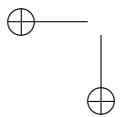
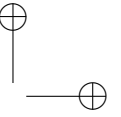
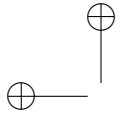
- Paper viii:** M. BERG, K.-M. PERSSON, J. WU, E. LIND, H. SJÖLAND, AND L.-E. WERNERSSON, "InAs nanowire MOSFETs in three-transistor configurations: single balanced RF down-conversion mixers" *Nanotechnology*, vol. 25, pp. 485203, Nov. 2014.
- Paper ix:** K. M. PERSSON, M. BERG, M. BORG, J. WU, H. SJÖLAND, E. LIND, AND L.-E. WERNERSSON, "Vertical InAs nanowire MOSFETs with  $I_{DS}=1.34$  mA/ $\mu$ m and  $g_m=1.19$  mS/ $\mu$ m at  $V_{DS}=0.5$   $I_{DS}=1.34$ " in *70th Annual Device Research Conf. (DRC)*, pp. 195–196, Jun. 2012.
- Paper x:** S. JOHANSSON, K.-M. PERSSON, M. BERG, J. WU, J. SVENSSON, L.-E. WERNERSSON, AND E. LIND, "RF characterization of vertical InAs nanowire MOSFETs" in *12nd Swedish System-on-Chip Conf. (SSoCC)*, May. 2013.
- Paper xi:** J. WU, D. JACOBSSON, B. M. BORG, K. A. DICK, AND L.-E. WERNERSSON, "InGaAs nanowires grown by metalorganic vapor phase epitaxy for future device application" in *41st International Symposium on Compound Semiconductor (ISCS)*, May. 2014.

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# INTRODUCTION





# 1

## Background

SINCE 1947 when the first transistor was invented by John Bardeen, Walter Brattain and William Shockley [1, 2], electronics was transited into an unprecedented era. The revolution was further boosted later in 1960s with the advent of the first integrated circuits (ICs). During the last several decades, the number of transistors per chip roughly doubled every 24 months via the continuous downscaling of the transistor size, following Gordon E. Moore's prediction in 1965 [3,4]. Since the increased packing density of modern ICs went hand in hand with an exponentially increased performance in both speed and power efficiency, fulfilling Moore's law became a major goal of the entire electronics semiconductor industry.

However, geometrical downscaling became less attractive after 2002, since Si complementary metal-oxide-semiconductor (CMOS) technology entered into the so-called power-constrained scaling era after the power dissipation on chip reached  $100 \text{ W/cm}^2$  [5]. Sacrificing speed seemed inevitable to avoid overheating if a further increase in transistor density was pursued. This limitation became the driving force to exploit the multi-core system after 2004 where the computer tasks were separated into parallel problems and designated to separate cores to ensure the highest efficiency in power usage. The effective performance of multi-core CPUs, however, relied strongly on the parallelization degree of the computer tasks instead of the addition of more cores, as demonstrated by Gene Amdahl in 1967 [6], which finally limited the gain of this technology.

In the future, a revolution of the basis, i.e. the transistors, is highly expected since it means not only a breakthrough of these current limitations in pursuing Moore's law, but also more flexibility in fulfilling the diversified needs as the era of Internet of Thing [7] is coming. These stimulate today's

industry and academy to rethink the way we realize the most fundamental building-block of electronics, the metal-oxide-semiconductor field-effect transistor (MOSFET). One promising candidate for the future is the gate-all-around (GAA) nanowire-based devices, in combination with the advanced high-speed material, which is the subject of this thesis.

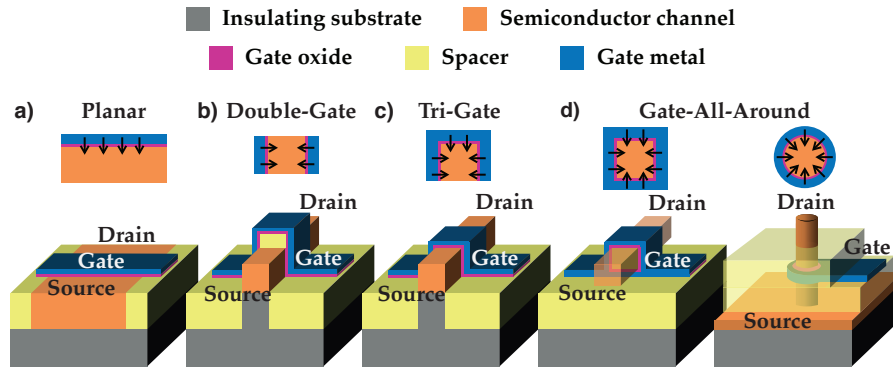
In this chapter, we lay the background of the thesis, including both the benefits and challenges in realizing vertical standing GAA III-V/high- $\kappa$  nanowire MOSFETs.

## 1.1 EVOLUTION OF TRANSISTOR ARCHITECTURE

One key problem associated with downscaling MOSFETs is the short channel effects (SCEs), such as the drain induced barrier lowering, the sub-threshold slope degradation, the threshold voltage roll-off etc. These undesirable effects all result from the reduced efficiency of gate electrostatic control as the gate length is aggressively reduced and SCEs lead to increased dynamic and static power dissipations in modern ICs.

One solution is to redesign the transistor architecture so that the electrical field from the gate affects the channel simultaneous from multiple directions. This allows further scaling of the gate length without losing gate control. Figure 1.1 shows the evolution of the transistor architecture from the conventional planar, to multiple-gate, and finally to GAA MOSFETs. The tri-gate MOSFET in (c) has been commercially realized by Intel in 2012 for the 22 nm node [8], and as reported, this technology increases the performance by 37 %, and meanwhile reduces the power dissipation by 50 %, as compared to the planar MOSFET technology [9] in figure 1.1(a).

The GAA geometry, (d), is expected to provide the ultimate electrostatic control, and in recent years, it has begun to attract increasing interest. Auth. et al. showed that compared to the double-gate geometry, (b), the cylindrical GAA geometry enables the minimum effective gate length to be reduced by 40 % [10]. Lateral GAA MOSFETs formed by removing the substrate under the tri-gate transistors have been recently reported with very promising performance [11]. Meanwhile the introduction of the vertical nanowire formation, either through top-down [12] or bottom-up [13] approaches, provides an another platform to realize the vertical standing GAA geometry. This gives additional benefits. First of all, the vertical nanowire geometry enables the possibility to integrate the circuit components in the vertical dimension with small footprints. This can further increase the circuit density with the same chip size. Besides, the nanowire formation methodologies usually can relax strains caused by lattice mismatch between different materials. This enables the possibility to realize more complicated heterogeneous junctions both



**Figure 1.1:** Evolution of the transistor gate geometry: (a) planar; (b) double-gate; (c) try-gate; (d) gate-all-around (both lateral and vertical). The black arrows illustrate the direction of the electric field at different surfaces

axial [14] and radial [15], as well as the possibility to incorporate advanced materials onto the cost-effective Si platform [16, 17]. Promising results of MOSFETs based on the technology have been published in recent years [18].

## 1.2 III-V SEMICONDUCTORS AND HIGH- $\kappa$ DIELECTRICS

Except for power dissipation, another concern for electronics is the speed. High speed ICs, independent on application areas, in general rely on a large on-state drain-source current of the MOSFETs,  $I_{ds,on}$ , in order for a fast charging and discharging of gate and load capacitors at each IC stage. However, as scaling down the supply voltage became a trend for modern ICs in order to reduce the power dissipation, retaining the diminished on-performance of Si MOSFETs (a high  $I_{ds,on}$ ) is challenging [19]. Thus low-power, high-speed electronics attracted increasing interest and for modern ICs, the on/off-current ratio,  $I_{on}/I_{off}$ , and the quality value,  $Q=g_{m,max}/SS_{min}$  (maximum transconductance/minimum sub threshold slope), become very important figures of merit to evaluate the transistor performance.

$I_{ds,on}$  is proportional to the total amount of charges available in the channel,  $Q_{ch}$ , and the velocity that these charges travel due to the electrical field induced by the source-drain bias,  $v_d$ .  $Q_{ch}$  is directly related to the gate capacitance density,  $C_g$  (in  $F/m^2$ ), through  $Q_{ch}=A \cdot C_g \cdot (V_{gs}-\psi_s)$ , where  $A$  is the gate area and  $(V_{gs}-\psi_s)$  is the voltage drop over the gate dielectric.  $v_d$  is directly related to the charge mobility,  $\mu$ , by  $v_d=\mu \cdot \zeta_{ds}$ , in which  $\zeta_{ds}$  is the drain-source electrical field. Before around 2005,  $C_g$  was increased by scaling the oxide thickness,  $t_{ox}$ . However, as  $t_{ox}$  was reduced down to a few nanometers,

**Table 1.1:** Relative dielectric constant, band gap and conduction band offset with respect to InAs for high- $\kappa$  dielectrics and SiO<sub>2</sub>

	$\kappa$	$E_g$ (eV)	$\Delta E_{c,InAs}$ (eV)
SiO <sub>2</sub>	3.9	9	4.1
Al <sub>2</sub> O <sub>3</sub>	9	8.8	3.6
HfO <sub>2</sub>	25	5.8	2.5

**Table 1.2:** Electron and hole mobilities ( $\mu_e$  and  $\mu_h$ ) of some selected semiconductors [20]

(cm <sup>2</sup> /Vs)	Si	Ge	GaSb	GaAs	In <sub>0.53</sub> Ga <sub>0.47</sub> As	InAs	InSb
$\mu_e$	1400	3900	3000	8500	12000	40000	77000
$\mu_h$	450	1900	1000	400	300	500	850

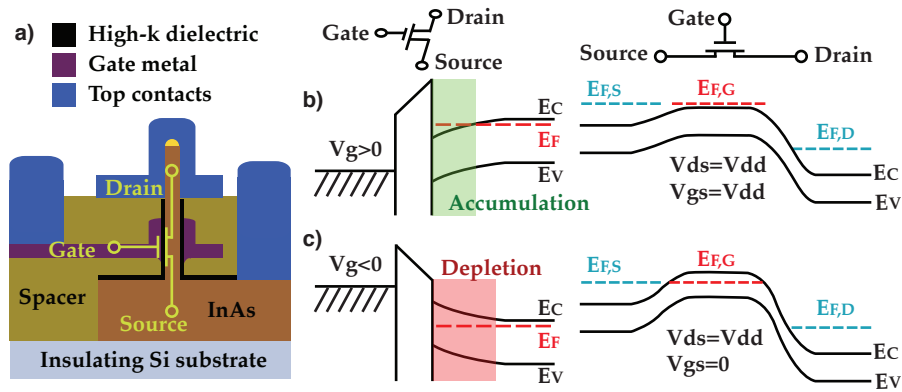
the gate leakage due to quantum mechanical tunneling became significant and the static power dissipation of ICs increased. To solve the problem, an alternative approach by increasing the effective dielectric constant,  $\kappa$  was proposed. High- $\kappa$  material, such as Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub>, was then introduced into the transistor fabrication, which solved the leakage issue by enabling thicker oxides [21]. A comparison of electrical properties between high- $\kappa$  material and SiO<sub>2</sub> is shown in table 1.1. The commercial usage of high- $\kappa$  has been realized by Intel for the 45 nm node in 2007. To boost  $\mu$ , on the other hand, high-speed semiconductor materials beyond the conventional Si have to be considered. III-V compound semiconductor hence attracted great interest in recent years. Table 1.2 presents electron and hole mobilities ( $\mu_n$  and  $\mu_p$ ) of a few selected semiconductors. As can be seen, Si is inferior to III-V semiconductors in general within which InAs and In<sub>0.53</sub>Ga<sub>0.47</sub>As show fairly high  $\mu_n$ , making them promising for future n-MOSFETs. Although InSb shows the highest  $\mu_n$ , its narrow band gap is making it hard to avoid band-to-band tunneling in an InSb based MOSFET. In this thesis, the InAs MOSFET is chosen as the subject due to several reasons. Except for high  $\mu_n$ , InAs can also form ohmic contacts due to the Fermi level pinning at the metal-semiconductor junction [22, 23]. Moreover, promising performance of InAs nanowire MOSFETs, both DC and RF, has been reported recently based on the technique of an InAs buffer layer grown on low-cost Si substrate [24]. All of those make InAs highly attractive. In term of hole mobility, Ge and GaSb are very good candidates for future p-type MOSFETs [25, 26]. The ITRS roadmap

has speculated that the replacement of Si by III-V in CMOS technology will take place in around 2018-2026 with an about 50 % increase in switching speed and 40 % in power efficiency for the 10 nm node technology [27]. For analog applications, such as amplifiers, III-V semiconductors are already used due to the higher speed requirements at the lower cost sensitivity. High electron mobility transistors (HEMTs), metal-semiconductor field-effect transistors (MESFETs) and heterojunction bipolar transistors (HBTs) based on III-V materials are quite important nowadays due to the excellent high frequency performance the material provides as compared to Si [28,29].

### 1.3 ENHANCEMENT-MODE InAs/HIGH- $\kappa$ VERTICAL GAA NANOWIRE MOSFET

InAs/high- $\kappa$  vertical GAA nanowire MOSFETs are thus a promising candidate for future electronics. Figure 1.2(a) presents a vertical GAA nanowire MOSFET in common source configuration. The source contact in this work is realized by a highly n-doped InAs buffer layer on a the highly-resistive p-type Si substrate. On the buffer layer nanowires are grown by epitaxy, followed by high- $\kappa$  dielectric deposition. The gate/drain contacts are realized using metal sputtering. Between them are low- $\kappa$  dielectric spacers. The band diagrams in (b)-(c) illustrate how a n-type enhancement mode MOSFET works. As a positive gate bias,  $V_{gs}$  is applied to the gate node, electrons in semiconductor are attracted towards the surface by the electrical field. The charge accumulation provides a current channel as long as a drain-source bias,  $V_{ds}$ , is applied. As a negative  $V_{gs}$  is applied to the gate, the electrical field created beneath the gate will repel electrons, hence depleting the channel. The transistor is thus switched off.

MOSFETs provide two basic functions for modern ICs: 1) the logic-switch function for digital applications, i.e. using high and low input/output voltages to represent the logic 1 and 0 [26]; 2) the signal-amplifier function for analog and RF applications, i.e. using a small input signal variation,  $\delta v_{gs}$ , to generate a large output signal change,  $\delta i_{ds}$  [30]. MOSFETs are inherently very suitable for digital application since the use of voltage to control the channel leads to a reduced power dissipation as compared to HBTs. However, the analog performance of MOSEFTs is inferior than e.g. HBTs due to the smaller transconductance. Nowadays, since more and more stringent requirements are put on the power dissipation for modern ICs [5], there is a trend to develop MOSFET-based analogue and RF ICs.

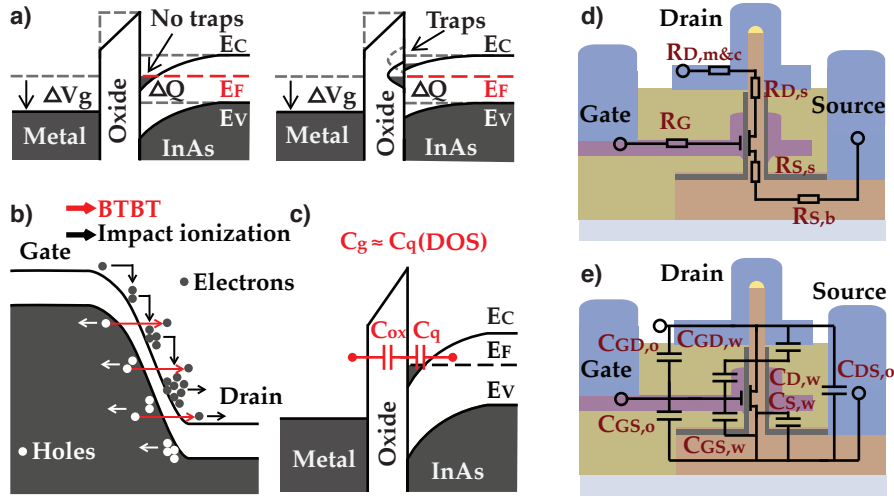


**Figure 1.2:** Schematics of (a) an enhancement-mode vertical GAA InAs/high- $\kappa$  nanowire MOSFET, (b) the band diagram of the transistor on-state, and (c) the band diagram of the transistor off-state.

## 1.4 CHALLENGES

To realize the new type of MOSFETs with the anticipated performance is challenging, and the challenges can be divided into two categories. One is from the MOSFET itself. The other is from the parasitic components arising when connecting the MOSFET with the external world. In fact, the active region serving as a functioning MOSFET is only the gated segment, as shown in figure 1.2(a), whereas the other parts of the nanowire, as well as the contacts, work purely as leads connecting the MOSFET with other circuit components or measurement probes. In this section, both the intrinsic and the extrinsic parts will be discussed.

The key functions of a MOSFET rely on the performance of the MOS gate stack, and since it is made by combining the crystalline semiconductor and the amorphous dielectric, defects at the semiconductor/dielectric interface and inside the dielectric, characterized by the interface trap density,  $D_{it}$ , and the border trap density,  $N_{bt}$ , respectively, are unavoidable and usually large [31,32]. This significantly constrains the MOSFET performance since the charging or discharging of the defect-induced trap states across the band gap greatly reduces the movement of the Fermi Level with gate voltage, figure 1.3(a), finally resulting in increased SS [33] and reduced  $I_{on}$  and extrinsic  $g_m$  [34]. The InAs/high- $\kappa$  system usually results in  $D_{it}$  and  $N_{bt}$  in the order of  $10^{13} \text{ eV}^{-1}\text{cm}^{-2}$  and  $10^{19} \text{ eV}^{-1}\text{cm}^{-3}$ , respectively [35–38], which is far higher than in the Si/SiO<sub>2</sub> system [39,40]. Another challenge is the narrow band gap of InAs, 0.35 eV [20]. The first trouble of using a narrow band gap channel is the impact-ionization and band-to-band tunneling (BTBT) at the gate-drain



**Figure 1.3:** (a) Band diagrams of the MOS gate stack with and without trap states. (b) Band diagram of the gate-drain junction, showing the impact ionization and band-to-band tunneling. (c) Band diagram of the MOS gate stack, showing the problem due to the small density of state (DOS) of InAs. (d)-(e) Parasitic resistances and capacitances. In the subscripts, s, m, b, w, and o denote contact, metal, bottom, wire, and overlap, respectively, and S, D, and G denote source, drain and gate.

junction, figure 1.3(b). This increases the MOSFET output conductance,  $g_d$ , hence reducing the device self-gain  $g_m/g_d$  and cutoff frequency  $f_t$  [41, 42], and reduces the breakdown voltage, hence restricting the transistor power applications [43, 44]. Besides, the narrow band gap is always associated with a small density of state (DOS) [20], and thus another problem arises due to the quantum capacitance limit (QCL), figure 1.3 (c). In brief, scaling the dielectric thickness cannot give a continuous increase in gate capacitance density since  $C_g$  is finally dominated by quantum capacitance (or semiconductor capacitance),  $C_q$ , which is proportional to semiconductor's DOS.

Parasitics outside the MOSFETs pose another type of challenge, figure 1.3(c). The existence of these components dramatically hinders the extrinsic performance of the MOSFETs, which to some extent is more crucial than the intrinsic. As shown in the figure, the parasitic capacitances can severely slow down the ICs since charging/de-charging these capacitors takes time [18], whereas the parasitic resistances limits the effective voltage drops between electrodes, hence degrading  $I_{on}$  and  $g_m$  significantly. Besides, the existence of these components makes the characterization of the intrinsic performance



difficult.

The thesis aims at solving the problems related to the challenges from the nanowire MOSFET itself. But before that, methods to reduce the parasitics are developed, since they can conceal the intrinsic performance significantly, as discussed in later chapters.

# 2

## Planar InAs/High- $\kappa$ MOS Gate Control

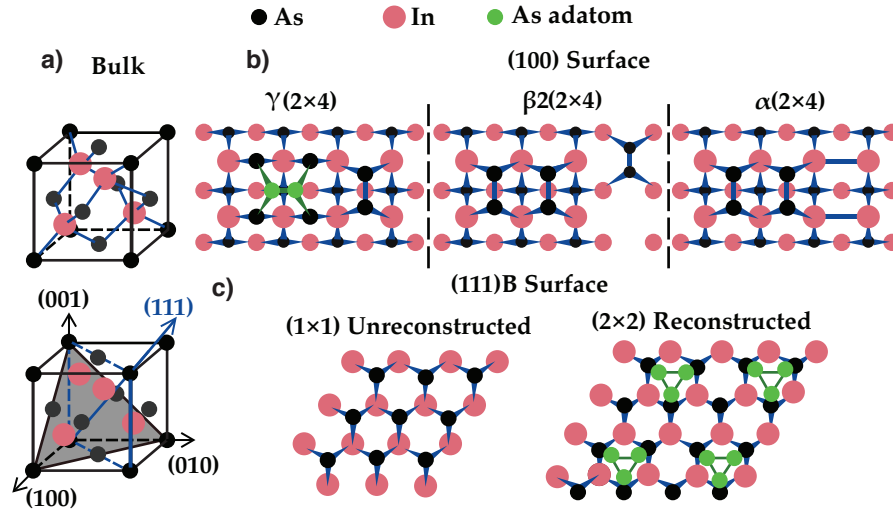
*H*IGH-efficiency InAs/high- $\kappa$  metal-oxide-semiconductor (MOS) gate control is a key to realize a high-performance MOSFET. However, the gate performance is hampered in reality by defects resident both inside the high- $\kappa$  layer and at the high- $\kappa$ /InAs interface. These defects contribute a significant amount of trap states across the band gap, which restricts the control of Fermi-level movement [45], therefore increasing the sub-threshold slope, and reducing the extrinsic transconductance as well as the charge mobility and the on-state current. Indeed, the large defect density is one of the most important challenges for III-V material to replace Si in the existing technology nodes [40]. Thus, a major task in the development of next-generation high-speed, low-power electronics is to reduce these trap states down to tolerable levels.

To manage the task, reliable characterization techniques both to profile the trap density across the band gap and to determine the chemical species across the interface are necessary. Planar MOS capacitance-voltage (C-V) measurements in combination with X-ray photoelectron spectroscopy (XPS) measurements have become a staple in studying MOS gate stacks. For over 70 years, there have been great achievements, based on these techniques [46–49], which enables understanding and further improvements of the III-V MOS performance. The results have revealed that high performance MOSFETs rely intimately on the detailed processing conditions including substrate surface preparation, dielectric deposition, and post-annealing etc. The planar MOS study thus is the starting point of the thesis to understand the InAs/high- $\kappa$  system. The knowledge gained from the study can either be used to improve the planar InAs/high- $\kappa$  MOSFET performance or be transferred directly to the nanowire MOSFET technology.

## 2.1 SUBSTRATE SURFACE

The control of the high density of structural defects at the InAs surface is the most task crucial for the InAs/high- $\kappa$  MOS gate stack. Naturally, the surface structure is determined by the bulk crystal, and for the case of bulk InAs, it crystalizes into the so-called zinc-blend (ZB) structure, figure 2.1(a). The structure consists of two interlocking face-centered-cubic (FCC) lattices, one of each constituted by In and As, respectively, with the basis at  $(0,0,0)$  and  $(1/4,1/4,1/4)$ . Each In atom (or As atom) is bonded with four As atoms (or In atoms) at four neighboring tetragonal sites. InAs has partially ionic and partially covalent bonds with a lattice constant of  $6.0584 \text{ \AA}$ , and the covalent radiuses of  $1.44 \text{ \AA}$  and  $1.2 \text{ \AA}$  for In and As atoms, respectively. In general, the surface structure cannot repeat exactly its bulk structure due to the bond scission at the terminating plane. The resulting surface after bond scission is full of "dangling" bonds and is energetically unstable. To reduce the free energy of the system, adjacent surface atoms tend to bond together forming dimers, accompanied by a re-arrangement of the atoms on the entire surface, and the resulting surface usually has a highly ordered structure but significantly different from the bulk crystal. This process is termed surface reconstruction.

The InAs semiconductor can be terminated in various planes, as depicted in figure 2.1(a). The most widely studied is the (100) plane. The InAs(100) surface is a polar unstable surface, which can end up with either the In or the As monolayer. The As terminated surface could be beneficial since it provide an As cap, which may prevents the formation of the highly stable In oxide that is detrimental for the device performance, as discussed in later sections. In addition, bonds on the (100) surface exhibit a more covalent nature. The resulting possible reconstructions are very complicated [50–52], ranging from the In-rich  $(4 \times 2)$  In-dimer surface to the As-rich  $(4 \times 4)$  As-trimer surface, depending on the specific growth conditions. Figure 2.1(b) illustrates the most common III-V (100) surface reconstructions within the transition region of  $(2 \times 4)$  between the two extremes. As can be seen, an InAs(100) surface could consist of a large amount of In or As dimers, vacancies as well as dangling bonds and anti-sites (not shown). Besides, the surface In proportion steadily increases from the As-rich  $\gamma(2 \times 4)$  towards the In-rich  $\alpha(2 \times 4)$ . These surface species will influence the final MOS performance significantly [53]. Compared to the (100) surface, the (111)B surface shows more promising character but MOSFETs based on the surface have not been well studied yet. The InAs (111)B surface is As-terminated but with a larger surface atom density than (100). However, the surface bonds exhibit more ionic nature. Astonishingly, stable unreconstructed (111)B surfaces are prevalently found [54], although some researchers also found a  $(2 \times 2)$  As trimer reconstruction on the As-



**Figure 2.1:** (a) Zinc-blende crystal structure of bulk InAs. (b)-(c) Possible surface reconstructions of InAs (b) (100) surface and (c) (111)B surface. The As adatoms are usually found on As-rich surfaces obtained by growing the crystal with high As pressure and low temperature [58], and can be thought of as the opposite to the As surface vacancies.

rich surface [55], figure 2.1(c). In the unreconstructed condition, As dangling bonds are occupied. Mankefors et al. demonstrated that the stability of the surface results from the charge redistribution over several atomic layers so that the charges are transferred from the surface to the bulk [54]. In later sections, MOS C-V characteristics using both surfaces are studied in detail. The (111)A surface is also studied in the thesis, which is an In-terminated surface with  $(2 \times 2)$  In vacancies in general [56], however, all devices made on this surface show huge leakage currents, and thus no electrical measurements were performed. This could be attributed to the fact that there is a 2D electron gas layer (2DEG) commonly observed across the clean InAs (111)A surface, opposite to the unreconstructed (111)B surface that cannot host a 2DEG [57].

## 2.2 NATIVE OXIDES AND ATOMIC LAYER DEPOSITION

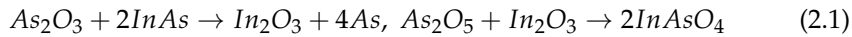
Compared to defects introduced by the surface reconstruction, it is found in Paper I that the quality of the InAs/high- $\kappa$  interface is influenced more by the presence of various native oxides due to the narrow band gap of InAs (as shown later in the following sections). InAs surfaces exposed to air usually consist of As  $5+$ , As  $3+$  and In  $3+$  oxides [59], resulting in In-O or As-O

**Table 2.1:** List of stable InAs oxides and their bulk oxide Gibbs free energies  $\Delta G$  (kcal/mol) [60]

Oxide	As <sub>2</sub> O <sub>3</sub>	As <sub>2</sub> O <sub>5</sub>	In <sub>2</sub> O <sub>3</sub>	InAsO <sub>4</sub>
$\Delta G$	-137.7	-187	-198.6	-209.4

bonding configurations across the surface that provide trap states. In table 2.1, stable InAs oxides and their bulk oxide Gibbs free energies are listed. It can be seen that, in general, As native oxides are less stable than In oxides and are readily removed.

It has been found that at elevated temperatures, the unstable As oxides in InAs will convert to more stable ones through the reaction [60]



A surface pre-cleaning procedure before the high- $\kappa$  deposition, usually termed as "passivation" in device technologies, is found to reduce the amount of the native oxides by either reacting with the As-O and In-O bonds or by forming e.g. In-Si bonds in advance, hence preventing the As-O and In-O bond formation. Commonly used cleaning chemicals include chalcogenides (e.g. (NH<sub>4</sub>)<sub>2</sub>S<sub>x</sub> solutions [61]), or etchants (e.g. HCl solution [62]). Alternatively, other surface treatments such as As-flux capping [63], hydrogen plasmas [62], Si over-layer growth on III-V [64] etc. are also used. These approaches are again more efficient in reducing the amount of unstable As oxides than In oxides. In fact, the most efficient approach in removing the native oxides is through the "self-cleaning" during the high- $\kappa$  dielectric atomic layer deposition (ALD) [61], as explained below.

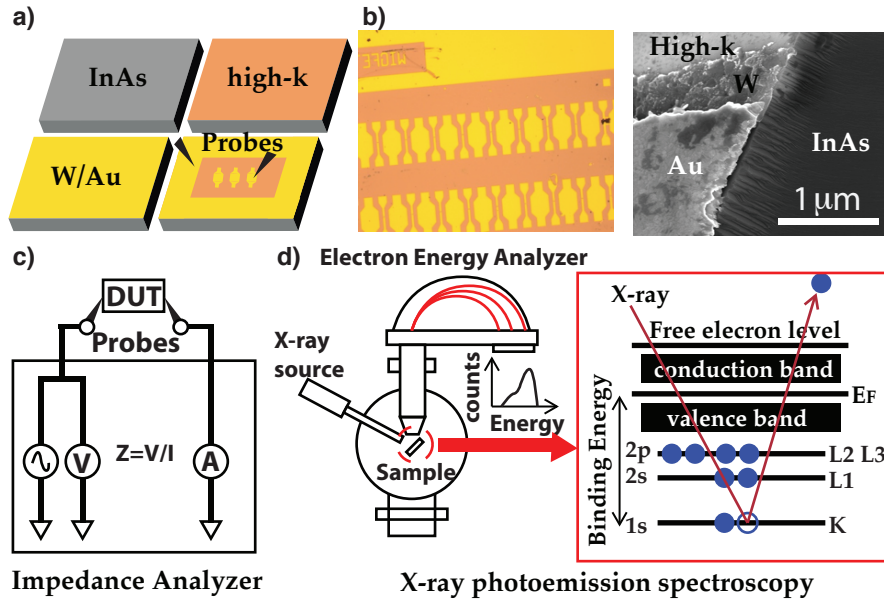
ALD is based on the hydrolysis reaction between water and alkyls such as trimethyl-aluminum (TMAI) and Tetrakis(dimethylamino)hafnium (TDMA-Hf). To deposit e.g. Al<sub>2</sub>O<sub>3</sub> on InAs, short pulses of TMA are introduced into the ALD reactor chamber. Each TMA pulse is followed by a short water pulse. The hydrogen bonds in water will break the methyl bonds in TMA, forming gaseous CH<sub>4</sub> and leaving a Al-O layer on the substrate surface. One such a cycle of pulses usually gives 1 Å Al<sub>2</sub>O<sub>3</sub>. In-situ XPS measurements [47,61,65] have revealed that the ligand exchange reaction also occurs between metal precursors and surface native oxides, and several cycles of TMAI pulses are found to greatly reduce the As native oxides by converting As-O bonds to As-Al or As-Hf bonds. However, ALD is less efficient in removing In<sub>2</sub>O<sub>3</sub> since In-O-Al or In-O-Hf bonds usually results from the ligand exchange reaction. Besides, the ALD process, or any oxidation process, creates other types of defects such as dangling bonds and dimers etc. at the III-V/high- $\kappa$

interface [32]. In addition, the ALD deposited high- $\kappa$  material is usually not purely amorphous but polycrystalline.

### 2.3 MOS CAPACITOR FABRICATION AND MEASUREMENTS

Planar MOS capacitors were fabricated on n-type InAs substrates with (100) and (111)B orientations. The doping density for the two cases were comparable,  $3.5 \times 10^{16} / \text{cm}^3$  and  $7.5 \times 10^{16} / \text{cm}^3$  for (100) and (111)B surfaces, respectively. The samples were pre-treated in HCl solution (HCl:H<sub>2</sub>O 1:1) for 1 min and then rinsed in 2-isopropanole (IPA) for 15 s. 80 cycles of high- $\kappa$  oxide (24 cycles for XPS measurements) were deposited on the sample under various deposition temperatures in a Cambridge Nanotech Savannah-100 ALD chamber, using either TMAI or TDMA-Hf and water as precursors. The deposition always started by one alkyl pulse for self-cleaning. W/Au contacts were then sputtered, followed by patterning using UV lithography and dry/wet etching of the metals. After that, some samples were annealed in hydrogen forming gas at 400 °C for 5 min. Figure 2.2 (a) shows the schematic of the processing as well as the optical microscope image of the final devices plus a SEM image of the capacitor cross-section.

The C-V characteristics of the MOS capacitors were measured by a 4294A impedance analyzer. A simplified schematic of the measurement setup is shown in figure 2.2(b), which includes a signal source, a voltmeter and an ammeter. The input signal to the device under test (DUT) consists of a small AC signal superimposed on a DC bias sweep. In reality AC and DC voltages are supplied separately. The vectors (both magnitudes and phase angles) of the small signal current and voltage are measured by the voltmeter and ammeter, from which the complex impedances of the DUT can be obtained. In reality, the ammeter is replaced by an I-V converter consisting of an operational amplifier with a negative feed-back to increase the accuracy and robustness of the measurements, and, besides, an open-short-load calibration before the measurements is necessary in order to completely remove the parasitic components inside the measurement setup. The frequency bandwidth of the small signal is from 40 Hz to 110 MHz. To characterize the interfacial chemistry, samples with 24 cycles of high- $\kappa$  oxide and of uncoated references were measured by XPS at beam-line I311 of the MAX-II synchrotron, as illustrated in figure 2.2(c). An X-ray with energy  $E_{\text{photon}}$  was incident onto the sample, which ejected core electrons of different surface species. The energy difference between the Fermi level and the core level where the excited electron previously resided is called binding energy,  $E_{\text{binding}}$ , and for different species,  $E_{\text{binding}}$  of the same core level is different. Hence the energy can be used as a finger print to identify the existence and amount of different



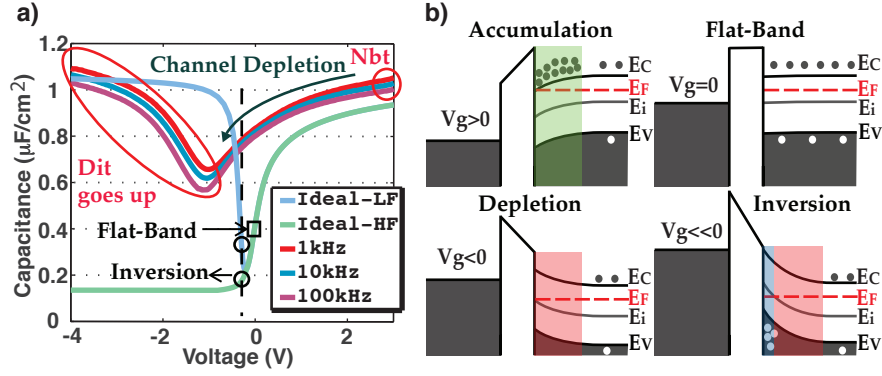
**Figure 2.2:** (a) Schematic of the planar MOS capacitor fabrication. (b) Optical microscope image of the MOS capacitors and SEM image of the capacitor cross-section. (c) Schematic of the Impedance analyzer setup. (d) XPS measurements.

species. The generated electrons were collected through an energy analyzer where a magnetic field was applied. Under the Lorentz force, the trajectories of electrons with different ejection kinetic energies,  $E_k$ , bended with different radius, which enabled the energy selective election counting and thereby the chemical species quantification. The measured  $E_k$  is converted to  $E_{binding}$  by  $E_{binding} = E_{photon} - (E_k + \Phi)$ , in which  $\Phi$  is the work function that is the energy difference between the Fermi level and the free electron level.

## 2.4 DEVICE CHARACTERIZATION

### 2.4.1 MOS CAPACITOR C-V CHARACTERISTICS

In this subsection, the measured C-V degradation due to trap states will be discussed. Figure 2.3 shows the comparison of measured and simulated C-V curves as well as the band diagrams of different bias regimes. The measured capacitances are determined from the measured impedances by first subtracting the series resistance in the probes and contacts and then adopting a model with a capacitor in parallel with a conductor. The simulated C-V



**Figure 2.3:** (a) Comparison between the measured and ideal InAs/high- $\kappa$  C-V characteristics. (b) Band diagrams of different bias regions.

curves are obtained by solving Poisson’s equation using Fermi-Dirac statistics [49, 66] with the non-parabolic band effect considered [48], but contains no trap states, hence reflecting the ideal C-V characteristics. For the ideal cases, accumulation, depletion and inversion can be readily reached since the Fermi level can be easily tuned across the band gap without hinderance. A steep slope of the capacitance decrease between 1 V and 0 V reflects a quick depletion of the channel. The capacitance finally reaches a minimum of 0.2  $\mu\text{F}/\text{cm}^2$ , corresponding to the maximum depletion width. In addition, the frequency modulation in the inversion region (negative biases) should be strong due to the larger time constant of the minority carriers. In contrast, the measured C-V curves of InAs/high- $\kappa$  MOS capacitors are far from ideal. In the case, the Fermi level can only be tuned between accumulation and depletion, and larger voltage span is needed to charge and de-charge the trap states inside the band gap. The C-V curves, thus, show a significant stretching. Besides, an additional trap capacitance  $C_{it}$ , originating from the interface trap response to the input ac signal, is added to the intrinsic semiconductor capacitance  $C_s$  at each bias, which increases the total measured capacitance. This effect can most clearly be seen from the increased minima of the measured C-V curves. Finally the  $C_{it}$  is also frequency dependent through a trap time constant,  $\tau$ . The characteristic frequency of  $C_{it}$  can be written as [67]

$$f_c = \frac{1}{\tau} = \frac{\sigma v_t N_C}{\exp(\Delta E/kT)}, \quad (2.2)$$

where  $\Delta E$  is the energy difference between the Fermi level and the conduction band edge (CBE);  $k$ ,  $T$ ,  $\sigma$ ,  $v_t$ ,  $N_C$  are the Boltzmann constant, temperature, trap cross-section, electron thermal velocity and effective electron density of



state in the conduction band, respectively. This means that the frequency modulation of  $C_{it}$  becomes strong as the Fermi level can be moved further away from the CBE (larger  $\Delta E$ ). In the figure, however, the C-V curves show a fairly small frequency dependance at negative biases, indicating that the Fermi level movement is restricted nearby the CBE. It is thus believed that the rise in capacitance below -1.5 V does not result from the minority carrier response, but from an increased interface trap density (hence increased  $C_{it}$ ) towards mid-gap. Finally, a frequency dispersion in the strong accumulation region is common observed, which originates from the response of trap states inside the oxide (border traps) [68]. The non-ideality of the measured C-V curves, in fact, contains all the information of traps in the system.

#### 2.4.2 TRAP CHARACTERIZATION BY LOW FREQUENCY C-V FITTING

To characterize the interfacial trap density across the energy gap, a low frequency C-V fitting method has been developed. At low frequencies, the charge response of interfacial defect states can follow the input small signal variation, as illustrated in figure 2.4(a). Under such circumstances, these states act as a capacitor,  $C_{it}$ , parallel to the intrinsic semiconductor capacitor,  $C_s$ . The total capacitance measured can thus be modeled as

$$\frac{1}{C_{tot}(V_g)} = \frac{1}{C_{ox}(V_g)} + \frac{1}{C_s(V_g) + C_{it}(V_g)}, \quad (2.3)$$

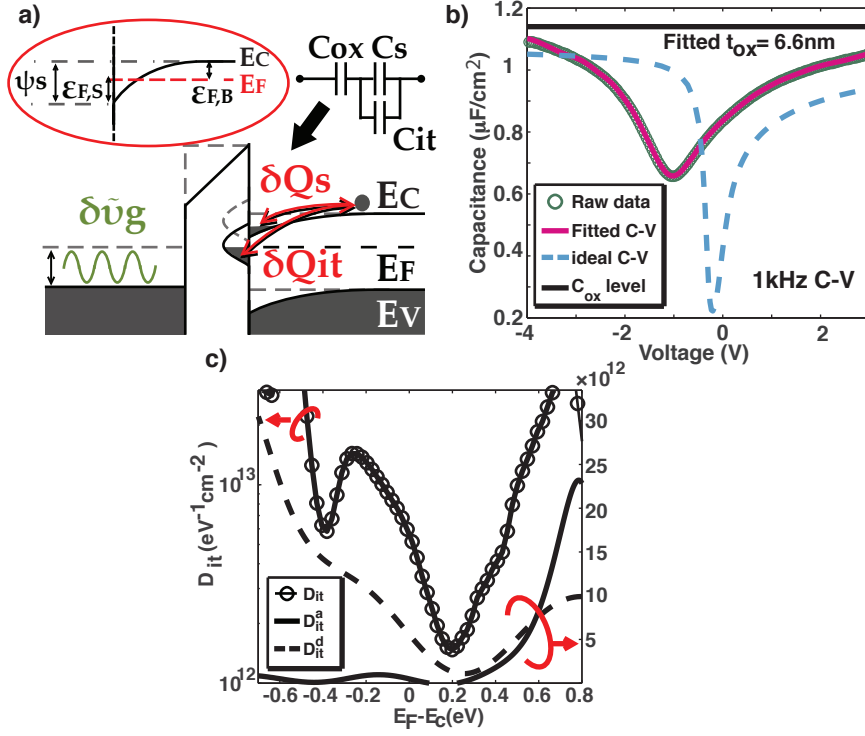
where  $C_{ox}$  is the oxide capacitance. The next task is thus to evaluate  $C_{tot}$  and  $V_g$  at each relative Fermi level location ( $E_F - E_c$ ) with the interface trap density profile, i.e.  $D_{it}(E_F - E_c)$ , and  $C_{ox}$  as the fitting parameters until the measured and evaluated C-V curves fit each other.

$C_s$  can be evaluated by solving Poisson's equation, which, by applying Gauss theorem, can be expressed as

$$Q_s = \text{sign}(\varepsilon_{F,S} - \varepsilon_{F,B}) \sqrt{-2\varepsilon_s kT \int_{\varepsilon_{F,B}}^{\varepsilon_{F,S}} [N_d^+ + p(\varepsilon_{F,S}) - n(\varepsilon_{F,S})] d\varepsilon_{F,S}}, \quad (2.4)$$

where  $Q_s$  is the semiconductor surface net charge,  $p$  and  $n$  are the hole and electron densities, respectively,  $N_d^+$  is the ionized dopant concentration,  $\varepsilon_s$  is the InAs dielectric constant, and  $\varepsilon_{F,S}$  and  $\varepsilon_{F,B}$  are relative Fermi level location at the interface and inside the bulk normalized to the thermal energy,  $kT$ , as illustrated by the inset in figure 2.4(a).  $n$ ,  $p$  and  $N_d^+$  can be evaluated from the Fermi-Dirac statistics, which gives

$$n = \frac{2N_C}{\sqrt{\pi}} \int_0^{\infty} \frac{\sqrt{x(1+\alpha x)}(1+2\alpha x)}{1 + \exp(x - \varepsilon_{F,S})} dx \quad (\alpha = kT(1 - m_e^*)^2/E_g), \quad (2.5)$$



**Figure 2.4:** (a) Band diagram and low frequency MOS capacitor charge response to the small input signal.  $E_C$ ,  $E_V$  and  $E_F$  represent the semiconductor conduction band edge, valence band edge and Fermi level, respectively.  $\delta Q_s$  and  $\delta Q_{it}$  are small variations of charge density in the semiconductor surface energy levels and the trap states, in response to the low frequency small input signal  $\delta v_g$ . The inset shows how the surface band bending  $\psi_s$ , relative Fermi level location at the interface  $\epsilon_{F,S}$  and in the bulk  $\epsilon_{F,B}$  are related. (b) Low-frequency C-V fitting. (c) Trap densities used in achieving good fit in (b).

$$p = \frac{2N_V}{\sqrt{\pi}} \int_0^{\infty} \frac{x}{1 + \exp(x - (\epsilon_{F,S} + \epsilon_g))} dx, \quad (2.6)$$

and

$$N_d^+ = \frac{N_d}{1 + 2\exp(\epsilon_{F,S})}, \quad (2.7)$$

where  $N_C$  and  $N_V$  denote the effective density of states (DOS) in the conduction and valence bands. The  $\alpha$  in equation 2.5 is the nonparabolicity factor, in which  $m^*$  and  $E_g$  are the electron effective mass and band gap of InAs.

Since for InAs, the DOS in the conduction band is small, the Fermi level can easily move quite far into the conduction band. The non-parabolic band effect thus become significant [48]. For p, one can simply assume a Fermi-Dirac distribution of holes. In addition, the ionization effect of dopants is considered by assuming that the dopant level overlaps the CBE.  $C_s$  then can be evaluated by

$$C_s(\varepsilon_{F,S}) = dQ_s(\varepsilon_{F,S})/d\varepsilon_{F,S} \quad (2.8)$$

The  $C_{it}$  can be obtained the same way, i.e.

$$Q_{it}(\varepsilon_{F,S}) = \int_{-\infty}^{\varepsilon_{F,S}} D_{it}^a(x)dx - \int_{\varepsilon_{F,S}}^{\infty} D_{it}^d(x)dx, \quad C_{it}(\varepsilon_{F,S}) = \frac{dQ_{it}(\varepsilon_{F,S})}{d\varepsilon_{F,S}}, \quad (2.9)$$

where the  $Q_{it}$  is the net electron density in interface states, similar to  $Q_s$  in equation 2.8. The interface trap states are classified into donor type and acceptor type. The trap density of the donor type,  $D_{it}^d$ , peaks below mid-gap, whereas the trap density of the acceptor type,  $D_{it}^a$ , peaks above mid gap. In the fitting, both  $D_{it}^d$  and  $D_{it}^a$  are simulated by a Gaussian function with coefficients as the fitting parameters. The donor type trap is positive when empty and neutral when charged. The acceptor type trap, on the contrary, is neutral when empty and negative when charged, as shown in equation 2.9.

Finally  $\varepsilon_{F,S}$  can be related to  $V_g$  by

$$V_g(\varepsilon_{F,S}) = \psi_s + \frac{Q_s(\varepsilon_{F,S})}{C_{ox}} + \frac{Q_{it}\varepsilon_{F,S}}{C_{ox}}, \quad \text{where } \psi_s = \frac{kT(\varepsilon_{F,S} - \varepsilon_{F,B})}{q}. \quad (2.10)$$

$\psi_s$  and  $q$  are the surface band bending, figure 2.4(a), and the elementary charge, respectively.

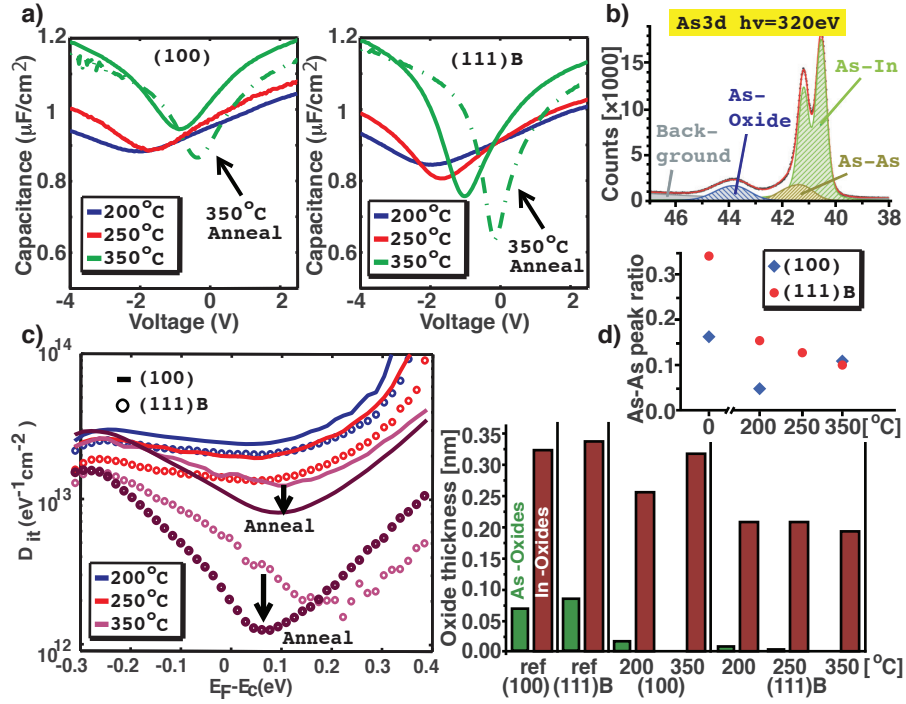
The measured C-V curve can be perfectly fitted by the approach, as shown in figure 2.4(b), using the trap density profiles in figure 2.4(c). As can be seen, due to the low DOS of InAs, the ideal C-V curve cannot reach  $C_{ox}$  level under strong accumulation because of the smaller  $C_s$  in series with  $C_{ox}$ . Smaller  $C_s$  reduces the gain in  $t_{ox}$  scaling for enhancement-mode MOSFETs, making it readily reach the quantum capacitance limit. However, the low frequency C-V fitting method have a few shortcomings. Firstly, it cannot discriminate the densities of surface border traps from the interface traps, so the evaluated  $D_{it}$  represents the upper limit of interfacial defects. Secondly, for  $D_{it}$  below  $10^{12}$   $\text{eV}^{-1}\text{cm}^{-2}$ , the method will introduce errors since the difference between the real and ideal C-V curves will be too small to resolve. Thirdly the accuracy will gradually decrease towards the valence band edge and further into the conduction band since the values evaluated there are based on interpolation rather than on real measurements. However, the approach is still far better, to some extent, than the commonly used conductance method or Terman

method [66] since the widest energy range of  $D_{it}$  profiling is obtained, and no true high frequency C-V curves or conductance peaks are needed, which are usually not observed for room temperature C-V measurements of InAs MOS capacitors.

### 2.4.3 ALUMINUM OXIDE

The InAs/Al<sub>2</sub>O<sub>3</sub> gate stack is studied in detail. Figure 2.5(a) shows the measured C-V characteristics of InAs/Al<sub>2</sub>O<sub>3</sub> capacitors with different InAs orientations and Al<sub>2</sub>O<sub>3</sub> deposition temperatures. In general, the (111)B surfaces show better C-V modulation than (100) surfaces, e.g. less C-V stretch-out, lower capacitance minimum etc., which indicates better interface quality. Besides, a higher Al<sub>2</sub>O<sub>3</sub> deposition temperature and the use of a post-annealing step are found to improve the interface for both surfaces. Figure 2.5(c) shows the corresponding  $D_{it}$  profiles extracted using the low frequency fitting method. As can be seen, the (111)B surfaces have smaller  $D_{it}$  values in general. Besides, when increasing the thermal budget, through the use of either a high Al<sub>2</sub>O<sub>3</sub> deposition temperature or a post annealing step, a significant drop of  $D_{it}$  near the CBE is observed for both surfaces. For trap states near the mid gap (about -0.15 eV), however, a strong reduction of  $D_{it}$  is only observed for the (111)B surface. Figure 2.5(b) shows different components of the fitted As 3d spectra measured by XPS, from which the amounts of different surface species can be extracted, figure 2.5(d). As can be seen, the (111)B surfaces, after ALD deposition, have smaller amounts of native oxides (but larger amounts of As-As bonds) than (100) surfaces in general, indicating a more efficient self-clean during ALD for the (111)B surface. Besides, by increasing the thermal budget, the amount of the As native oxides keeps decreasing for both surface orientations, whereas that of the In-oxides slightly decrease for (111)B surfaces, but increase for (100) surfaces. A similar trend to In-oxides is found for As-As bonds, as shown in the inset. The As-As bonds can come from either dimers or anti-sites, and it is difficult to distinguish their origin.

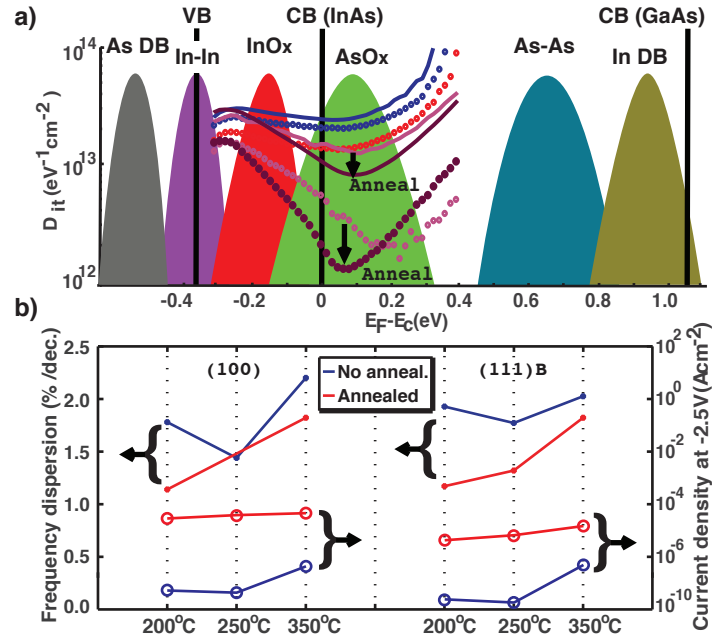
The comparison between C-V and XPS results indicates a correlation between As-oxides and  $D_{it}$  near the CBE, and a correlation between In-oxides and  $D_{it}$  towards the mid-gap. By combining the conclusion of this work with the current understanding on GaAs [32,53], the possible origins of trap states across the band gap for both InAs and GaAs are qualitatively illustrated and compared in figure 2.6(a). As can be seen, due to the narrow band gap of InAs, the dominant trap origins near the CBE and midgap, which are critical for n-MOSFET applications, are changed, as compared to GaAs. For the latter, the trap origins near the CBE and midgap are Ga-dangling bonds and As-As dimers, respectively [32]. The strategies to reduce the gap states for small



**Figure 2.5:** (a) Comparison of the deposition temperature and annealing influence on the 1 kHz C-V characteristics of (100) and (111)B samples. (b) XPS spectrum with fits for various species of the As 3d core-level obtained with a photon energy of 320 eV. (c)  $D_{it}$  v.s.  $E_t - E_c$  extracted using the low frequency fitting method as a function of InAs orientation, oxide deposition temperature and annealing. The x-axis denotes the position of the trap level  $E_t$  with respect to the conduction band edge  $E_c$ . (d) Absolute thicknesses of As-oxide and In-oxide, extracted from the measured As 3d and In 3d spectra, as a function of the high- $\kappa$  deposition temperature. The inset shows the relative intensity of the spectral component of As-As bonds, as compared to the bulk In-As bonds, for different high- $\kappa$  deposition temperatures. 0°C refers to the corresponding reference samples without high- $\kappa$  ALD.

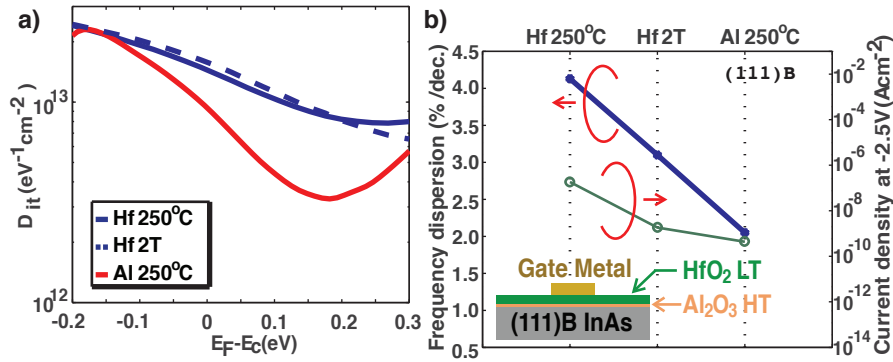
band gap InAs is hence far different than that for the larger band gap GaAs, and since it is easier to decomposed the As-oxides than to remove the Ga-dangling bonds and dimers, it could be beneficial to use InAs as the channel material also in terms of the gate electrostatic control. Although the removal of In oxides is difficult, it could be managed by fine control of the surface termination or facets as for the case of nanowires.

The border traps inside the high- $\kappa$  layer can be qualitatively studied by eval-



**Figure 2.6:** (a) Comparison of the possible trap state origins across the band gap between InAs and GaAs, adapted after the works by Wang et al. [32] and Robertson [53]. (b) Accumulation capacitance frequency dispersion and gate leakage current density at  $V_g$  of -2.5 V as a function of the processing condition.

uating the frequency dispersion of the accumulation capacitance  $C_a$  [68,69], as shown in figure 2.3(a). The slope of  $C_a$  v.s.  $\log(f)$ , in the unit of percentage per decade, is proportional to the border trap density,  $N_{bt}$ , according to Heiman and Warfield’s charge tunneling model [68]. Figure 2.3(b) shows the comparison of frequency dispersion and gate leakage current density for different samples. It can be seen that the high deposition temperature in general results in worse high- $\kappa$  layer and increased leakage. This could be due to the high- $\kappa$  layer crystallization, which increases the amount of traps and tunneling leakage. Annealing in forming gas can passivate the defects since hydrogen atoms can penetrate into the layer, however it usually results in an elevated gate leakage since the external atom penetration introduces additional current paths. This also significantly limits the use of post-annealing in the MOSFET fabrication. Thus to obtain both a better interface and a better high- $\kappa$  layer, a two-temperature deposition scheme can be a good solution.



**Figure 2.7:** (a) Comparison of (a)  $D_{it}$ , (b) frequency dispersion and gate leakage current density for MOS capacitors with Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> using both a single-temperature and a 2-temperature deposition schemes. The inset in (b) shows the schematic of the proposed optimal gate stack for InAs/high- $\kappa$  MOSFETs.

#### 2.4.4 HAFNIUM OXIDE

The InAs/HfO<sub>2</sub> gate stack is also studied, and since the HfO<sub>2</sub> has far higher  $\kappa$  (table 1.1), it is more promising than Al<sub>2</sub>O<sub>3</sub>. However, HfO<sub>2</sub> in general is far inferior in terms of quality. Figure 2.7 shows the comparison of  $D_{it}$ , frequency dispersion and gate leakage of HfO<sub>2</sub> (blue, solid) and Al<sub>2</sub>O<sub>3</sub> (red, solid) deposited under the same temperature, 250 °C, and on the same InAs surface, (111)B. The poorer  $D_{it}$  profile reflects a less efficient self-cleaning of native oxides for HfO<sub>2</sub>. The larger frequency dispersion and leakage, on the other hand, are due to the fact that HfO<sub>2</sub> can crystallize at lower temperature than Al<sub>2</sub>O<sub>3</sub>, and hence it is a less amorphous dielectric. Results of using a 2-temperature HfO<sub>2</sub> deposition scheme (2T) is also shown (dashed), in which the first 10 cycles of HfO<sub>2</sub> are deposited at 250 °C and the remaining 70 cycles are deposited at 150 °C. By comparing the 2T HfO<sub>2</sub> and single-temperature HfO<sub>2</sub> results, it can be seen that the interface quality is preserved for the 2T scheme due to the high temperature deposition of the first 10 cycles, whereas a significant improvement of the high- $\kappa$  layer quality is gained. In the future, since the HfO<sub>2</sub> has higher  $\kappa$  but poorer quality on InAs, a sandwiched interfacial Al<sub>2</sub>O<sub>3</sub> deposited at high temperature between the substrate semiconductor and the low-temperature deposited HfO<sub>2</sub> could be a solution, as shown by the inset in figure 2.7(b), to preserve the benefits of both high- $\kappa$  materials as much as possible.

# 3

## InAs/High- $\kappa$ Vertical Wrap-Gated Nanowire MOS Gate Control

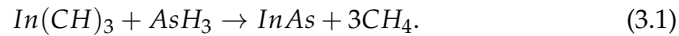
**D**EVELOPING the C-V technique to investigate the vertical GAA nanowire MOS gate control is challenging, especially when the conventional geometry of vertical nanowire MOSFETs needs to be conserved so that the knowledge gained is applicable to these devices. As shown in figure 1.3, in order to approach the intrinsic performance of a nanowire MOSFET, the spacer layers between electrodes needs to be thin enough [70] so that the associated series resistances are minimal. This, however, results in large parasitic overlapping capacitances between contacts, which can readily conceal the measured intrinsic MOS C-V characteristics that are usually small. This is also a reason why detailed C-V studies on vertical nanowire MOS capacitors are seldom found in literature [71,72]. In the thesis, the problem is solved by using a finger gate contact approach [18], which, hence, enables detailed  $D_{it}$  profiling and gate control optimization for vertical nanowire MOSFETs. In addition, radio-frequency (RF) C-V characterization of vertical GAA nanowire MOS capacitors is realized for the first time. Combined with a complete small-signal equivalent circuit model ranging over the entire measurement frequencies, this technique allows us to evaluate both interface and border traps, channel resistivity, and quality factor of the vertical GAA nanowire MOSFETs. In this chapter, the nanowire growth will be discussed first, since, as demonstrated in chapter 2, the gate stack performance relies intimately on the semiconductor surface condition and nanowires usually exhibit large differences in terms of surface condition, as compared to their planar counterparts. After that, detailed  $D_{it}$  profiling for nanowire MOS gate stacks is presented. Finally, The RF C-V technique is introduced.



### 3.1 NANOWIRES USED FOR MOSFETS

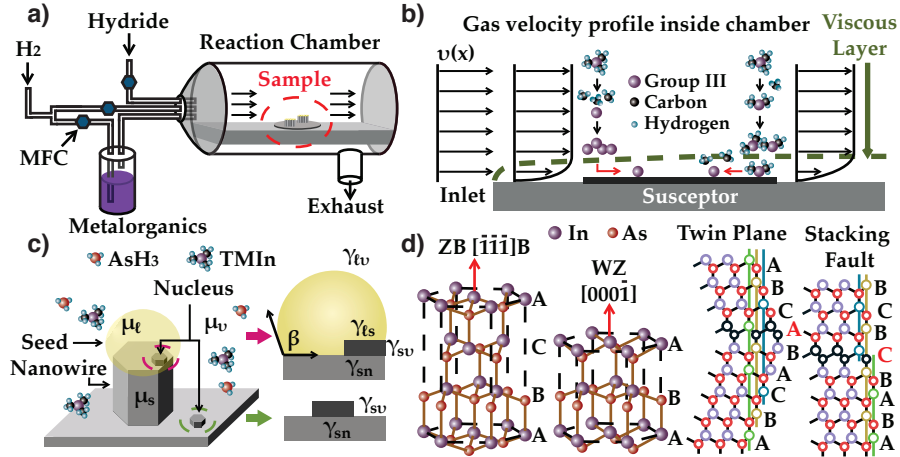
#### 3.1.1 NANOWIRE GROWTH

Nanowires can be formed in various ways, either top-down or bottom-up. In the thesis, nanowires are grown by low pressure (100 mbar) metalorganic vapor phase epitaxy (MOVPE) using Au as seed particles [13]. Figure 3.1(a) illustrate how a horizontal-reactor cold-wall MOVPE system works, in which hydrogen is used to carry the metalorganics (mainly group III and dopant precursors) stored in the bubblers into the reaction chamber. Meanwhile, the group V gas is also supplied and except for trimethylantimony (TMSb), most of the group V precursors are gaseous hydrides. The gas flow rates are controlled by mass flow controllers (MFCs). In the reaction chamber, the sample is placed onto a graphite susceptor heated by infrared lamps. Excess gases will be exhausted and burned safely. The chemical reactions during the epitaxial growth are in fact very complicated, including a stepwise release of methyl and hydrogen in precursor gas molecules via either homogeneous or heterogeneous reactions or both. The net reaction for growing InAs can be expressed as



One drawback of MOVPE is that the  $-\text{CH}_3$  in metalorganics usually cannot be removed completely due to the incomplete decomposition, leaving some carbon incorporated into the grown material, which contributes to a background doping level for the final devices. [73,74].

In the reaction chamber, figure 3.1(b), the molecules of different gaseous precursors often behave differently during the growth. According to fluid dynamics, the velocity of the flowing gas drops close to the hot susceptor surface, forming a viscous layer. The layer boundary is defined by the velocity drop by 1 %. If the rate-limiting process is the transport of growth species through the layer (left arrow), the growth is termed mass-transport limited growth. On the contrary, if the rate-limiting process occurs on the substrate surface (right arrow), it is called kinetic-limited growth, which gives a temperature dependent growth rate. Trimethylindium (TMIn) can decompose homogeneously in  $\text{H}_2$  and completely above  $350^\circ\text{C}$  [75]. This temperature is far lower than the normal growth temperature. Trimethylgallium (TMGa) for example, however, can only decompose completely above  $550^\circ\text{C}$  [76] that is higher than the temperature used for most nanowire growth. Joyce et al. examined the nanowire radial growth rates as a function of the growth temperature for both InAs and GaAs nanowires and found that a mass-transport limited growth behavior has already occurred above  $420^\circ\text{C}$  for InAs, but for GaAs, the growth remains kinetic-limited at least above  $500^\circ\text{C}$  [77]. This fundamental difference is a main challenge when growing



**Figure 3.1:** (a) Schematic illustration of the MOVPE reactor for crystal growth. (b) Gas velocity profile inside the reaction chamber, as well as two rate-limiting mechanisms for crystal growth. (c) Schematic illustration demonstrating the nanowire growth mechanism. (d) Schematics of ZB and WZ crystal structures, as well as two main types of defects, i.e. twin plane and stacking fault, commonly observed during nanowire growth.

ternary InGaAs nanowires, as discussed in detail in chapter 4.

The reason why nanowires grow cannot be explained merely by thermodynamics. Nanowire growth, to some extent, is a result of the kinetic benefit of nucleation at the vapor-solid-liquid (VLS) triple phase boundary (TPB) [78]. As shown in figure 1.3(c), for growth to proceed, a supersaturation between the supply phase (vapor) and the grown phase (solid) of the growth species, with the chemical potential of  $\mu_v$  and  $\mu_s$ , is first necessary. In the presence of liquid Au seed particles, it requires that  $(\mu_v - \mu_l) > 0$  and  $(\mu_l - \mu_s) > 0$  for nanowires to grow, where  $\mu_l$  denotes the chemical potential of the growth species in the liquid droplets. This thermodynamic requirement seems to say the bulk growth is always more favorable than the nanowire growth since  $(\mu_v - \mu_s)$  is larger both than  $(\mu_v - \mu_l)$  and  $(\mu_l - \mu_s)$ . Taken into account kinetics now, the nucleation rate  $\kappa_{nuc}$  is given by

$$\kappa_{nuc} = v_0 e^{-\Delta G/kT} \quad (\Delta G = -V_n \Delta \mu + \gamma_n A_n) \quad (3.2)$$

where  $k$ ,  $T$  and  $v_0$  are the Boltzmann constant, growth temperature and a pre-factor. The change in Gibbs free energy by nucleation,  $\Delta G$ , is given in the bracket, in which the first term describes the energy reduction when a nucleus forms where  $V_n$  and  $\Delta \mu$  represent the nucleus volume and the chemical

potential difference per III-V pair per unit volume between the supply phase and the solid phase; the second term describes the additional energy due to the formation of new interfaces of the nucleus where  $A_n$  and  $\gamma_n$  are the nucleus area and interface energy per unit area. The equation indicates a critical nucleus size where  $\Delta G$  reaches its maximum. Nuclei beyond the size will expand, whereas those below the size will shrink, both of which cause reduction in  $\Delta G$ . This maximum  $\Delta G$  can be thought of as the energy barrier for growth to occur. Comparing same nuclei at the TPB and the substrate, the changes in Gibbs free energies are

$$\Delta G_{TPB} = -V_n \Delta \mu + [Ph\gamma_{vs}x + Ph\gamma_{ls}(1-x)] - Ph\gamma_{lv}x \sin \beta + A\gamma_{sn} \quad (3.3)$$

and

$$\Delta G_{substrate} = -V_n \Delta \mu + Ph\gamma_{vs} + A\gamma_{sn} \quad (3.4)$$

in which  $P$ ,  $A$  and  $h$  are the perimeter, top surface area and height (a single III-V pair bilayer) of the nucleus;  $x$  is the fraction of the nucleus exposed to the vapor;  $\gamma_{vs}$ ,  $\gamma_{lv}$ ,  $\gamma_{ls}$  and  $\gamma_{sn}$  are interfacial energies per unit area of vapor-solid, liquid-vapor, liquid-solid and solid-nucleus interfaces ( $\gamma_{sn}$  equals to 0 for zinc-blende (ZB) stacking), figure 3.1(c). As can be seen, the additional interfacial energies of the nucleus formation at the TPB, the second term in the bracket, is smaller than that at the substrate since  $\gamma_{ls}$  is smaller than  $\gamma_{vs}$ , and, besides, the elimination of some Au liquid-vapor contact area due to the nucleus formation, the third term in equation 1.3, further reduces  $\Delta G_{TPB}$  significantly. Hence the nucleation rate of nanowire in the presence of Au liquid droplets is greatly enhanced, compared to that at substrate surface [78].

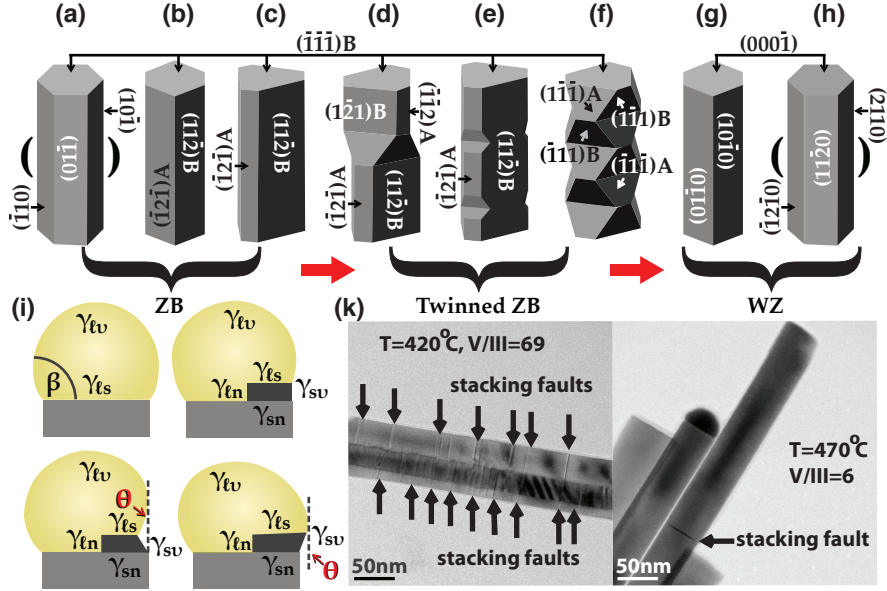
This new nucleation scenario promotes a possibility to switch the nanowire crystalline phase between the cubic ZB and the hexagonal wurtzite (WZ) as long as the stacking of one type at the TPB is preferential to the other by providing a lower  $\Delta G$  [79,80]. Figure 3.1(d) shows the comparison of WZ and ZB crystal structures along the nanowire growth directions,  $[000\bar{1}]$  and  $[\bar{1}\bar{1}\bar{1}]$ , respectively. The stacking sequences for ZB and WZ are ABCABC and ABAB with each letter representing a bilayer of In-As. The key difference is the  $60^\circ$  rotation of In atoms in the C stack of ZB within each  $\text{AsIn}_4$  tetrahedron in the same layer, compared to its WZ counterpart. WZ is never possible for bulk InAs since its denser stacking results in a larger atom repulsion along the growth direction, which in turn adds an extra energy,  $\gamma_{sn}$ , in  $\Delta G$ . Because the nearest-neighbor distances and lattice constants are very close for ZB and WZ, either type usually cannot dominate the entire nanowire growth since the  $\Delta G$  difference is small. A sudden change from one crystal type to another can be readily generated by any fluctuations during the growth, which results in metastable multiphase structures including twin planes for ZB and stacking faults for WZ or polytypism for commonly-grown nanowires. In figure 3.1(d),

examples of twin planes and stacking faults are shown. The colored bars are used to clarify the repetition of stacking. A twin plane is, in essence, a monolayer of WZ inserted into the ZB structure, which reverses the ZB stacking from ABC to CBA, while stacking faults are ZB monolayers inserted into the WZ structure.

### 3.1.2 CRYSTALLINE PHASE CONTROL

Numerous studies have been performed with the target of growing stacking defect free nanowires [78–81]. Several groups have recently attempted to clarify the influence of these defects on the transport properties of lateral intrinsic nanowire FETs [82, 83]. In this chapter, we demonstrated an extended understanding of the growth condition influence on the vertical GAA nanowire MOSFET performance. To begin with, experimental results as well as the theoretical explanation to achieve pure WZ nanowires will be presented first in this subsection.

Pure WZ nanowires are the target for several reasons. Firstly, WZ is more prevalent for the high-supersaturation growth of InAs nanowires [78]. Besides, ZB facets tend to grow laterally [84], forming a tapered shell. This is highly unwanted for high-performance nanowire MOSFET channels. The high overgrowth tendency is attributed to the higher surface energy of ZB facets, which results in higher lateral nucleation rate and shorter growth specie diffusion length along the nanowire. In addition, the ZB structure can have complicated facets, each of which could have different electronic properties like the bulk InAs (111)A and (111)B surfaces discussed in chapter 2. In contrast, the WZ structure usually exhibits simple facet conditions, namely the {1100} family, which resembles the non-polar (110) surface of bulk InAs [85]. Pure WZ nanowires can be realized by simply varying two basic growth parameters, the growth temperature (T) and the group-V and -III flow rate ratio (V/III ratio). Joyce et al. [79] clarified this using an extended nucleation model, and revealed that the key resides at the growth-condition dependent facet energies. Figure 3.2(a) shows the main facets for an InAs nanowire. For twin free ZB, the polar {112} family is the most common facets, (b), although the plausible {110} family, (a), was also discussed in Ref [79]. {110} facets were found at the ZB/WZ interface by Lehmann et al. [84]. Because {112}B has a lower surface energy, {112}B planes are usually elongated, resulting in the morphology in (c). Twinned ZB structures are shown in (d)-(f). A single twin can rotate the ZB facets by 60 degrees, (d). Similarly, the {112}B facet will elongate so that the morphology in (e) becomes more common, with twin grooves on the sides. For periodically twinned ZB, (f), the polar {111} family usually dominates the facets although some other types e.g. polar {113} facets are also observed. If the twin period becomes



**Figure 3.2:** Schematic illustrations of (a)-(h) possible nanowire morphologies and crystalline phase transitions, and (i) the nucleus, liquid nano-particle, and nanowire, indicating key parameters.  $\beta$  and  $\theta$  are liquid droplet contact angle and facet inclination angle.  $\gamma_{tv}$ ,  $\gamma_{ts}$ ,  $\gamma_{tn}$ ,  $\gamma_{sv}$ ,  $\gamma_{sn}$  are interfacial energies per unit area of the corresponding interfaces. (k) HRTEM images of intrinsic InAs nanowires growth by the LT (left) and HT (right) growth schemes.

a monolayer, ZB transfers to WZ with only the hexagonal prism geometry composed of non-polar {1100} facets commonly found, (g). In a minority of highly tapered WZ nanowires, the {1120} family can also be found, which is also non-polar with the hexagonal prism geometry.

As discussed, there is a critical nucleus size where  $\Delta G$  reaches its maximum (See equation 3.2). By equating the derivative of  $\Delta G$  with respect to the nucleus size to zero, one can obtain the enthalpy barrier  $\Delta G^*$  for the growth to occur

$$\Delta G_{WZ}^* = \frac{b^2 h \Gamma_{WZ}^2}{2c(\Delta\mu - \frac{\gamma_{sn}}{h})} \text{ or } \Delta G_{ZB}^* = \frac{b^2 h \Gamma_{ZB}^2}{2c\Delta\mu} \quad (3.5)$$

in which  $b$  and  $c$  are geometrical factors of the nucleus.  $\Delta\mu$  and the total change in interfacial energies due to the nucleus formation  $\Gamma$  are given by

$$\Delta\mu = k_B T \ln \frac{C_{In} C_{As}}{C_{In,eq} C_{As,eq}}; \quad (3.6)$$

$$\Gamma = (1-x)\gamma_{In} + x \left[ \frac{\gamma_{sv}}{\cos\theta} + \gamma_{ls} \tan\theta + \gamma_{lv} \tan\theta \left( \frac{\beta \sin^3\beta - \cos^3\beta + 3\cos\beta - 2}{(\cos\beta - 1)^2} \right) \right] \quad (3.7)$$

$C_x$  and  $C_{x,eq}$  in equation 3.6 represent the concentrations of the reactant  $x$  during growth and at equilibrium within the InAs crystal. During growth In is supplied by the Au-In alloy nano-particle, so  $C_{In}$  and  $C_{In,eq}$  refer to the In concentrations in the alloy. As is supplied to the nanowire directly from the vapor phase due to its low solubility in Au, so  $C_{As}$  and  $C_{As,eq}$  refer to the vapor phase As concentrations. Equation 3.7 is an expansion of equation 3.3 and the corresponding  $\theta$  and energy terms are shown in figure 3.1(b). For  $\Delta G_{WZ}^* < \Delta G_{ZB}^*$ ,  $\Gamma_{WZ} < \Gamma_{ZB}$  and  $\Delta\mu \gg \frac{\gamma_{sn}}{h}$  are both required. Thus increasing temperature will promote the WZ growth due to increased  $\Delta\mu$ . The V/III ratio dependence is less straightforward, since the  $C_{In}/C_{In,eq}$  and  $C_{As}/C_{As,eq}$  are not independent for MOVPE growth. The supply of In from the substrate diffusion depends on the As concentration. In fact, a stronger V/III ratio dependence of the WZ/ZB transition is observed, as compared to the T dependence. The key of the transition resides at  $\gamma_{vn}$  which can e.g. change from 36 meV/Å to 56 meV/Å for the 111B facet of ZB, but be unchanged at 46 meV/Å for the 1100 facet of WZ as the As concentration is reduced. This change is probably due to the fact that the polar ZB facets have the lowest energy surface reconstruction under As over-pressure, e.g. the As-trimmer reconstruction, as discussed in chapter 2, whereas the non-polar WZ facets are unlikely reconstructed. Hence reducing V/III ratio can provide an energetic benefit for the WZ formation. Figure 3.2(d) shows the transmission electron microscopy (TEM) images of InAs nanowires grown at 420 °C with a V/III ratio 69 (denoted as LT scheme in the later sections), and under 470 °C with V/III ratio 6 (denoted as HT scheme in the later sections). The molar fraction of AsH<sub>3</sub> was  $1.92 \times 10^{-4}$ , and that of TMIn was  $2.79 \times 10^{-6}$  and  $3.04 \times 10^{-5}$  for the LT and HT scheme, respectively. Nanowires in both pictures show the WZ dominant crystalline phase, however, the HT nanowires exhibit almost no stacking faults, whereas the LT nanowires have at least  $10 \times$  more defects.

The validity of the V/III ratio dependence has to be clarified. Lower V/III ratio giving purer WZ is generally valid for MOVPE where the growth is group III limited because an overpressure of group V precursor is always needed for MOVPE to prevent the group III clustering. If the growth is instead group V limited which is common for MBE due to the high desorption rate of As and the low pressure, the trend can be reversed. The As supply will be dominated more and more by the Au seed adsorption when lowering the V/III ratio, resulting in that the nucleation occurs only inside the seeds instead

of at the TPB, which resembles the case of the 2D nucleation and thus the formation of WZ stacking will lose all the kinetic benefit due to the  $\gamma_{sn}$ . Lower V/III ratio thus leads to purer ZB. The detailed modeling of this case is given in Ref [86].

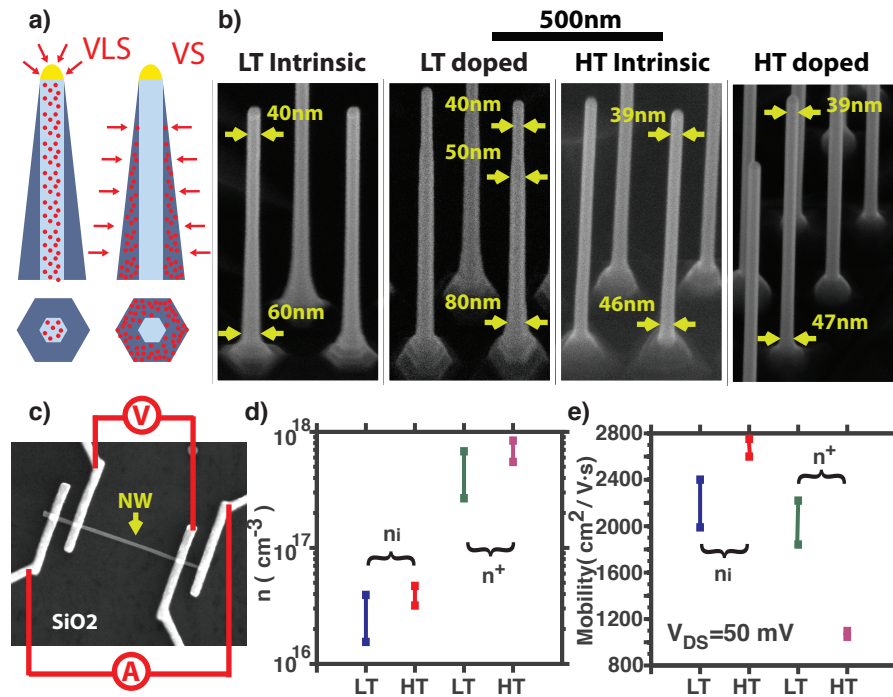
### 3.1.3 IN-SITU DOPING

For MOSFET applications, in-situ doping is necessary in order to reduce the parasitic series resistances. Dopants can be incorporated into the nanowire by two means, figure 3.3(a), either through the vapor-liquid-solid axial growth or through the vapor-solid lateral growth. Many researches have shown that introducing dopants during the nanowire growth will change the growth dynamics dramatically, which can have a strong impact on the nanowire crystal structure and surface quality [87]. Figure 3.3(b) shows the intrinsic and doped nanowires grown by the LT and HT growth schemes, where the molar fractions of TESn were  $1.22 \times 10^{-7}$  and  $3.49 \times 10^{-7}$ , respectively. As can be seen, nanowires grown under the LT scheme show significant overgrowth in the presence of doping, whereas the HT is less affected by doping in terms of the overgrowth.

Carrier concentrations and mobilities were evaluated from four-point transport measurements on the back-gated lateral nanowire FETs [82], (c). After growth, the nanowires, with a diameter of about 40-50 nm, were transferred onto a pre-patterned Si chip with 100 nm of thermally grown SiO<sub>2</sub> serving as the back-gate dielectric. Four electrodes were defined by electron beam lithography (EBL) in polymethyl methacrylate (PMMA), followed by the thermal evaporation and lift-off of Ni/Au. The electrical performance of the fabricated back-gated FETs was then characterized with a standard electrical probe station. The nanowire resistivity,  $\rho_{nw}$ , was evaluated from the four-probe current-voltage (I-V) measurement by  $\rho_{nw} = R \cdot \frac{A}{L}$ , where R, A, and L are measured resistance, nanowire cross-sectional area and nanowire length between electrodes, respectively. The nanowire mobility,  $\mu_n$ , was evaluated from the measured back-gate transconductance,  $g_m$  by

$$\mu_n = g_m \frac{L^2}{V_{ds} C_g} \quad (3.8)$$

in which  $V_{ds}$  is the drain-source bias,  $C_g$  the total gate capacitance evaluated using a finite element model (Comsol Multiphysics) [82]. Finally the effective mobile carrier concentration,  $n$ , was calculated by  $n = \frac{1}{\rho \mu_n}$ . (d) and (e) show evaluated carrier concentrations and maximum mobilities at  $V_{DS}=50$  mV for nanowires in (b). It can be seen that the intrinsic HT nanowires have a slightly higher background doping level, probably resulting from the higher TMI molar fraction causing more carbon incorporation. Meanwhile, the doped



**Figure 3.3:** (a) Schematic illustrations showing two doping mechanisms. (b) SEM images for intrinsic and doped nanowires grown by LT and HT schemes. (c) Fabricated four-probe back-gate lateral nanowire FET used for transport measurements, together with the illustration of how four-probe I-V measurements are performed: in order to remove the influence of the contact resistances, the current is applied between the two outer electrodes, while the voltage drop between the two inner electrodes is measured. (d)-(e) show the extracted mobile carrier concentrations,  $n$ , and mobilities,  $\mu_n$ .

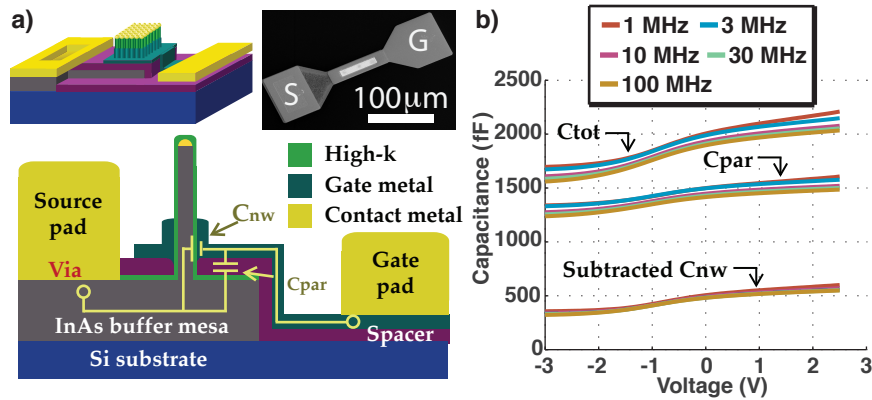
nanowires show a similar doping level for these two schemes. The mobility of the HT intrinsic nanowires is the highest, but it drops significantly when doped.

### 3.2 NANOWIRE MOS CAPACITOR FABRICATION

#### 3.2.1 PARASITIC CAPACITANCE V.S. GATE CAPACITANCE

In this subsection, the challenge of fabricating nanowire MOS capacitors is presented. Nanowire MOS capacitors are essentially nanowire MOSFETs without the drain contact. Figure 3.4(a) shows a MOS capacitor fabricated,





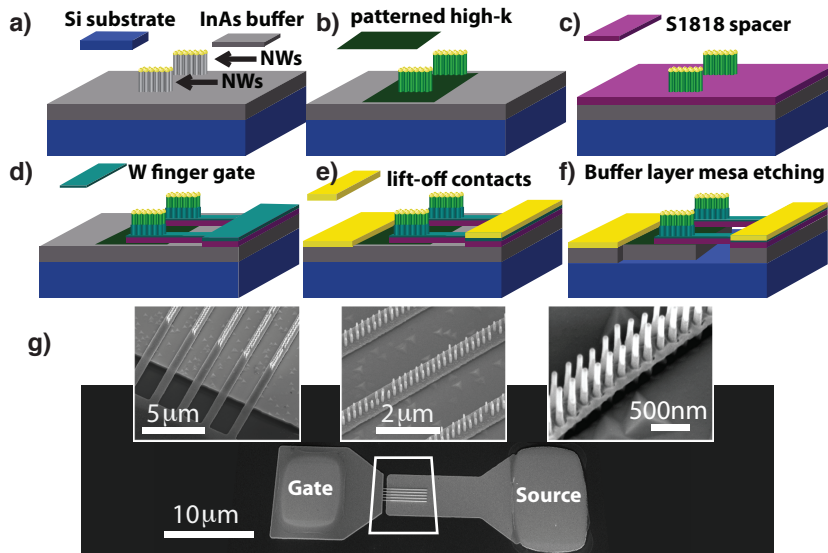
**Figure 3.4:** (a) Schematic illustration and SEM image of vertical nanowire MOS capacitors, fabricated using the conventional vertical nanowire MOSFET fashion. (b) Measured C-V characteristics of the fabricated device,  $C_{tot}$ , and references (without nanowires),  $C_{par}$ . Nanowire MOS capacitances ( $C_{nw}$ ) are then obtained from subtraction.

following the conventional MOSFET fashion. Devices were made along an array of nanowires grown on a doped InAs buffer layer using EBL defined Au seeds. The InAs layer would serve as the source contact. High- $\kappa$  dielectrics were deposited and patterned after nanowire growth. Usually buffer mesas were etched directly after the step with the patterned high- $\kappa$  as the etching mask to isolate the source from the rest of the electrodes. After that, a source-gate spacer layer was deposited and thinned down, followed by the gate metal contact patterning. The gate length was defined by spinning on photoresist and thinning it down to the desired thickness, followed by metal etching on the nanowire side walls. If MOS capacitors were to be made, via holes were opened at some part of the mesa using a shadow mask followed by spacer reactive ion etching (RIE) and high- $\kappa$  wet-etching inside these holes. Finally source/gate probing pads were deposited using a lift-off approach. If MOSFETs were to be made instead, the second spacer layer was defined before the via hole opening, and then followed by the via hole opening, high- $\kappa$  etching together with the high- $\kappa$  on the nanowire side walls protruded out of the second spacer, and top contact patterning including drain and source/gate probing pads. To reduce the series resistance, the spacer layers need to be thin. This causes a large parasitic overlapping capacitance  $C_{par}$  obscuring the nanowire MOS capacitance measurements. Figure 3.4(b) shows the measured C-V curves of MOS capacitors made this way with and without nanowires. The latter was used to quantify the  $C_{par}$ . Nanowire capacitance  $C_{nw}$  was extracted by subtracting the  $C_{par}$  from the measured total capacitance  $C_{tot}$ .

It can be seen that  $C_{par}$  dominates the measured  $C_{tot}$ . The small value of the  $C_{nw}$  obtained by subtracting between two large values thus makes the analysis unreliable. To provide reliable C-V analysis, minimizing  $C_{par}$  is critical.

### 3.2.2 FINGER GATE NANOWIRE MOS CAPACITOR

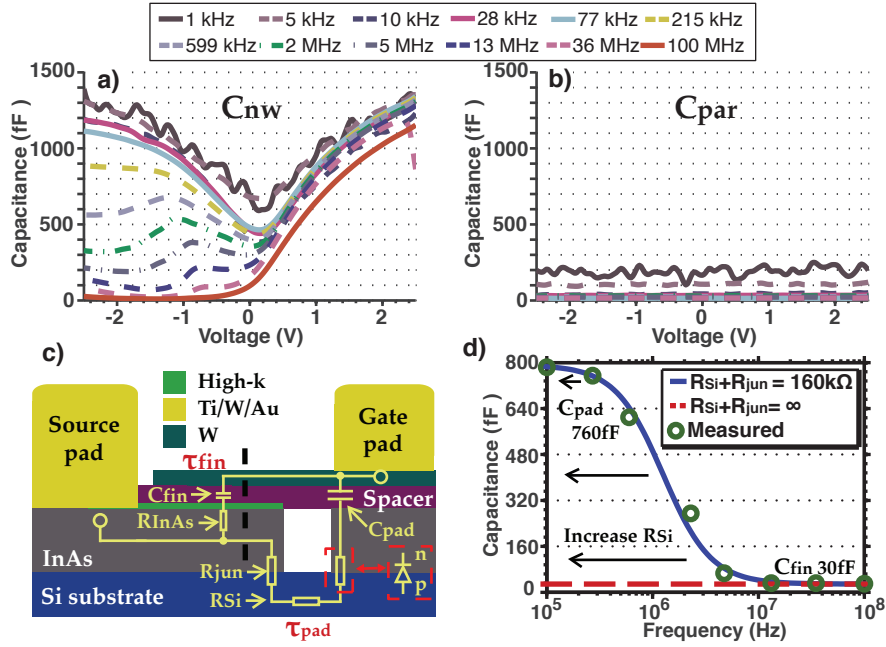
Due to the challenges in device fabrication and characterization, detailed vertical nanowire C-V studies were seldom reported, and although some solutions were proposed, they were basically based on tailoring the device architecture via the use of either comparably thick isolation layers with long nanowires [71] or plasma-enhanced high doping of the entire device region followed by selective etching the nanowire surface [72]. These approaches resulted in a far different semiconductor surface condition before high- $\kappa$  deposition, as compared to the optimal case for transistor applications [18]. In this thesis, a finger-gate technique was adopted to minimize  $C_{par}$  while keeping the optimal MOSFET geometry, as shown in figure 3.5 (a)-(f). Devices were fabricated on a highly resistive Si(111) substrate covered by a 300-nm-thick InAs buffer layer, (a). Au seed particles were deposited using an EBL lift-off process, followed by the InAs nanowire growth by MOVPE with AsH<sub>3</sub> and TMI<sub>n</sub> as precursors, and TESn as the dopant source. After growth, a high- $\kappa$  bilayer dielectric was deposited by ALD with 10 cycles of Al<sub>2</sub>O<sub>3</sub> at 260 °C followed by 50 cycles of HfO<sub>2</sub> at 100 °C. The high- $\kappa$  was patterned afterwards using UV-lithography to serve as the mesa etching mask (b). Then instead of etching the mesa, the wafer was spin-coated by S1818, followed by defining a 100-nm-thick spacer by RIE, (c). A 60-nm-thick W layer was sputtered and subsequently patterned together with the spacer beneath to form the finger-shaped gate contact, (d). To achieve this geometry, PMMA 950A4 resist was exposed by Deep UV lithography and EBL. The former removed the excessive W across the sample, whereas the latter removed the fine areas near the nanowires. After development, the W film together with the spacer beneath was etched by RIE, which resulted in a gate contact consisting of 5 fingers in parallel, each 900 nm wide and about 30  $\mu$ m long. PMMA 950A4 after spin-on gave 300 nm long gate length. Finally, Ti/W/Au pads were deposited and patterned using lift-off onto the gate/source regions, which was followed by buffer-layer mesa etching, (e)-(f). Source and gate pads were isolated after the mesa etching with a part of the gate fingers suspended in air due to the under-etch of InAs. Each MOS capacitor had 1500 nanowires placed in zigzag rows with a pitch of 200 nm. The nanowire diameter was varied from 30 nm to 50 nm across the sample, which resulted in a length variation from 700 nm to 1000 nm. Reference devices without nanowires for subtracting the  $C_{par}$  were also fabricated next to each MOS capacitor. The scanning electron micrographs of one of the fabricated nanowire MOS capacitors are shown in



**Figure 3.5:** (a)-(f) Schematic layout of the vertical wrap-gated nanowire MOS capacitor processing. (g) SEM images of the fabricated nanowire MOS capacitor.

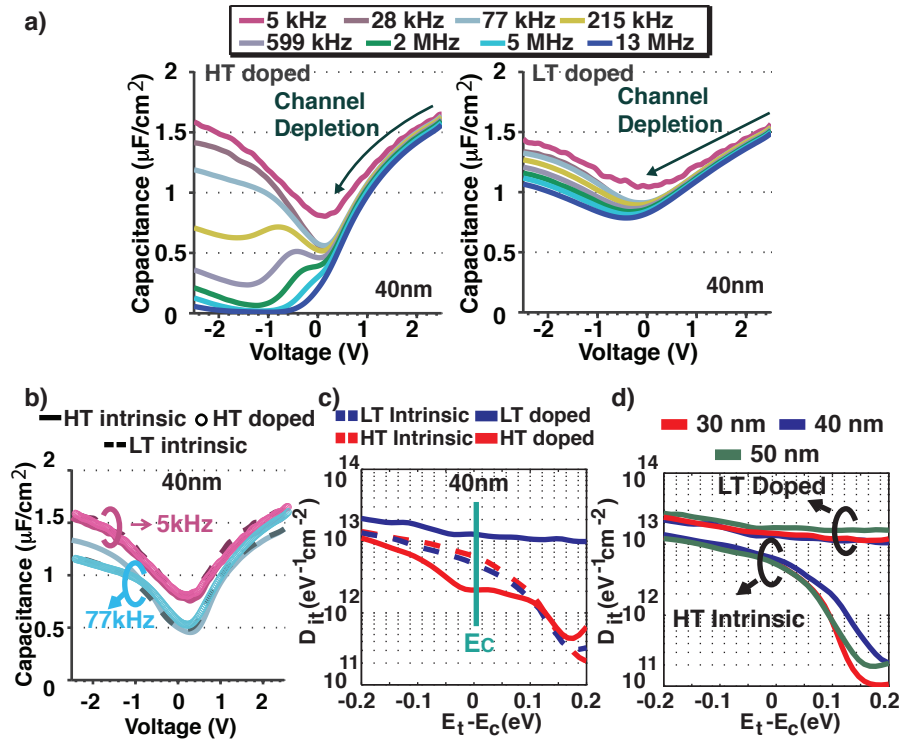
figure 3.5(g).

Figure 3.6(a) and (b) show the subtracted nanowire C-V characteristics and the parasitic C-V characteristics measured from the reference device. As can be seen, by adopting the finger gate approach,  $C_{par}$  is greatly reduced to levels far smaller than the nanowire MOS capacitance  $C_{nw}$ , and more importantly, it does not show any voltage modulation, which is crucial for a reliable MOS C-V analysis. A frequency dependent  $C_{par}$  is observed, and the dependence is well understood by including the leakage resistance through the Si substrate into the parasitic circuit, figure 3.6(c), which consists of two InAs/Si junction resistors,  $R_{jun}$ , in series with the Si substrate resistor,  $R_{Si}$ . The complete parasitic circuit hence consists of two lumped RC branches, the pad and the finger, separated by the black dashed line. At low frequencies, the total  $C_{par}$  is dominated by the pad capacitance  $C_{pad}$ , which is large due to the large pad area. But because of a larger RC time constant,  $\tau_{pad}$ , the charge response through the capacitor diminishes at elevated frequencies, which leaves the small finger capacitance ( $C_{fin}$ ) dominating the high frequency  $C_{par}$ -V characteristics. To test this, a reference device is made on a leaky n-doped Si substrate, following the same processing workflow. The total leakage resistance,  $R_{Si}+R_{jun}$  is measured to be around 160 k $\Omega$ . Using the known device dimensions, the total  $C_{par}$  as a function of the frequency is calculated,



**Figure 3.6:** (a) and (b) are subtracted nanowire C-V characteristics and measured parasitic C-V characteristics. (c) Parasitic circuit including the parasitics both from the pad and from the fingers with RC time constants of  $\tau_{pad}$  and  $\tau_{fin}$ , respectively. (d) Calculated and measured parasitic capacitance as a function of the gate voltage.

as shown by the blue line in figure 3.6(d), which fits the measured data (green circle line) well. As the substrate leakage resistance increases, the transition frequency where  $C_{pad}$  dominates over  $C_{fin}$  decreases. For an ideal insulating Si substrate, one can only see  $C_{fin}$  in measured  $C_{pad}$ , as shown by the red dashed line. In our research, we used a highly p-doped Si substrate to increase the total leakage resistance. This replaced the InAs/Si junction resistor of the pad side by a reverse-biased diode, as shown by the red bracket, hence greatly increasing the resistance across the junction. Although a forward-biased diode was obtained inevitably on the junction of the other side, the voltage drop across that diode was small. Therefore, the total substrate leakage resistance was increased, which could give a  $C_{par}$  below about 200 fF at 1kHz, roughly, as shown in figure 3.6(b).



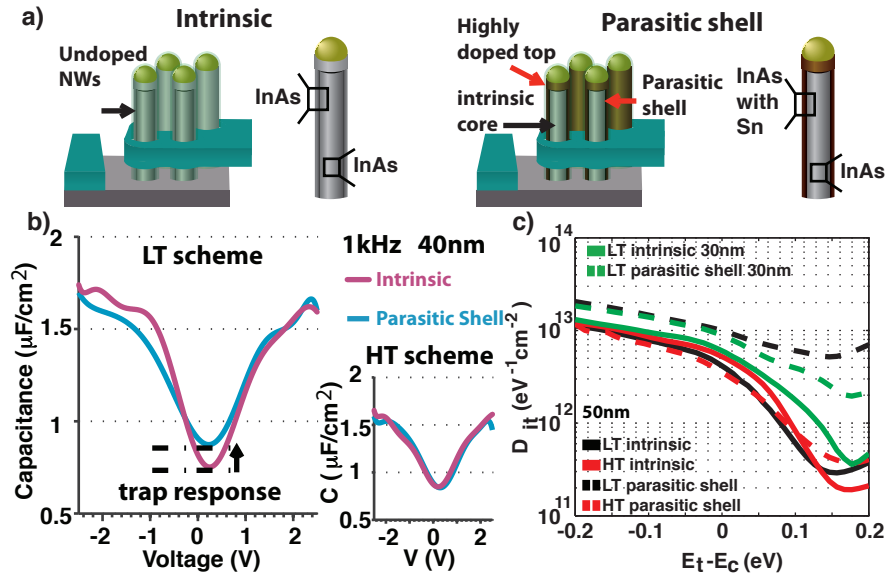
**Figure 3.7:** Comparison of (a) doped 40-nm-diameter nanowire MOS C-V characteristics grown by the HT and LT growth schemes; (b) C-V characteristics between the intrinsic and HT doped nanowire MOS capacitors; (c)  $D_{it}$  profiles for various cases ( $E_c$  denotes the conduction band edge); (d)  $D_{it}$  profiles for nanowires with different diameters (here only the HT intrinsic and LT doped are shown. The trend holds for other cases as well).

### 3.3 TRAP DENSITY PROFILING

Detailed CV studies are performed for the different growth schemes discussed in section 3.1.2 (see figure 3.2(k)) and doping strategies mentioned in section 3.1.3 (see figure 3.3(b)). Our results indicate that the gate stack quality for intrinsic nanowires is independent on the here studied growth schemes. However, introducing doping causes a remarkable difference for nanowires grown under different growth conditions. Figure 3.7(a) shows the comparison of C-V characteristics of doped nanowire grown by HT and LT schemes. The HT doped nanowire MOS capacitor shows far better gate stack performance, manifested by a far more efficient depletion of the channel. Meanwhile, the frequency modulation at negative biases for the case is pronounced. This

could result from the increase in trap response life time (see equation 2.2), or frequency dependent hole response, which means true inversion could be reached, or the series resistances along the nanowire, as discussed in the following section. But all these relies on moving the Fermi level away from the conduction band edge to further deplete the nanowire channel. The LT doped nanowire, on the contrary, show quite similar C-V characteristics as the planar case. Figure 3.7(b) shows the comparison between the intrinsic and HT doped nanowire MOS C-V curves. The C-V modulations are quite similar, which demonstrates that the HT growth scheme is very robust against the doping influence, as compared to the LT scheme.  $D_{it}$  profiles are extracted for various cases, figure 3.7(c), using the low frequency fitting method described in section 2.4.2.  $D_{it} < 10^{12} eV^{-1} cm^{-2}$  is observed near the conduction band edge for intrinsic and HT doped nanowire MOS gate stacks. This is far lower than the planar InAs/high- $\kappa$  gate stack with the same ALD deposition conditions when determined by the same extraction method [49]. The lower  $D_{it}$  value for the nanowire-based device could be due to the non-polar WZ{-1100} facets that have a lower surface energy and a smaller possibility of surface reconstruction [79, 88]. Finally, no diameter dependance of  $D_{it}$  is observed within the diameter range from 30 nm to 50 nm, figure 3.7(d).

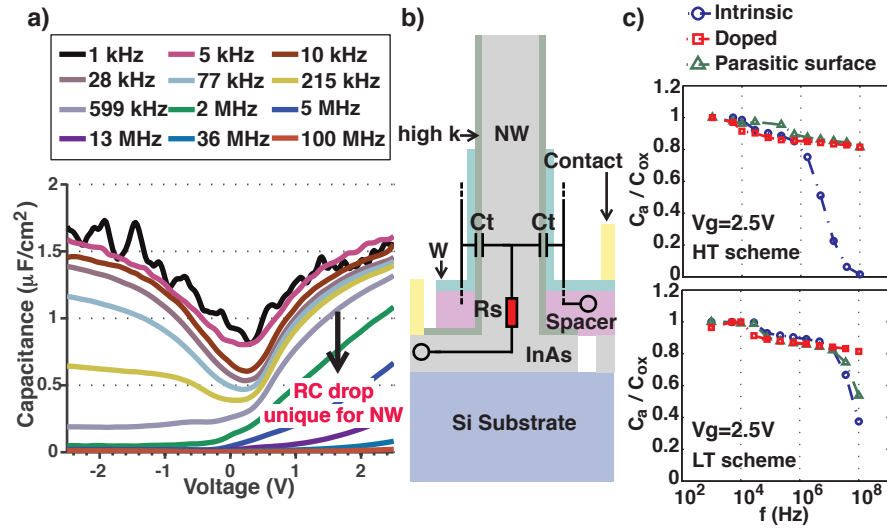
The reason for the reduced doping influence on  $D_{it}$  by using the HT growth scheme is further verified. It could result either from the different TESn environment the nanowire surface is exposed to, or from a more stable surface formed by using the tailored growth scheme. Because a higher TMIn molar fraction is used, the TESn/TMIn ratio during the HT doped nanowire growth is smaller and the growth rate is higher. This indicates that the doped nanowires grown by the HT scheme could be exposed to the TESn environment either for shorter time or with less TESn concentration in the gas flow. To identify the reason, the third set of samples was prepared, in which intrinsic nanowires were grown using the two schemes up to 700-800 nm. Then the TMIn flow was turned off with the chamber purged under  $AsH_3$  for 4 min. Meanwhile, the temperature and TMIn flow rate for both types of samples were set identical to the LT scheme for the later growth, hence ensuring the same TESn environment for the nanowire surfaces. After that TMIn was re-supplied, together with a high TESn flow,  $3.49 \times 10^{-6}$  molar fraction. Only a 50 nm short segment of highly-doped InAs was grown, a segment that was not gated in the final MOS capacitors. The intrinsic channel surface during this process was exposed to the same dopant ambient. A possible doped parasitic shell was formed. No apparent morphology change and diameter increase for this set were observed in neither growth scheme, as compared to their intrinsic counterparts due to the short growth time. Figure 3.8(a) shows the schematic illustrations of this set and the intrinsic case. Comparison of the C-V curves for 40-nm-diameter nanowire capacitors is



**Figure 3.8:** (a) Schematic illustrations of the intrinsic and parasitic shell nanowire MOS capacitors. (b) Comparison of 1 kHz C-V curves of 40-nm-diameter nanowire MOS capacitors with and without the shell grown by two schemes. (c) Comparison of  $D_{it}$  profiles of 50(30)-nm-diameter nanowires with and without the parasitic shell grown by different growth schemes.

shown in (b). A degradation of the interface quality is already visible for the LT scheme with such a short time dopant exposure, whereas that for HT scheme is conserved. Figure 3.8(c) shows the corresponding  $D_{it}$  profiles for other diameter cases, which shows consistent trend with (b). The different degrees of dopant influence for LT and HT growth are thus attributed to the fact that the HT growth scheme results in a better quality of the nanowire surface with reduced amount of ZB stacking faults, and the ZB stacking defects enhance the lateral growth. Thus the improved surface properties of the nanowire core prevent the local dopant incorporation on the surface.

The frequency dependent C-V characteristics of intrinsic nanowire MOS capacitors exhibit an interesting feature, giving clues of the doping mechanism. As shown in figure 3.9(a), the accumulation capacitance for intrinsic nanowire capacitors is reduced significantly above 500 kHz. This is mainly due to the large series resistance ( $R_s$ ) along the nanowire combined with the vertical geometry as shown in (b). Due to the large time constant, charges cannot respond to the input signal at a relatively low frequencies, causing the measured capacitance drops. Hence a larger  $R_s$  results in a lower transition



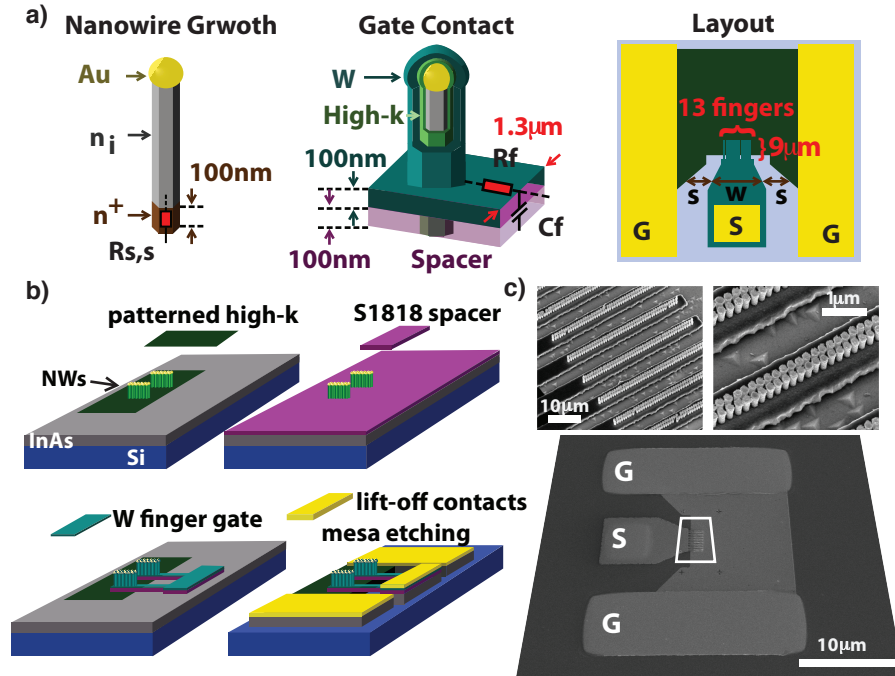
**Figure 3.9:** (a) Frequency dependent intrinsic nanowire MOS capacitor C-V characteristics. (b) Simplified RC model. (c) Normalized accumulation capacitance (at gate bias of 2.5 V) v.s. frequency for various cases.

frequency. The entire nanowire should be modeled by a distributed RC-network, as discussed in section 3.4. Figure 3.9(c) shows the normalized accumulation capacitance v.s. frequency for all cases discussed so far. It can be seen that for LT growth the parasitic shell device shows identical behavior to the fully doped case, whereas that for HT growth is similar to its intrinsic counterpart with a slightly increased transition frequency (lower  $R_s$ ). This implies that the doping incorporation mechanism changes from presumably being surface- to being bulk- dominated when using the tailored growth scheme.

### 3.4 COMPLETE EQUIVALENT CIRCUIT MODEL AND RF C-V CHARACTERISTICS

As discussed in previous section, the series resistance along the nanowire exerts profound influence on high-frequency nanowire MOS C-V characteristics, which indeed should be modeled by a R-C distributed network [90]. This provides room to further dig into the nanowire C-V technique in order for more comprehensive understanding of the vertical GAA nanowire MOSFET. The RF C-V technique, together with a complete small-signal equivalent circuit model ranging from 1 kHz to 67 GHz, is developed in the thesis.





**Figure 3.10:** (a) Schematic illustrations of the RF-compatible nanowire MOS capacitor design. (b) Schematic layout of the processing. (c) SEM images of RF nanowire MOS capacitors.

By fitting the simulated and measured data, nanowire interface trap density and border trap density are extracted separately. Besides, nanowire channel resistivity ( $\rho_{nw}$ ) and gate-length dependent quality factor are also obtained.

### 3.4.1 RF-COMPATIBLE NANOWIRE MOS CAPACITOR DESIGN

For RF C-V characterization, some changes in device design are necessary, figure 3.10(a). To begin with, the nanowire series resistance of the ungated portion,  $R_{s,s}$  needs to be minimized, since  $R_{s,s}$  can conceal the intrinsic nanowire RC network behavior, dominating the transition frequency of the C-f characteristics. This problem was solved by initiating the nanowire growth by a short highly-doped segment ( $\sim 100$  nm) using a TESn molar fraction of  $2.79 \times 10^{-6}$  before the intrinsic nanowire growth, together with an aggressive thinning of the spacer layer thickness ( $\sim 80$  nm in average). Too thin spacer will cause too high leakage current at high biases. Besides, the series resistances along the finger electrodes also need to be minimized. This was addressed by increasing the cross-sectional area of the finger (100

nm thickness  $\times$  1.3  $\mu\text{m}$  width) and by shortening the finger length (10  $\mu\text{m}$ ), in addition to patterning 13 parallel fingers. In this work, nanowires were covered with W entirely by using PMMA 950 A8 as the mask resist which, after spin-on, resulted in a  $\sim 2$   $\mu\text{m}$ -thick layer. Finally, the RF compatible layout using a 50  $\Omega$  coplanar wave guide design was adopted in order to match the high-frequency measurement setup to avoid the power wave reflection. To achieve this, the pad/gap width ratio  $w/s$  was set to 1.5. Except for these changes, the device processing was basically the same as before, figure 3.10(b). A scanning-electron micrograph of the fabricated nanowire capacitor is shown in figure 3.10(c).

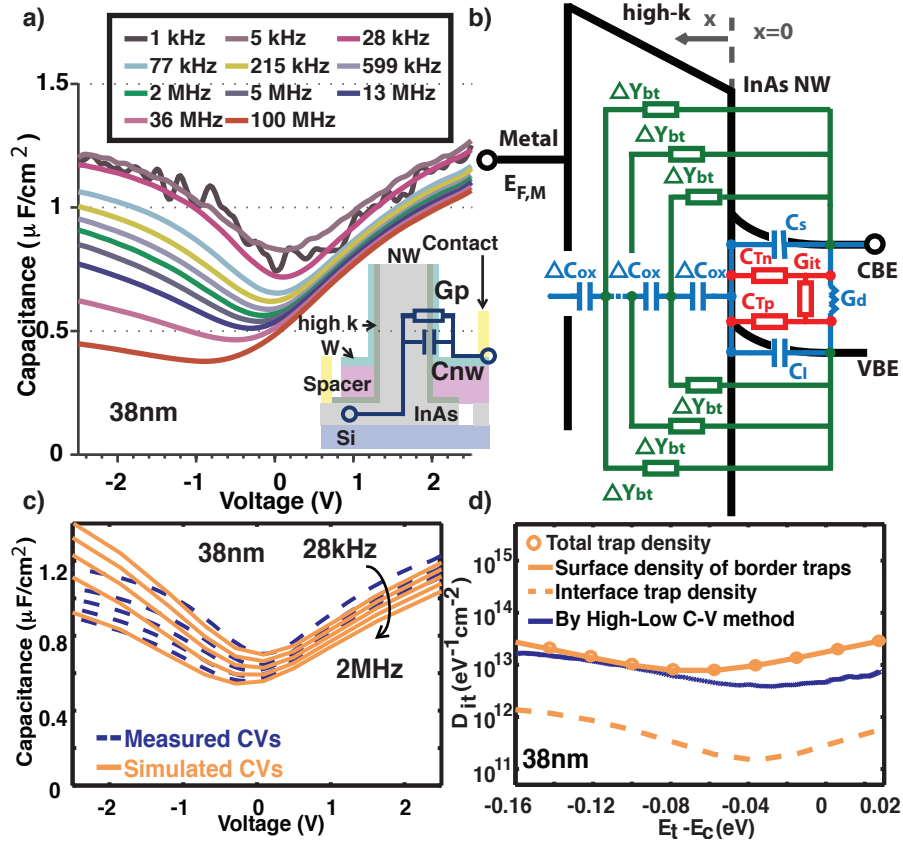
### 3.4.2 LOW FREQUENCY FULL TRAP MODEL

Low frequency C-V characteristics contain all the information about trap state densities of both interface traps,  $D_{it}$ , and border traps,  $N_{bt}$ . Figure 3.11(a) shows the nanowire C-V characteristics measured by an impedance analyzer. The inset indicates the lumped parallel model used to extract nanowire capacitances. To determine  $D_{it}$  and  $N_{bt}$  separately, the lumped parallel model needs to be replaced by a complete low frequency small-signal equivalent circuit [91,92], figure 3.11(b), which simulates the intrinsic semiconductor charge response (blue), interface trap response (red), and the border trap response (green) via the surface band-bending (or  $E_F - E_C$ ) dependent circuit elements. As the gate bias changes,  $E_F - E_C$  at the interface varies. The values of the circuit elements change, from which the trap densities at the energy level,  $E_t$ , coinciding with the  $E_F$  are probed and extracted. In the circuit, components of intrinsic charge response are evaluated by solving Poisson’s equation, as discussed in chapter 2, with the majority carrier response (semiconductor capacitance  $C_s$ ) and minority carrier response (inversion capacitance  $C_I$ ) evaluated separately. The hole generation/recombination through bulk diffusion is also included in the model through a conductor  $G_d$ , and is given by

$$G_d = \frac{q\mu_h n_i^2}{L_d N_d} \quad (3.9)$$

where  $\mu_h$ ,  $n_i$ ,  $L_d$  and  $N_d$  are hole mobility (about 260  $\text{cm}^2/\text{Vs}$ ), hole diffusion length (about 10 nm) and doping level (about  $1 \times 10^{17} \text{cm}^{-3}$ ), respectively. The total oxide capacitance  $C_{ox}$  is adjusted to give the best fit. Following the conventional Shockley-Read-Hall theory [66], the interface trap response is modeled by an electron trap impedance ( $C_{Tn}$ ), a hole trap impedance ( $C_{Tp}$ ) and a generation/recombination impedance ( $G_{it}$ ), which are given by:

$$C_{Tn} = \frac{q^2}{kT} \int \frac{D_{it}(\epsilon) \tau_n^- 1 f_0(\epsilon) (1 - f_0(\epsilon))^2}{[j\omega f_0(\epsilon) (1 - f_0(\epsilon)) + \tau_p^- 1 f_0(\epsilon) + \tau_n^- 1 (1 - f_0(\epsilon))]} d\epsilon \quad (3.10)$$



**Figure 3.11:** (a) Nanowire low-frequency C-V characteristics extracted using a lumped G-C parallel model, as shown in the inset. The nanowire diameter is 38nm. (b) Schematic layout of the full trap small-signal equivalent circuit model, together with an illustration of the band structure (black lines), in which CBE, VBE and  $E_{F,m}$  denote conduction band edge, valence band edge and metal contact Fermi level. (c) Measured and simulated low-frequency C-V curves. (d) Trap density profiles extracted from the fitting.

$$C_{Tp} = \frac{q^2}{kT} \int \frac{D_{it}(\epsilon) \tau_p^{-1} f_0(\epsilon)^2 (1 - f_0(\epsilon))}{[j\omega f_0(\epsilon)(1 - f_0(\epsilon)) + \tau_p^{-1} f_0(\epsilon) + \tau_n^{-1} (1 - f_0(\epsilon))]} d\epsilon \quad (3.11)$$

$$G_{gr} = \frac{q^2}{kT} \int \frac{D_{it}(\epsilon) \tau_n^{-1} \tau_p^{-1} f_0(\epsilon)(1 - f_0(\epsilon))}{[j\omega f_0(\epsilon)(1 - f_0(\epsilon)) + \tau_p^{-1} f_0(\epsilon) + \tau_n^{-1} (1 - f_0(\epsilon))]} d\epsilon, \quad (3.12)$$

where  $f_0$  is the Fermi-Dirac distribution function. The electron/hole trap time constant  $\tau_n/\tau_p$  is related to surface charge concentration  $n_s/p_s$  by an semiclassical interface trap capture cross-section  $\sigma_{0n}/\sigma_{0p}$  via  $\tau_n = (\sigma_{0n}n_s v_{th})^{-1} / \tau_p = (\sigma_{0p}p_s v_{th})^{-1}$ , in which  $v_{th}$  is the thermal velocity.  $\sigma_{0n}$  and  $\sigma_{0p}$  are adjusted to give the best fit. Zeros in these equations denote capture cross-sections at the interface, as indicated in the figure. Finally, the border trap contribution is modeled by elastic tunneling theory [68]. An electron can be trapped by a trap site inside the oxide a distance  $x$  from the interface by tunneling through the potential barrier of the gate dielectric. The capture cross-section of the site at  $x$  can be related to that at interface ( $x=0$ ) via an exponentially decaying function

$$\sigma_{xn}(x, \varepsilon) = \sigma_{0n} e^{-x/\lambda_n} \left( \lambda_n = \frac{\hbar}{\sqrt{8m_e^*(E_C^{OX} - E)}} \right), \quad (3.13)$$

where  $\lambda_n$  is the electron wave attenuation coefficient,  $m_e^*$  is the electron effective mass,  $E$  and  $E_C^{OX}$  are the electron energy and the tunneling barrier which is the energy difference of conduction band edges between the dielectric and semiconductor at the interface. Similarly for holes at the valence band, the tunneling is modeled using hole capture cross-section  $\sigma_{xp}$ , hole wave attenuation coefficient  $\lambda_p$  and hole tunneling barrier  $E_V^{OX}$ . Both  $E_C^{OX}$  and  $E_V^{OX}$  are adjusted to give the best fit. The time constants of the traps at  $x$  away from the interface are thus given by  $\tau_n(x, \varepsilon) = (n_s v_{th,n} \sigma_{xn})^{-1}$  and  $\tau_p(x, \varepsilon) = (p_s v_{th,p} \sigma_{xp})^{-1}$ . At a given measurement angular frequency  $\omega$ , border trap states up to  $x = \lambda n \frac{\omega}{\omega_0}$  can respond the small input signal variation, in which  $\omega_0 = \frac{1}{\tau_0}$  is the frequency when only the border traps at the interface can respond. The change in frequency results in charging and discharging of traps at  $x + \delta x$  around the point  $x$  in response to the small signal. The equivalent capacitance of border traps is thus a function of both  $x$  and energy  $\varepsilon$ , and given by

$$\Delta C_{bt}(x, \varepsilon) = \frac{q}{kT} f_0(\varepsilon)(1 - f_0(\varepsilon)) N_{bt}(x, \varepsilon) \Delta x \Delta \varepsilon \quad (3.14)$$

where  $N_{bt}(x, \varepsilon)$  is the border trap density at  $x$  with energy  $\varepsilon$ . The energy loss of the trapping/de-trapping process can be modeled by an incremental conductance in series with  $\Delta C_{bt}$  through the trap time constant  $\tau(x, \varepsilon)$ . The admittance contributed by the border trap at  $x$  with energy  $\varepsilon$  is thus given by

$$\Delta Y(x, \varepsilon) = \int \int j\omega \Delta C_{bt}(x, \varepsilon) / (1 + j\omega\tau(x, \varepsilon)) \Delta x d\varepsilon. \quad (3.15)$$

As the measurement frequency increase, branches at larger  $x$  drops due to larger trap time constants. As  $\omega = \omega_0$ , only the border traps projected to

**Table 3.1:** Parameters used in the fitting in figure 3.11(c).

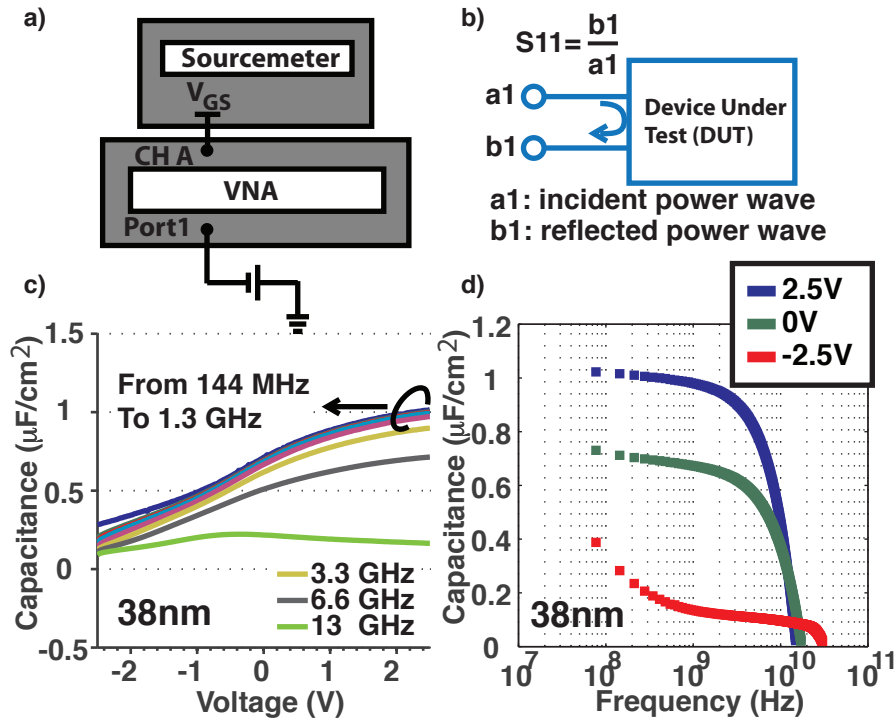
$C_{ox}$ ( $\mu F/cm^2$ )	$N_d$ ( $cm^{-3}$ )	$\sigma_{0n}$ ( $cm^{-2}$ )	$\sigma_{0p}$ ( $cm^{-2}$ )	$E_C^{OX}$ (eV)	$E_V^{OX}$ (eV)
2	$1 \times 10^{17}$	$1 \times 10^{-14}$	$1 \times 10^{-15}$	2.5	2.6

the interface can respond. The impedances of the circuit are numerically calculated to fit the measured impedance data. In the fitting, both  $D_{it}$  and  $N_{bt}$  are assumed to be a superposition of two Gaussian functions, as discussed in chapter 2, with one donor type and one acceptor type, and is extracted when the best fit is obtained.

Figure 3.11(c) shows the comparison of measured and simulated C-V curves from 28 kHz to 2 MHz. The parameters used in the fitting is shown in table 3.1. A relative dielectric constant  $\kappa$  of 14 is obtained, if we assume the oxide thickness is 6 nm (i.e. 1 cycle of ALD give 1 Å oxide). Figure 3.11(d) shows the extracted trap densities, including  $D_{it}$ ,  $N_{bt}$  projected to the interface (within 2 nm from the interface), and the total trap density. As seen, the total trap density is dominated by  $N_{bt}$  that is basically at the similar level as the recently reported planar InAs/high- $\kappa$  gate stacks [91]. And the nanowire MOS capacitor has far lower  $D_{it}$  ( $<10^{-12}$  eV $^{-1}cm^{-2}$  from CBE towards mid gap) than the planar case.  $D_{it}$  extracted here is also far lower than that in Fig 3.7, which is obtained using the low-frequency fitting approach.  $D_{it}$  extracted using the combined high-low frequency C-V method (blue curve) is also shown, which agrees well with the total trap density evaluated using the full trap model. This demonstrates the reliability of the fitting.

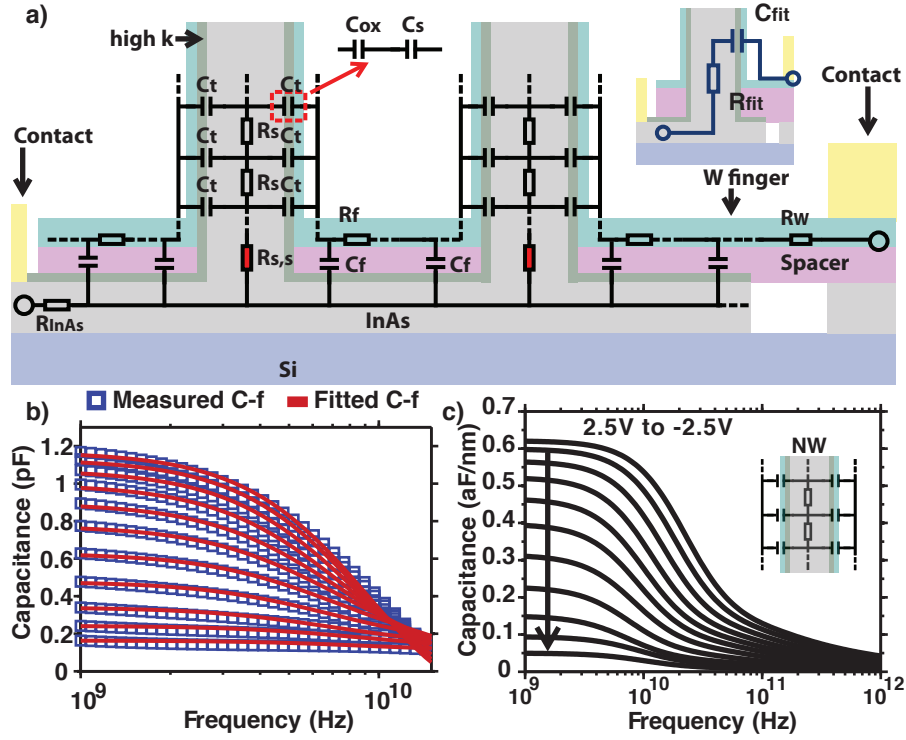
### 3.4.3 RF C-V SMALL SIGNAL MODEL

RF C-V was measured using an Agilent E8361A Vector Network Analyzer (VNA) [93], figure 3.12(a), with the frequency ranged from 10 MHz to 67 GHz. A ground-signal-ground probe with a pitch of 100  $\mu m$  was connected to one VNA port with the DC bias supplied by a Keithley sourcemeter. At each DC bias, S-parameters (only  $S_{11}$  was of interest for the case, figure 3.12(b)) were measured as a function of the frequency, using a small RF power (-27 dBm). S-parameters were used because it is difficult to achieve short and open circuits for high-frequency measurements, which are required to accurately measure voltage and current. Instead S-parameters were measured at the constant impedance of the measurement setup (50  $\Omega$ ), as seen from the device-under-test (DUT). To achieve this, a SOL (short-open-load) calibration was performed first, which set the 50  $\Omega$  reference plane in front of the probe tip. After it, the measurement would not be influenced by impedances in the probe and cable. Deembedding of the parasitic circuit was done by an on-chip



**Figure 3.12:** (a) Schematic illustration of the RF C-V measurement setup. (b) S-parameters.  $a_1$  and  $b_1$  denote the measured incident and measured reflected wave powers. (c) High-frequency nanowire C-V characteristics extracted from the S parameters, using the lumped R-C parallel model in figure 3.11. (d) C-f characteristics at three bias conditions corresponding to accumulation (2.5 V), depletion (0 V) and inversion (-2.5 V).

reference structure. Next to each nanowire capacitor, there was a reference device (the same structure but without nanowires). The measured admittance of DUT,  $y$ , was obtained from measured  $S_{11}$  through  $y = (1 - S_{11}) / (1 + S_{11})$ . After subtracting the  $y$  of the parasitic circuit measured from the reference, the nanowire capacitance was extracted using the lumped parallel model. Figure 3.12(c) shows the nanowire C-V characteristics above 100 MHz. As seen, from 100 MHz to 1.3 GHz, the C-V curves are almost frequency independent, indicating a reduced trap response. Beyond 1.3 GHz, a significant reduction occurs due to the series resistance discussed before. The frequency dependence of  $C_{nw}$  is more clearly shown in figure 3.12(d). At around  $10^9$  Hz, the C-f curves become flat for all three bias conditions, and beyond that a drop reflecting a typical R-C distributed network behavior occurs [94], similar to



**Figure 3.13:** (a) Schematic layout of the high-frequency distributed RC network model of nanowire MOS capacitors. (b) Comparison of the measured and fitted C-f characteristics. (c) Simulated effective C-f characteristics of a single nanowire after subtracting the parasitic circuit.

that in figure 3.9.

The RC distributed network behavior can be used to evaluate nanowire MOS channel resistivity  $\rho_{nw}$  and quality factor  $Q_{nw}$ . The latter is defined by

$$Q_{nw} = \frac{X_{nw}}{R_{nw}} = \frac{1}{\omega C_{nw} R_{nw}}, \quad (3.16)$$

where  $X_{nw}$  and  $R_{nw}$  are the reactive and resistive parts of the capacitor impedance, and is an important figure of merit for circuit design, where a highest possible  $Q_{nw}$  is usually desired. For this purpose, a complete RC model is devised, figure 3.13(a). The high frequency equivalent circuit consists two RC distributed networks. First, each single nanowire is modeled by a distributed RC network, including the intrinsic nanowire capacitances ( $C_t$ ) and the series resistances within the gated channel ( $R_s$ ) as well as the non-gated part ( $R_{s,s}$ ). Besides, each gate finger is also modeled as a distributed

**Table 3.2:** Extracted parasitic circuit elements from the reference sample C-f characteristics

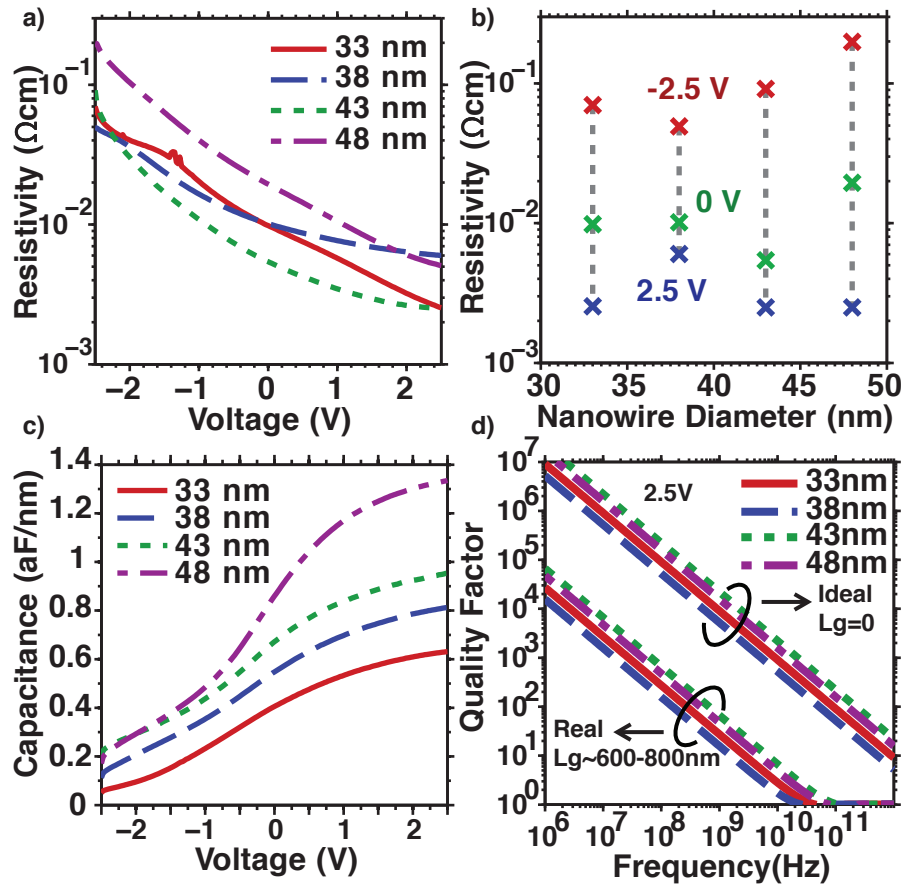
Total $R_f$ / finger	Total $C_f$ / finger	$R_w$ / finger	$R_{InAs}$
3 $\Omega$	70 fF	1 $\Omega$	10 $\Omega$

RC network, consisting of parasitic overlap capacitances ( $C_f$ ) and series resistances along the finger electrode ( $R_f$ ). Further parasitics include the outer series resistances of the gate fingers ( $R_w$ ) and the InAs buffer layer ( $R_{InAs}$ ).  $C_t$  and  $C_f$  are extracted from the C-V measurement data about  $10^9$  Hz, where neither series resistances nor traps influence.  $R_{s,s}$  is obtained from the real part of the measured impedance at the highest frequency where the measured capacitance drops to zero. At zero capacitance the entire gated segment of the nanowire stop responding the input, making the measured impedance only that of the un-gated part.  $R_s$  and  $R_f$  are fitting parameters, and  $R_{InAs}$  and  $R_w$  are estimated, based on previously measured data [18,95]. All of these elements are assumed to be frequency independent and are combined in a circuit model. The equivalent impedance is calculated using transmission line parameters, from which the equivalent capacitances are extracted using a lumped series model, as shown by the inset in figure 3.13(a). A perfect fit between the measured and simulated equivalent capacitances is achieved, figure 3.13(b).

By using reference samples, the parasitic elements in the surrounding structure are extracted, table 3.2. After subtracting these components, C-f characteristics corresponding only to the distributed RC-network inside the nanowire are obtained, figure 3.13(c). As the maximum capacitance is determined at low frequencies, the resistivity can be obtained from the effective capacitance degradation, for each bias point. This method assumes that both the capacitances and the resistances are frequency independent, which is a reasonable assumption in the accumulation and depletion regions. For large negative voltages (inversion region), the effect from the RC-network becomes difficult to distinguish from the intrinsic capacitance modulation. The RC distributed network behavior will be concealed by the minority carrier generation/recombination conductance,  $G_d$  (figure 3.10(b)). In this region, the validity of the model is degraded, as  $C_t$  will become frequency dependent. But since the true inversion is not reached (figure 3.11(d)), as for most InAs/high- $\kappa$  MOS system, the evaluation provided here should be fairly accurate.

The extracted  $\rho_{nw}$  are shown in figure 3.14(a) as a function of the gate bias and in figure 3.14(b) as a function of the nanowire diameter at three bias



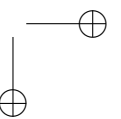
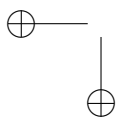
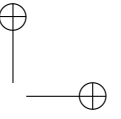
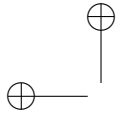


**Figure 3.14:** Nanowire resistivity as a function of (a) the gate bias for various diameters, and (b) the nanowire diameter at three bias points. (c) Intrinsic nanowire high-frequency C-V characteristics after subtracting the influence of series resistances along the nanowire, corresponding only to a unit segment of the nanowire. (d) Diameter dependent quality factors as a function of the frequency extracted at a gate bias of 2.5 V.

points. No diameter dependence of  $\rho_{nw}$  is observed within the studied diameter range. The results obtained using the RF C-V approach are consistent with the previous work [82], in which the  $\rho_{nw}$  was measured using four-probe back-gate DC I-V method (figure 3.3). One benefit of using the RF C-V method is that the determined  $\rho_{nw}$  is more accurate since first there are no high requirements on ohmic contacts, as compared to the I-V approach, and secondly the measurements are done directly on the GAA MOSFET structure.

Due to the use of a GAA geometry, a far better  $\rho_{nw}$  on-/off-state ratio is obtained. The best device shows  $\rho_{nw}$  on-/off-state ratio of  $10^{-2}$  in this work, as compared to the back-gate I-V measurement results [82]. Another benefit of the approach presented here is that the capacitance and resistance are evaluated simultaneously, which provides a way to determine the gate-length dependent vertical nanowire MOSFET quality factors.

By subtracting the series resistances along the nanowire, the high-frequency intrinsic nanowire  $C_t$ -V characteristics, corresponding to an infinitely thin slice of the nanowire, are extracted, figure 3.14(c). The gate-length dependence of the quality factor then is evaluated, figure 3.14(d). By extracting both the intrinsic capacitance and resistance of the nanowire, the quality factor corresponding to the shortest gate length possible can be calculated (the ideal case). Compared to the fabricated nanowire capacitors with gate length of 600-800 nm, it shows a clear improvement in performance by scaling down the device gate length due to the reduced series resistance. As can be seen, it is possible for devices with short gate lengths to achieve quality factors exceeding 100 at 60 GHz, which may be compared with conventional thin-gate oxide MOS varactors with a quality factor of about 20 at 20 GHz [96]. The quality factors evaluated here are in good agreement with the simulation data presented in [90].



# 4

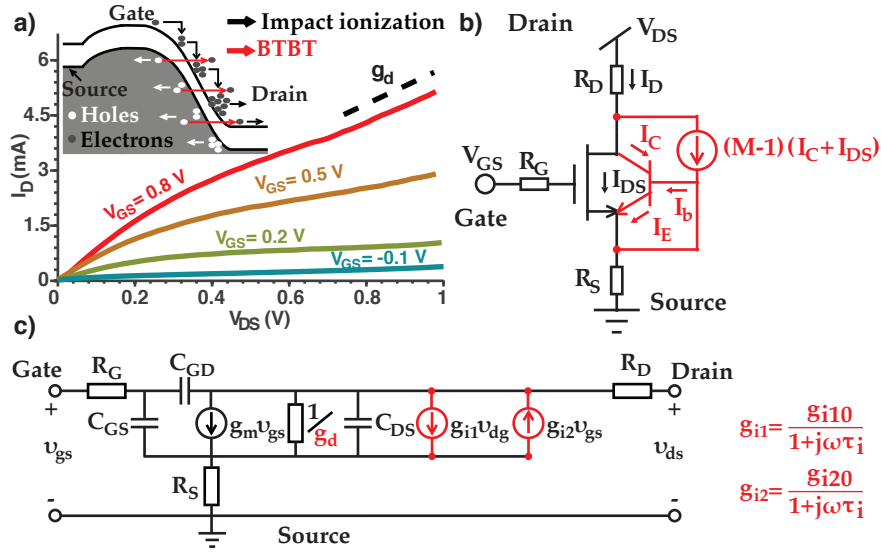
## Asymmetric InAs/InGaAs Vertical Nanowire MOSFETs

**N**ARROW band gap InAs nanowires are attracting increasing interest for high speed electronics due to the high electron mobility and injection velocity of InAs [20,97], in addition to the improved electrostatic control by using the GAA geometry. However, the use of narrow band gap material results inevitably in large impact-ionization and band-to-band (BTBT) tunneling at relatively lower biases [42], which also leads to a low breakdown voltage [44]. These effects greatly limit the device performance. Currently, vertical GAA InAs nanowire MOSFETs are all facing this challenge [98,99].

In this chapter, we analyze the problem and put forth a solution in realizing high mobility vertical nanowire MOSFETs with low impact-ionization and BTBT tunneling via the use of an asymmetric InAs/InGaAs transistor design. The relaxation of the lattice-mismatch induced strain for nanowire epitaxial growth provide us with more freedom in band engineering and transistor design.

### 4.1 IMPACT-IONIZATION AND BAND-TO-BAND TUNNELING FOR InAs NANOWIRE MOSFETS

To begin with, a qualitative discussion of the impact ionization and BTBT influence on device and IC performance is necessary. Figure 4.1(a) shows the measured common-source output characteristics of a n-type InAs/high- $\kappa$  vertical nanowire MOSFET, fabricated following the approach in Ref [18]. For  $V_{DS}$  beyond 0.6 V, the drain current,  $I_D$ , does not saturate as for an ideal MOSFET in the on-state, resulting in a finite output conductance  $g_d = \frac{I_D}{V_{DS}}$ . This can be an indication that BTBT and impact ionization begin to dominate.



**Figure 4.1:** (a) Output characteristics of a vertical GAA InAs/high- $\kappa$  nanowire MOSFET at various  $V_{GS}$ . The inset shows the schematic illustration of the MOSFET band diagram with impact ionization and BTBT. MOSFET DC model (b) and small signal AC model (c), which include the BTBT and impact ionization effects (labeled by red color). For DC performance (b), a parasitic equivalent npn bipolar transistor is added.  $M$  is the multiplication factor of the npn bipolar transistor. In the small signal AC model (c), two additional current sources with frequency dependent transconductances of  $g_{i1}$  and  $g_{i2}$  are included.  $g_{i1}$  and  $g_{i2}$  are related to their DC values ( $g_{i10}$  and  $g_{i20}$ ) through an impact ionization time constant  $\tau_i$ .

In fact, a n-type MOSFET inherently has a parasitic equivalent npn bipolar transistor associated with it, as depicted in figure 4.1(a). This can be seen from its band diagram, as shown in the inset in the figure. The influence can be modeled through the multiplication factor  $M$  of the bipolar transistor that can be evaluated using the Miller formula [100].  $M$  initially increases slowly with the drain voltage but rapidly at the junction avalanche breakdown point. The narrow band gap material usually has a higher ionization rate, hence larger  $M$ , due to the ease in generating electron/hole pairs as a high energy electron is traveling through the drain-gate junction. For digital applications, impact ionization and BTBT cause degraded off-state performance, including increased sub threshold slope, off-current, and drain induced barrier lowering [101]. This in turn raises the power dissipation (essential for very-large-scale integration (VLSI)) and also limits the on-current for a given off-

current (essential for the speed of digital ICs). For analog and RF applications, the requirement for off-state performance is less strict. Figures of merit such as low-frequency open-circuit voltage gain  $A_{V,OC}$ , cut-off frequency  $f_t$  and maximum oscillation frequency  $f_{max}$  are instead of crucial importance.  $f_t$  and  $f_{max}$  are defined as the frequencies at which the current gain  $h_{21}$  and the unilateral power gain  $U$  (the power gain when any feedback path for the power is neglected) reaches unity (0 dB). Figure 4.1(c) shows the MOSFET small signal equivalent circuit. The influence of impact ionization and BTBT can be modeled by two current sources with frequency dependent transconductances of  $g_{i1}$  and  $g_{i2}$  [42].  $g_{i1}$  and  $g_{i2}$  are related to their DC values ( $g_{i10}$  and  $g_{i20}$ ) through an impact ionization time constant  $\tau_i$ . Due to the finite generation rate of these processes,  $\tau_i$  is large and the influence of the two current sources can be neglected at high frequencies. BTBT and impact ionization have a stronger influence on  $g_d$  which is increased for high  $V_{DS}$  (figure 4.1(a)). The analytical expressions of  $A_{V,OC}$ ,  $f_t$  and  $f_{max}$  can be derived as:

$$A_{V,OC} = g_m / g_d, \quad (4.1)$$

$$\frac{1}{2\pi f_T} = \frac{C_{GS} + C_{GD}}{g_m} + \frac{(C_{GS} + C_{GD})(R_S + R_D)g_d}{g_m} + (R_S + R_D)C_{GD}, \quad (4.2)$$

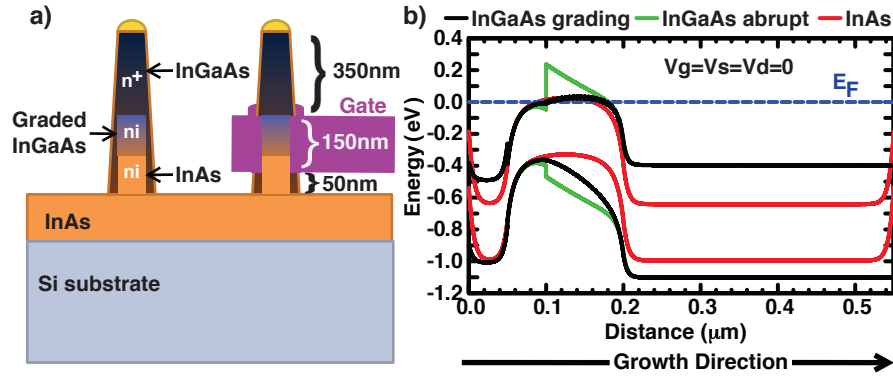
and

$$f_{max} = \frac{1}{2} \sqrt{\frac{f_T}{2\pi C_{GD}(R_S + R_G) + \frac{g_d(R_S + R_G)}{f_T}}}, \quad (4.3)$$

where R and C represent resistance and capacitance with subscripts S, D and G for source, drain and gate, respectively. As can be seen, increased  $g_d$  causes reduced gain and maximum working frequencies, which has also been demonstrated by Mo. et al. [41] where the complete circuit simulation was performed. Finally impact ionization and BTBT result in a reduced breakdown voltage,  $V_{BD}$ . An empirical relation between the semiconductor band gap  $E_g$  and  $V_{BD}$  of the abrupt p-n junction is given in Ref [44] as

$$V_{BD} = 60 \left( \frac{E_g}{1.1} \right)^{3/2} \left( \frac{N_B}{10^{16}} \right), \quad (4.4)$$

where  $N_B$  is the bulk doping level. This significantly constrains the use of narrow band gap InAs based devices for high power applications.



**Figure 4.2:** (a) Schematic illustration of the asymmetric InAs/InGaAs nanowire MOSFET design. The InAs buffer layer and the nanowire top segment are used as the source and drain regions. (b) Band structure along the proposed nanowire MOSFET in (a) (black), in comparison with the band structures of the InAs nanowire MOSFET with the same doping (red) and the same InAs/InGaAs MOSFETs but with an abrupt junction instead of a graded junction (green). In the simulation, the doping levels equal to  $10 \times 10^{16} \text{ cm}^{-3}$  and  $10 \times 10^{19} \text{ cm}^{-3}$  for the intrinsic and highly doped segments are used.

## 4.2 ASYMMETRIC InAs/InGaAs VERTICAL NANOWIRE MOSFET DESIGN

Since impact-ionization and BTBT tunneling usually only occur at the gate-drain junction where the electric field is larger than elsewhere, increasing the band gap at the junction is beneficial. Meanwhile it is preferable to keep a InAs channel for high injection velocity. In the thesis, we propose an asymmetric InAs/InGaAs vertical nanowire MOSFET design, figure 4.2(a). An intrinsic InAs nanowire segment (100 nm) is grown first, followed by intrinsic InGaAs (100 nm) in which the Ga concentration in the nanowire is graded from 0 to 0.4. After that, a highly doped  $\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$  segment (about 350 nm) is grown. The growth condition for the top segment is adjusted to enhance a shell overgrowth, covering the entire nanowire. The purple bar indicates how the gate contact is placed with respect to the nanowire, and before sputtering the gate metal, the highly doped shell in the gate region is selectively etched, leaving an intrinsic channel for better gate electrostatic control. The highly doped shell below the gate region serves as a socket to reduce the series resistance [102]. Detailed processing is given in the following section.

Figure 4.2(b) shows the simulated band structure for the proposed nanowire MOSFET (black). In comparison, the band structures of the InAs nanowire MOSFET with the same doping strategy is also shown (red). As

can be seen, by using the InGaAs segment, the band gap at the the gate-drain junction (at about  $0.2 \mu\text{m}$ ) is increased. In this design, the use of grading is necessary, since an abrupt change from the intrinsic InAs to the intrinsic InGaAs will cause a barrier in the conduction band (figure 4.2(b), green line), which will greatly reduce the on-state current.

### 4.3 Ga INCORPORATION CONTROL IN InGaAs NANOWIRES

To control the Ga concentration in InGaAs nanowires, high resolution X-ray diffraction (HRXRD) was used for ex-situ monitoring the growth. The InGaAs nanowires, in this work, were grown on InAs (111)B substrates using aerosol-deposited Au nano-particles as seeds.  $\text{AsH}_3$ , TMIIn and TMGa were used as precursors. A 60-nm-long InAs segment was first grown, followed by the several-micron-long InGaAs nanowire growth. The total molar fraction of group III and group V materials were constant,  $\chi_{[\text{TMGa}+\text{TMIIn}]}=3.04 \times 10^{-5}$  and  $\chi_{[\text{AsH}_3]}=3.84 \times 10^{-4}$ , resulting in a V/III ratio of 12.55, and the growth temperature was  $450^\circ\text{C}$ . The solid concentration of Ga in the InGaAs nanowires,  $x$ , was controlled by varying the vapor phase concentration of TMGa,  $x_V=\chi_{\text{TMGa}}/\chi_{[\text{TMGa}+\text{TMIIn}]}$ . More details of the growth can be found in paper VI.

#### 4.3.1 HIGH RESOLUTION X-RAY DIFFRACTION OFF NANOWIRES

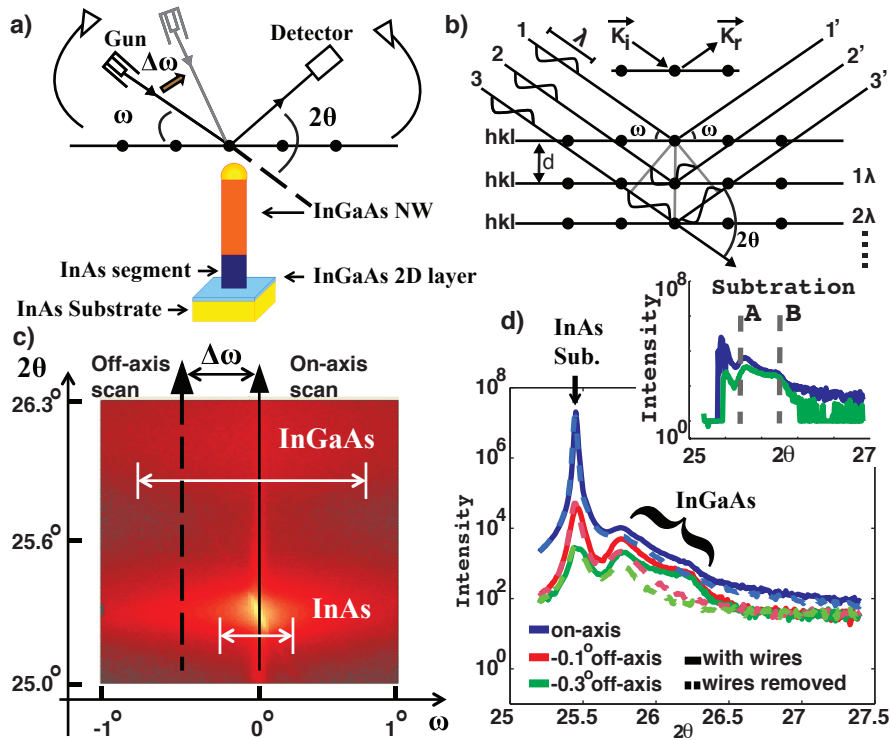
Figure 4.3(a) shows the HRXRD  $2\theta$ - $\omega$  scan along the InAs(111)-reflection used to characterize the Ga solid phase concentration,  $x$ , in the nanowires. X-rays are irradiated onto the sample with an incident angle of  $\omega$ , and the reflected x-ray is collected at an angle of  $2\theta$  with respect to the incident beam path. When scanning  $\omega$ ,  $2\theta$  is also changed, as indicated by the arrows in the figure. For conventional scans, no offset of the incident angle,  $\Delta\omega$ , is added, and thus  $\theta=\omega$  always holds, which allows the constructive interference to occur at some certain  $\theta$  (Bragg angle), as long as the Bragg diffraction condition

$$n\lambda = 2d \sin(\theta) \quad (4.5)$$

is valid, in which  $\lambda$ ,  $n$  and  $d$  are the x-ray wave number, an integer and the lattice constant of measured crystal along the reflection direction, respectively. An amplified signal is detected in the spectrum at these Bragg angles, from which the lattice constant of the  $\text{In}_{(1-x)}\text{Ga}_x\text{As}$  crystal,  $d_{\text{In}_{(1-x)}\text{Ga}_x\text{As}}$ , can be evaluated. With known lattice constants of pure WZ InAs and GaAs [84,103],  $x$  can be determined by using Vegard’s law:

$$d_{\text{In}_{1-x}\text{Ga}_x\text{As}} = (1-x)d_{\text{InAs}} + xd_{\text{GaAs}}. \quad (4.6)$$





**Figure 4.3:** (a) Schematic illustration of the HRXRD  $2\theta$ - $\omega$  scan. (b) Constructive interference at a Bragg angle. (c) Spectral mapping around the InAs(111)-reflection of an InGaAs nanowire sample. (d)  $2\theta$ - $\omega$  scan of (c) with  $0^\circ$ ,  $-0.1^\circ$  and  $-0.3^\circ$  incident angle offsets. The dashed curves are the background spectra, measured after removing the nanowires by ultrasonication. The inset shows the subtraction of the background signals (dashed) from the measured total signals (solid), which contains only the information of the nanowires.

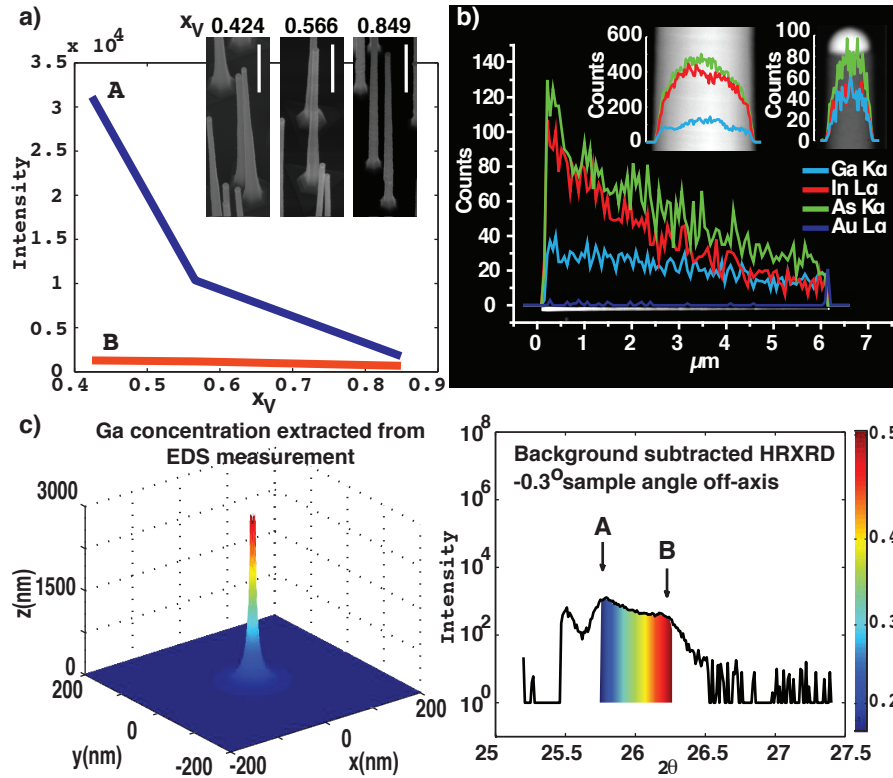
One challenge to characterize nanowires using the technique is the multiple structures present in the sample. As can be seen in (a), the collected signal during  $2\theta$ - $\omega$  scans contains reflections from the InAs substrate, the InGaAs 2D growth layer and InGaAs nanowires. Figure 4.3(c) shows a mapping around the InAs(111)-reflection of an InGaAs sample, which is obtained by measuring the rocking curve (sweeping  $\omega$ ) at each fixed  $2\theta$  (y-axis). The InAs substrate peak at  $25.4^\circ$  has the highest intensity. The shoulder between  $25.8^\circ$  and  $26.3^\circ$  is from InGaAs, which consists of both the 2D layer reflection and the nanowire reflection. To distinguish them, we utilize the fact that for nanowires that have small dimensions, the diffraction peak exhibits an in-plane broadening in  $\omega$ . Thus if a small incident angle offset  $\Delta\omega$  is added to the  $2\theta$ - $\omega$

scan, as shown in (a), the diffraction peak will decrease less for nanowires, as compared to planar layer [104]. The black arrows in the mapping indicate the direction for the conventional  $2\theta$ - $\omega$  scans, and measured spectra are shown in figure 4.2(d). It can be seen that the InGaAs shoulder decreases dramatically at the left end, which can indicate the proportion of spectrum comes from the 2D layer. This conclusion is further supported by measuring the same sample after removing the nanowires using ultrasonication (dashed). As can be seen, the peak to the left end does not disappear, which can thus be attributed to the planar layer.

After subtracting the 2D layer spectra, the remaining spectra are shown in the inset in figure 4.3(d), which contains only the information from the nanowires. In this work, this remaining shoulder is verified to result from a Ga concentration gradient along the nanowire, evolved during the growth. Figure 4.4(a) shows the intensities of the left and right ends of the InGaAs shoulder as a function of the  $x_V$ , as well as the nanowire SEM images. When increasing  $x_V$ , only the left end of the InGaAs shoulder decreases, accompanied by a reduced overgrowth at the nanowire bottom segment. This indicates that the remaining shoulder in figure 4.3(d) is in fact a result of overlapping peaks coming from different segments along the nanowire with the left side (lower Ga concentration) corresponding to the bottom of the nanowires and the right to the top. This Ga concentration gradient is clearly shown by the energy dispersive x-ray spectroscopy (EDS) measurement, figure 4.4(b). It can be seen that the Ga concentration gradient originates from the enhanced In incorporation at the bottom of the nanowire. In contrast, the incorporation of Ga along the nanowire is fairly constant. Lateral EDS scans (inset) indicate an In-rich shell formed at the bottom of the nanowire. Finally,  $x$  is extracted both from the EDS measurement and from the HRXRD spectrum, figure 4.4 (c). It can be seen the evaluated  $x$  using two approaches are in good agreement. Thus it is possible to use HRXRD to provide a spatial-resolved chemical concentration evaluation along vertical grown ternary nanowires.

### 4.3.2 InGaAs NANOWIRE GROWTH MODEL

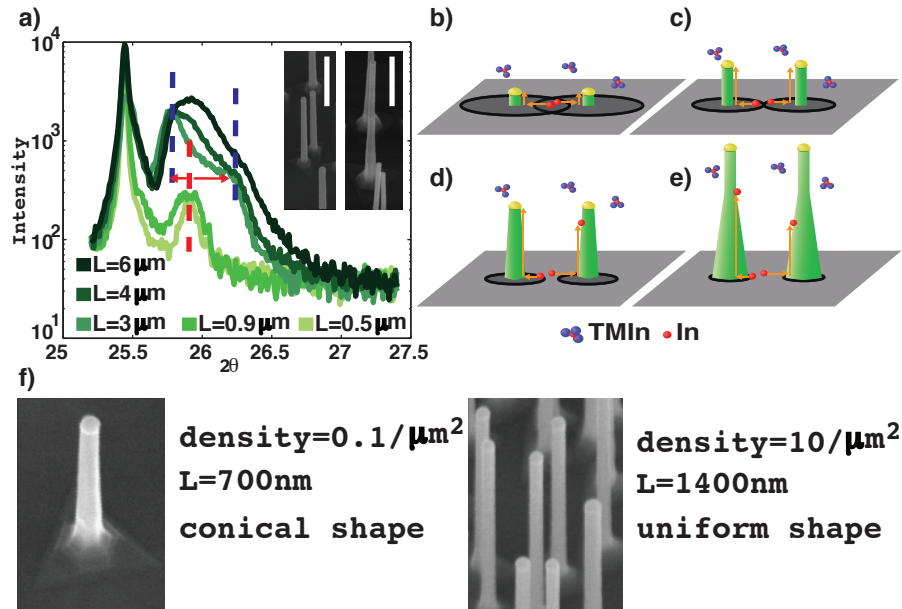
Further studies on the HRXRD spectrum evolution for nanowires grown with different times can be explained by an In-atom diffusion dependent growth model. Figure 4.5(a) shows the HRXRD spectra for nanowires with length from 500 nm to 6  $\mu\text{m}$ , as well as the SEM images of the 900 nm and 3  $\mu\text{m}$  nanowires. As can be seen, the HRXRD show a single peak for nanowires below 1  $\mu\text{m}$ , indicating a uniform chemical composition along the nanowires, which is consistent with the untapered nanowire morphology in SEM. Above 1  $\mu\text{m}$ , the peak starts evolving in a shoulder with two ends separated towards higher (right end) and lower (left end) angles. As discussed, this corresponds



**Figure 4.4:** (a) Variation of the HRXRD intensities at two ends of the InGaAs shoulder (the inset in figure 4.3(d)) with  $x_V$ . The inset shows the corresponding SEM images of InGaAs nanowires with increased  $x_V$ . The scale bar in the SEM images denote 500 nm. (b) Axial EDS line-scan imaged in STEM mode of In, Ga, As and Au along a 6- $\mu\text{m}$ -long nanowire. The inset shows the radial EDS line-scans at the bottom and the top of the nanowire. (c) Ga concentration distribution along a 3- $\mu\text{m}$ -long nanowire, extracted from the axial EDS line-scan and from the HRXRD spectrum using Vegard's law.

to a Ga concentration gradient. A tapered morphology is also observed beyond this length. After about 3  $\mu\text{m}$ , the position of the right end of the shoulder does not change, which indicates that the chemical composition of the upper segments of the nanowires will hardly be influenced by the growth time anymore.

This evolution can be explained by figure 4.5[(b)-(e)]. During the growth, nanowires collect material by three mechanisms [77, 105]: reactants directly impinging on the Au particles (1); reactants adsorbed on the substrate (2)



**Figure 4.5:** (a) Evaluation of the HRXRD spectrum for samples grown for different times. The arrow bars in the SEM images denote 500 nm. (b)-(e) A simplified model of InGaAs nanowire tapering formation and composition gradient evolution. (f) InGaAs nanowires grown on samples with Au particle densities of  $0.1/\mu\text{m}^2$  and  $10/\mu\text{m}^2$ .

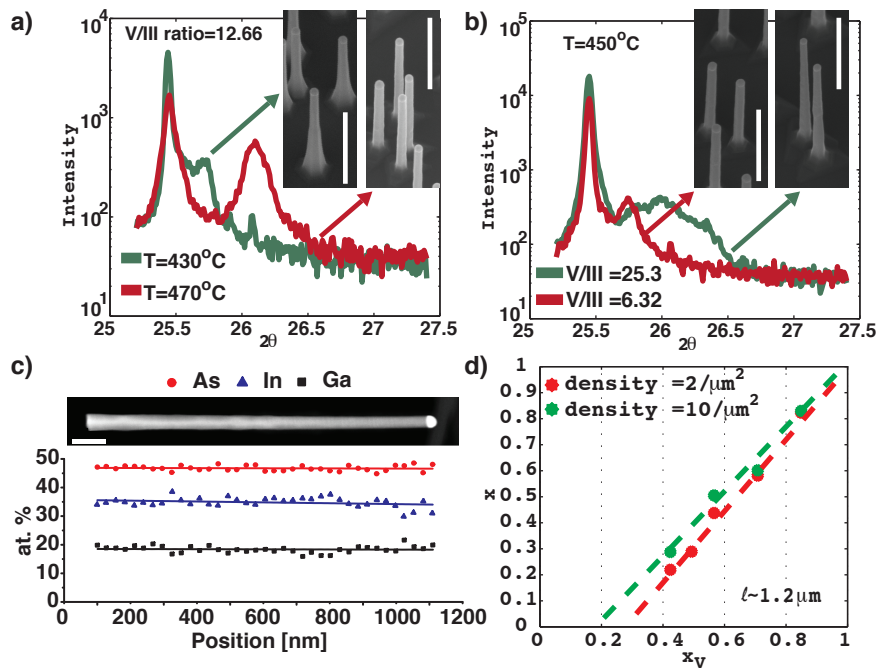
and on the nanowire sidewalls (3), and then diffusing along the nanowires. The mechanism 1 is less important here, since this flux does not change as the nanowires are growing, hence not impacting the concentration gradient. The mechanism 3 can also be omitted according to the simulation work done by Ye et al. [105] who showed that with and without the nanowire sidewall adsorption and diffusion, the difference of Ga concentrations between the bottom and the top of the nanowire is below 0.1 and about 0.3, respectively, after the nanowire grows for several  $\mu\text{m}$ . A 0.3 difference agrees well with our experimental results, which indicates that mechanism 3 only has trivial contribution. Also omitted in the model is the Ga atom diffusion from the substrate and the temperature-dependent TMGa pyrolysis [106]. As can be seen in figure 4.4(b), the Ga incorporation along the nanowire is quite constant and the tapering is mainly caused by the overgrowth of a In-rich shell for long nanowires. The lower supply of Ga from the substrate could be due to the relatively small diffusion length of Ga atoms and the incomplete TMGa decomposition. As shown in the figure, the growth behavior can be explained

through an effective In-atom vapor-liquid-solid (VLS) diffusion length, which is the maximum possible distance for In atoms to diffuse to the Au particle-nanowire interfaces, hence contributing to the VLS axial growth. On substrate, it corresponds to an effective collection area, and when nanowires grow longer, this area will shrink. Below  $1 \mu\text{m}$ , the collection areas between every two adjacent Au particles are overlapping, if the Au particle density is high enough. All decomposed In atoms impinging between Au particles can either reach the triple-phase-boundary and contribute to the axial growth or be desorbed. No compositional gradient and In-rich tapering form during the growth. As the nanowires grow longer, the collection areas shrink and collection areas between two neighboring particles are no longer overlapping. The gradient and tapering then begin to evolve, since the In atoms fall outside the areas cannot reach at the Au particle, but are likely to incorporate into the nanowire sidewall. As the nanowire length further increases, the collection area finally equals to the nanowire foot print area. After that, all the In atoms collected from the substrate cannot reach the Au particle and can only contribute to radial overgrowth. This is in agreement with that the HRXRD InGaAs shoulder do not shift after  $3 \mu\text{m}$ .

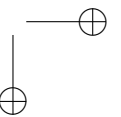
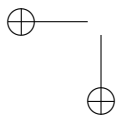
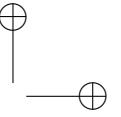
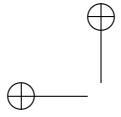
According to the model, increasing the Au seed density will increase the amount of collection area overlap, hence increasing the achievable maximum length of InGaAs nanowires with uniform chemical composition and morphology. This is verified and shown in figure 4.5(f) with lower Au seed density samples giving more tapered growth even at the shorter nanowire length.

### 4.3.3 NANOWIRE MORPHOLOGY AND Ga CONCENTRATION CONTROL

Varying the density to achieve uniform, long enough InGaAs nanowires is somehow less flexible. However, the growth model in figure 4.5 also indicates that an increased In diffusion length can also result in longer uniform InGaAs nanowires, and this can be accomplished by increasing the growth temperature and reducing the V/III ratio, as discussed in chapter 3 section 3.1.2. In this work, the V/III ratio is varied by changing the  $\chi_{[\text{AsH}_3]}$ . Figure 4.6(a) shows the results, which demonstrate that a better compositional and morphological uniformity is obtained by using the high temperature, low V/III ratio growth scheme. Figure 4.6(b) shows the atomic percentage extracted from the EDS measurement along a  $1.2\text{-}\mu\text{m}$ -long InGaAs nanowire grown at  $470^\circ\text{C}$  and V/III ratio 6. As can be seen, the chemical composition is constant along the entire nanowire. Finally, by using the HRXRD technique, the Ga solid concentration,  $x$ , as a function of the TMGa vapor composition,  $x_V$  can be determined, figure 4.6(d).



**Figure 4.6:** (a)-(b) Comparison of the HRXRD spectra, together with the SEM images, of samples grown at different temperature and V/III ratio. The scale bars in the SEM images denote 500 nm.  $x_V$  used is 0.566. (c) Atomic percentages of In, Ga, and As, extracted from the EDS line-scan, along a nanowire grown at  $470^\circ\text{C}$  and V/III ratio 6, together with the HRTEM images. The arrow bar denotes 100 nm. (d)  $x$  v.s.  $x_V$  for different nanowire densities. The growth conditions used are the same as in (c).



# 5

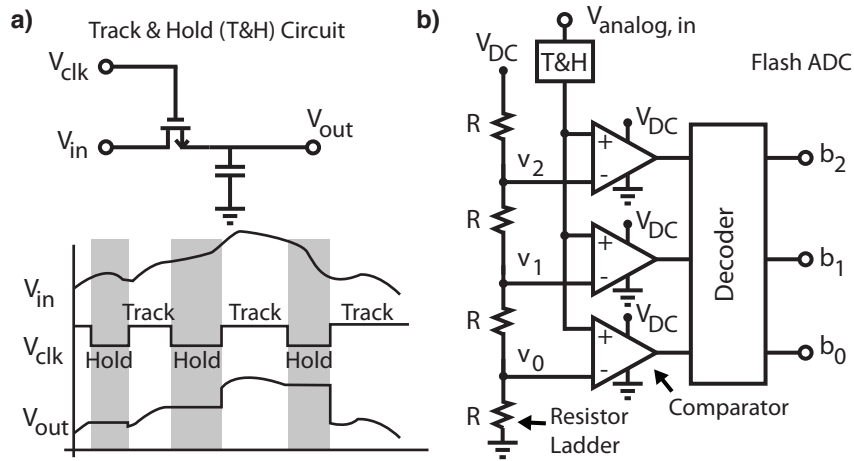
## Track-and-Hold Circuit Integrated along Vertical InAs Nanowires

**E**XCEPT for gate-all-around geometry and ease in integrating III-V material on Si, another benefit in using vertically grown nanowires in electronics is the small footprint of the devices. The vertical realization of devices allows integrating circuit components along the vertical direction while maintaining a small footprint. This can further increase the packing density of the modern ICs and reduce the cost of the chip. In this thesis, we realized track-and-hold circuits using vertical InAs/high- $\kappa$  nanowire MOSFETs and capacitors.

Track-and-hold circuit is a fundamental building block in mixed-signal applications, e.g. in analog-to-digital (A/D) and digital-to-analog (D/A) converters. It consists of a MOSFET loaded by a metal-insulator-metal (MIM) capacitor, figure 5.1(a). Analog input and clocking signals are sent to the drain and gate of the MOSFET. The output is read at the MOSFET source. The MOSFET operates as a switch, i.e. a gate voltage dependent resistor. At each clocking high, the MOSFET is switched on, and the output tracks or samples (if the clocking period is short) the input. At each clocking low, the transistor is switched off. The capacitor will hold the charges for a while during the period, and the output signal will hold the latest sampling voltage as well. For the simplest A/D converter (ADC), flash ADC (figure 5.1(b)), for instance, the track-and-hold signal is then sent to the inputs of a group of comparators in parallel. The number of the comparators determines the converted bits. At each clocking period, the track-and-hold signal will be compared with a series of constant voltage levels generated by a resistor ladder. The output of each single comparator will be 1 if the track-and-hold signal is higher than the voltage level of the input of that comparator, and 0 if it is lower. The analog signal is thus converted to the digit signal.

In this thesis, track-and-hold circuit integration is realized along vertical





**Figure 5.1:** (a) The simplest realization of a track-and-hold circuit. (b) Schematic illustration of a flash ADC.

nanowires. Details of the processing and measurements can be found in Paper VII.

# 6

## Conclusion and Outlook

**I**N the work of this thesis, InAs/high- $\kappa$  MOS gate stacks were investigated in detail using both the C-V and the XPS techniques. The origin of the specific trap state energy distribution was clarified and compared to the well studied InGaAs and GaAs materials. The results highlight the benefit of using InAs as the n-MOSFET channel material. Strategies to optimize the InAs/high- $\kappa$  MOS gate performance were presented.

The second focus of the thesis was the improvement of vertical GAA nanowire MOS gate stacks. By developing the fabrication scheme and design, conventional C-V techniques were successfully applied to vertical GAA nanowire MOS systems.  $D_{it}$  below  $10^{12}$  eV<sup>-1</sup>cm<sup>-2</sup> near the MOS semiconductor conduction band edge was achieved. Furthermore, RF C-V measurements, together with the development of a complete small-signal equivalent circuit model, for vertical GAA nanowire MOS devices were presented for the first time, which enabled characterization of border trap density, interface trap density, channel resistivity and quality factor of the vertical nanowire MOS devices.

In spite of the promising electrical properties, one challenge associated with the narrow band gap InAs, in terms of the MOSFET application, is the larger impact-ionization and band-to-band tunneling at high drain biases that limit the intrinsic performance for this type of devices. In the work of this thesis, an asymmetric InAs/InGaAs vertical nanowire MOSFET design was proposed, taking advantage of the efficient strain relaxation of nanowire epitaxial growth. Control of the InGaAs nanowire composition was successfully demonstrated.

Finally, a vertical integration scheme was developed in the thesis, where track-and-hold circuits, consisting of a MOSFET in series with a metal-

insulator-metal capacitor, were successfully fabricated along vertical InAs nanowires.

In the future, vertical nanowire MOSFETs can be a promising candidate for electronics. It allows a relatively easy way to realize gate-all-around geometry, hence providing better scalability than those competing technologies. Besides, the ease in integrating high mobility III-V material on cost-effective Si substrates makes it very attractive to industry, as compared to III-V planar MOSFETs. Last but not least, the vertical nanowire geometry offers a possibility to increase the transistor density when arranged in the vertical direction. Circuit integrations along the vertical dimension are also expected in the future to further reduce the wafer size and cost of modern ICs.

One critical challenge limiting the commercialization of the technology is the complexity in fabrication, as compared to planar devices. Novel methods, with regards to both fabrication and characterization, are needed in the future in order to realize the large scale production. In terms of the performance, vertical nanowire based devices are in general suffering from a comparably poor off-state performance. This limits the use of the devices in digital logics due to the increased power dissipation. Solutions can be the use of novel band engineering e.g. TFETs or the modification of the device architecture e.g. aggressively thinning the channel thickness. Despite those restrictions in digital applications, vertical nanowire devices might be commercialized first for analog applications if its RF performance can be continuously improved and the noise level can be continuously reduced. These remaining issues are waiting to be solved someday.

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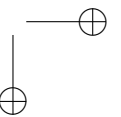
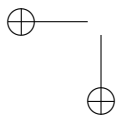
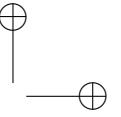
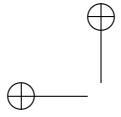
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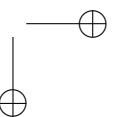
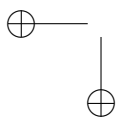
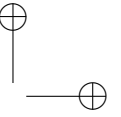
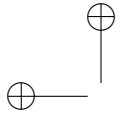
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# PAPERS







## Papers included in the thesis

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### *Paper I*

- **Al<sub>2</sub>O<sub>3</sub>/InAs metal-oxide-semiconductor capacitors on (100) and (111)B substrates**

*J. Wu, E. Lind, R. Timm, M. Hjort, A. Mikkelsen, and L.-E. Wernersson*  
*Applied Physics Letters*, vol. 100, pp. 132905, Mar. 2012, DOI: 10.1063/1.3698094.

Download at: <http://scitation.aip.org/content/aip/journal/apl/100/13/10.1063/1.3698094>

### *Paper II*

- **High- $\kappa$  oxides on InAs 100 and 111B surfaces**

*E. Lind, J. Wu, and L.-E. Wernersson*  
*ECS Transactions*, vol. 45, no. 3, pp. 61–67, Apr. 2012, DOI: 10.1149/1.3700872.

Download at: <http://ecst.ecsdl.org/content/45/3/61>

### *Paper III*

- **Low trap density in InAs/High- $\kappa$  nanowire gate stacks with optimized growth and doping conditions**

*J. Wu, A. S. Babadi, D. Jacobsson, J. Colvin, S. Yngman, R. Timm, E. Lind, and L.-E. Wernersson*  
*Nano Letters*, Manuscript accepted on March 2016, DOI: 10.1021/acs.nanolett.5b05253

Download at: <http://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b05253>

### *Paper IV*

- **RF characterization of vertical wrap-gated InAs/high- $\kappa$  nanowire capacitors**

*J. Wu, K. Jansson, A. S. Babadi, M. Berg, E. Lind, and L.-E. Wernersson*  
*IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 584–589, Feb. 2016, DOI: 10.1109/TED.2015.2506040.

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### *Paper V*

- **Extrinsic and intrinsic performance of vertical InAs nanowire MOSFETs on Si substrates**

*K.-M. Persson, M. Berg, M. B. Borg, J. Wu, S. Johansson, J. Svensson, K. Jansson, E. Lind, and L.-E. Wernersson*  
*IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2761–2767, Sep 2013, DOI: 10.1109/TED.2013.2272324.

Download at: [http://ieeexplore.ieee.org/xpls/abs\\_all.jsp?arnumber=6563112](http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6563112)

**Paper VI**

- **Control of composition and morphology in InGaAs nanowires grown by metalorganic vapor phase epitaxy**

*J. Wu, B. M. Borg, D. Jacobsson, K. A. Dick, and L.-E. Wernersson*

*Journal of Crystal Growth*, vol. 383, pp. 158–165, Aug 2013, DOI: 10.1016/j.jcrysgro.2013.07.038.

Download at: <http://www.sciencedirect.com/science/article/pii/S0022024813005666>

**Paper VII**

- **3D integrated track-and-hold circuit using InAs nanowire MOSFETs and capacitors**

*J. Wu, and L.-E. Wernersson*

*IEEE Electron Device Letters*, Manuscript (to be submitted)