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Published in:
2012 American Control Conference (ACC)

DOI:
[10.1109/ACC.2012.6315304](https://doi.org/10.1109/ACC.2012.6315304)

2012

[Link to publication](#)

Citation for published version (APA):
Cervin, A. (2012). Stability and Worst-Case Performance Analysis of Sampled-Data Control Systems with Input and Output Jitter. In *2012 American Control Conference (ACC)* (pp. 3760-3765). IEEE - Institute of Electrical and Electronics Engineers Inc.. <https://doi.org/10.1109/ACC.2012.6315304>

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Stability and Worst-Case Performance Analysis of Sampled-Data Control Systems with Input and Output Jitter

Anton Cervin

Abstract—When a feedback controller is implemented in a networked embedded system, the computations and communications induce delays and jitter, which may destabilize the control loop. The majority of previous work on analysis of control loops with time-varying delays has focused on output (actuation) jitter. In many embedded systems, input (sampling) jitter is also an issue. In this paper, we analyze the combined effect of input and output jitter on the stability and performance of linear sampled-data control systems. The analysis is performed via a loop transformation involving two time-varying uncertainties. We show how the input-output gains of the linear part of the transformed system can be computed using a fast-sampling/fast-hold approximation. At the same time, we reduce the conservativeness of a previous stability theorem for pure output jitter.

I. INTRODUCTION

In modern applications, a feedback controller is often implemented as a distributed task in a networked embedded computer system, together with many other tasks. The real-time scheduling of shared resources (CPUs and communication networks) introduces delay and jitter in the control loop, which in turn may lead to performance degradation and—in extreme cases—instability. Bounds on the delay and jitter of a distributed task can be computed using scheduling theory (e.g., [1]). Ideally, these results should be combined with control theory to guarantee, at design time, that the implemented controller will be stable (and well performing).

Stability analysis of control loops with time-varying delays has been a very active research area since the late 1980s, when the interest in networked control systems started to take off, e.g., [2], [3], [4], [5]. Only a few works have however considered the combined effect of input jitter (also known as *sampling jitter*) and output jitter. Input jitter is common in networked embedded systems, and may be the result of, e.g., poor time resolution, preemption from higher-priority tasks, or remote, asynchronous sampling.

In a stochastic, networked control setting, both input and output jitter was considered in [6]. Assuming independent stochastic delays, known delay distributions and that all delays could be measured on-line, an LQG-optimal, jitter-compensating controller was derived. No method for analyzing the resulting closed-loop performance was given, however. Inspired by [4] and [6], the Jitterbug toolbox [7] was developed to facilitate stochastic performance analysis of sampled-data control loops with various types of random

delays, including input and output jitter. Again, all time-varying delays were modeled by independent stochastic variables with known probability distributions. Stability could be guaranteed in the mean-square sense.

An approximate analysis for sampled-data control systems with input and output jitter was developed in [8]. Invoking the w -transform and making continuous-time approximations of the jitter-induced errors, the author proposed a set of approximate stability tests and associated performance analysis methods.

This paper extends the sufficient stability analysis developed by Kao and Lincoln [9], [10]. They studied continuous-time, discrete-time, and sampled-data control systems with a single time-varying delay element in the control loop, and developed simple but powerful stability criteria based on the small gain theorem. The only assumption about the time-varying delay was knowledge of its minimum and maximum values. The real delay could hence be constant or time-varying, stochastic or deterministic. The current paper deals exclusively with the sampled-data case and contains the following contributions:

- Under subsample output jitter, we show how some of the conservatism of Kao and Lincoln’s analysis for can be reduced via an alternative loop transformation involving a gate operator.
- We show how the combined effect of input and output jitter can be analyzed via a novel loop transformation that contains two error paths: one continuous-time path for the input jitter and one sampled-data path for the output jitter. Both stability and worst-case performance (as measured by the \mathcal{L}_2 -induced gain from a load disturbance to the output) are analyzed.
- We detail how the input-output gains of the linear part of the transformed system can be computed via a fast-sampling/fast-hold approximation [11], as a side effect allowing also unstable plants to be analyzed.

The rest of this paper is outlined as followed. The system model is presented in Section II, followed by the stability and performance analysis in Section III. Some numerical results are given in Section IV, and the paper is concluded in Section V.

Notation

The \mathcal{L}_2 -norm of a signal $f(t)$ is denoted by $\|f\|$. The \mathcal{L}_2 -induced gain of a continuous-time system G and the ℓ_2 -induced gain of a discrete-time system G are both denoted by $\|G\|$.

This work has been supported by the Swedish Research Council, the LCCC Linnaeus Center, and the ELLIIT Excellence Center.

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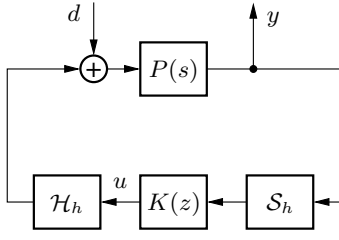


Fig. 1. Nominal system model with continuous-time plant $P(s)$, periodic sampler S_h , discrete-time controller $K(z)$, and hold circuit \mathcal{H}_h .

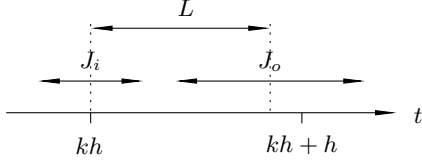


Fig. 2. Controller timing model with input jitter J_i , output jitter J_o , and nominal input-output delay L .

II. SYSTEM MODEL

A. Nominal System Model

The nominal system model is a standard linear sampled-data control loop (see Fig. 1), consisting of a strictly proper, single-input–single-output, continuous-time plant $P(s)$, a periodic sampler with interval h , a proper, discrete-time controller $K(z)$ (assuming positive feedback), and a zero-order hold circuit. It is assumed that the nominal closed-loop system is stable. The performance of the system is measured by the \mathcal{L}_2 -induced gain from the disturbance input d to the plant output y . (Defining other performance inputs and outputs would be a trivial extension.)

B. Timing Model

The time-varying delays introduced by the implementation are characterized by three non-negative parameters: the input jitter J_i , the output jitter J_o , and the nominal input-output delay L (see Fig. 2). Ideally, the controller should execute at periodic time instances $t_k = kh$, $k = \{0, 1, 2, \dots\}$. With jitter and delay, however, the controller input is sampled somewhere in the interval $[t_k - J_i/2, t_k + J_i/2]$, and the output is updated somewhere in the interval $[t_k + L - J_o/2, t_k + L + J_o/2]$. It is natural to assume that the earliest possible output operation cannot take place before earliest possible input operation, and that the latest possible input operation cannot take place after the latest possible output operation. It follows that any valid set of timing parameters must respect

$$|J_i - J_o| \leq 2L \quad (1)$$

Note that no other restrictions than the one above applies. The timing model hence allows both $L > h$ and $J_i, J_o > h$. Further note that the model does not care about *how* or *whether* the actual controller timing varies from period to period.

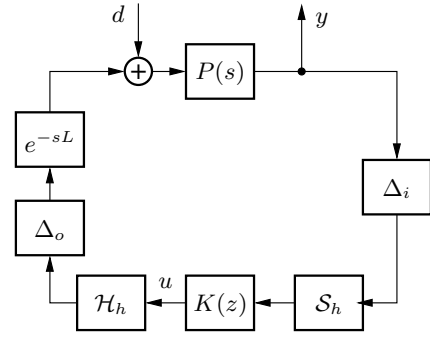


Fig. 3. Sampled-data system with continuous-time plant $P(s)$, time-varying delay operator Δ_i , periodic sampler S_h , discrete-time controller $K(z)$, zero-order hold \mathcal{H}_h , time-varying delay operator Δ_o , and nominal input-output delay e^{-sL} .

C. System Model with Delay and Jitter

The sampled-data system with delay and jitter is modeled as shown in Fig. 3. The nominal input-output delay is modeled as a delay at the plant input, while the jitters are modeled using a pair of time-varying delay operators:

$$\Delta_i(v) = v(t - \delta_i(t)), \quad -J_i/2 \leq \delta_i(t) \leq J_i/2 \quad (2)$$

$$\Delta_o(v) = v(t - \delta_o(t)), \quad -J_o/2 \leq \delta_o(t) \leq J_o/2 \quad (3)$$

Here, $\delta_i(t)$ and $\delta_o(t)$ may assume any values within their bounds at a given time t . It should be pointed out that the time-varying delays cannot be lumped together, since the various elements in the control loop do not commute.

Note that no relationship is assumed between $\delta_i(t)$ and $\delta_o(t)$. In reality, the delays are likely to be dependent. This is especially true if $J_i + J_o > 2L$, since the output operation cannot take place before the input operation in a real system. This may introduce some conservativeness in the analysis.

III. ANALYSIS

A. Analysis under Pure Output Jitter

The case of pure output jitter (obtained by setting $J_i = 0$) was treated in [9], [10]. We here review the result of main interest to us:

Theorem 1 (Corollary 3.4 in [9], p. 121): For the control loop in Fig. 3, with strictly proper and stable $P(s)$, proper $K(z)$, nominal delay e^{-sL} , and zero input jitter, the closed-loop system is stable under any output jitter satisfying (3) if

$$\left| \frac{P_{\text{alias}}(\omega)K(e^{i\omega})}{1 - P_{\text{delay}}(e^{i\omega})K(e^{i\omega})} \right| < \frac{\sqrt{2}}{\tilde{N}|e^{i\omega} - 1|}, \quad \forall \omega \in [0, \pi], \quad (4)$$

where $\tilde{N} = \sqrt{[N]^2 + 2[N]g + g}$, $g = N - [N]$, $N = J_o/h$, $P_{\text{delay}}(z)$ is the zero-order-hold discretization of $P(s)e^{-sL}$, and

$$P_{\text{alias}}(\omega) = \sqrt{\sum_{k=0}^{\infty} \left| P\left(i(\omega + 2\pi k)\frac{1}{h}\right) \right|^2}.$$

Proof sketch: The delay operator Δ_o is transformed into a direct feedthrough path and an error path, as shown in Fig. 4.

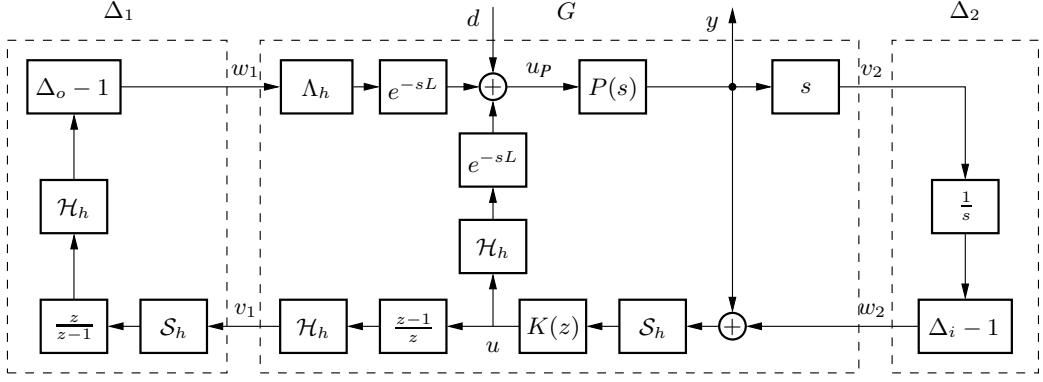


Fig. 5. Loop transformation with time-varying uncertainties Δ_1 and Δ_2 , representing induced errors due to output jitter and input jitter, respectively. The gate operator Λ_h blocks the error signal w_1 during certain intervals in each period.

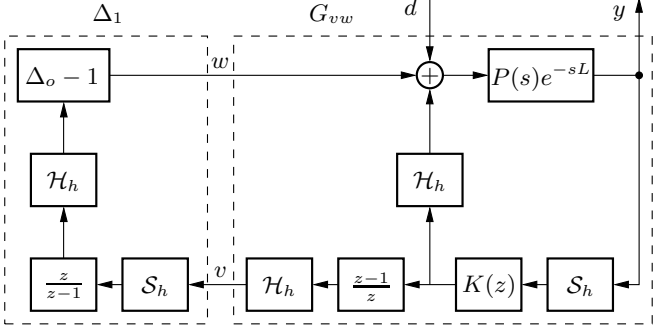


Fig. 4. Loop transformation of sampled-data control loop with pure output jitter (from [9], [10]).

The gain of the time-varying uncertainty Δ_1 , assuming zero-order-hold input signals of period h , can be shown to be

$$\|\Delta_1\| = \frac{\tilde{N}}{\sqrt{2}} \quad (5)$$

(see [9], pp. 128–129). The gain of the linear, time-periodic system G_{vw} is computed using an aliasing formula from [12]. The small gain theorem then gives the result. \square

Note that the requirement for a stable $P(s)$ is due to the chosen method for calculating the \mathcal{L}_2 -induced gain of the mixed system G_{vw} . In this paper, we rather propose to use a fast-sampling/fast-hold approximation [11] to compute the gain, removing the need for a stable plant model.

B. Improving the Output Jitter Analysis

Theorem 1 can be quite conservative for small amounts of output jitter, because the gain of Δ_1 is proportional to $\sqrt{J_o}$ for $J_o < h$. Some of the conservativeness can be reduced by noting that the error signal w must be zero during certain intervals in each period if $J_o < h$. It is thus possible to include a periodic *gate operator* Λ_h with the following behavior at the input of G_{vw} , without affecting the system under analysis:

$$\Lambda_h(w) = \begin{cases} w(t), & kh - J_o/2 \leq t \leq kh + J_o/2 \\ 0, & kh + J_o/2 < t < kh + h - J_o/2 \end{cases} \quad (6)$$

When $J_o < h$, the inclusion of the gate operator will modify the gain of G_{vw} by approximately a factor $\sqrt{J_o/h}$, creating a near-linear relationship between J_o and the loop gain $\|\Delta_1\| \cdot \|G_{vw}\|$. The gate operator will act as a feedthrough path when $J_o \geq h$.

C. Analysis under Input and Output Jitter

In order to analyze the combined effect of input jitter and output jitter, we introduce a new loop transformation that contains two error paths, see Fig. 5. The output jitter is modeled using the same sampled-data error path as before. By contrast, the input jitter delay operator acts on a continuous signal, requiring a continuous-time model of the jitter-induced error. According to [9], [10], the gain of the time-varying uncertainty Δ_2 in Fig. 5 is given by

$$\|\Delta_2\| = \frac{J_i}{\sqrt{2}} \quad (7)$$

To arrive at a sufficient stability criterion via the small gain theorem, we need to compute all input-output gains of the mixed continuous-time/discrete-time system G in Fig. 5. To facilitate the gain computations, we first make fast-sampling/fast-hold approximations of the continuous-time signals d , w_1 , y and v_2 with the short interval $\delta = h/N$, $N \gg 1$, and invoke discrete-time lifting according to [11]. In the lifted system, the continuous-time signal $d(t)$ is represented by its fast-sampled approximation

$$\hat{d}(k) = \begin{bmatrix} d(kh) \\ d(kh + \delta) \\ \vdots \\ d(kh + (N-1)\delta) \end{bmatrix} \quad (8)$$

and similarly for $\hat{w}_1(k)$, $\hat{y}(k)$, and $\hat{v}_1(k)$. Further, let $\hat{w}_2(k) = w_2(kh)$ and $\hat{v}_1(k) = v_1(kh)$.

Next, we sample the continuous-time parts of G . Assuming that $P(s)$ has the state-space representation $(A, B, C, 0)$, the plant and the continuous-time differentiator block are

described by

$$\begin{aligned}\dot{x}_P(t) &= Ax_P(t) + Bu_P(t) \\ y(t) &= Cx_P(t) \\ v_2(t) &= C\dot{x}_P(t) = CAx_P(t) + CBu_P(t)\end{aligned}\quad (9)$$

The plant input signal u_P contains contributions from the plant disturbance, the gated output jitter error signal, and the delayed control signal. To simplify the formulas below, the nominal input-output delay is represented as $L = \lfloor L \rfloor + \tau$. The integer delay part can be included as an extra factor $z^{-\lfloor L \rfloor}$ in $K(z)$.

Sampling (9) with the interval h and introducing the shorthand notation $\Phi_t = e^{At}$ and $\Gamma_t = \int_0^t e^{As}Bds$, we obtain

$$\begin{aligned}x_P(k+1) &= \Phi x_P(k) + \Gamma_0 u(k) + \Gamma_1 u(k-1) \\ &\quad + \Gamma_d \hat{d}(k) + \Gamma_{w_1} \hat{w}_1(k) \\ \hat{y}(k) &= C_y x_P(k) + D_{y0} u(k) + D_{y1} u(k-1) \\ &\quad + D_{yd} \hat{d}(k) + D_{yw_1} \hat{w}_1(k) \\ \hat{v}_2(k) &= C_{v_2} x_P(k) + D_{v_20} u(k) + D_{v_21} u(k-1) \\ &\quad + D_{v_2d} \hat{d}(k) + D_{v_2w_1} \hat{w}_1(k)\end{aligned}\quad (10)$$

where

$$\begin{aligned}\Phi &= \Phi_h \\ \Gamma_0 &= \Gamma_{h-\tau} \\ \Gamma_1 &= \Phi_{h-\tau} \Gamma_\tau \\ \Gamma_d &= [\Phi_{h-\delta} \Gamma_\delta \quad \Phi_{h-2\delta} \Gamma_\delta \quad \cdots \quad \Gamma_\delta] \\ C_y &= \begin{bmatrix} C \\ C\Phi_\delta \\ \vdots \\ C\Phi_{h-\delta} \end{bmatrix}, \quad C_{v_2} = \begin{bmatrix} CA \\ CA\Phi_\delta \\ \vdots \\ CA\Phi_{h-\delta} \end{bmatrix} \\ D_{yd} &= \begin{bmatrix} 0 & & & \\ C\Gamma_\delta & & 0 & \\ \vdots & & \vdots & \ddots \\ C\Phi_{h-2\delta} \Gamma_\delta & C\Phi_{h-3\delta} \Gamma_\delta & \cdots & 0 \end{bmatrix} \\ D_{v_2d} &= \begin{bmatrix} CB & & & \\ CA\Gamma_\delta & & CB & \\ \vdots & & \vdots & \ddots \\ CA\Phi_{h-2\delta} \Gamma_\delta & CA\Phi_{h-3\delta} \Gamma_\delta & \cdots & CB \end{bmatrix}\end{aligned}$$

The delayed control signal gives rise to

$$\begin{aligned}D_{y0}(l) &= \sum_{m=\tau/\delta+1}^N D_{yd}(l, m) \\ D_{y1}(l) &= \sum_{m=1}^{\tau/\delta} D_{yd}(l, m)\end{aligned}$$

and similarly for D_{v_20} and D_{v_21} . Finally, the gated output

jitter error signal gives rise to

$$\Gamma_{w_1}(l, m) = \begin{cases} \Gamma_d(l, m), & \min(|\tau + (\frac{1}{2} - m)\delta|, \\ & |\tau + (\frac{1}{2} - m)\delta + h|) \leq J_o/2 \\ 0, & \text{otherwise} \end{cases} \quad (11)$$

and similarly for D_{yw_1} and $D_{v_2w_1}$.

Next, we formulate the discrete-time closed-loop system, with state vector $[x_P^T \ x_K^T \ u^T(k-1)]^T$, inputs \hat{d} , \hat{v}_1 , and \hat{w}_2 , and outputs \hat{y} , \hat{w}_1 , and \hat{w}_2 . Assume that $K(z)$ has the state-space realization $(\Phi_K, \Gamma_K, C_K, D_K)$. The closed-loop system then becomes

$$\begin{bmatrix} x_P(k+1) \\ x_K(k+1) \\ u(k) \end{bmatrix} = \begin{bmatrix} \Phi + \Gamma_0 D_K C & \Gamma_0 C_K & \Gamma_1 \\ \Gamma_K C & \Phi_K & 0 \\ D_K C & C_K & 0 \end{bmatrix} \begin{bmatrix} x_P(k) \\ x_K(k) \\ u(k-1) \end{bmatrix} + \begin{bmatrix} \Gamma_d & \Gamma_{w_1} & \Gamma_0 D_K \\ 0 & 0 & \Gamma_K \\ 0 & 0 & D_K \end{bmatrix} \begin{bmatrix} \hat{d}(k) \\ \hat{w}_1(k) \\ \hat{w}_2(k) \end{bmatrix}$$

$$\begin{bmatrix} \hat{y}(k) \\ \hat{v}_1(k) \\ \hat{v}_2(k) \end{bmatrix} = \begin{bmatrix} C_y + D_{y0} D_K C & D_{y0} C_K & D_{y1} \\ D_K C & C_K & -1 \\ C_{v_2} + D_{v_20} D_K C & D_{v_20} C_K & D_{v_21} \end{bmatrix} \begin{bmatrix} x_P(k) \\ x_K(k) \\ u(k-1) \end{bmatrix} + \begin{bmatrix} D_{yd} & D_{yw_1} & D_{y0} D_K \\ 0 & 0 & D_K \\ D_{v_2d} & D_{v_2w_1} & D_{v_20} D_K \end{bmatrix} \begin{bmatrix} \hat{d}(k) \\ \hat{w}_1(k) \\ \hat{w}_2(k) \end{bmatrix} \quad (12)$$

According to [11], the ℓ_2 -induced gain of the discrete-time lifted system will uniformly and approach the \mathcal{L}_2 -induced gain of the original system as N grows. Correcting for the fact that \hat{v}_1 and \hat{w}_2 were introduced as unlifted variables above, we recover the input-output gains of the original system G through

$$\begin{aligned}\|G_{yd}\| &\approx \|G_{\hat{y}\hat{d}}\| \\ \|G_{yw_1}\| &\approx \|G_{\hat{y}\hat{w}_1}\| \\ \|G_{yw_2}\| &\approx \|G_{\hat{y}\hat{w}_2}\|/\sqrt{N} \\ \|G_{v_1d}\| &\approx \|G_{\hat{v}_1\hat{d}}\| \cdot \sqrt{N} \\ \|G_{v_1w_1}\| &\approx \|G_{\hat{v}_1\hat{w}_1}\| \cdot \sqrt{N} \\ \|G_{v_1w_2}\| &= \|G_{\hat{v}_1\hat{w}_2}\| \\ \|G_{v_2d}\| &\approx \|G_{\hat{v}_2\hat{d}}\| \\ \|G_{v_2w_1}\| &\approx \|G_{\hat{v}_2\hat{w}_1}\| \\ \|G_{v_2w_2}\| &\approx \|G_{\hat{v}_2\hat{w}_2}\|/\sqrt{N}\end{aligned}\quad (13)$$

(Note that $\|G_{v_1w_2}\|$ is computed without error, since both the input and output are true discrete-time signals.)

We are now ready to formulate the main result of the paper.

Theorem 2: Define the gains

$$\begin{aligned}
g_{00} &= \|G_{yd}\| \\
g_{01} &= \|G_{yw_1}\| \cdot \|\Delta_1\| \\
g_{02} &= \|G_{yw_2}\| \cdot \|\Delta_2\| \\
g_{10} &= \|G_{v_1d}\| \\
g_{11} &= \|G_{v_1w_1}\| \cdot \|\Delta_1\| \\
g_{12} &= \|G_{v_1w_2}\| \cdot \|\Delta_2\| \\
g_{20} &= \|G_{v_2d}\| \\
g_{21} &= \|G_{v_2w_1}\| \cdot \|\Delta_1\| \\
g_{22} &= \|G_{v_2w_2}\| \cdot \|\Delta_2\|
\end{aligned} \tag{14}$$

where $\|\Delta_1\|$ and $\|\Delta_2\|$ are given by (5) and (7), and where the input–output gains of G are computed according to (10)–(13). For the control loop in Fig. 3, with strictly proper $P(s)$, proper $K(z)$, and nominal delay e^{-sL} , the closed-loop system is stable under any input and output jitter satisfying (2) and (3) if

$$\begin{aligned}
g_{11} &< 1 \\
g_{22} &< 1 \\
g_{12}g_{21} &< (1 - g_{11})(1 - g_{22})
\end{aligned} \tag{15}$$

Moreover, if the closed-loop system is stable, then the worst-case gain from d to y is bounded by

$$\|y\| \leq \left([g_{01} \ g_{02}] \begin{bmatrix} 1-g_{11} & -g_{12} \\ -g_{21} & 1-g_{22} \end{bmatrix}^{-1} \begin{bmatrix} g_{10} \\ g_{20} \end{bmatrix} + g_{00} \right) \|d\| \tag{16}$$

Proof: The proof is a straight-forward application of the small gain theorem. For the signals in the closed-loop system, it holds that

$$\begin{aligned}
\|y\| &\leq g_{00}\|d\| + g_{01}\|v_1\| + g_{02}\|v_2\| \\
\|v_1\| &\leq g_{10}\|d\| + g_{11}\|v_1\| + g_{12}\|v_2\| \\
\|v_2\| &\leq g_{20}\|d\| + g_{21}\|v_1\| + g_{22}\|v_2\|
\end{aligned} \tag{17}$$

If the small gain conditions (15) are fulfilled, then it is possible to solve for $\|y\|$ by eliminating $\|v_1\|$ and $\|v_2\|$ in (17), yielding the finite-gain input-output relationship in (16). \square

IV. EXAMPLES

We here give two examples of how the jitter analysis can be applied.

Example 1 (Pure output jitter)

In the first example, we illustrate how the conservativeness of Kao and Lincoln [9], [10] for subsample output jitter is reduced by the new analysis. Let the system be given by

$$P(s) = \frac{1}{s}, \quad K(z) = -\frac{1.3}{z}, \quad h = 0.5, \quad J_i = 0$$

The constant delay margin for this system is

$$L_m = 0.455$$

We vary the nominal delay L between 0 and L_m and compute the maximum tolerable output jitter J_o for each value of

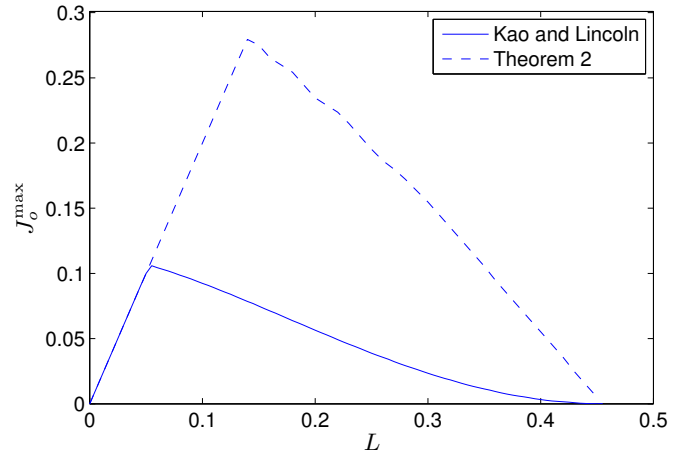


Fig. 6. Maximum allowable output jitter (J_o^{\max}) as a function of the nominal input-output delay (L) for the system in Example 1.

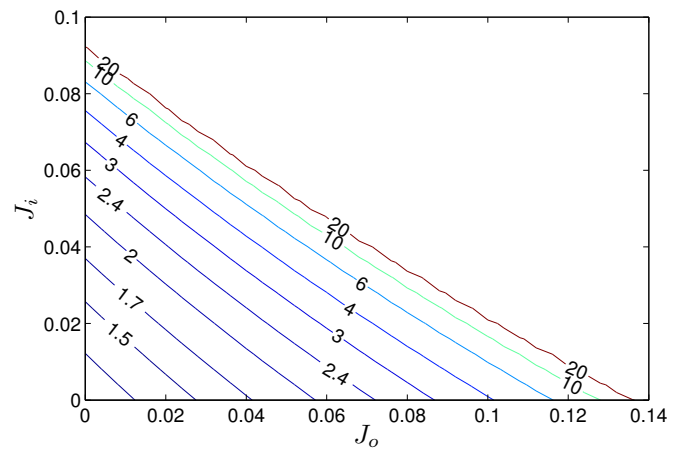


Fig. 7. Worst-case performance degradation as a function of the amount of input jitter (J_i) and output jitter (J_o) for the system in Example 2.

L , first using Kao and Lincoln’s criterion, and then using Theorem 2. The results are shown in Fig. 6. The ramp at the start of the plot is due to the restriction $J_o \leq 2L$. It is seen that Theorem 2 can indeed guarantee stability for much larger values of the output jitter.

Example 2 (Input and output jitter)

In the second example, we analyze the worst-case performance degradation of a system with both input and output jitter. Let the system be given by

$$\begin{aligned}
P(s) &= \frac{1}{s^2 - 0.01} \\
K(z) &= \frac{-12.95z^2 + 10z}{z^2 - 0.2181z + 0.1081}, \quad h = 0.2
\end{aligned}$$

We fix $L = 0.08$ and independently vary J_i and J_o between 0 and $2L$. Fig. 7 reports the performance degradation of the system relative to the nominal case $L = J_i = J_o = 0$. It is seen that this system is slightly more sensitive to input jitter than to output jitter. The performance degradation level curves bend only very slightly inwards, indicating that the combined analysis is not very conservative.

V. CONCLUSION

We have extended the stability analysis in [9], [10] to handle systems with both input jitter and output. A sufficient stability criterion was derived, which takes three timing parameters into account: the input jitter, the output jitter, and the nominal input-output delay. The criterion is based on the small gain theorem and requires the calculation of the input-output gains of a linear, time-periodic system using, e.g., lifting. The criterion can be used to guarantee the stability and performance of a control task executing in a real-time system.

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