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Strain and Charge Transport in InAsP-InP and InP-InAs Core-Shell Nanowires

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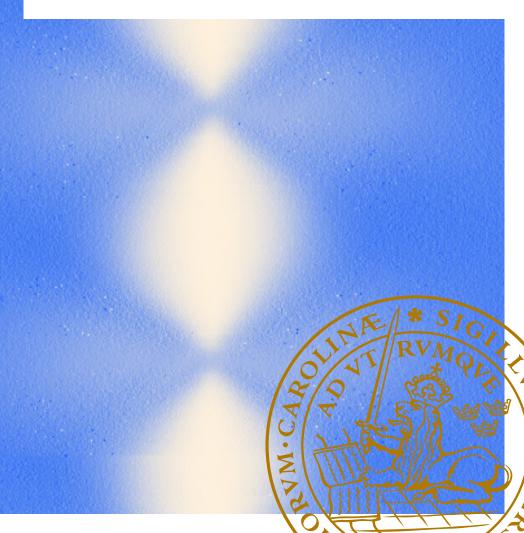
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Strain and Charge Transport in InAsP-InP and InP-InAs Core-Shell Nanowires

DAVID GÖRANSSON DEPARTMENT OF PHYSICS | FACULTY OF ENGINEERING | LUND UNIVERSITY



Strain and Charge Transport in InAsP-InP and InP-InAs Core-Shell Nanowires

David Göransson



DOCTORAL DISSERTATION

by due permission of the Faculty of Engineering at Lund University, Sweden. To be publicly defended on Monday, April 29th 2019, at 9:15 in Rydberg lecture hall at the Department of Physics, Sölvegatan 14, Lund.

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Abstract:		
The mechanical, optical, and electrical pro thesis. The semiconductor materials are gr (nanowires) having a length of ~ 1 µm an such as optical detectors, photovoltaics, lig of quantum devices, for the study of quantu	own by metal-organic vapor ph d diameter of ~ 100 nm. Nano ht emitting diodes, and transis	ase epitaxy, yielding wire shaped crystals wires are relevant for many applications, tors. Nanowires are also used in the field
In this thesis, InAsP-InP and InP-InAs core-shell nanowires of wurtzite crystal phase are investigated. The InAsP nanowires are grown epitaxially by the method of Au particle assisted vapor-liquid-solid growth. They are then covered by an InP surface layer to obtain InAsP-InP core-shell nanowires. The mechanical strain is measured in the core-shell nanowires by use of X-ray diffraction. The atomic plane spacing is obtained and related to the mechanical strain which originate from the epitaxial interface between core and shell. The strain is found to be oriented mainly along the axis of the nanowires. This axial strain is shown to increase with the thickness of the InP shell layer. This increase of strain is also found in measurements of the bandgap of the InAsP cores in the core-shell nanowires.		
The growth method selective area epitaxy is applied to produce pure wurtzite crystal phase InP-InAs core-shell nanowires. The InAs shell exhibit triangular cross section and the InP core has hexagonal cross section. The charge carrier accumulation in the InAs shell enables the formation of a quantum structure that produce conducting channels located along the corners of the triangular shell. The electrical transport through the InAs shell is investigated at temperatures < 1 K. The nanowires are first probed by Coulomb blockade transport. A method with four contact electrodes connected to the InAs shell is used to investigate the directional dependence of the Coulomb blockade, demonstrating that the corners of the shell are highly coupled and that electrons are delocalized over the full shell volume. Next, transport measurements with low resistance superconducting contacts show induced superconductivity. A gate tunable supercurrent is produced and a directional dependence of the conductance is found in the InAs shell.		
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Strain and Charge Transport in InAsP-InP and InP-InAs Core-Shell Nanowires

Doctoral Thesis

David Göransson 2019



Division of Solid State Physics Department of Physics Lund University *Front cover*: Differential conductance is shown as a function of gate voltage and source-drain bias. The diamond structure demonstrate the Coulomb blockade effect and the measurement was performed on an InP-InAs core-shell nanowire.

Back cover: A triangular InP-InAs core-shell nanowire is shown, having Ti/Au electrodes on the surface. The image was acquired in a scanning electron microscope.

Cover photos by David Göransson

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For Eva, Jonathan and Inna

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Abstract

The mechanical, optical, and electrical properties of III-V semiconductor heterostructures are investigated in this thesis. The semiconductor materials are grown by metal-organic vapor phase epitaxy, yielding wire shaped crystals (nanowires) having a length of ~ 1 μ m and diameter of ~ 100 nm. Nanowires are relevant for many applications, such as optical detectors, photovoltaics, light emitting diodes, and transistors. Nanowires are also used in the field of quantum devices, for the study of quantum dots and Josephson junctions.

In this thesis, InAsP-InP and InP-InAs core-shell nanowires of wurtzite crystal phase are investigated. The InAsP nanowires are grown epitaxially by the method of Au particle assisted vapor-liquid-solid growth. They are then covered by an InP surface layer to obtain InAsP-InP core-shell nanowires. The mechanical strain is measured in the core-shell nanowires by use of X-ray diffraction. The atomic plane spacing is obtained and related to the mechanical strain which originate from the epitaxial interface between core and shell. The strain is found to be oriented mainly along the axis of the nanowires. This axial strain is also found in measurements of the bandgap of the InAsP cores in the core-shell nanowires.

The growth method selective area epitaxy is applied to produce pure wurtzite crystal phase InP-InAs core-shell nanowires. The InAs shell exhibit triangular cross section and the InP core has hexagonal cross section. The charge carrier accumulation in the InAs shell enables the formation of a quantum structure that produce conducting channels located along the corners of the triangular shell. The electrical transport through the InAs shell is investigated at temperatures < 1 K. The nanowires are first probed by Coulomb blockade transport. A method with four contact electrodes connected to the InAs shell is used to investigate the directional dependence of the Coulomb blockade, demonstrating that the corners of the shell are highly coupled and that electrons are delocalized over the full shell volume. Next, transport measurements with low resistance superconducting contacts show induced superconductivity. A gate tunable supercurrent is produced and a directional dependence of the conductance is found in the InAs shell.

Populärvetenskaplig sammanfattning

I denna avhandling presenteras metoder och resultat från experminetella undersökningar av elektriskt ledande material, halvledare, som har formen av stavliknande trådar med ca en mikrometers längd och enbart 100 nanometer i diameter, så kallade nanotrådar. Materialen framställs med kristallväxt så att mycket små kristaller med välkontrollerad geometrisk form växer fram, stående på en kristallyta. Elektriska, mekaniska och optiska egenskaper i nanotrådarna undersöks med syftet att förstå hur den geometriska formen samt hur vissa ytlager påverkar dessa egenskaper. Nanotrådar har stor potential inom områden som ljusdetektorer, ljusdioder, solceller, samt elektroniska komponenter för datorer.

Halvledarmaterial har stor betyselse för dagens samhälle. De utgör den funktionella delen i de flesta elektroniska och optoelektroniska komponenter. En halvledare har normalt en elektrisk ledningsförmåga som är lägre än den hos metaller men högre än i isolatorer. Utmärkande för halvledare är att en elektrisk spänning kan användas för att styra den elektriska ledningsförmågan i materialet. Detta är möjligt eftersom elektriska fält påverkar antalet ledande partiklar (elektroner) som är tillgängliga och kan bidra till en elektrisk ström i en halvledare. I grunden är det den principen som används för att styra strömmen i en enskilld transistor, vilken utgör den grundläggande "byggstenen" i en dator. En transitor är en komponent som har en ledande kanal bestående av en halvledare. Strömmen som flyter genom kanalen kan tänkas vara en flod i rörelse. Med en elektrisk spänning kan floden blockeras i analogi med att stäng luckorna i en damm så att flödet sinar. Detta används för att generera signaler eller för att utföra beräkningar med en dator. De halvledare som används är oftast monokristallina, vilket innebär att atomerna som bygger upp materialet sitter i ett ordnat mönster av rader och kolumner med t.ex. räta vinklar som i en kubisk struktur, eller med 120 graders vinkel i den hexagonala. Mönstret upprepas på exakt samma sätt i hela kristallen. Kristallint kisel är idag ett välkänt halvledarmaterial, eftersom det utgör basen för industriella elektronikkomponenter, t.ex. transistorer. Det är även detta material som används i solceller. De stora tillverkningsvolymerna av krinstallint kisel har medfört mycket låga priser på solceller.

Den gradvisa förminskningen av kiselkretsar har medfört stora förbättringar av kiseltransistorers prestanda, detta möjligjordes genom allt mer förfinade tillverkningsmetoder. Förminskningen av transistorerna ger fördelar så som högre arbetsfrekvens och lägre energiförbrukning. Ett viktigt problem är däremot att vidare utveckla prestandan inom detta område, eftersom det nu är uppenbart att dagens transistorer har problem med t.ex. strömläckage vilket medför ökad strömförbrukning och därmed förhindrar ytterligare förminskning. De minsta transistorerna är nu i stroleksordning av ca 10 nm (10 miljondelars millimeter), därmed kan flera miljarder transistorer få plats på ytan av ett chip. En möjligt väg till förbättring är att ersätta kisel med en halvledare som uppvisar bättre egenskaper.

Exempelvis kan III-V halvledare vara ett alternativ, eftersom elektronerna som bär strömmen i dessa material rör sig med högre hastighet. Dessutom är effektiviteten hög för ljusabsorption och emission. På grund av detta tillverkas detektorer och ljusdioder för optiska signaler som sänds över fiberoptiska nätverk, av III-V halvledare. III-V halvledare består till hälfen av grundämnen från grupp III i det periodiska systemet, så som indium (In) och till andra hälfen av grupp V exempelivs fosfor (P) och arsenik (As).

Inom optoelektroniska komponenter används III-V halvledare idag på grund av de specifika våglängder, av ljusets spektrum, som materialen kan absorbera och emittera. Våglängden på ljuset som emitteras från en halvledare är relaterat till den energimängd och materialparameter som benämns bandgap. Halvledare kan inte skicka ut eller absorbera våglängder som är längre än en viss maximal våglängd, och som har en energi som är mindre än bandgapet. Genom välkontrollerad kristallväxt kan den kemiska sammansättningen i III-V materialen kontrolleras som t.ex. i InAsP. Det är därmed möjligt att välja ut våglängder som materialet kan absorbera och emittera, genom andelen arsenik och andelen fosfor. Det kan t.ex. vara 50% indium, 10% arsenik och 40% fosfor.

Komponenter med mycket små storlekar är även intressanta eftersom helt ny funktionalitet baserat på kvantfysik blir möjlig. Ett exempel på sedana strukturer är kvantprickar. Dessa prickar är ofta kristaller av halvledare som har tillräckligt liten volym för att elektronerna ska kunna visa sina vågegenskaper. Kristallens längd, bredd och höjd ska vara av undefär samma storlek som elektronernas våglängd. I det fallet påverkas materialets optiska och elektriska egensakper på ett fundamentalt sätt. Förenklat kan elektroner i kvantprickar beskrivas som stående vågor. I analogi med svängade gitarrsträngar har dessa vågor våglängder som precis får plats i kvantpricken. I III-V halvledare är en stor energimängd kopplad till de stående vågorna, därför är de lämpade som material för kvantprickar. Intressant är att de stående vågorna ger mycket väldefinierade färger vid ljusemission vilket kan utnyttjas för att skicka signaler eller detektera signaler med specifika våglängder. Kvantfenomen kan också studeras genom att låta en elektriskt ström flyta genom en kvantprick, strömmen behöver då passera genom en stående våg. I detta fall är det nödvändigt att tillverka elektriska kontaker av lika små dimensioner som sedan placeras på kvantpricken.

Det finns idag planer på att skapa en helt ny teknologi baserat på kommunikation och beräkning med väldefinierade sammankopplade kvanttillstånd, så kallade kvantdatorer. Potentiellt möjliggör dessa system en mycket hög beräkningskapacitet för specifika beräkningsproblem. Ofta är supraledare en komponent i dessa system. Elektroner i supraledande material övergår till ett speciellt kvanttillstånd om temperaturen sänks under en kritisk temperatur vilken oftast är mindre än -200 °C. Hög temperatur medför värmeenergi som förstör kvanttillsåndet. Det supraledande kvanttillståndet innebär att alla elektroner ingår i en gemensam vågform, där elektriska resistansen blir lika med noll. Förutom att detta är ett intressant fysikaliskt fenomen, har supraledare stora användingsområden t.ex. i magnetisk resonanstomografi och nyligen även i tågbanor. Intressanta kvantfenomen uppstår även då en liten halvledare och två supraledare kopplas samman (Josephsonövergång), vilka möjligen kan användas i framtida kvantdatorer.

Denna avhandling bygger på experimentella undersökningar av tunna kristallina trådar, nanotrådar, vilka framställs av III-V materialen InAsP, InP och InAs genom en kristallväxtprocess, som benämns metal-organic vapor phase epitaxy (MOVPE). Nya växtmetoder har gjort det möjligt att kontrollera kristallernas storlek och form med mycket hög noggranhet, vilket gör dem relevanta för industriell tillverkning. Av stort vikt är att framställa flera lager av halvledare t.ex. en tråd av InAsP med ett ytlager av InP, som är anpassat så att atomer i InAsP binds kemiskt till InP atomer en-till-en i gränssnittet utan att defekter uppstår, så som vakanta atompositioner. Diametern och längden på trådarna samt lagertjockleken på skalen kan styras i växtmetoden. Det intressanta med dessa lager är att den elektroniska funktionaliteten kan påverkas samt att ytan av kärnan kan bli passiviserad, genom reducerad mängd defekter vid ytan.

I avhandligen undersöks både mekaniska, elektriska och optiska egenskaper i dessa trådar med kärna-skal struktur. Vid växt av skalet uppstår nämligen en mekanisk töjning utmed längden av tråden eftersom avstånden mellan atomerna i olika III-V material varierar. När skalet växer tvingas atomerna till positioner som är likvärdiga i båda materialen och därmed förändras atomernas avstånd genom töjningen. Det medför ett mycket högt tryck och ungefär 1% förändring av atomavstånden. Resultaten visar att energin för bandgapet ändras och därmed energin och våglängden av emitterat ljus. De redovisade mätningarna visar att ljusets våglängd minskade som en funktion av skalets tjocklek för InAsP-InP nanotrådarna, vilket beror på de minskade atomavstånden. Vidare mäts atomavstånden med Röntgendiffraktion, vilket visar på att atomavstånden är beroende av skalets tjocklek, samt att defekter ej uppstod. Detta resultat viktigt inom tekniker baserade på detektion eller emission av infrarött ljus.

Kristallstrukturen och de elektriska egenskaperna hos InP-InAs kärna-skal nanotrådar med triangelformade InAs skal undersöktes vidare. Resultaten visar på en hög renhet i kristallfasen, vilken är av hexagonal symmetri, så kallad wurtzite. Elektriska mätningar vid temperaturer lägre än -273 °C utförs för att studera känsliga kvanttillstånd i nanotrådarnas triangulära InAs skal. Först konstrueras och karaktäriseras tranistorer byggda av nanotrådarna, vilka utgör en strömbärande kanal. Transistorerna är sådana att enbart en elektron i taget tillåts passera kanalen. Resultateten från denna studie är främst att enskillda elektronladdningar är fördelade över hela InAs skalets volym. Slutligen studeras likadana nanotrådar, kontakterade med supraledande aluminum. Resultateten från denna studie visar att en superström (ström vid en exakt spänning av noll volt) vilken flyter genom nanotrådarna, är mätbar, samt att ett elektrisk fält kan styra storleken på strömmen. Den elektriska kopplingen mellan det triangulära InAs skalets hörn undersöks sedan genom att studera ledningsförmågan mellan dessa. Denna geometri, vilken är ett resultat av kristallväxten, kan i framtida experiment förfinas ytterligare för att möjliggöra Josephsonövergångar som är lämpade för kvantdatorer.

List of Papers

I. Measurements of strain and bandgap of coherently epitaxially grown wurtzite InAsP-InP core-shell nanowires

David J. O. Göransson, M. T. Borgström, Y. Q. Huang, M. E. Messing, D. Hessman, I. A. Buyanova, W. M. Chen, H. Q. Xu.

In review for Nano Letters

I planned and performed the growth experiments to obtain InAsP-InP coreshell nanowire samples with a series of varied InP shell thickness. The XRD measurements and SEM imaging was performed by me. I performed data analysis and extracted strain data from the XRD measurement. I then analyzed the strain dependence in the photoluminescence data. I reviewed the literature and wrote the main parts of the paper.

II. Structure investigation of InAs_{0.26}P_{0.74}-InP core-shell nanowires grown on (111) InP substrate

Sergey Lazarev, <u>David J. O. Göransson</u>, Magnus T. Borgström, Maria E. Messing, H. Q. Xu, Dmitry Dzhigaev, Oleksandr M. Yefanov, Sondes Bauer, Tilo Baumbach, Robert Feidenhans, Lars Samuelson, and Ivan A. Vartanyants.

Submitted to Nano Letters

I initiated the study and planned and performed the nanowire growth experiments. The SEM measurements and the parts of the XRD measurements, which were performed at Lund Nano Lab, were performed by me. I took part in many discussion sessions with the co-authors where we analyzed the interpretations of the data collected by the co-authors. I contributed to the analysis of the strain and composition effects in the nanowires and wrote parts of the paper.

III. Coulomb blockade from the shell of an InP-InAs core-shell nanowire with a triangular cross section

David J. O. Göransson, M. Heurlin, B. Dalelkhan, S. Abay, M. E. Messing, V. F. Maisi, M. T. Borgström, and H. Q. Xu.

Appl. Phys. Lett. 114, 053108 (2019)

I initiated the project and the growth experiments with selective-area growth of InP-InAs core-shell nanowires. I investigated and performed the clean-room processing and electron beam lithography on the growth substrates as well as the lithography for the electrical contacts to the nanowires. I performed the transport measurements and the data analysis. I reviewed the literature and wrote the main parts of the paper.

IV. Proximity Induced Superconductivity in Triangular InP-InAs Core-Shell Nanowires

David J. O. Göransson, B. Dalelkhan, V. F. Maisi, M. E. Messing, M. T. Borgström, and H. Q. Xu.

In Manuscript

I performed the nanowire growth experiments, the processing of the electrical contacts to the nanowires by electron beam lithography, and the transport measurements. I finally performed the literature review, and the data analysis. I wrote the main parts of the paper.

Papers not included in the thesis

V. Electron transport study of InSb nanowire quantum dots defined by side gates

B. Dalelkhan, <u>D. J. O. Göransson</u>, V. F. Maisi, A. Burke, P. Caroff, and H. Q. Xu

In Manuscript

VI. Ambipolar and temperature dependent transport properties of InSb nanowires grown by chemical vapor deposition
B. Dalelkhan, V. F. Maisi, <u>D. J. O. Göransson</u>, C. Thelander, K. Li, Y. J. Xing, and H. Q. Xu

In Manuscript

Abbreviations

NW	Nanowire
Si	Silicon
InAs	Indium arsenide
InP	Indium phosphide
InAsP	Indium arsenide phosphide
MOVPE	Metal-organic vapor phase epitaxy
SAG	Selective area growth
TMIn	Trimethylindium
WZ	Wurtzite
ZB	Zinc-blende
Ti	Titanium
Al	Aluminium
Au	Gold
XRD	X-ray diffraction
LED	Light emitting diode
SEM	Scanning electron microscope
TEM	Transmission electron microscopy
EBL	Electron beam lithography
NS	Normal-superconductor
SNS	Superconductor-normal-superconductor
JJ	Josephson junction
DC	Direct current
AC	Alternating current
AR	Andreev reflection

Introduction

In this chapter, background and motivations are given for the experimental work presented in the papers I to IV.

1.1. Semiconductor Technology

Electronic semiconductor devices have transformed society by enabling high speed digital information processing. One of the most important devices is the semiconductor transistor, which was first demonstrated at Bell labs around 1948 [1]. Today, Si transistors are the basic building blocks of digital computers. Solar cells are also important devices which are predominantly made from Si. The large production volumes of such solar cells has recently lead to solar energy prices below that of competing energy sources in many parts of the world [2].

To improve performance of the above devices, Si could be replaced by alternative semiconductors. The speed of transistors and the efficiency of solar cells can be increased by selecting a semiconductor, or combinations of several, that have better inherent material properties. The materials studied in this thesis, III-V semiconductors, can be an alternative to Si. These materials are formed from the elements of group III (B, Al, Ga, In) and group V (N, P, As, Sb) of the periodic table. Many of the III-V semiconductors show higher carrier velocity compared to Si, which is a benefit in high frequency transistors [3]. Most of them also show superior efficiency in emission and absorption of light, because of their direct bandgap.

Optical detectors (or emitters) working in infra-red wavelengths are typically made from ternary III-V material, such as InGaAs [4]. These are commonly operated around the wavelength of $\lambda \approx 1550$ nm in the low-loss fiber-optics window, which is used in optical fiber communication. In these applications, III-V semiconductors are used due to their small band gap (corresponding to infra-red wavelengths). In this thesis, InAs_xP_{x-1} is investigated because of its potential applications in photodetectors and photovoltaics. This material exhibits a similar bandgap range as InGaAs and is, therefore, applicable to infra-red photodetectors [5]. The wurtzite (WZ) crystal phase InAsP bandgap decreases with arsenic fraction (x) from 1.50 eV in InP [6] to 0.48 eV in InAs [7], having the corresponding wavelength range of 830 - 2600 nm (at low temperatures). The bandgap can, thereby, be tuned to be relevant for specific applications.

Novel geometries and epitaxial growth methods of III-V transistor channels are currently investigated with the aim of replacing Si in transistors [8]. The power consumption of logic transistors was gradually decreased, while the operating frequency was increased, over the past 50 years. This was made possible by downscaling of the transistors, following Moore's law. However, achieving further progress today is more difficult. One of the major problems is the power consumption with consequent heat generation in the transistors. The increasing use of information technology has many positive aspects, but it also leads to an increased energy consumption world wide [9]. This is problematic since emission of greenhouse gases accompany the electricity generation in most cases. To decrease the energy waste, it is relevant to investigate novel transistor designs.

Computation is predicted to be possible with two level quantum states known as qubits. In some applications, quantum computers and quantum simulators built from coupled qubits, could potentially offer great improvements over the classical transistors[10]. Accurate and fast calculations of many-body states is one possible application [11]. Several different systems of coupled qubits have been produced, such as spin qubits in semiconductor quantum dots [12][13][14]. However, a problem with most qubits is the short coherence times. Interestingly, edge states of topological nature, known as Majorana bound states, could potentially offer decoherence protection [15]. Such states were recently found experimentally in one-dimensional wires made from InSb [16][17] and InAs [18][19], which were contacted to superconductors. Experimental studies on induced superconductivity in InAs nanostructures, demonstrated in this thesis, are motivated by these recent developments.

1.2. Semiconductor Nanowires

In this thesis, InAsP-InP and InP-InAs wire shaped semiconductor heterostructures are investigated, so called core-shell nanowires. The nanowires have a diameter of 200-100 nm, or smaller, and a length of about 1 μ m. First, the crystal structure and the strain in the nanowires, due the heterointerface, is experimentally investigated in the InAsP-InP system, in papers I and II. Then, the charge transport properties of InP-InAs nanowires are investigated at low temperatures in paper III, using Ti/Au contacts, and in paper IV with Ti/Al superconducting contacts. Examples of such nanowires are illustrated in Fig. 1.1.

Nanowires are considered relevant for field effect transistors [20][21][22], optoelectronics [23][24], and solar cells [25]. Early results on particle assisted epitaxial growth of III-V and Si nanowires has inspired a large number of

experimental studies in these areas [26][27][28][29]. Nanowires are, furthermore, free standing and vertically aligned self-assembled semiconductors, that can provide high quality facets and surfaces, which leads to high carrier mobility [30]. The epitaxial growth of nanowires potentially gives low surface roughness as compared to etched structures that are traditional used in industry (the top-down processing scheme). For example, it was demonstrated that WZ InP nanowires grown by the selective area method in metal-organic vapor phase epitaxy (MOVPE), exhibit high quantum efficiency in laser applications [31].

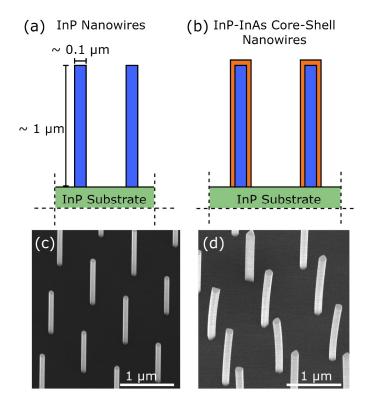


Figure 1.1. Schematic illustration of InP nanowires standing vertically on a InP substrate in panel (a) and InP nanowires with InAs shell in panel (b). (c) Wurtzite InP nanowires grown by MOVPE are imaged by a scanning electron microscope, standing vertically on the InP substrate. The image is acquired with a tilt of 30°. (d) Wurtzite InP-InAs core-shell nanowires grown by MOVPE are imaged as in (c). The core-shell nanowires in (d) show bending due to strained shell growth.

Nanowires exhibit several interesting properties. The geometry of the nanowires has proven to be efficient for collecting photons, by the nanowires acting as antennas, which is an advantage in solar cells and photodetectors [25]. They also efficiently emit photons and can be grown with integrated quantum dots [32].

Many electronic and optoelectronic devices are typically manufactured from several planar layers of different III-V materials formed by epitaxial growth, where the atomic crystal structure is carried over across the interface. Such layer combinations are known as heterostructures. The difference in atomic spacing (lattice constants a and c) of the III-V materials, however, cause large stress and strain in the layers. Defects thereby appear at the interfaces of the layers, leading to degradation of the device performance. It is, for this reason, difficult to obtain defect free heterostructures, except for specific combinations of III-V materials. Fortunately, the stress can be reduced for devices of small dimensions below ~ 100 nm, which is the case in nanowire heterostructures [33]. At these small dimensions, the stress and strain can in some cases relax at the free surfaces and defects can be avoided. In Fig. 1.1(a) and (c) examples of InP nanowires standing on an InP substrate are shown. In Fig. 1.1(d) such nanowires with an InAs shell are shown, where the nanowires bend under the stress caused by the lattice parameter mismatch.

In sufficiently thin nanowires the electrons are highly confined in the radial direction giving rise to standing electronic wave functions. While along the nanowire axis, they form freely propagating wave functions. The density of states is then considered close to one-dimensional (1D). The confinement can also be arranged in all three dimensions to form a quantum dot. Few-electron nanoscale devices, such as electrostatically gated quantum dots, is a highly active field of research. Quantum dots can be formed by alternating the material in the axial nanowire growth, to form axial segments [29][34]. The electrons can then be trapped by the potential energy difference of the conduction bands of the different materials. In the case of InAs and InP heterostructures, the InAs conduction band is lower in energy compared to that of InP, leading to accumulation of electrons in InAs.

1.3. InAsP-InP and InP-InAs Core-Shell Nanowires

In papers I and II, X-ray diffraction is used to study the atomic plane spacing of strained InAsP-InP core-shell nanowires. The strain of the core was measured in the direction along the nanowire axis as well as in a perpendicular direction. In paper I, the plane spacing of the InAsP core was shown to gradually decrease with increasing InP shell thickness, due to increasing compressive strain in the core. The study shows that InAsP-InP heterostructures can be epitaxially grown in the geometry of core-shell nanowires that are defect free. The lattice parameter of InAsP increases with As fraction, leading to an increasing lattice parameter mismatch between InP and InAsP. The mismatch between InAs and InP is given by $f_0 = (c_{InAs} - c_{InP})/c_{InP} = 3.2\%$.

Even in the absence of defects, the influence of the strain in the heterostructure need to be considered, due to its effect on the electronic band structure. Particularly, the

bandgap is changed by ~ 100 meV/percent strain. A reduced bandgap has been shown to enhanced conductivity for InAs-InGaAs nanowires under uniaxial tensile strain [35]. Additionally, the induced deformation displaces the relative positions of the atoms in the lattice so that a polarization of the crystal can appear, (the piezoelectric effect). The strained InAs-InP core-shell nanowires have been predicted to show piezoelectric polarization along the [111] or [0001] directions of the crystal. This polarization could be used to create an electric field along the axis of the nanowire to produce a photovoltaic effect [36][37].

Charge transport experiments on InAsP-InP nanowires were initially performed. These were aimed at detecting the piezoelectric polarization effect that is predicted to appear in axially strained nanowires. However, this data showed no conclusive evidence of polarization, likely due to the high resistance of the non-linear Schottky type contacts that were obtained. It was instead found that InP-InAs core-shell nanowires exhibit interesting low-temperature transport properties and very low contact resistance. Similar core-shell nanowire have been used in the investigations of coherent electron transport phenomena that appear in the tube morphology. The Aharonov-Bohm effect was observed [38][39] and the Majorana bound states have been theoretically investigated [40] in such structures.

In paper III and IV InP-InAs core-shell nanowires of pure WZ crystal structure were grown by the selective area method. The overall cross section of the InAs shell was triangular and the InP core was geometrically hexagonal. The shell thereby formed three conductive corner as illustrated in Fig. 1.2. We explored some of the properties of this novel structure by low-temperature transport measurements. First, Ti/Au contacts forming barriers at the interface were used. This resulted in a Coulomb blockade effect, corresponding to electrons being delocalized over the entire InAs shell structure. Second, in paper IV the same nanowires were studied by applying superconductor Ti/Al contacts in various configurations. Supercurrent could be measured, and the critical supercurrent was analyzed as a function of gate voltage. The contact quality could furthermore be analyzed. Finally, the conductance both along the nanowire axis, and perpendicular to the axis, was found to be governed by the triangular morphology of the InAs shell.

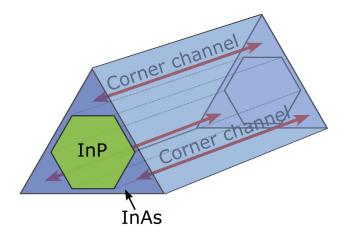


Figure 1.2. Schematic illustration of a triangular InP-InAs core-shell nanowire. Electrically conductive channels are formed along the three InAs corners, as a consequence of electron accumulation in the InAs shell.

2. Properties of Semiconductor Materials

In crystalline materials such as III-V semiconductors, the atoms are arranged in a periodic structure. The crystal structure is of great importance for the electronic and optical properties of the materials, which will be briefly described in this chapter.

2.1. Crystal Structure

Bulk InAs and InP are stable in the cubic ZB structure [41]. Interestingly, the III-V nanowires can be formed in the WZ structure which has hexagonal symmetry [42]. The WZ phase could be advantageous in some applications, since the symmetry of the crystal phase influences the optical and electronic properties, such as the polarization of emitted photons [43] and effective mass of the charge carriers [44]. Heterostructures formed from alternating ZB and WZ phases have also been realized in InAs nanowires, which can be used to form quantum dots [45][46]. Both ZB and WZ are formed due to the tetrahedral bonding between the group III and group V atoms. In these bonds, each group III atom is centered between four group V atoms. The crystal structures and lattice parameters of ZB and WZ are shown in Fig. 2.1.

The positions of the atoms in a crystal lattice (direct lattice) are found by shifting the unit cell of the structure by an integer number, n_i , in the directions of the lattice vectors, \mathbf{a}_i . For a cubic crystal, the translations are thereby written as,

$$\mathbf{R} = n_1 \mathbf{a}_1 + n_2 \mathbf{a}_2 + n_3 \mathbf{a}_3. \tag{2.1}$$

In cases where the interaction of the crystal atoms and wave phenomena such as light or electrons is considered, it is useful to express the lattice in reciprocal space. The reciprocal lattice of the direct lattice, is a set of points given by the set of reciprocal space vectors \mathbf{G}_{hkl} . The vectors are composed of reciprocal lattice vectors \mathbf{b}_i , as shown by the equation

$$\mathbf{G}_{hkl} = h\mathbf{b}_1 + k\mathbf{b}_2 + l\mathbf{b}_3, \tag{2.2}$$

where h, k, and l are integers known as Miller indices. Any **G** is related to the lattice vectors **R** by the following equation, which is the definition of the reciprocal lattice,

$$e^{i\mathbf{G}\cdot\mathbf{R}} = 1. \tag{2.3}$$

A crystal plane is identified by specifying a normal vector to the plane in reciprocal space, using the Miller indices. The distance between the direct lattice planes with indices h, k, l, is denoted d_{hkl} and can be found by the inverse of the reciprocal lattice vector **G**_{hkl} by

$$d_{hkl} = 2\pi/|\mathbf{G}_{hkl}|. \tag{2.4}$$

In the WZ structures the indices are instead h, k, i, l. The WZ unit cell is hexagonal and the first three lattice vectors \mathbf{a}_1 , \mathbf{a}_2 , and \mathbf{a}_3 lie in the (0001) plane with 120° separation, while \mathbf{a}_4 (**c**) is perpendicular to the (0001) plane. The [111] direction in the ZB structure corresponds to the [0001] direction in the WZ structure. However, the plane distances in InP and InAs in this direction is found by X-ray diffraction to be longer in WZ compared to ZB [47][48].

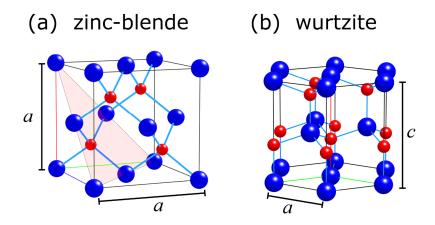


Figure 2.1. (a) Schematic representation of the unit cell of a zinc-blende III-V semiconductor, having a cubic structure, where the blue atoms represent the group III and the red atoms represent to group V elements. a indicates the lattice parameter. Chemical bonds are shown by the blue lines and the (111) plane is drawn as a red triangle. (b) The atomic structure of the hexagonal wurtzite crystal structure. a and c indicate the lattice parameters.

Growth of III-V nanowires is commonly performed along the <111> directions, which is along the space diagonal of the cubic unit cell. Single crystal WZ structure can be obtained in nanowires with small diameters, and under selected conditions during MOVPE growth [49]. However, in many cases of Au seeded nanowire growth, the difference in energy of formation between the ZB and WZ structure is so small that uncontrolled switching between the two structures along the nanowire growth axis occurs [50]. This process results in so called stacking faults.

The difference between ZB and WZ structures is the atomic layer stacking A, B and C of the (111) or (0001) planes. In the ZB structure, the stacking sequence is ABC, while in WZ it is AB. In Fig. 2.2, the two structures are shown and the atomic layers A, B and C are indicated.

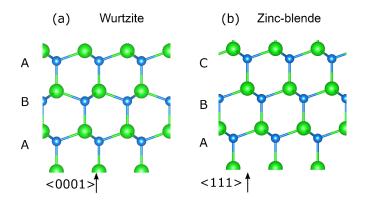


Figure 2.2. The atomic layers and chemical bonds in the WZ and ZB structures are shown in (a) and (b), respectively. (a) The stacking sequence of A and B layer types along the [0001] direction result in WZ structure. (b) The ABC sequence along the [111] direction result in the cubic ZB structure.

2.2. Electronic Structure

Semiconductors typically exhibit electrical conductivity in between that of insulators and metals. The electrical conductivity of all three types of materials is due to the energy band structure, which is the relation between the total energy E and the wave number k of the electron in the crystal. In the III-V semiconductors, valence electrons form chemical bonds, which results in delocalized electrons. As the bonds are formed between the neighboring atoms, the narrow atomic levels of the isolated atoms widen to bands [51]. The bands are separated by a bandgap E_g , as shown in Fig. 2.3.

At temperatures close to zero K, electrons occupy all states in the valence bands and the states in the conduction bands are empty. This gives a very low electrical

conductivity since the electrons in filled bands are not free to accelerate and cannot contribute to a net current.

The electronic dispersion relation E(k) can be found by solving the time independent Schrödinger equation (S.E), with a periodic potential V(r) created by the lattice atoms [52],

$$H\psi(r) = \left[\frac{-\hbar^2}{2m}\nabla^2 + V(r)\right]\psi(r) = E\psi(r).$$
 (2.5)

The solutions to the S.E are periodic wave functions (Bloch functions) of the form $\psi_k(r) = e^{ik \cdot r} u_k(r)$ [52], which are propagating plane waves multiplied by a periodic function $u_k(r)$.

Close to the edge of the conduction band, E_{CB} , and valence band, E_{VB} , the dispersion relation of the wave functions can be approximated to parabolic functions, which are shown schematically for WZ InAs [53][54] in Fig. 2.3. The kinetic energy of electrons in a parabolic band can be written as,

$$\varepsilon(k) = \frac{\hbar^2 k^2}{2m^*}.$$
(2.6)

In the WZ structure, the valence bands are separated at k = 0 into three bands, labeled A, B, and C. The upper valence band, A, as shown in Fig. 2.3, is separated from B by the crystal-field splitting ΔE_{CF} . This splitting arises due to the lack of spatial symmetry in the crystal, since the [0001] direction (z) is not identical to the perpendicular directions in the x-y plane of WZ crystals [44]. The splitting is not found in the ZB structure [55]. Below these bands is the C band which is separated from the A and B bands by the coupling of the electron spin and orbital angular momentum (spin-orbit coupling), as indicated by the A-C difference of ΔE_{SO} in Fig. 2.3.

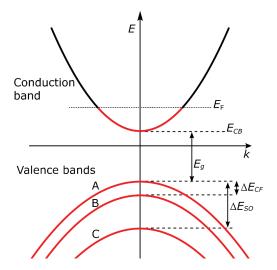


Figure 2.3. Schematic illustration of the parabolic bands of a wurtzite semiconductor, such as InAs. States that are occupied by electrons are shown by solid red. E_{CB} indicates the conduction band edge. The valence bands are split into the bands, A, B, and C. The Fermi level E_F is located above E_{CB} due to electron accumulation at the InAs surface.

In order to achieve simplified transport calculations we may in many cases resort to a semi-classical description that builds on replacing the mass of the electrons m_e with an effective mass m_e^* . The effective mass is related to the curvature of a band as described below. The velocity of the electrons is obtained from the group velocity v_g of the electronic wave functions, given by the derivative of the band [52],

$$v_g(k) = \frac{\hbar^{-1} \partial \varepsilon(k)}{\partial k}.$$
 (2.7)

The acceleration of the electrons can then be related to the time derivative of the crystal momentum, $\hbar k$, and the effective mass, by Newton's second law,

$$\frac{\hbar}{m^*}\frac{dk}{dt} = \frac{dv_g}{dt} \Leftrightarrow$$
(2.8)

$$\frac{1}{m^*} = \hbar^{-2} \frac{\partial^2 \varepsilon(k)}{\partial k^2}.$$
(2.9)

The real effective mass varies with k since the bands are not exactly parabolic, which means that a constant effective mass can be assumed only for small range of k.

At finite temperature T, a small fraction of the electrons in the valence band are thermally excited to the conduction band, leading to larger electron density in the conduction band for higher temperatures. The probability of an energy level being occupied by an electron is given by the Fermi-Dirac distribution function F,

$$F = (1 + e^{(E - E_{\rm F})/k_{\rm B}T})^{-1}, \qquad (2.10)$$

where *E* is the energy, $k_{\rm B}$ is the Boltzmann constant, and $E_{\rm F}$ is the Fermi level (where F = 0.5), which is also denoted electrochemical potential μ . In Fig. 2.4, the Fermi function is plotted for T = 300 K and T = 50 mK, where the corresponding thermal energy $E_{th} = k_{\rm B}T$, is 26 meV and 4.3 µeV, respectively.

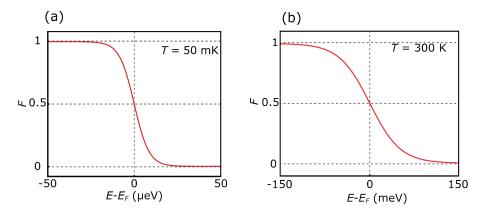


Figure 2.4. The Fermi-Dirac distribution function *F*, is shown in (a) for the temperature T = 50 mK and in (b) T = 300 K. Note the different scales of the horizontal energy axis in (a) and (b).

The unoccupied states close to the top of the valence band are referred to as holes, and also contribute the charge transport. These are quasiparticles with a positive charge *e* and positive effective mass of $m_h^* = -m_e^*$ (of the valence band). The holes therefore move along the electric field direction and add to the total current.

The Fermi level is located close to the center of the bandgap in a semiconductors without impurities (intrinsic). At low temperatures, such as 1 K, there are thereby almost no electrons excited to the conduction band. The charge carrier density in the conduction or valence band can be increased or decreased by several methods. Dopant atoms, that are elements with a different valency, can be added to the crystal. These atoms become ionized and release or bind one or more electrons, thereby

changing the number of free carriers. Acceptor dopants (*p*-type) bind electrons and releases holes to the valence band. Donor dopants (*n*-type) on the other hand release electrons to the conduction band. Localized charges can also change the carrier density by causing accumulation of carriers that are attracted to the charge. For instance, a gate electrode with a potential applied between the semiconductor and the metal cause accumulation of charges at the surface of the semiconductor. In intrinsic InAs, surface states pin the Fermi level above the conduction band edge [56], leading to a large electron density at the surface even at low temperatures.

In heterostructures of InP-InAs or InP-InAsP, the conduction and valence band edges are offset (type-I offset) as shown in Fig. 2.5. The conduction band in InAs is lower in energy than the conduction band of InP, leading to confinement of electrons to InAs. The valence band exhibit opposite offset, which confine holes to InAs.

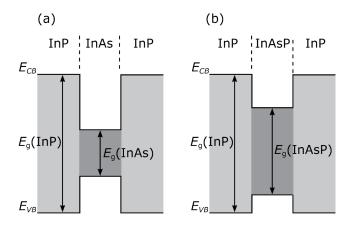


Figure 2.5. Band offsets of InP-InAs and InP-InAsP heterostructures. (a) The offset of the conduction band edges result in potential barrier for electrons in the InAs conduction band. (b) The conduction band offset of InAsP-InP is smaller than that of InAs-InP, and increases with the fraction of As in InAsP.

In electron transitions between the conduction band and valence band, photons can be emitted. These photons have the energy of the difference between initial state in the conduction band and the final state in the valence band. Spectroscopic measurements of photoluminescence (PL) is used in paper I to determine the bandgap dependence on strain. In the PL measurements, electrons in the valence band are first excited to the conduction band by laser light. After this, they lose kinetic energy by thermalization and thereby reach an energy close to the conduction band edge. There, the electrons recombine with holes in the valence band, and emit one photon each.

2.3. Introduction to Charge Transport

We first consider the electrical conduction in a large scale semiconductor channel contacted by two contacts. The electrical conductivity σ relates the current density J to the external electric field E. The field is given by $E = \Delta V/L$, where ΔV is the voltage difference between the two contacts and L is the distance between them. The current density is then $J = \sigma E$.

The electrical current in a semiconductor is carried by the electrons in the conduction band and by the holes in the valence band. The charge carriers are accelerated by the electric field, and due to imperfections and other sources of scattering in the crystal, they travel in average a distance l (mean free path) until the gained momentum is lost. The mean time since the last collision is denoted τ and the mean velocity increase is the drift velocity v_d . For the electrons, this leads to the current density, $J = -env_d$, where $v_d = -eE\tau_e/m_e^*$, e is the elementary charge, n is the electron volume density, and the subscript e refers to electrons. The conductivity expression for holes and electrons combined is then [57]

$$\sigma = \frac{e^2 n \tau_e}{m_e^*} + \frac{e^2 p \tau_h}{m_h^*} = e n \mu_e + e p \mu_h$$
(2.11)

where p is the carrier volume density of the holes, and the subscripts h refers to holes. The mobility, μ , is commonly used to describe the conductivity of a diffusive semiconductor.

At low temperatures and short distances, the above diffusive mechanics is not always valid. Particularly when L < l the carriers are not diffusively scattered as they travel the length of the channel. This is referred to as ballistic transport. The transport at low temperature is characterized by the relative size of the four length scales which are, the system size L, the elastic mean free path, l_e , the Fermi wavelength, $\lambda_{\rm F} = 2\pi/k_{\rm F}$, and the phase coherence length $l\varphi$. The momentum and phase of the electron wave function is conserved during elastic scattering but the direction of propagation is randomized. The preservation of the phase means that quantum interference effects are possible at larger distances than l_{e} . Elastic scattering is often caused by impurity ions in the crystal and the surface of the material, since these do not give rise to time dependent potentials [58]. Inelastic scattering on the other hand, result in loss of the kinetic energy and momentum. It also randomizes phase, resulting in a limited phase coherence length $l\varphi$. Such events are typically due to electron-phonon scattering [58]. Furthermore, the electronelectron scattering also produces a loss of phase coherence [59]. The Fermi wavelength, is relevant for $L \approx \lambda_{\rm F}$, as the quantum confinement effect then appears. The length l_e can be set by the density of impurity ions, and the surface scattering. Surface scattering is likely the main contribution in nanoscale devices due to the non ideal surfaces and short distances to the surfaces from any point in the device. For instance, in the case of two-dimensional electron gas (2DEG) where highly ordered surfaces are prepared, l_e can reach values > 300 µm [60] and mobility > 10⁷ cm²/Vs has been reported [61]. The collisions are then spaced several 100 µm apart. In nanowires, such as InAs and InGaAs nanowires, the mean free path has been shown to be in order of 100-200 nm [8][22]. These mean free path values are likely to be limited by surface scattering. The effect may be mitigated by reducing the carrier density close to the surface. It has been shown that a mobility of 11500 cm²/Vs can be obtained for InAs nanowires covered by a thin InP shell [30], which is likely due to passivation of the surface of the InAs nanowires [30][62].

For the case of InAs and for high *n*-type doping density in the semiconductor, the Fermi level is above the conduction band edge, E_{CB} , as discussed above, $(E_{\rm F} > E_{CB})$. For the low-temperature transport measurements considered in this thesis, the thermal energy of the electrons is considered small compared to the Fermi level, and $(E_{\rm F} - E_{CB}) >> k_B T$. This means that the electrons participating in transport are located close to $E_{\rm F}$, where their velocity is $v_{\rm F} = \sqrt{2(E_{\rm F} - E_{CB})/m_e^*} = \hbar k_{\rm F}/m_e^*$. The mean free path l and scattering time τ are then related by $l = v_{\rm F}\tau$. The conduction band pinning at the InAs surface results in a Fermi velocity of $v_{\rm F} \approx 1 \times 10^8$ cm/s for ZB crystal phase [63]. However, the effective mass of WZ InAs is predicted to be larger than that of ZB phase, with $m_e^* \approx 0.04m_e$ [53], resulting in a lower Fermi velocity for the same $E_{\rm F}$. It, however, remains close the $v_{\rm F}$ of typical metals, for instance Al, which has $v_{\rm F} \approx 2 \times 10^8$ cm/s [64].

3. Growth of Nanowires

In this chapter, some of the key principles of the growth process will be discussed, with main focus on the growth of InP, InAs and InAsP by the precursors trimethylindium, phosphine and arsine. The MOVPE growth of nanowires consists of both chemical and physical processes that involve several steps of chemical reactions and transport (mass flow) of the reactants. To steer the growth of the crystals and the specific events occurring in the process, the supplied precursor gas flow and the growth substrate temperature is commonly controlled, as input parameters.

3.1. Reactor and Growth Materials

The nanowires studied in this thesis were grown by metal-organic vapor phase epitaxy (MOVPE) which also is referred to as metal-organic chemical vapor deposition (MOCVD). This method is the most common for epitaxial deposition of III-V semiconductors in the industry and can currently be scaled for simultaneous processing of about 5 wafers of 200 mm diameter in a single reactor unit.

The growth system used for the current work is equipped with a horizontal flow quartz tube reactor cell with a graphite susceptor for heating the growth substrates with a maximum diameter of about one inch. The susceptor which function as sample holder, is heated by an RF coil through induction, to the desired growth temperature, while the rest of the reactor cell is cold. A schematic of the growth system is shown in Fig. 3.1. During the growth, hydrogen gas (H₂) with a pressure of 100 mBar and a flow of 5.8 l/min is used as a carrier gas. The chemical elements used in the growth are supplied through the molecules of the source gases. These are introduced in a mixture with the carrier gas, which then flows through the reactor over the susceptor. The gas mixture composition can be modulated as a function of time, for instance to grow abrupt heterostructures, composition gradients or doping gradients.

The group III elements can be supplied in the form of organometallic precursors, such as trimethylindium (TMIn) having the chemical formula (CH₃)₃In. The metalorganic liquids or solids are stored in bubblers, which are containers designed so that the carrier gas can be passed through the liquid or powder and mix with the vapor of the compound. In the case of TMIn, the temperature used in this work is 17 °C where it is in the solid phase. The group V sources, phosphine (PH₃) and arsine (AsH₃), are the metal hydride gases, and can be directly injected into the reactor. To control the flow of all gases, a set of mass flow controllers (MFCs) are used. Essentially they are computer controlled valves that modulate the gas flows rates.

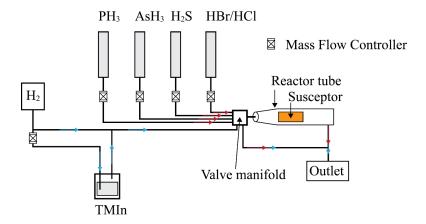


Figure 3.1. Schematic diagram of the MOVPE system used for nanowire growth. The growth substrate is placed on top of the susceptor in the quartz tube reactor. The susceptor is heated by an induction coil wrapped around the reactor. The metal hydride gases, dopant source gas H_2S , and etchant gas HBr and HCl, are stored in gas tubes. The flowrates from the tubes are controlled by MFCs. The TMIn gas is carried by the H_2 gas flow, which goes into the TMIn bubbler, and collects a small amount of TMIn as it is mixed with the vapor of the TMIn, the gases then proceed to the valve manifold. Through the valve manifold, the gases can be injected into the reactor as the growth process is activated, or be sent to the ventline.

3.2. Crystal Growth by Metal-Organic Vapor Phase Epitaxy

The process of InP growth starts with TMIn and PH_3 being injected into the reactor and then transported towards the growing crystal surface by diffusion. The precursor molecules are adsorbed and dissociated by pyrolysis at the hot surface (pyrolysis can also take place in gas phase), the atoms finally incorporated into the crystal, typically at an atomic step site where the number of chemical bonds are larger than at the flat surface. Thus, after many intermediate reaction steps, solid InP and methane gas and are formed, the overall reaction can be written

$$(CH_3)_3In(g) + PH_3(g) \rightarrow InP(s) + 3CH_4(g),$$

where g refers to gas phase and s refers to solid phase. At low temperatures, the thermal energy of the reactant is not large enough overcome the potential barrier for precursor pyrolysis and the nucleation barrier. In this case, the growth is kinetically limited. The rate (k) of a kinetically limited process is proportional to an exponential factor with temperature dependence following an Arrhenius function [65], $k = Ae^{-E_a/k_BT}$ where A is a pre-exponential factor, E_a is the activation energy, k_B is the Boltzmann constant and T is the absolute temperature. In higher temperatures, the potential barriers are overcome by the reactants, the growth rate can instead be limited by the transport of the reactants towards the crystal. In the electronic applications, a low concentration of impurity atoms is preferred. One important impurity in MOVPE grown materials is carbon, which originates from to the use of the metal-organic precursors. The carbon affects the III-V materials by acting as a dopant [66] which introduces some difficulty for the fabrication of electronic devices where the doping is undesirable. The carbon atoms may be incorporated into the crystal by incomplete pyrolysis of TMIn.

To understand the driving force for crystallization, the thermodynamics of the system need to be considered. For the volume of the solid crystal to form in the presence of the gas phase, the total change of Gibbs free energy G is required to be negative during the transfer of atoms from the gas phase to the solid phase. A convenient quantity is therefore the derivative of G with respect to the number of atoms, at constant temperature and pressure, which is known as the chemical potential μ .

The driving force of the crystal growth is the non-equilibrium state, where the reactants in gas phase have a higher chemical potential than the atoms in the solid crystal. The difference in chemical potential is given by $(\Delta \mu = \mu_s - \mu_v)$ where subscripts *s* refers atoms in the solid phase, and *v* atoms in the vapor phase. By elevating μ_v , it is possible to increase the chemical potential difference. This can be achieved by increasing the pressure of the gas phase relative to the equilibrium pressure for a certain temperature, as shown for a single component system [65] by

$$\Delta \mu = -k_{\rm B}T \ln(p/p_e) \tag{3.1}$$

where $k_{\rm B}$ is the Boltzmann constant and T is the absolute temperature, p is the pressure and p_e is the equilibrium pressure (at temperature T).

3.3. Au Particle Seeded Nanowire Growth

The growth of the nanowires by liquid Au seed particles follows the vapor-liquidsolid (VLS) mechanism, which was proposed by Wagner and Ellis in 1964 who observed growth of Si wires nucleated by Au particles [26]. The method was later applied to growth of GaAs and InAs nanowires [27], and GaAs-InAs axial nanowire heterostructures [67]. The Au particle alloys with the group III atoms and form an eutectic melt with a high concentration of the group III atoms, this allows for growth at the droplet/substrate interface with an increased rate for a specific temperature range where the growth on the bare substrate can be relatively low. Recent experiments have shown that nanowire growth also can occur while the seed particle is in the solid state, by the process of solid state diffusion which is known as vaporsolid-solid (VSS) growth [68]. In the VLS process, the group-III (Indium in this work) atoms that are initially adsorbed on the substrate or nanowire side facets, diffuse towards the Au droplet where they accumulate due to the locally lower chemical potential. The growth process is show schematically in Fig. 3.2. It has been suggested that VLS growth proceeds by nucleation of an atomic layer at the triple phase boundary (TPB) where the liquid seed particle, the vapor, and the solid crystal meet [50]. The precise dynamics of the nucleation in VLS growth is currently under research. However, recent in situ transmission electron microscopy (TEM) studies of growing Au seeded GaAs nanowires at low pressure, show that axial growth of the nanowires proceeds layer by layer and that nucleation initiates at the TPB, when the WZ structure is formed [69].

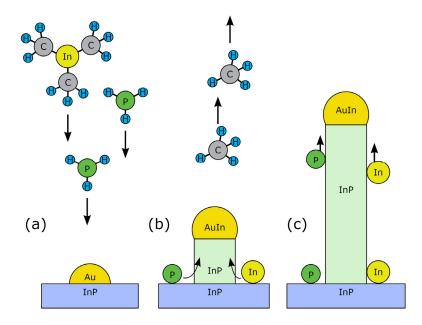


Figure 3.2. Schematic illustration of nanowire growth by Au seed particles. (a) Precursor molecules TMIn and PH₃ diffuse down towards the InP substrate. (b) Precursors decompose by pyrolysis at the substrate surface and are then transported towards the Au particle by surface diffusion. The InP nanowires grow by incorporation of the In and P atoms at the InP-AuIn interface. (c) The growth continues axially due to the larger growth rate at the InP-AuIn interface, however growth can also take place at other positions where an InP surface is exposed, leading to radial growth of the nanowire.

3.4. Au Seeded InAsP-InP Core-Shell Nanowires

In experiments carried out in papers I and II, the structural properties of WZ InAsP-InP core-shell nanowires were investigated by X-ray diffraction, and transmission electron microscopy. Photoluminescence spectroscopy was used to determine the bandgap of the nanowires. The method used to grow the nanowires was described by Wallentin *et al* [70]. First, the Au seed particles were deposited on the InP (111)B substrates by an aerosol technique [71] resulting in particles with 40-45 nm diameter. The core-shell nanowires were then grown in a single growth run, where the InAsP cores were first grown at 420 °C. The composition of InAsP was controlled by the arsine to phosphine flow ratio. In this case, a series of samples with varied flow ratio were grown to obtain a flow ratio calibration curve of the InAsP core nanowires were found to exhibit tapering, with the base ~ 5 nm larger in diameter than the top. Typically, axial and radial growth in combination lead to

a cone shaped nanowire, however, due the use of HBr gas during the core growth process, the growth in radial direction can be minimized which results in less tapering [72]. The growth of the InP shell was performed after interrupting the core growth by turning off the TMIn flow. The InP shell growth temperature was set to 550 °C in order to promote the radial growth on the sides of the nanowires and decrease the axial growth rate. On the top of the nanowires it is observable that an InP particle is formed with an irregular shape, see Fig. 3.3(c-g). This particle may form when the Au particle becomes unstable during the shell growth conditions.

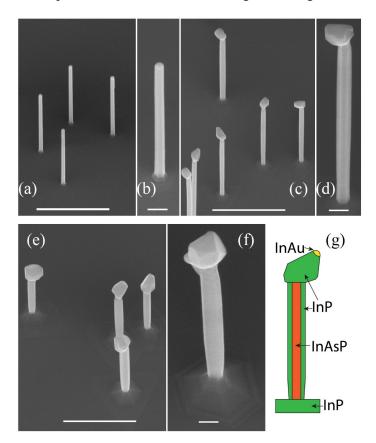


Figure 3.3. (a-b) SEM images of InAsP nanowires with a diameter of ~ 42 nm, grown by Au seed particle assisted MOVPE growth. (c-d) InAsP-InP core-shell nanowires with a shell thickness of ~ 15 nm. (e-f) InAsP-InP core-shell nanowires with a shell thickness of ~ 25 nm. (g) Schematic illustration of a core-shell nanowire. The scale bars in (b), (d), and (f) are 100 nm and in (a), (c), and (e) they are 1 μ m. The figure is adapted from paper I.

The crystal structure of the nanowires is WZ, as can be determined from the TEM analysis. Examples of TEM images of the core-shell nanowires are shown in Fig. 3.4(a-b). The density of stacking sequence faults was ~ $20-50/\mu$ m. Importantly, in the shell growth on the nanowire side facets, the stacking sequence is typically locked. The InP shell and the InAsP core therefore have the same crystal structure, and the stacking fault, marked by the red arrow in Fig. 3.4(a) continues from the core to the shell.

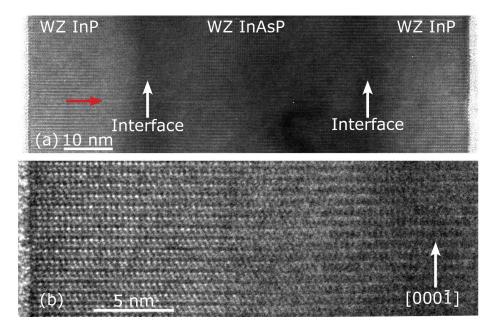


Figure 3.4. (a) High resolution TEM image of a WZ InAsP-InP core-shell nanowire. The interface between core and shell is indicated by the vertical arrows. The horizontal red arrow indicates a stacking sequence fault where the AB stacking sequence is broken. The stacking sequence is seen to extend through the full cross section of both core and shell. (b) High resolution TEM image of the same nanowire as in (a), at higher magnification. The arrow indicates the crystallographic direction $[000\overline{1}]$ which is the same in (a). The images were acquired by Dr. Maria E. Messing.

3.5. Selective Area Nanowire Growth

Crystal growth in the nanowire geometry can be performed by the selective area growth (SAG) method, where essentially, a single crystal growth substrate is covered with a thin mask and the growth occurs selectively in openings of the mask, where the substrate is uncovered, as illustrated in Fig. 3.5. To obtain nanowire growth, the substrate is typically covered by a SiO_2 or SiN_x mask with circular

openings with the same diameter as the desired nanowires. The openings can be fabricated by nanoimprint lithography or electron beam lithography (EBL) using a resist layer, followed by etching in the resist pattern. In contrast to Au seeded growth, there is no metal droplet present in SAG, which eliminates the possibility of Au contamination. Fabrication of long, high aspect ratio GaAs [73] InAs [74] and InP [75] nanowires of high crystal quality has been demonstrated using this method, as well as core-shell nanowire such as InP-InAs [76].

Initially, the geometry of the nanowires is defined by the geometry of the mask openings, the vertical growth proceeds by selective growth on the exposed nanowire facets. The shape of the final crystal is determined by the relative growth rates of these facets. High growth rate is obtained for facets that have high surface energy [77]. The InP nanowires grown by SAG, grow preferentially in the [111] direction [78]. The crystal structure of the SAG InP nanowires can be controlled by the use growth temperature and V/III flow ratio. A growth temperature of 730 °C and V/III ratio of 80 resulted in pure WZ InP nanowires can be grown with as large diameter as 600 nm [31]. These nanowires can exhibit good optical quality as was found from the quantum efficiency of the photoluminescence [31].

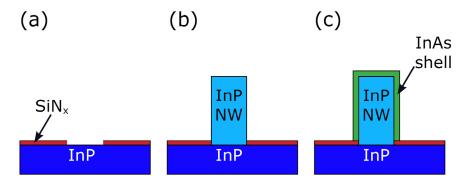


Figure 3.5. (a) InP growth substrates are prepared with a layer of SiN_x. The layer is then etched down in reactive ion etching with a patterned EBL resist as etch mask, this results in openings in the SiN_x. (b) InP nanowires are grown in the openings of the SiN_x mask selectively. The growth is seen to be vertical due to anisotropic growth rate of the exposed facets. (c) InAs growth is performed at reactor conditions where isotropic growth occurs for all exposed facets.

3.6. Selective Area Growth of InP-InAs Core-Shell Nanowires

In this work, pure WZ InP-InAs core-shell nanowires have been fabricated by the selective area technique described above and in the methods of paper III. To prepare substrates for growth, first the InP [111] substrate with a SiN layer of ~ 27 nm thickness was spin-coated with an EBL resist. The resist was exposed in EBL and then developed. A square array of circular openings, 50-60 nm in diameter, with 1 μ m pitch was patterned. The samples were then etched by oxygen plasma ashing to widen the holes to ~ 100 nm in diameter and remove resist from the bottom of the openings. The substrates were then etched in reactive ion etching to remove the SiN film in the openings. The InP core diameter was controlled by the diameter of SiN openings. The method allows a high degree of flexibility as the nanowire diameters are easily varied by tuning the plasma ashing time. A cleaning procedure was then performed. First the resist was removed by the solvent Remover 1165 and then plasma ashing was performed to remove resist residues. Additionally, HF diluted in water can be used to further etch the SiN surface in order to minimize residues and contamination from the processing.

The growth of the WZ InP nanowires was performed at 710 °C with a III/V precursor flow ratio of ~ 2000 . Such nanowires showed vertical sidewalls, with a diameter decrease of less than 1 nm/um growth length, owing to the minimal growth on the side facets. The TMIn flow was turned off to end the InP core growth. The temperature was lowered to 460 °C and the phosphine was turned off and arsine was turned on, about 1 min before turning on TMIn, which initiates the InAs growth. The InAs shell was here grown by using a V/III ratio of 125 and lower temperature to yield a uniform growth on the side of the InP nanowires [77]. In SEM images taken after growth of InP core samples, it was observed that the side facets correspond to WZ $(1\overline{1}00)$ by comparing to the cleaved edge of the ZB substrates which are of the {110} plane family [79]. The InAs-InP core-shell nanowires exhibited the same facet orientation, as shown in Fig. 3.6. The shell morphology was however mostly of triangular cross sections. For some growth samples, a mix of roughly equally many hexagonal and triangular shells where found while other growth samples showed a majority of triangular shells particularly for InP core diameter < 120 nm. Similar triangular shapes in InP-InGaAs shell growth was previously reported by Heurlin et al [80]. In the present work, InP-InAs nanowires are investigated with the motivation that 1D subbands can be confined to the corners of the triangular InAs shell, created by the quantum confinement effect. This will be discussed in chapters 7 and 8.

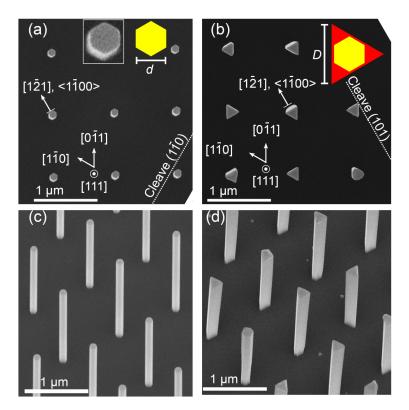


Figure 3.6. (a) InP nanowires grown by selective-area MOVPE, imaged by a SEM along the surface normal direction of the growth sample. The nanowires show a hexagonal cross section with side facets oriented in <1100> directions. The cleaved side of the InP (111)A substrate is indicated by the dashed line. (b) InP-InAs core-shell nanowires imaged as in (a). The triangular side facets are seen to be oriented in the same crystallographic directions as the side facets of the core nanowire in (a). The inset cross-section schematic shows the orientations of the core and shell facets. The yellow hexagon represents the InP core and the red triangle represents the InAs shell. (c) Tilted view (30°) of the InP nanowires. (d) Tilted view (30°) of the InP-InAs core-shell nanowires. (a), (b), and (d) are adapted from paper III with permission of AIP Publishing.

TEM analysis of the selective area grown nanowires was used to investigate their crystal structure. It was found that the nanowires exhibit pure WZ structure with no stacking faults except at the very top facet, at the interface between the InP core and InAs shell. This interface is shown in the TEM image of Fig. 3.7.

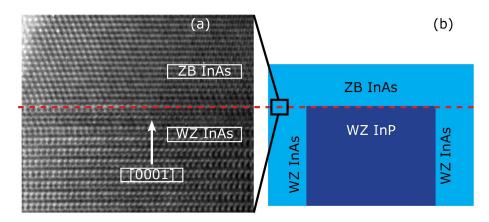


Figure 3.7. (a) High resolution TEM image of an InP-InAs core-shell nanowire grown by selective area MOVPE, showing a transition from WZ to ZB structure in the InAs shell, close to the top facet of the nanowire. This transition from WZ to ZB in the axial direction [0001] is maintained throughout the (0001) plane at the position indicated by the red dashed line. The transition is possible since the WZ InP core ends as indicated by the red dashed line. ZB InAs shown above the line was grow vertically on top of the InP core as shown in (b), therefore, obtaining a stacking sequence preferential to the growth conditions of InAs shell. The TEM image was acquired by Dr. Maria E. Messing.

4. Strain in Core-Shell Nanowires

In this chapter, mechanical strain is first described in general terms. The built in strain in core-shell nanowire heterostructures is then discussed.

4.1. Introduction to Strain

The strain component ε_{xx} along the x-axis in a crystalline material can be understood as a change of the atomic plane spacing Δd relative to the equilibrium spacing d_0 , the strain is then written as $\varepsilon_{xx} = \Delta d/d_0$. For describing the strain in 3D, a matrix is used, and the components of this matrix are found by the derivative of the displacement vector field $\mathbf{u}(x, y, z)$. This vector field gives the distance and direction that each point in the material has been shifted by an elastic deformation. The components of the strain matrix are given by

$$\varepsilon_{ij} = \frac{1}{2} \left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i} \right),\tag{4.1}$$

where x_i and x_j are the spatial Cartesian coordinates, u_i and u_j are the components of the displacement field. The indices refer to the Cartesian axes. In the Voight notation, the strain components are arranged in a vector of six components, given by

$$\boldsymbol{\varepsilon} = \{\varepsilon_{xx}, \varepsilon_{yy}, \varepsilon_{zz}, 2\varepsilon_{yz}, 2\varepsilon_{xz}, 2\varepsilon_{xy}\}^{\mathrm{T}}.$$
(4.2)

The linear relation between stress and strain, (Hook's law), can be written as an equation where the material specific elastic constants form the matrix C. Hook's law is then written as

$$\boldsymbol{\sigma} = \mathbf{C}\boldsymbol{\varepsilon},\tag{4.3}$$

where $\boldsymbol{\sigma}$ is the stress, given by

$$\boldsymbol{\sigma} = \{\sigma_{\boldsymbol{\chi}\boldsymbol{\chi}}, \sigma_{\boldsymbol{\gamma}\boldsymbol{\gamma}}, \sigma_{\boldsymbol{Z}\boldsymbol{Z}}, \sigma_{\boldsymbol{\gamma}\boldsymbol{Z}}, \sigma_{\boldsymbol{\chi}\boldsymbol{Z}}, \sigma_{\boldsymbol{\chi}\boldsymbol{\gamma}}\}^{\mathrm{T}}.$$
(4.4)

One important case is the epitaxial thin-film growth of a semiconductor onto an atomically flat and thick (~ 100 μ m) substrate. A normal vector along the *x*-axis, perpendicular to the substrate surface is first considered. When the growing film has a smaller lattice parameter than the substrate material, the resulting strain component in the *x*-axis direction, ε_{xx} , is negative in the film due to the Poisson effect. This can be derived from the condition that the stress in *x*-direction is zero [65]. However, for directions perpendicular to the *x*-axis (in-plane), the film material expands to match the substrate lattice parameter, resulting in positive ε_{yy} and ε_{xx} .

From Hook's law we see that elastic strain requires mechanical energy (strain energy). As the thickness of the growing layer increases over a critical value, the strain energy becomes too large, leading to formation of defects such as dislocations which release the strain energy.

4.2. Strained Core-Shell Nanowires

For core-shell nanowire heterostructures, the strain along the growth axis is similar to the in-plane strain of a heterostructure composed of two thin films that are decoupled from any substrate. The relative thicknesses and the elastic constants of the two film materials determine the final strain state. When the crystal structure is coherent (free from defects in the lattice and at the interface) the two materials are strained so that the positions of the atoms are shifted as illustrated in Fig. 4.1, following [65]. The atomic spacing in the in-plane directions is in-between that of the two bulk values.

The core-shell nanowire structure is different from the thin film case, as the core material is embedded in the shell. The shell can therefore apply stress to the core in both the radial and the axial directions [81]. As will be discussed below, for the strain of core material with a larger lattice parameter than that of the shell, a compressive strain results in both the cross-section plane and the direction of the growth axis.

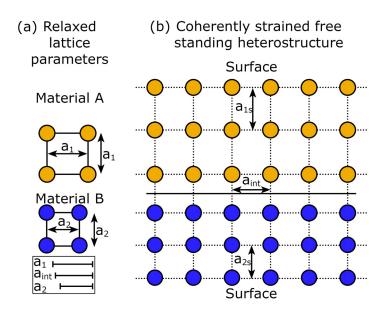


Figure. 4.1. (a) The lattice parameter a_1 of material A and a_2 of the material B are related by $a_1 > a_2$. (b) Schematic illustration of the epitaxial interface of a free-standing thin film heterostructure, viewed along the interface plane (solid black line), showing the positions of the atomic columns. The distance between atoms in the in-plane direction, denoted a_{int} is the same in both materials due to the epitaxial interface, where $a_1 > a_{int} > a_2$. The atomic spacing in the vertical direction in material A, a_{1s} , is elongated ($a_{1s} > a_1$), and for material B it is compressed ($a_{2s} < a_2$), by the action of the Poisson effect, due to the absence of stress in this direction.

Nanowire heterostructures show potential for use in applications since dislocations are less likely to form, as compared to planar heterostructures. It has been shown that the strain energy of a radially grown shell on a nanowire core is lower compared to that of a thin film grown on a thick substrate. This is due to the cylindrical geometry [82] and the small elastic energy required to strain a core with a diameter of a few tens of nanometers [83][33]. In the case of the core-shell nanowires, it is thereby possible to extend the radial shell growth to larger thickness, t_s , and still avoid the formation of misfit dislocations. A critical core diameter D_c is furthermore predicted [83], for core diameters below which, the nanowires can be grown dislocation free even for infinite shell thickness. The D_c depends on the lattice parameter misfit f_0 . For the WZ InAs-InP system with $f_0 = 3.2\%$, D_c is predicted to be about $D_c \approx 30$ nm. For other III-V materials such as InP-GaAs, GaSb-InSb, GaAs-GaP, D_c was observed to decrease with increasing mismatch following $D_c \propto$ $f_0^{-2.5}$ [33]. Generally, dislocation defects can be formed when the shell thickness of the core-shell nanowire is large enough so that the strain energy exceeds the energy of defect formation [84]. The critical shell thickness, therefore, depends on the

accumulated strain energy in both core and shell. An increase of the core diameter thereby results in a decrease of the critical shell thickness. However, the exact energy of defect formation naturally depends on the type of defect. Detailed experimental observation of dislocations have been accomplished by TEM analysis of the Ge-Si core-shell nanowires [85] and GaAs-Si core-shell nanowires [86], as well as in InAs-InP and GaAs-GaP core-shell nanowires [33].

Experimental studies of the strain state ε in core-shell nanowires of various material combinations have been performed by several groups. One of the methods for this purpose is photoluminescence (PL) spectroscopy. Even a small strain, such as 0.1% can result in ~ 10 meV change of the bandgap and therefore shifts of the PL spectra. This method was applied to GaAs–GaInP core-shell nanowires which showed changed the bandgap of the GaAs core from 1.37 to 1.61 eV [87]. An increased PL intensity due to passivation of the GaAs surface by the shell was also shown [87]. In InAs-InAsP core-shell nanowires, a PL blue shift of > 100 meV for the InAs core was induced by strain [88]. This study demonstrated increased PL intensity by a factor 10² which was linked to passivation of nonradiative surfaces states of the InAs core.

A drawback of the PL spectroscopy method is that the strain components produce a combined effect on the bandgap. However, the strain components are directly assessed by XRD, since the crystal plane spacing in all directions of the lattice can be measured individually. The strain can then be calculated by comparing the plane spacing of the strained sample to the lattice parameters in samples without strain. Raman spectroscopy has also been used for strain measurements.

In an XRD experiment on InAs-InAs_xP_{1-x} core-shell nanowires, a good agreement with numerical strain calculations was found [89]. Coherent epitaxy was demonstrated for nanowires having an InAs core dimeter of ~ 70 nm, and InAs_xP_{1-x} shell with thickness of 36 nm and a composition of x = 0.74.

We now turn to the theoretically predicted strain state in core-shell nanowire structures which has been investigated by several groups [90][36][37][91]. In Fig. 4.2, a coordinate system is defined as shown. The WZ [0001] and ZB [111] directions are here set equal to the z-axis. The calculations have shown that the principal strain along the z-axis, ε_{zz} , is approximately constant in the core and the shell respectively. The principal strains along x and y axes (ε_{xx} and ε_{yy}) are also constant in the core, but in the shell they decrease along the radial direction, towards the outer surface of the shell. Furthermore, ε_{xx} and ε_{yy} in the shell have opposite sign and their sum is small [90]. In the core, the strains ε_{xx} and ε_{xx} are approximately related to ε_{zz} , by, $\varepsilon_{xx} + \varepsilon_{yy} = 0.44\varepsilon_{zz}$ [36]. In paper II the lattice parameters are measured in strained InAsP-InP core-shell nanowires by X-ray diffraction, demonstrating that for the InAsP core, $\varepsilon_{xx} \approx 0.5\varepsilon_{zz}$. However, this proportionality could depend on the number of dislocation defects present in the

nanowires. From the above, it is clear that the dominating strain component is along the *z*-axis, ε_{zz} .

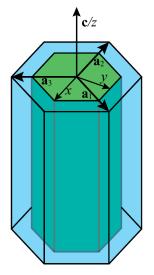


Figure 4.2. Tilted view of a Cartesian coordinate system (x, y, z). The lattice vectors of the WZ crystal are shown by the arrows \mathbf{a}_i and \mathbf{c} . The core of the nanowire (shown in green) grows along the direction of the *z*-axis. The shell layer is shown in blue.

The exact strain components are difficult to obtain analytically due to the anisotropic stiffness of the semiconductor materials. A simplified equation for the ε_{zz} strain was presented by Boxberg *et al* [37], which was found to deviate from numerical data by less than 1%. In this model, the nanowire is assumed to be infinitely long for simplicity. The atomic plane distances in the z-direction of both core and shell are set to be equal. The strain of the core-shell nanowire is such that the material with larger bulk lattice parameter (the InAsP core) is compressed and the material with smaller lattice parameter (the InP shell) is elongated along the growth direction (z-axis). The total force acting on the cross section plane (0001) along the z-axis in the core is balanced by the total force acting in the opposite direction in the shell. An equation containing only the cross-section area, Young's modulus and the lattice parameters of the core and shell materials can then be obtained. The Young's modulus, Y_{ij} , for a specific direction is derived from the case where the material is subjected to pressure only along this direction. Young's modulus for the axial stress along the z-axis, Y_{zz} , is defined by the equation

$$Y_{zz} = \frac{\sigma_{zz}}{\varepsilon_{zz}}.$$
(4.5)

The analytical expression for the strain in the core in the axial direction of the coreshell nanowires is then given by

$$\varepsilon_{zz} = \frac{1 + A_c Y_{zc} / A_s Y_{zs}}{c_c / c_s + A_c Y_{zc} / A_s Y_{zs}} - 1$$
(4.6)

where A_c and A_s are the cross-section areas of the core and shell respectively, c_c and c_s are the lattice parameters of the core and shell materials in unstrained condition, Y_{zc} and Y_{zs} are the Young's moduli in the axial direction of the core and shell, respectively.

5. X-ray Diffraction Analysis

Materials that are periodically ordered on the atomic scale can typically be structurally characterized by X-ray diffraction (XRD). Since the discovery in 1912 by Max von Laue, X-ray diffraction has become an important tool for characterization of crystalline materials. It is also a common method for determination of molecular structure, such as the structure of proteins [92]. The type of X-ray source is chosen based on the required diameter, intensity and coherence of the X-ray beam. For the purpose of analyzing samples of mm size, a low intensity X-ray beam from an X-ray tube can be sufficient. However, for nanostructures such as nanowires, a highly intense X-ray beam of a synchrotron ring is often applied. Atomic plane distance can be measured by XRD with an error of $\sim 0.03\%$ [48].

5.1. Single Crystal X-ray Diffraction Principles

As X-rays with wavelength, λ , propagate through a crystal, they become partially reflected at each atomic plane, which result in a reflection pattern of spots (diffraction pattern). In the case of a monochromatic source, the incoming X-rays have a small range of wavelengths, so that very narrow diffraction spots are generated. Diffraction patterns appear, as the monochromatic waves are elastically scattered from a large number of successive parallel planes. They then interfere constructively at specific scattering angles. At these angles, the phase differences of the waves reflected from the planes is 2π as shown in Fig. 5.1. The diffraction maxima can in this case form with very narrow angular distribution due to the large number of planes and narrow wavelength distribution of the source. The atomic plane distance, *d*, is related to the scattering angle 20 and the X-ray wavelength, λ , by Bragg's law, which was introduced by W. L. Bragg and W.H. Bragg in 1913. It is given by

$$2d\sin\theta = n\lambda,\tag{5.1}$$

where *n* is an integer.

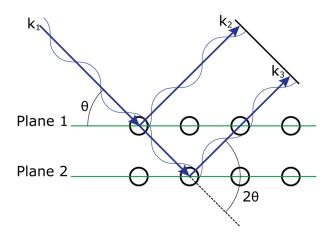


Figure 5.1 Diffraction of X-ray waves upon two crystal planes is illustrated, where the circles represent the atomic positions in space. k_1 is the incident wave vector while k_2 and k_3 are the wave vectors of the reflected waves. The scattering angle is 2θ while the incident angle is θ . Constructive interference is obtained when the path length difference between the waves of k_2 and k_3 results in a relative phase shift of $n2\pi$ (where *n* is an integer), as illustrated by the wave forms.

The condition for constructive interference can also be obtained by analysis of the reciprocal space vectors, \mathbf{G}_{hkl} , that belong to a specific crystal. The wave vectors of the incident X-rays change direction and preserve their norm when scattered elastically, as given by, $|\mathbf{k}_i| = |\mathbf{k}_f|$, where \mathbf{k}_i and \mathbf{k}_f are the wave vectors of the incident and scattered waves respectively. The scattering vector $\Delta \mathbf{k}$ is given by $\Delta \mathbf{k} = \mathbf{k}_f - \mathbf{k}_i$. The constructive interference condition, that result in an intensity maxima, is satisfied when a reciprocal lattice vector is equal to the scattering vector, $\mathbf{G}_{hkl} = \Delta \mathbf{k}$ [64].

5.2. Nanowire X-ray Diffraction Methods

In this work, XRD is utilized for analyzing the composition and strain of InAsP nanowires and InAsP-InAs core-shell nanowires. The XRD measurements are performed on as-grown vertically aligned nanowires, standing in the direction of the surface normal on single crystal InP (111)B substrates. The setup used is equipped with an X-ray tube which has a Cu target. A schematic illustration of the setup is shown in Fig. 5.2. The X-rays are generated by electronic transitions from the L to the K shell of the atoms in the Cu target, such as Cu K_{α} with $\lambda = 1.5406$ Å and energy of 8.05 keV. The X-ray emission spectrum of the anode is guided by diffraction through a series of Ge crystals to achieve monochromatic X-rays. In the XRD measurements, the InP substrate and the detector were initially oriented with

the $[\overline{111}]$ direction of the substrate along the scattering vector. This vector is defined by the X-ray beam and the detector angle. The alignment is achieved by adjusting the angle ω of sample with respect to the incident X-ray beam, and by adjusting the detector angle, 2 θ , with respect to the incident X-ray beam, to find the diffraction peak of the (111) planes of the substrate.

During the measurement of an XRD spectra, ω is varied, while the detector angle is co-varied, so that ω and θ are changed at the same rate, while the X-ray source position is fixed. Additionally, a constant offset of ω , denoted ω_{offset} , can be used to change the angle of the crystal orientation with respect to the measured scattering vector.

In the above described coupled scan, is important that the direction of the measured scattering vector remains fixed with respect to the reciprocal lattice vectors. The norm of the scattering vector at a diffraction peak is then used for calculating the atomic plane distances.

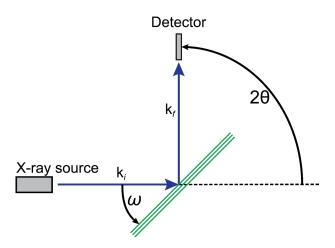


Figure 5.2. Schematic illustration of an X-ray diffraction setup $(2\theta \cdot \omega)$. The X-ray source is stationary while the crystal and detector are rotated around the point where the beam enters the crystal surface, as shown by the blue arrow marked k_i. During the measurement, the angle between the incident beam and the crystal planes is ω while the detector is at 2 θ . The atomic planes in the sample are illustrated by the solid green lines.

The spectra obtained in the XRD measurements were analyzed by converting the 2θ angles to the plane spacing *d*. The measured peak position of the InP (111) plane was compared to the known value for the ZB InP bulk, the measured spectrum was then shifted so the (111) peak coincides with the bulk value. This procedure reduces the random error in the peak positions that was introduced by the imperfect alignment of the crystal sample and the rotational axis of the detector and sample holder. The error was estimated to be in the range 0-0.02°.

The (111) diffraction peak of bulk ZB InP is located at $2\theta = 26.281^{\circ}$ with the above X-ray source wavelength and the bulk lattice constant of $a_{InP} = 5.8687$ Å. The WZ InAs_xP_{1-x} nanowires were aimed to be of the composition $x \approx 0.25$ -0.35, which resulted gives the peak position of $2\theta \approx 26$ -25.9°. The wide background signal from the substrate and the small angle between the nanowire peak and the substrate peak, introduces some difficulty in the characterization of the signal originating from the nanowires. The detector signal in the substrate peak maxima is found to be in the order of 10^6 counts per second (CPS) while the nanowires show an intensity in the range 10^2 - 10^3 CPS. As was shown by Borg *et al* [93], it is possible to reduce the XRD signal of the (111) planes of the substrate by tilting the substrate $\sim 0.1^{\circ}$ with respect to the [111] direction. The error introduced is very small (a deviation in the order of 10^{-5}). The main point is that the misalignment does not reduce the nanowire signal to the same extent, since there is a random tilt of the nanowires. The tilt can be in the order of 1° (see paper II), resulting in wider angular distribution of the diffraction spots of the nanowires compared to the substrate.

5.3. Strain in InAsP-InP Core-Shell Nanowires

In paper I, the lattice parameter c of the WZ nanowires is measured in XRD, showing that the increasing InP shell thickness produce an increase of axial strain in the core of the InAs_{0.35}P_{0.65}-InP core-shell nanowires. The strain approximately follows Equation (4.6) within ~ 15%. The axial strain is found to increase towards $\varepsilon_{zz} = -0.8\%$ for a shell thickness of ~ 25 nm and with a core diameter of 40-45 nm. By the small difference from the calculated strain values for dislocation free coreshell nanowires, it is concluded that the misfit dislocation density is low in the nanowires. In Fig. 5.3(a), the XRD spectra of the InAsP-InP core-shell nanowires are shown for various shell thicknesses. The increasing 20 angle of the nanowire XRD peaks in Fig. 5.3(a) from 25.9 to 26.1, which demonstrate the decreasing lattice parameter c.

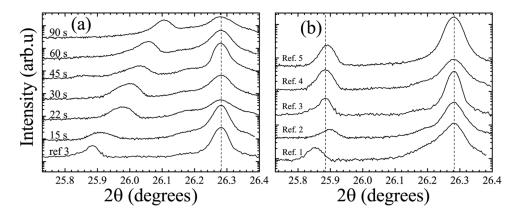


Figure 5.3. (a) XRD spectra measured on InAsP-InP nanowire samples, showing the scattering angle 20, with the scattering vector aligned along the $[\overline{1111}]/[000\overline{1}]$ direction. $\omega_{offset} = 0.1^{\circ}$ is used. Intensity is shown in log scale. A wavelength of 1.54059 Å was used. The peaks at 20 = 26.28° are due to the (111) planes of the InP substrate. The peaks at 25.9-26.1° originate from vertically aligned nanowires. The curve marked ref 3 is a sample with InAsP nanowire cores without shell, the spectra are marked by the InP shell growth time. (b) Reference growth runs of InAsP nanowires without shell are shown. The positions of the peaks are shifted randomly due to variations of the composition in the InAsP alloy. The figure is adapted from paper I.

The strain values (average strain of all nanowires for each growth sample) are calculated from the plane spacing that are obtained from the XRD measurements. The XRD measurements of the unstrained InAsP reference nanowires, which are used as reference data for unstrained lattice parameters, are shown in Fig 5.3(b). The strain values, ε_{zz} , of the InAsP cores are calculated by Equation (5.2), and are plotted in Fig. 5.4. The mean diameters of the InAsP-InP core-shell nanowires from each growth sample were measured by a SEM, and are shown on the horizontal axis in Fig. 5.4.

$$\frac{c_{\text{InAsP-InP}} - c_{\text{Ref InAsP}}}{c_{\text{Ref InAsP}}} = \varepsilon_{zz}$$
(5.2)

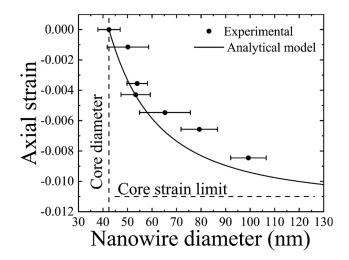


Figure 5.4. The axial strain values ε_{zz} (calculated by Equation (5.2)) of the InAsP-InP coreshell nanowire growth samples are shown. The average diameters of the nanowires of each growth sample are shown on the horizontal axis. The analytical model plotted as a solid line is obtained by Equation (4.6). The figure is adapted from paper I.

In paper II, similar core-shell nanowires with $InAs_{0.26}P_{0.74}$ -InP structure and total diameter of ~ 95 nm were investigated. The cores were ~ 45 nm in diameter and contained a sulphur doping gradient along the growth axis. The sulphur precursor gas flow started at level n_1 in the beginning of the nanowire growth, it was then lowered to n_2 for the central part of the nanowire core, and finally it was increased to n_1 again at the top end of the nanowires. This step was performed in order to provide a low doped segment in the center of the nanowire cores. The purpose of the low doping segment was to enable photocurrent spectroscopy measurements in the nanowires with low doping density. The higher doping at the ends of the InAsP cores was intended to provide low resistance contacts.

In XRD measurements it was observed that the XRD spectra of the nanowires exhibit a split peak, which had a smaller shoulder peak, and a main peak with larger intensity. This splitting could be due to formation of dislocations at the core-shell interface.

XRD measurements of the nanowires that were performed with a synchrotron beam, are shown in Fig. 5.5. The positions of the intensity peaks in the XRD map (contour plot of intensity) correspond to reciprocal space vectors that satisfy constructive interference conditions. The vector Q_z is aligned with the [0001] direction, and Q_x is aligned with the [11 $\overline{2}0$] direction. The strain in the InAsP cores is calculated with Equation (5.2) (as in paper I), by using the main peak position, labeled as Peak 1 in Fig. 5.5(a). The smaller intensity maximum is labeled Peak 2 in Fig. 5.5(a). Considering that Peak 1 shows larger intensity, it can be understood that this peak

arises due to a main material volume in the nanowires. Peak 1 also correspond well to simulations of the XRD measurements, which include a random tilt angle of the nanowires.

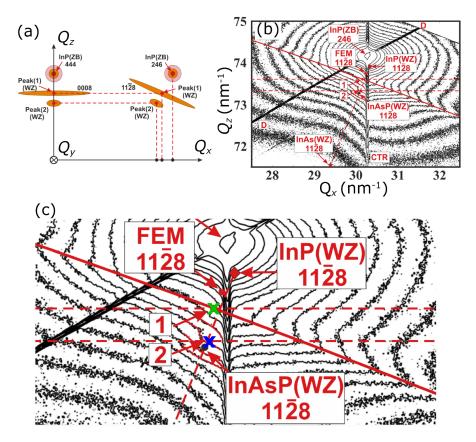


Figure 5.5. (a) Schematic illustrations of the X-ray intensity in reciprocal space map measurements of InAsP-InP core-shell nanowires. On the left side are measurements shown with the scattering vector aligned along the [0001] direction (symmetric measurement). On the right side, a schematic illustration is shown of an asymmetric reciprocal space map, where the vertical axis (Q_z) is aligned along the [0001] direction and the horizontal axis (Q_x) is aligned along the [1120] direction. The peak 1 and peak 2 illustrate the diffraction intensity maxima of the nanowires. (b) The measured reciprocal space map. X-ray intensity is constant along the black contour lines. The two nanowire peaks are labeled 1 and 2. The reciprocal space points of relaxed WZ InAsP, WZ InP and WZ InAs are shown. (c) Enlargement of panel (b). The two horizontal dashed lines show the Q_z positions of peaks 1 and 2, as determined from symmetric measurements. The InAs₂₆P₇₄ calculated position for relaxed core material is shown as a black dot with label InAsP(WZ) 1128. The nanowire peak 1 (green x) and peak 2 (blue x) are shown. Peak 1 is elongated along the solid red line. The position of the fully strained core of the core-shell nanowire, calculated by the finite element method is indicated by FEM 1128. The figure is adapted from paper II, and was prepared by Dr. S. Lazarev.

The position of Peak 1 corresponds to a strain of $\varepsilon_{zz} = -0.004$ in the cores, with respect to unstrained InAs_{0.26}P_{0.74}. The lattice parameter *a* shows a larger uncertainty due to the angular width of Peak 1. It was, however, estimated to be $a = 4.164 \pm 0.005$ Å. When compared to the relaxed InAs_{0.26}P_{0.74}, the in-plane strain is found to be $\varepsilon_{xx} = -0.003 \pm 0.001$. Both strain components ε_{xx} and ε_{zz} are thereby shown to be compressive in the core.

6. Device Fabrication for Electrical Measurements

In this chapter, a method for device fabrication is discussed. To enable electrical measurements on single nanowires, devices with metal contacts on the surface of the nanowires were fabricated by an electron beam lithography process. Initially, about 100 nanowires were mechanically transferred from a growth substrate to a prefabricated Si substrate by the use of a sharp clean-room paper tip. Nanowires were selected and located by the use of markers on the Si substrate. Contact patterns were then designed for each nanowire. The pattern design was exposed in an EBL and electrodes were evaporated on to the nanowires. The Si substrate was equipped with a fully covering backside metal contact and a top layer of SiO₂ so that a capacitive coupling between the nanowire and the backside contact was formed, which was used for controlling the electron density of the nanowire during the charge transport measurements.

6.1. Preparation of Si Device Substrates

The Si device substrates were fabricated with two layers of markers on the top side. The first layer was made by UV lithography and the second by EBL. In both cases metal was thermally evaporated in the exposed resist pattern, followed by lift-off. The UV pattern consisted of large area electrodes with 100 μ m wide bonding pads (as shown in Fig. 6.2) to enable bonding of metal wires to the devices, or electrical measurements with probe needles contacted to the bonding pads. The EBL pattern consisted of cross markers (a few μ m long and 50 nm wide lines) and 100 nm wide dots, which provided a local coordinate system on the surface. The coordinates enabled the alignment during the EBL exposure of the contact electrode pattern, to single nanowires.

As shown in the illustration of Fig. 6.1, step (1), an *n*-type two-inch Si wafer was initially covered with 130 nm SiO₂ by thermal oxidation to form an electrically insulating layer. As shown in step (2), the oxide was removed from the backside of the wafer by a buffered oxide etch, while the top was covered by a resist layer for protection. The backside was then metalized by thermal evaporation of ~ 10 nm Ti

and ~ 100 nm Au, as shown in step (3). Here, the Ti functions as a sticking layer which is necessary since Au does not stick well to Si or SiO₂. Au is used primarily to provide a good electrical contact. The alignment markers were then fabricated on the top-side oxide by EBL. As shown in step (4), the topside oxide was spin-coated with an EBL resist. Exposure to the electron beam alters the chemical bonds of the resists, which then can be dissolved by a developer. The result is shown in step (5). Evaporation was then used to apply metal to the exposed pattern as shown in step (6). The final step, (7), known as lift-off, consist of dissolving the the resist, which also removes evaporated metal on top of it. However, the metal evaporated in the exposed pattern still remains.

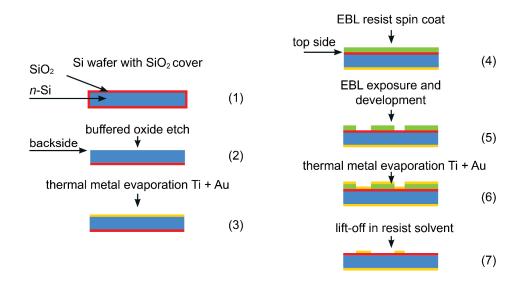


Figure 6.1. Steps for preparation of Si substrates for single nanowire devices. Steps (1-3) show the removal of thermal oxide and thermal evaporation of Ti/Au onto the backside of the Si wafer. Steps (4-7) show the EBL patterning and thermal evaporation of metal alignment markers with subsequent lift-off.

6.2. Single Nanowire Devices Processing

The process used for fabrications of contacts on the InP-InAs core-shell nanowires is described below. The first step of nanowire devices fabrication is the transfer of nanowires on to the pre-made Si device substrates. The nanowires were placed on the alignment markers, in 100 μ m wide deposition areas, as shown by the area marked red in the SEM images of Fig. 6.2(b). SEM images of the transferred

nanowires and the alignment markers were then acquired. A contact pattern was designed with these markers as a reference coordinate system.

The EBL process for depositing the contact pattern stared with spin coating of a 200-400 nm thick resist (in this case PMMA a4) which was then baked on a hotplate. After exposure, the pattern was developed in MIBK and then rinsed in IPA. Next, the developed resist was etched in oxygen plasma to remove any residues of resist in the developed pattern. The InAs surface of the nanowires was then etched in ammonium sulfide ((NH₄)₂S_x diluted water), in order to remove the native oxide so that the contact metal could be evaporated on to the bare InAs surface. Following Suyatin *et al* [94], a stock solution of 20% ammonium sulfide was prepared by mixing 3 molar sulphur powder into the ammonium sulfide. A few minutes prior to evaporation, the stock solution was further diluted in water in the ratio of 1:79. Etching was then performed at 42 °C, by using a temperature controlled water bath, for 5-6 min. To minimize oxide regrowth, the sample was placed in a thermal evaporator directly after the oxide etch was completed. Deposition of the desired metal contacts was then performed. The final step was lift off, which was performed in the solvent Remover 1165 and was followed by a rinse in IPA.

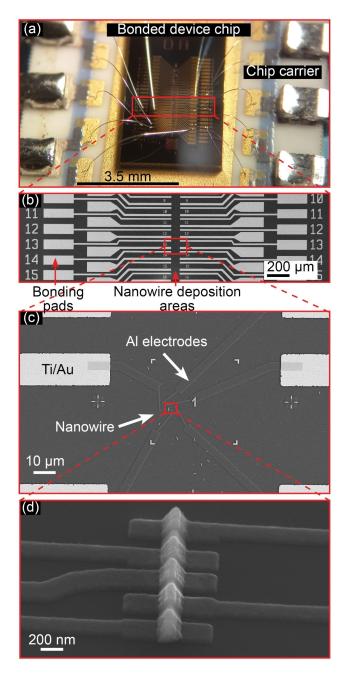


Figure 6.2. (a) Optical image of a Si device chip with bond wires between the bonding pads and the chip carrier. (b) SEM image of the Ti/Au bonding pad pattern and the nanowire deposition areas. (c) SEM image of a nanowire contacted by Ti/Al electrodes (center red rectangle). Two alignment crosses are visible, one on each side of the red rectangle. (d) Magnified SEM image of a single nanowire, contacted by Ti/Al electrodes (tilted view).

7. Low Dimensional Transport

In this chapter, a short introduction to charge transport in nanowires is given. Then follows transport measurement in the Coulomb blockade regime in triangular InP-InAs core-shell nanowires.

7.1. 1D Transport

For a narrow semiconductor wire aligned along the z-axis with a diameter in the order of the Fermi wavelength, $\lambda_F = 2\pi/k_F$, the solutions to the S.E of the electrons are standing waves in the radial directions (x-y plane) and freely propagating waves along the wire axis, as shown by the parabolic bands in Fig. 7.1. It is then possible to write the wave function as $\varphi(x, y, z) = \varphi(x, y)e^{ik_z z}$. Such solutions are known as subbands. The standing waves $\varphi(x, y)$ in the x-y plane give rise to an energy spacing between the subbands having different quantum numbers.

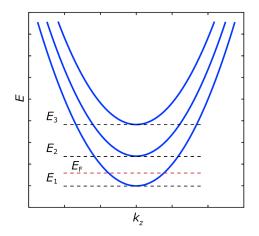


Figure 7.1. The energy E(k) for the three subbands with lowest energy. The energy E_1 , is the subband of lowest energy at $k_z = 0$. Only this subband is occupied for the indicated position of E_F .

The number of occupied subbands is given by the position of $E_{\rm F}$, the thermal energy $k_{\rm B}T$, and the spacing between the subbands, see Fig. 7.1. In some cases, analytical functions can be obtained, for simple cross-section geometries.

The current, I_{1D} , along the axis of the 1D system, can be calculated by the 1D density of states $\rho_{1D}(E)$, and the carrier velocity v(E) of the carriers in each occupied subband,

$$\rho_{1\rm D}(E) = \frac{1}{\pi\hbar} \sqrt{2m^*/(E - E_0)},\tag{7.1}$$

where E_0 is the energy of the lowest state in the subband. The Fermi-Dirac distribution is considered to be a step function at the Fermi level for simplicity: F = 1 for $E \le E_F$, F = 0 for $E > E_F$. As shown in Fig. 7.2, electrons that contribute to the current travel from left (source contact) to right (drain contact) in the semiconductor channel, and reside at energies inside the bias energy window, $eV_{sd} = \Delta \mu = \mu_s - \mu_d$. Here, the electrochemical potential of the source contact metal is μ_s , and that of the drain contact is μ_d . The current I_{1D} for all subbands (of index *n*) is given by [59]

$$I_{1\mathrm{D}} = e \sum_{n} \int_{\mu_d}^{\mu_s} v_n(E) \rho_{1\mathrm{D},n}^+(E) \, dE.$$
(7.2)

The density of states is taken for only positive k states (ρ_{1D}^+) . After summation over N subbands, the integral evaluates to $G = I_{1D}/V_{sd} = N2e^2/h = NG_0$. The conductance is therefore constant for a constant number of subbands. G_0 is referred to as the conductance quantum. The transmission probability can also be included to account for scattering, in the case of non-ballistic transport. With an average transmission probability, T, we obtain the conductance of $G = NG_0T$.

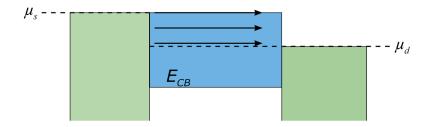


Figure 7.2. The applied potential difference between the source and drain metal contacts, $eV_{sd} = \mu_s - \mu_d$ is illustrated at low temperature. The electrons in the semiconductor channel (center block) travel from the left to the right metal contact. Here, only the electrons inside the potential energy window ($\mu_s > \mu > \mu_d$) produce a net current. E_{CB} denotes the conduction band edge.

7.2. Nanowire Field Effect Devices

The field effect, simplified, is the modulation of charge density in a material by the use of an external electric field. This effect is typically obtained through the use of a voltage on a gate electrode which is capacitively coupled to a semiconductor channel through a thin dielectric layer. The electric field will modulate the potential energy of the states in the semiconductor and allow filling, or depopulating them. In this thesis the field effect is used for the purpose of controlling the charge density in the InAs shell of the InP-InAs core-shell nanowires.

The nanowire devices used in paper III and IV are fabricated from an *n*-type Si wafer that acts as a uniform conductor or global gate electrode below dielectric layer of 130 nm thick SiO₂, hence a capacitive coupling is formed as the nanowire is placed on top of the SiO₂. This gate capacitance is denoted C_g . When a voltage V_g is applied to the gate electrode, a charge of ΔQ_{NW} is accumulated in the nanowire, having a gate voltage dependence as,

$$\Delta Q_{NW} = C_g V_g. \tag{7.3}$$

For the case of low electron density typical for semiconductors, C_g is also a function of the charge density of the nanowire, generally decreasing with lower value of charge density [95].

For the geometry of a cylindrical metal wire placed on a dielectric layer, such as SiO_2 , with a metal plate behind it, the following analytical expression is applicable to calculate the gate capacitance [96],

$$C_g = 2\pi L \varepsilon_0 \varepsilon_e / \operatorname{acosh}\left(\frac{t_{ox} + r}{r}\right),\tag{7.4}$$

where L is the length of the wire, ε_0 the vacuum permittivity, and $\varepsilon_e \approx 0.5\varepsilon_r(\text{SiO}_2)$ is the effective relative permittivity the dielectric layer. The factor of ~ 0.5 is necessary to account for that the wire is not embedded in the SiO₂. t_{ox} is the thickness of the dielectric layer, and r is the radius of the wire. In paper III, the above equation is applied to calculate the back gate capacitance of the nanowires, and was found to be in good agreement with the measured capacitance.

7.3. Coulomb Blockade Effect

Electrons (or holes) that are confined to a small volume (charge island) in a conductor, are strongly affected by the Coulomb interaction acting between them and the capacitance to the surroundings. This leads to the possibility to control the number of electrons on the island. So called single electron transistors can be constructed due to this effect. One example of a charge island is a quantum dot in a semiconductor. Such a dot, coupled to source and drain tunneling contacts, is shown in Fig. 7.3(a). As described in Ref. [97], when a single electron is added to the island, the electrochemical potential of the electrons on the island increases by the charging energy $(E_c = \mu(N) - \mu(N - 1))$, where N is the number of electrons occupying the island. This energy can be written as, $E_c = e^2/C_{\Sigma}$, where C_{Σ} is the total capacitance of the island. The confinement due to the tunnelling contacts result in a residence time Δt for the electrons on the island, as there is a finite probability for escape per unit time. The Heisenberg uncertainty relation, $\Delta E \Delta t > h$, can be used to estimate the tunnel barrier resistance, R, required to localize the electrons to the island. The time constant for charging the island is given by $\Delta t = RC_{\Sigma}$. Using this Δt and E_c defined above, we obtain the minimum tunnel barrier resistance $R > h/e^2 \approx$ 25.8 k Ω . At low temperatures, where E_c is larger than the thermal energy $k_{\rm B}T$ and when E_c is larger than the energy supplied by the bias window, eV_{sd} , current oscillations as a function of gate voltage appear, known as Coulomb oscillations.

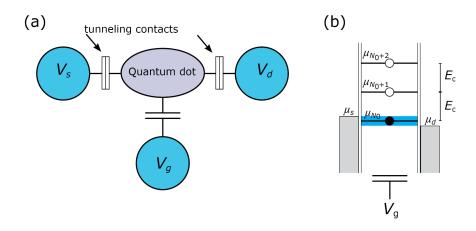


Figure 7.3. (a) A quantum dot or charge island is depicted as a volume connected by tunneling barriers to left and right contacts. The contacts have voltages V_s and V_d respectively. A gate contact, shown with a voltage V_g , is capacitively coupled to the island. (b) Electrochemical potential diagram of the island showing the charging energy E_c as the energy difference between single electron charging numbers. Current will flow when the bias window $\mu_s - \mu_d$ (marked by blue) is aligned so that a level lies inside the window. The gate voltage V_g shifts the levels by changing the electrochemical potential μ in the dot.

To understand the effect better, we first define the electrochemical potential as the change of the total energy, E_N , when a single electron is added to the island, as shown by equations (7.5)-(7.7) [97] [98],

$$\mu_N = E_N - E_{N-1} \tag{7.5}$$

$$E_N = \frac{e^2 N^2}{2C_{\Sigma}} - eN \frac{C_g}{C_{\Sigma}} V_g$$
(7.6)

$$\mu_N = \frac{e^2}{C_{\Sigma}} (N - \frac{1}{2}) - e \frac{C_g}{C_{\Sigma}} V_g.$$
(7.7)

The first term in Equation (7.6) is the electrostatic energy of the island at zero gate voltage, where $C_{\Sigma} = C_s + C_d + C_g$ is the capacitances between the island and the source contact, the drain contact, and the gate electrode respectively. The second term is the electrostatic potential energy due to the capacitance between the gate and the island, as a function of the gate voltage V_g . A lever arm factor for the gate is then defined as $\alpha = C_g/C_{\Sigma}$. The charging energy E_c follows from Equations (7.7)-(7.8),

$$E_c = \mu_N - \mu_{N-1} = \frac{e^2}{C_{\Sigma}}.$$
(7.8)

A blockade, i.e. blocked current condition can appear beacuse a current requires a change of the number of electrons on the island, which requires the addition energy to be supplied. The quantum energy level spacing of the island is here considered to be smaller than the thermal energy $k_{\rm B}T$, and can then be neglected. As described in Ref. [99], a current can flow through the island from the source to the drain electrode when the bias window contains one or several electrochemical potential levels μ_N , as shown in Fig. 7.3(b). This condition is possible to arrange by applying a gate voltage to shift a electrochemical potential level into the bias window, or by enlarging the bias window by increasing the source-drain voltage V_{sd} . For electrons, the levels move down linearly with increasing gate voltage is very small compared to E_c/e . Fig. 7.4 shows, as an example, Coulomb oscillations measured in InP-InAs core-shell nanowires, described in paper III. The details of this experiment are discussed below.

In the conducting state, current flow is achieved by sequential single electron tunnelling. A single electron first tunnel out from the island, and goes to the contact with the lowest electrochemical potential. The island is then sequentially filled by another electron coming from the contact with higher potential. The number of electrons on the island is thereby oscillating between N and N - 1.

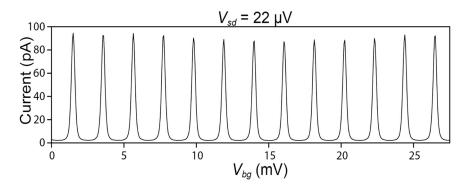


Figure 7.4. Coulomb current oscillations measured at the base temperature of 14 mK in a dilution refrigerator, as a function of back-gate voltage. The device consists of a InP-InAs core-shell nanowire contacted by Ti/Au electrodes. The figure is adapted from paper III.

For bias voltage and gate voltage applied in combination, the levels μ_N can be accessed as shown in Fig. 7.5. The current of the Coulomb blockade forms a diamond structure (stability diagram) when plotted as a function of bias voltage and gate voltage. The areas of stable electron numbers, where the current is zero, are

shown in Fig. 7.5(a), as white diamonds. When one or both of the edges of the bias window are aligned with a level μ_N , the current will start to flow, causing a peak in differential conductance (dI_{sd}/dV_{sd}) . For cases where one or several levels are inside the bias window, a current flows as indicated by the solid blue colored areas. In Fig. 7.5(b), the level μ_{N0} is centered in the bias window, allowing current flow for bias voltages $V_{sd} \ll E_c/e$. In Fig. 7.5(c), the level μ_{N0} is below the bias window leading to zero current. In Fig. 7.5(d), the bias window touches both μ_{N0} and μ_{N0+1} , so that eV_{sd} is equal to the charging energy. In Fig. 7.5(e), a current can flow as the bias window is centered over the level μ_{N0+1} .

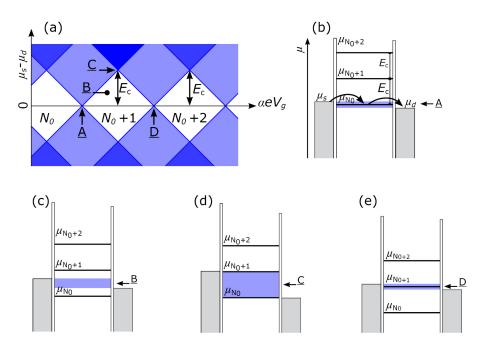


Figure 7.5. (a) Schematic stability diagram of a charge island. Current is shown as a function of gate voltage V_g and bias voltage V_{sd} . α is the gate lever arm. The white areas show zero current, the blue indicate a current and the dark blue shade indicates higher current. The numbers in the white diamonds indicate the number of electrons on the island. (b) Position <u>A</u>, the bias window is centered at the level μ_{N0} . Current can then flow at close to zero bias voltage. (c) Position <u>B</u>, the bias window is located between two levels, so that no current can flow. (d) Position <u>C</u>, the bias window covers the difference, $E_c = \mu_{N0+1} - \mu_{N0}$, and its edges are aligned with the two levels, allowing current flow. (e) Position <u>D</u>, the case is the same as in position <u>A</u>, but with the bias window centered at the level μ_{N0+1} .

7.4. Coulomb Blockade in InP-InAs Core-Shell Nanowires

In InP-InAs core-shell nanowires, electrons accumulate in the InAs shell since the InAs conduction band has lower potential energy. The electrons are, therefore, localized to the geometry of the shell. This electronic structure is investigated in paper III. Nanowire devices are constructed from a triangular InP-InAs core-shell nanowires placed on top of a back-gate oxide. Two contacts are fabricated onto each side of the nanowire to enable measurements of Coulomb blockade effect with bias voltage along the nanowire axis, as well as perpendicularly to it. The nanowire devices are then cooled down and measured by DC electrical transport at the base temperature of a dilution refrigerator (14 mK). A stability diagram from one of the measurements is shown in Fig. 7.6(a) and an SEM image of the device is shown in Fig. 7.6(b). For each gate voltage setting, the current is measured as a function of bias voltage, which is referred to as an I-V curve. The differential conductance is then calculated from the numerical derivative of the I-V curves. The resulting 2D map of the differential conductance is shown in Fig. 7.6(a). The peak spacing, ΔV_g , at zero V_{sd} , gives the capacitance between the back gate and the nanowire by $C_g =$ $e/\Delta V_g$. Here the peak spacing is 2.0 mV, which gives $C_g = 80$ aF. The upper corners of the Coulomb diamonds are located at $V_{sd} \approx 250 \ \mu\text{V}$, resulting in a charging energy of $\sim 250 \,\mu eV$. The measurement was, furthermore, performed for the contact pairs A-B, E-F, A-E, and B-F (see Fig. 7.6(b)). The stability diagrams from these measurements are similar, having the same back-gate capacitance and charging energy. From this fact it can be concluded that the same charge volume is probed in all measurements and the electrons are thereby free to move throughout the InAs shell of the nanowire.

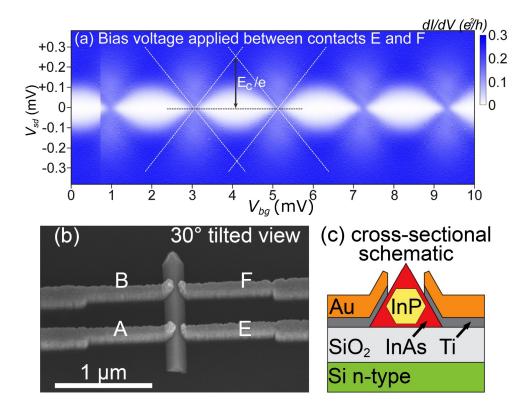


Figure 7.6 (a) Coulomb-blockade stability diagram. The differential conductance (color scale) is shown as a function of bias voltage V_{sd} between contacts E and F (shown in panel (b)) and back-gate voltage V_{bg} . The temperature is 14 mK. (b) The triangular InP-InAs coreshell nanowire contacted with four Ti/Au metal electrodes, is shown at a tilt angle of 30°. (c) Schematic cross-section view of the device in (b). The InP core of hexagonal geometry is surrounded by a InAs shell with triangular geometry. The figures are adapted from paper III with the permission of AIP Publishing.

7.5. Quantum Dot Transport

For the case of charge islands of size $L \approx \lambda_F$ it is necessary, in addition to the Coulomb blockade effect, to treat the electrons as quantum states. The states are solutions to the S.E. for single particles, namely single particle states. The charge island is in this case referred to as a quantum dot. Transport measurements on quantum dots formed in III-V materials of many geometries, such as discs [100] and rings [101], have been performed. These exhibit specific single particle spectra, derived from their geometry.

For decreasing size of the quantum dot, the energy difference between the single particle levels, ΔE_s , generally increase. In a wire shaped system, the two transverse directions are smaller than the longitudinal and, therefore, we observe a level spacing primarily due to the states quantized in the axial direction. In the 1D case, the levels (E_{1D}) are given by,

$$E_{1D} = \frac{\pi^2 \hbar^2}{2m_e^*} \frac{n^2}{L^2},$$
(7.9)

where n is an integer number and L is the length of the 1D system.

For the InP-InAs core-shell nanowires, we may as a first approximation consider a thin and cylindrical InAs shell. The electrons are in this case confined to the surface of the cylindrical shape. The wave function can then be factorized as angular momentum states and axial states. The single particle level spectra for such a cylindrical surface with radius r and length L, at zero magnetic field, is given by [102],

$$E_{mn} = \frac{\hbar^2}{2m_e^*} \left[\frac{m^2}{r^2} + \frac{\pi^2 n^2}{L^2} \right],$$
(7.10)

where m and n are the angular momentum quantum number and the axial state quantum number, respectively.

In the quantum Coulomb blockade regime, where E_c , $\Delta E_s > k_B T$ the single particle level spacing can be directly obtained from the stability diagram, since the addition energy $\Delta \mu_{dot}$ is then given by

$$\Delta \mu_{dot} = E_c + \Delta E_s. \tag{7.11}$$

The stability diagram of the quantum dot is in this case composed of diamonds of varying sizes. The smallest corresponds to electrons added to an already occupied single particle level. In this case, only the charging energy E_c need to be supplied, as in the Coulomb blockade described in section 7.3. To fill an unoccupied single particle level, the additional energy of ΔE_s , as in Equation. (7.11), is needed. In Fig. 7.7, a schematic stability diagram of a quantum dot is shown. The level spacing can be found by the peak spacing along the gate axis near zero bias voltage (by use of

the lever arm) or by bias voltage spectroscopy. The diamond in Fig. 7.7(a) containing N_0+1 electrons corresponds to adding an electron to an already occupied single particle level with addition energy of E_c . The diamond with N_0+2 electrons corresponds to adding an electron to an unoccupied single particle level having the addition energy of $E_c + \Delta E_s$.

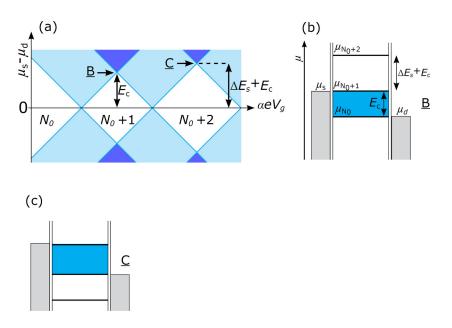


Figure 7.7. (a) Schematic stability diagram of a quantum dot. The current is shown as a function of gate voltage V_g and bias voltage V_{sd} . α is the gate lever arm. The white diamonds indicate zero current while the blue colored areas show a current, with a larger current shown by dark blue. The numbers in the white diamonds indicate the number of electrons on the island. (b) Position <u>B</u>, the bias window is centered between μ_{N0} and μ_{N0+1} and covers the energy separation of the charging energy E_c , allowing current flow. (c) Position <u>C</u>, the bias window covers the charging energy and the level spacing $E_c + \Delta E_s$, which results in a larger diamond.

As an example, a measured stability diagram of an InP-InAs core-shell nanowire exhibiting a single particle level spacing due to quantum confinement is shown in Fig. 7.8. The different sizes of the diamonds demonstrate the variation of addition energy. The features and lines of the Coulomb diamonds in Fig. 7.8 are sharper, as compared to the measurement in Fig. 7.6, which is due to better confinement of the electrons, resulting from the lower conductance of the tunneling contacts.

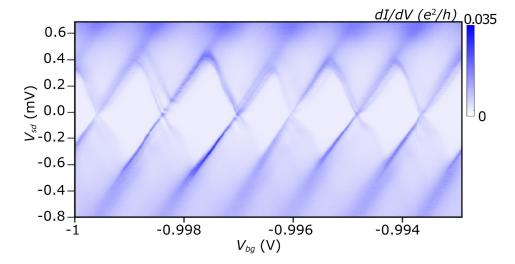


Figure 7.8. (a) Stability diagram of a quantum dot contained in a InP-InAs core-shell nanowire. The color scale shows the differential conductance dI_{sd}/dV_{sd} . The charging energy of the quantum dot is close to 300 µeV, as can be found from size of the smallest diamond.

7.6. Electrical Measurement Techniques

Electrical direct current (DC) measurements are performed in an automated dilution refrigerator (Oxford Triton) which is equipped with a vector magnet that can be operated in the range for x, y = 0-1000 mT and z = 0-8500 mT. The base temperature is ~ 14 mK.

In the present work, measurements are carried out by applying bias voltage to the source-drain contacts of the nanowire device as well as back-gate voltage. The two voltages are supplied from low noise DC voltage sources. The set points for the voltage sources were stepped sequentially through a software script. For each setting of V_{sd} and V_g , the current through the nanowire is measured by a current amplifier that is connected in series with the nanowire device. Due to noise in the current signal, an average value of the current was acquired over a 50-100 ms time window per current data point.

In measurements with four terminals, the voltage over the nanowire device was measured by a voltage amplifier. This allows for circumventing the voltage loss due to the resistance in the DC lines of the cryostat and noise filters, which accounted for $\sim 7 \text{ k}\Omega$. For measurements that required current bias (see chapter 8), a resistor outside of the cryostat is connected in series with the DC lines. In this case, more than 99% of the voltage is applied over the series resistor, which sets the current through the circuit. The nanowire devices measured in this way have a resistance of only a few k Ω .

8. Superconductivity in Nanowires by the Proximity Effect

Some of the fundamental properties of superconductors are introduced in this chapter. Then follows an introduction to Josephson junctions and measurements of induced superconductivity in InP-InAs core-shell nanowires.

8.1. Superconductivity

Superconductivity was discovered in 1911 by Heike Kamerlingh Onnes. Later, in 1957, the first microscopic theory, the BCS theory of superconductivity, was introduced by Bardeen, Cooper and Schreiffer [103]. In this theory, superconductivity is a consequence of the formation of electron pairs (Cooper pairs) at the Fermi level, having opposite momentum and spin. The Cooper pairs form due to a phonon mediated attractive interaction between the electrons. Cooper pairs can due to the total spin of zero, form a coherent quantum state. This results in a macroscopic wave function. The BCS gap 2Δ describes the energy required to excite quasiparticles (Bogoliubov quasiparticles) and break the Cooper pair. The presence of this gap protects the Cooper pairs from scattering and, therefore, results in zero resistivity. The gap at zero temperature was found to be related to the critical temperature T_c . A transition from normal metal to the superconducting state is observed at T_c . The gap and T_c are related by [104],

$$2\Delta_0 \approx 3.5 k_{\rm B} T_c. \tag{8.1}$$

The excited quasiparticles occupy states outside the gap, and the BCS gap decreases to zero as the temperature reaches the critical temperature T_c , following a function approximately as [105],

$$\frac{\Delta(T)}{\Delta_0} = \sqrt{\cos\frac{\pi T^2}{2T_c^2}},\tag{8.2}$$

where Δ_0 is the gap at T = 0. The gap Δ also goes to zero at the critical magnetic field B_c , and follows a magnetic field dependence as, $\Delta = \Delta_0 \sqrt{1 - (B/B_c)^2}$.

Prior to the BCS theory, V. L. Ginzburg and L. Landau constructed a theory for superconductivity (GL theory) [106], where the free energy of the system depends on a complex order parameter $\psi(\mathbf{r})$. The density of electrons, n_s , in the superconducting phase is then related to the order parameter by $n_s = 2|\psi(\mathbf{r})|^2$ [107]. In this theory, the superconducting state forms below the phase transition temperature T_c .

8.2. Hybrid Semiconductor-Superconductor Devices

The Josephson junction was first predicted by B. Josephson in 1962 [108]. It was demonstrated that a dissipationless current (supercurrent, I_s) can flow through a weak link such as a tunnel barrier formed by an insulator placed between two superconductors. These junctions are hence named Josephson junctions (JJs). JJs are of technical importance for instance in applications of highly sensitive magnetic field detectors.

In the GL theory, a net supercurrent can be obtained when the two wave functions of the two superconductors overlap inside the insulator (or normal conductor) and when there is a phase difference, $\Delta \varphi$, between the two superconductors [104]. The supercurrent-phase relation, at zero voltage difference between the two superconductors, is described by the DC Josephson effect, given by,

$$I_s = I_c \sin(\Delta \varphi), \tag{8.3}$$

where I_c is the critical (maximum) current of the JJ. The critical current is a function of the properties of each JJ. For short junctions I_c scales with the normal state conductance, G_n , as $I_c = G_n \pi \Delta/2e$, [104].

For a junction with an applied voltage, the AC Josephson effect is produced, given by,

$$I_s = I_c \sin(2eVt/\hbar), \tag{8.4}$$

where V is the bias voltage and t is time. In the AC effect, the time dependence of the phase difference results in an alternating current, for an applied constant bias voltage. This voltage to frequency relation is useful as a voltage standard since the frequency is related to the voltage by fundamental constants: $\omega = V2e/\hbar$.

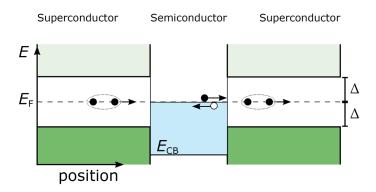


Figure 8.1. A superconductor-semiconductor-superconductor junction is illustrated at zero voltage between the superconductors. The superconducting gap is shown by 2Δ and the dark green areas show the occupied quasiparticle states. The states above $E_{\rm F} + \Delta$ are empty quasiparticle states. In the semiconductor the electrons occupy the states shown by the blue area, filling up the states from the conduction band edge $E_{\rm CB}$ to the Fermi level $E_{\rm F}$. In Andreev reflection, the electron in the semiconductor (filled dot) is retroreflected as a hole, the unfilled dot. This transfers a Cooper pair from the semiconductor to the superconductor.

A supercurrent can flow through a semiconductor or a metal connected between two superconductors due the proximity effect. The system can be approximated by a band model, where the quasiparticle states in the superconductors and the single electrons states in normal conductor are aligned as shown in Fig. 8.1. The proximity effect (the leakage of superconductivity into a normal conductor) is mediated by Andreev reflections (ARs) at the interface between the normal conductor and the superconductor [109][110] (NS interface). ARs describe how the Cooper pairs are transferred through a NS and SNS structures. An electron in the normal conductor is first reflected at the NS interface, as a hole with a negative wave vector (retroreflected). A Cooper pair is then formed in the superconductor from the two transferred electrons. The AR thereby transfers a charge of -2e from the normal conductor, retroreflected at the NS interface. However, they are retroreflected as electrons. In this case, a Cooper pair is removed from the superconductor and a charge of -2e is transferred to the normal conductor.

To maintain a supercurrent through a SNS junction, the length of the normal conductor need to be sufficiently short so that phase coherence of the electron and hole is maintained [110]. An exponential decrease of the critical current is therefore seen for junctions where the length exceeds the coherence length. This can also be understood as the decrease of the order parameter in the normal conductor.

JJs made with nanowires as the normal conductor in SNS junctions have been investigated in recent years. The density of electrons in the nanowires can be modulated by a gate voltage, which can be applied to control the critical current of the JJ [111][112][113][114][115]. InAs nanowires coupled to Al electrodes have

furthermore demonstrated a close to ideal supercurrent, producing current quantization, due to ballistic transport through a small number of occupied subbands in the nanowires [116]. These gate tunable nanowire JJs are also interesting for studies where a single 1D subband is used as a host for the so called Majorana bound states. Such quasiparticles states can appear at the end points of a 1D semiconductor nanowire channel coupled to a superconductor, when a magnetic field is applied [117]. InAs and InSb can be used for this purpose since they exhibits strong spinorbit coupling [117]. In experiments, the Majorana bound states were observed as zero energy states, producing a conductance peak at zero bias voltage [17][18][16]. The bias voltage dependent tunnelling current is used to probe the density of states of the end part of nanowires, which is made superconducting by a layer of superconducting metal.

8.3. Proximity Effect in Al Contacted InP-InAs Core-Shell Nanowires

In the experiments of paper IV, the InP-InAs core-shell nanowires with triangular InAs shell (that were described in section 3.6) are prepared with Ti/Al contacts, having a thickness of 5 nm Ti and 50 nm Al. The metals are evaporated onto the surface of the nanowires to form JJs of SNS type. The devices were cooled down in a dilution refrigerator and the characteristics of the JJs were measured in electrical DC transport. Primarily, back-gate voltage dependent switching current (maximum supercurrent) was observed in current bias measurements of the I-V (currentvoltage) characteristics of the JJs. A strong coupling between the corners of the triangular InAs shell was found by comparing the conductance along the nanowire axis and perpendicular to it.

Several device structures were investigated, such as device A and B, shown in Fig. 8.2(a) and (b), respectively. In device A, wide contact stripes are applied, to minimize the contact resistance. A short contact spacing is used, giving a minimal scattering in the nanowire channels. In device B, the current applied along and perpendicular to the nanowire axis is investigated to probe the coupling between the three corners of the InAs shell. In Fig. 8.2(b), the contacts form a rectangular pattern, so that current can be applied in the perpendicular direction such as between contacts 1-3 and 2-4.

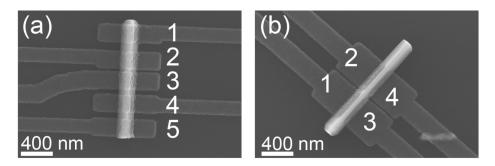


Figure 8.2. (a) SEM image of a InP-InAs core-shell nanowire with Ti/Al contact metal stripes (device A). The contacts labeled. (b) SEM image of device B, having the same construction as device A, but with a different contact arrangement. Transverse measurements are obtained between contacts on opposite sides such as 1-3, while axial measurements are between 1-2 and 3-4. The figures are adapted from paper IV.

In Fig. 8.3(a), current bias measurement are shown for device A, measured at 14 mK. The flat part of the I-V curves with zero voltage shows the supercurrent below the switching current point, I_s . From the measurements of the different contact pairs, it is concluded that the contact quality varied resulting in different switching current values. Most of the normal resistance (which was measured with a bias voltage above the superconducting gap, $eV_{sd} > 2\Delta$) is thereby due to the electrical transparency at the contact interfaces. In Fig. 8.3(b), the gate voltage dependence of the switching current is show. Decreasing switching current is observable with decreasing gate voltage. This is caused by the decrease of normal state conductance, G_n , with the gate voltage.

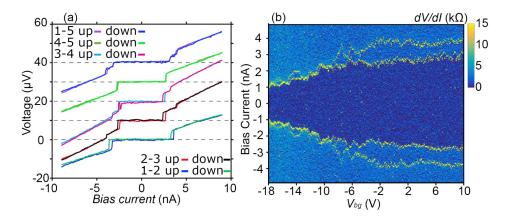


Figure 8.3. (a) Current bias measurements of device A. Each contact pair is measured by sweeping the current from negative to positive (up) and then back to negative (down). The contact numbers are shown. Voltage offsets of 10 μ V are used for clarity. (b) Differential resistance of device A for the Josephson junction between contacts 2-3 measured as a function of back-gate voltage. The yellow color shows a large differential resistance peak at the switching current. The figures are adapted from paper IV.

The conductance of device B was found to be dependent on the direction of the applied current or voltage. The differential conductance is shown in Fig. 8.4(a) for the various contact pairs of device B. In these measurements, the conductance is ~ $9 e^2/h$ between contacts on the same side facet of the nanowire (at bias voltages larger the superconducting gap, $2\Delta/e$). Between the contacts on opposite sides it is ~ $6 e^2/h$. The difference shows that the conductance is lower between the corners compared to the conductance along a single corner. The measurements on device A show a variation between $16 e^2/h$ and $20 e^2/h$ depending on contact combination.

The switching currents of device B are shown in Fig. 8.4(b). The switching currents of device B are much smaller compared to device A, which can be due to the lower normal state conductance. However, the large reduction of switching current and smooth curves in the I-V of Fig. 8.4(b) is also indicative of thermally activated switching. In such a case, the switching could be induced by the thermal fluctuation that destroy the stable phase difference between the two superconducting contacts.

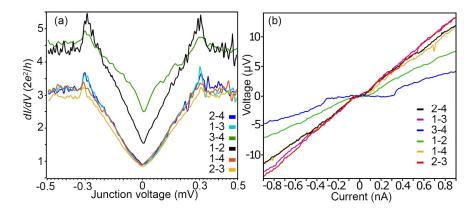


Figure 8.4. (a) Differential conductance is shown for voltage bias measurements of device B. The contact combinations 3-4 and 1-2 show differential conductance of ~ $3 e^{2}/h$ larger than the contact pair combination between the opposite side facets of the InAs shell (such as 1-3). (b) I-V curves measured in current bias on device B. The figures are adapted from paper IV.

9. Conclusions and Outlook

In papers I and II, strain and the bandgap of InAsP-InP core-shell nanowires are investigated. These nanowires are grown epitaxially by the VLS technique, using Au seed particles. The InAsP material has potential applications in optoelectronics and electronics in general. The surface passivation provided by the InP shell is one great benefit of the structure. The bandgap energy can be tuned in a wide range by the fraction of As and P in the nanowires. The bandgap of the InAsP nanowires, studied in the thesis, was close to 1.1 eV. For this perticular bandgap, photovoltaic devices can be a possible applicaton.

In paper I, the InAsP-InP nanowires were found to be of wurtzite crystal structure. From X-ray diffraction measurements of the plane spacing along the *c*-axis in the InAsP-InP nanowires, the strain along the nanowire axis (ε_{zz}) in the core was mapped out as a function of the InP shell thickness. The data shows a decreasing plane spacing with increasing shell thickness. The strain, furthermore, follows an analytical expression that is applicable to elastically strained free standing heterostructures. The increasing strain was found in PL spectroscopy, that showed an increasing bandgap of the InAsP cores with increasing InP shell thickness. The misfit dislocation density was found to be highly suppressed in the nanowires of paper I. This is a result of the small diameter (42 ± 5 nm) of the core nanowires and the cylindrical core-shell geometry of the heterostructure.

In paper II, similar InAsP-InP nanowires were investigated in X-ray diffraction experiments performed using an X-ray beam generated by a synchrotron ring. The nanowires had *n*-type sulphur doping gradient along the growth axis in the nanowire core. The X-ray diffraction peak of the (0002) planes measured on the ensemble of vertically standing nanowires, was split into two components: a main peak and a smaller shoulder peak. This indicates a partial axial strain relaxation in the nanowires. A relatively small linear misfit dislocation density was estimated from the measured splitting of the peaks. The lattice parameters *c* and *a* of the main peak were measured by X-ray diffraction reciprocal space mapping. It was found that the *a* and *c* parameters were both smaller compared to the relaxed InAs_{0.26}P_{0.74}. The *a* parameter showed a smaller decrease compared to the *c* parameter. These measurements are also in agreement with numerical calculations of strain in the core-shell nanowire, that show a larger strain along the axis of the core-shell nanowires compared to the strain components in the cross-section plane.

The upper limit of the strain (before the onset of dislocation formation) was not investigated, which could, however, be a relevant basis for further experiments. To this end, the composition of the InAsP could be tuned to increase the strain. The investigations could particularly address the onset of dislocation formation in terms of the three parameters: InAsP core diameter, InAsP composition and InP shell thickness. X-ray diffraction could be used to find the limiting parameter values. In one extreme case, for a sufficiently thin core diameter of the order of 10-20 nm, where possibly no dislocations are formed for any composition and shell thickness, due to the small volume and strain energy of the core.

In paper III, selective area growth of InP-InAs core-shell nanowire is performed. The morphology, crystal structure, and low temperature transport properties of the nanowires are investigated. In these nanowires, electrons are accumulated in the shell due to the lower conduction band energy of InAs. This results in confinement of the electrons to compressively strained channels located in the three corners of the triangular InAs shell. The InAs surface, furthermore, enables very low contact resistivity in absence of doping, due to the pinning of the Fermi level above the conduction band edge. Advantages of the selective area grown nanowires are found as compared to their Au seeded counterparts. First, the crystal structure of the selective area grown nanowire is of pure wurtzite phase and without stacking faults. Second, the growth of the shell was simplified in the absence of the Au particle. The top, in contrast to the Au seeded core-shell nanowires that exhibited uncontrolled growth under the Au particle during the shell growth.

The InAs shell of the core-shell nanowires exhibited a triangular geometry which could be relevant for applications of coupled 1D conduction channels and tubular InAs structures. Such prismatic InAs structures can be relevant for the study of topological states. The thickness of the triangular InAs shell is found to be greater at the corners (50-60 nm) compared to the center of the triangular facets where the thickness is 1-10 nm. These different thicknesses results in a quantum structure with three coupled channels in the corners of the shell.

Transport measurements that were performed at low temperature, demonstrated the Coulomb blockade effect, showing that electrons are delocalized over the full volume of the InAs shell. This shows that corners of the InAs shell are coupled, leading to the transfer of electrons between them. The measurements were performed with contacts applied to the side facets, so that Coulomb blockade could be measured both across the nanowire and along the nanowire axis. In further studies, it is relevant to investigate the strain state of the triangular InP-InAs coreshell nanowires.

Measurements of charge transport in the triangular InP-InAs core-shell nanowires were performed with thin film superconducting Al contacts (paper IV). The experiments were motivated by recent experiments on nanowire-superconductor hybrid devices. Josephson junctions were fabricated by the Al contacts placed with varying separation and in a configuration of partially covering contacts on the side facets of the nanowires. The switching current of the Josephson junctions was measured as a function of gate voltage. A back-gate tunable switching current was demonstrated. The coupling between the corner channels of the shell was investigated by applying current along and perpendiculary to the nanowire growth axis. The conductance was found to be larger along the wire, which is due to the shell morphology having variying thickness as described above. A strong coupling between the corners of the shell was deduced from the relative conductance of the perpendicular and axial contact orientations.

In future studies, the triangular core-shell nanowires could be developed further to produce epitaxial and well controlled coupled quantum structures. Further experiments where the shell thickness and core diameter is tuned, would enable control over the coupling between the corner channels. To reach lower coupling, the shell can be made thinner, which would result in a larger energy barrier, due to the quantum confinement, at the center of the shell facets, where the shell thickness is small. Coupled quantum dots could be fabricated by etching the shell to delimit its length, or by applying gate electrodes to the surface of the nanowires, so that electrostatic barriers can set the length of the quantum dot along the axis of the nanowire. Such gate electrodes can also be placed between the corners in the center of the side facets, to control the quantum dot coupling.

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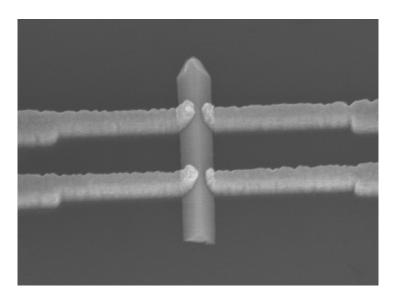
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