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Hybrid Control Techniques for Switched-Mode DC-DC Converters Part I: The Step-Down Topology

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***Abstract*— Several recent techniques from hybrid and optimal control are evaluated on a power electronics benchmark problem. The benchmark involves a number of practically interesting operating scenarios for a fixed-frequency synchronous step-down dc-dc converter. The specifications are defined such that good performance only can be obtained if the switched and nonlinear nature of the problem is respected during the design phase.**

I. Introduction

In this paper we investigate the capability of hybrid systems techniques for high performance design of power electronic devices. The system under consideration is a fixed-frequency step-down (buck) dc-dc converter. The absence of the discontinuous current mode makes the synchronous converter topology one of the simplest to tackle.

Despite its simplicity this circuit offers a number of challenges of hybrid nature that standard control techniques cannot handle in a systematic fashion. These challenges include the discontinuous dynamics due to switching as well as state constraints and control constraints that must be respected. The benchmark example investigated in this paper was first defined in [1] to which we also refer for a comprehensive survey of related works in the power electronics area.

Four research groups identified according to the affiliations (CNRS-CRAN, ETH, KTH, LTH) have applied recent ideas from the hybrid control area to the benchmark. CNRS-CRAN considers a new approach for predictive control where a one-step Newton algorithm is used to track a reference trajectory. The reference trajectory is updated by an adaptive loop.

ETH utilizes the ν-resolution model that allow state and control constraints to be considered explicitly and the inter-sampling behavior to be approximated. Explicit model predictive control is applied to derive a feedback controller and load variations are taken into account by adjusting the reference voltage using a Kalman filter.

The KTH team uses an extension of sampled data $\mathcal{H}_\infty$-control theory to pulse width modulated systems. One of the main innovations is to use averaged sampling in order to achieve robust tracking. An outer feedback loop takes care of state and control constraints. Finally, LTH employs the relaxed dynamic programming formulation from [2], were it is possible to take state and control constraints into account. The approximate optimal controller provides guaranteed robustness and stability margins.

The report [3] contains a more detailed account on the results discussed in this paper.

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II. Physical Model of the Synchronous Converter

The circuit topology of the synchronous step-down converter is shown in Fig. 1. By defining $x(t) = [i_\ell(t)\ v_c(t)]^T$ as the state vector, where $i_\ell(t)$ is the inductor current and $v_c(t)$ the capacitor voltage, the system is described by the following set of affine continuous-time state-space equations.

$$\dot{x}(t) = \begin{cases} Fx(t) + fv_s, & kT_s \leqslant t < (k + d[k])T_s, \\ Fx(t), & (k + d[k])T_s \leqslant t < (k+1)T_s. \end{cases} \quad (1)$$

where the matrices F and f are given by

$$F = \begin{bmatrix} -\frac{1}{x_\ell}(r_\ell + \frac{r_o r_c}{r_o + r_c}) & -\frac{1}{x_\ell}\frac{r_o}{r_o+r_c} \\ \frac{1}{x_c}\frac{r_o}{r_o+r_c} & -\frac{1}{x_c}\frac{1}{r_o+r_c} \end{bmatrix}, \quad f = \begin{bmatrix} \frac{1}{x_\ell} \\ 0 \end{bmatrix}. \quad (2)$$

The first equation in (1) holds when S_1 is conducting, the second when S_1 is off, and the *duty cycle*, $d[k]$, for the k-th period determines the fraction of the period where S_1 is on.

The output voltage $v_o(t)$ across the load r_o is expressed as a function of the states through

$$v_o(t) = g^T x(t) \quad \text{with} \quad g = \frac{r_o}{r_o + r_c}\begin{bmatrix} r_c & 1 \end{bmatrix}^T. \quad (3)$$

The model incorporates the parasitic elements, in particular the internal resistance of the inductor and the Equivalent Series Resistance (ESR) of the capacitor. Using normalized quantities, r_o denotes the output load which we assume to be resistive, r_c the ESR of the capacitor, r_ℓ is the internal resistance of the inductor, x_ℓ and x_c represent the inductance and the capacitance of the low-pass filtering stage, and v_s denotes the input voltage. The circuit parameters expressed in the per unit system are given by $x_c = \frac{70}{2\pi}$ p.u., $x_\ell = \frac{3}{2\pi}$ p.u., $r_c = 0.005$ p.u. and $r_\ell = 0.05$ p.u. If not otherwise stated, the output resistance is given by $r_o = 1$ p.u., the input voltage is $v_s = 1.8$ p.u., and the switching period is $T_s = 1$.

III. Modelling for Controller Design

Analysis and design of DC-DC converters are normally done using small signal approximations of averaged models [4]. The averaging technique is convenient to use but

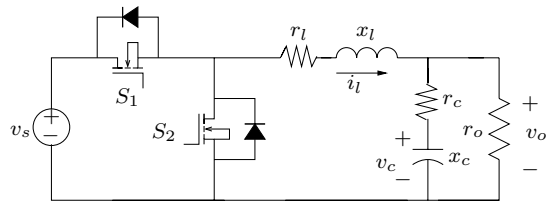

Fig. 1: Synchronous buck converter.

it offers only a low frequency approximation of the true dynamics where the effect of discontinuous switching is ignored. The modelling techniques discussed in the paper include several types of Piecewise Affine (PWA) models as well as sampled data models.

A. CNRS-CRAN: Switched linear system

We consider a switched linear control system given by:

$$\begin{aligned} \dot{x}(t) &= A_{\alpha(x,t)}x(t) + B_{\alpha(x,t)}E \\ y(t) &= Cx(t), \end{aligned} \tag{4}$$

where $x \in \mathbb{R}^n$ are the states, $E = v_s$, $\alpha(x,t) : \mathbb{R}^n \times \mathbb{R}^+ \to \{1, 2, \ldots, m\}$ is the switching function to be designed, and matrix pair (A_i, B_i), $1 \le i \le m$, defines a subsystem of (4).

The step-down converter belongs to the piecewise affine description (4) with $m = 2$ and

$$A = A_1 = A_2 = F, \quad B_1 = f, \quad B_2 = 0, \tag{5}$$

$$\alpha(x,t) = \begin{cases} 1 & t \in [kT_s, (k + d[k]T_s] \\ 2 & t \in [(k + d[k]T_s), (k+1)T_s)], \end{cases} \tag{6}$$

where the switching period for the step-down converter is $T_s = 1$ and $d[k]$ represents the k-th duty cycle. The aim of controlling the system (5)-(6) is to maintain the voltage over the load r_o at a constant value $v_{o,ref}$ and also to limit the current i_l. We propose a predictive control approach which relies on the use of Newton's algorithm. Since there always will be model uncertainty due to load changes or component variations, we define another system with the same structure:

$$\begin{aligned} \dot{\hat{x}}(t) &= \widehat{A}_{\alpha(x,t)}\hat{x}(t) + \widehat{B}_{\alpha(x,t)}E \\ \widehat{y}(t) &= \widehat{C}\widehat{x}(t). \end{aligned} \tag{7}$$

The system (7) will be denoted the identified model and the equation (4) represents the real system.

B. ETH: Discrete-time Piecewise Affine (PWA) Systems

Polyhedral Piecewise Affine (PWA) systems are defined by partitioning the state-space into polyhedra and associating with each polyhedron an affine state-update and output function [5].

In previous publications [6], [7] the notion of the ν-resolution model has been introduced as an effective way to describe the hybrid dynamics of the synchronous step-down converter. This modeling approach leads to a discrete-time PWA converter model that is valid for the whole operating regime of the system. Additionally, it captures the behavior of the controlled variables within the switching period, and, through the choice of the resolution ν, provides a direct trade-off between the accuracy of the obtained model and the complexity that it introduces. As shown in [8], the converter PWA model uses a transformed converter state vector x' comprising the inductor current and the *output* voltage, both scaled over the input voltage; for $\nu = 3$, the discrete-time PWA state-update map of the ν-resolution model amounts to

$$\begin{aligned} x'[k+1] &= \Phi^3 x'[k] + \\ &+ \begin{cases} \Phi^2\Psi 3d[k], & d[k] \in [0, \frac{1}{3}] \\ \Phi^2\Psi + \Phi\Psi 3(d[k] - \frac{1}{3}) & d[k] \in [\frac{1}{3}, \frac{2}{3}] \\ \Phi^2\Psi + \Phi\Psi + \Psi 3(d[k] - \frac{2}{3}), & d[k] \in [\frac{2}{3} 1] \end{cases} \end{aligned} \tag{8}$$

with $\Phi = e^{F\tau_s}$, $\Psi = \int_0^{\tau_s} e^{F(\tau_s - t)} dt\, f$ and $\tau_s = \frac{T_s}{3}$. Since (8) refers to the transformed state vector, the matrices F, f and g are different from the ones in (1); see [8] for exact expressions.

C. KTH: Sampled Data Modeling

Our starting point is the following class of pulse-width modulated systems where the dynamics periodically switches in a given order between two affine vector fields

$$\begin{aligned} \dot{x}(t) &= \begin{cases} \check{F}x(t) + \check{G}_1 w(t) + \check{G}_2, & t \in \check{\mathbf{I}}(d[k]) \\ \hat{F}x(t) + \hat{G}_1 w(t) + \hat{G}_2, & t \in \hat{\mathbf{I}}(d[k]) \end{cases} \\ v_o(t) &= \begin{cases} \check{H}_1 x(t) + \check{J}_1 w(t), & t \in \check{\mathbf{I}}(d[k]) \\ \hat{H}_1 x(t) + \hat{J}_1 w(t), & t \in \hat{\mathbf{I}}(d[k]), \end{cases} \end{aligned} \tag{9}$$

where

$$\begin{aligned} \check{\mathbf{I}}(d[k]) &:= [kT_s,\, (k + d[k])T_s) \\ \hat{\mathbf{I}}(d[k]) &:= [(k + d[k])T_s,\, (k+1)T_s), \end{aligned} \tag{10}$$

and $T_s > 0$ is the switching period and $d[k] \in [0,\ 1]$ is the kth duty cycle. The converter in Section II belongs to this class and corresponds to the case when the state vector is $x = [i_l,\ v_c]^T$. The signal w is used to model uncertainty and disturbances in the load. The corresponding matrices are $\check{F} = \hat{F} = F$, $\check{H}_1 = \hat{H}_1 = g^T$,

$$\check{G}_1 = \hat{G}_1 = \begin{bmatrix} \frac{1}{x_l}\frac{r_o r_c}{r_o + r_c} \\ -\frac{1}{x_c}\frac{r_o}{r_o + r_c} \end{bmatrix}, \quad \check{G}_2 = f v_s, \quad \hat{G}_2 = 0,$$

and $\check{J}_1 = \hat{J}_1 = -\frac{r_o r_c}{r_o + r_c}$. Finally, in addition to (9) there is a discrete time output signal ψ, which is used for control design. It has the following components:

$$\begin{aligned} \psi_1[k] &= (S_{\text{ave}} v_o)[k] := \frac{1}{T_s}\int_{(k-1)T_s}^{kT_s} v_o(t)\,\mathrm{d}t, \\ \psi_2[k] &= \begin{bmatrix} i_l(kT_s) & v_0(kT_s) \end{bmatrix}^T, \end{aligned} \tag{11}$$

where S_{ave} denotes averaged sampling. The full detail of the model can be found in [9].

The switching system is assumed to attain at least one periodic solution x^p of period T_s when $w = 0$. The corresponding output, denoted by v_o^p, is assumed to satisfy $(S_{\text{ave}} v_o^p)[k] = v_{o,ref}$, $\forall\, k$, which is referred to as the tracking condition.

Taking into account the disturbance $w(t)$, the signals of the disturbed system will be different from the nominal periodic

version of them (i.e., x^p and v_o^p). The control objective is to ensure robust asymptotic tracking; i.e., the condition $\lim_{k\to\infty}(S_{\text{ave}}v)[k] = v_{o,ref}$ is satisfied under the presence the w. For this purpose, we consider a $\mathcal{H}_\infty$ performance index between the output v and the load disturbance w. We consider a sampled data model of the system as a basis for the control design. The error signals $x - x^p$ and $v_o - v_o^p$ are characterized by a lifted system. The lifted system provides a precise description of the dynamics of the error signals at the switching instances and it allows the effect of the continuous time disturbance w to be exactly accounted for in an equivalent discrete time model [9].

D. LTH: Robust discrete time model

It is natural to formulate synthesis problems for fixed frequency pulse-width-modulated systems in discrete time. This is so because we can only make control decisions at discrete time instances, $k := T_s k \geq 0$. The exact state propagation between time k and $k+1$ can easily be obtained by integrating (1) over one period, we obtain

$$x[k+1] = \overline{\Phi}(r_o)x[k] + \overline{\Gamma}(d[k], r_o). \tag{12}$$

The matrices $\overline{\Phi}(r_o)$ and $\overline{\Gamma}(d, r_o)$ depend nonlinearly on the duty cycle and the load in such a way that the model is not suitable for control synthesis purpose. To obtain a model that is useful in combination with our synthesis approach we will make a constant linear approximation

$$x[k+1] = \Phi x[k] + \Gamma d[k]. \tag{13}$$

When the model (12) is replaced by (13) the largest error we make can be expressed as

$$J = \sup ||\Phi x + \Gamma d - (\overline{\Phi}(r_o)x + \overline{\Gamma}(d, r_o))||,$$

where the supremum is taken over $(x, d, r_o) \in X \times D \times R$, where X is the set of states were the model should be valid, R is the set of values the load can assume and $D = [0, 1]$. Naturally, we would like minimize J. The robust approximation problem is to compute

$$\text{minimize } J(\Phi, \Gamma)$$

over (Φ, Γ). Our ability to solve this problem depend on the choice of norm and the description of the set $X \times D \times R$, the candidates are those which makes the resulting problem a finite dimensional convex optimization problem.

Whatever model approximation we have decided to make there will always remain some errors. A simple, and yet effective, way to model this uncertainty is to introduce an integrator state. Since our goal is to achieve asymptotic tracking of the voltage reference we augment (12) with an integrator state

$$e[k+1] = e[k] - g^T x[k] + v_{o,ref}. \tag{14}$$

This integrator state can now be used for feedback, and thus the controller will have integral action.

IV. The Control Problem

The goal is to develop synthesis methods subject to a number of criteria. The resulting closed loop system should

- (i) maintain a constant switching frequency with at most one switch per period,
- (ii) ensure that control and state constraints are satisfied,
- (iii) be robust to input voltage changes and load disturbances
- (iv) provide a regulator that easily can be implemented.

These design criteria are of very different nature and most existing design techniques can explicitly take into account only a few of them. The synthesis methods discussed in the next section illustrates new ideas on how to explicitly consider such design constraints.

The assumption that all states and parameters can be measured and/or estimated was allowed as a starting point in all the considered cases. However, the quantities that can be measured in a practically implemented system are the input and output voltage and the current of the inductor.

V. Proposed Control Approaches

A. CNRS-CRAN: Predictive control with load estimation

We propose the predictive control scheme presented in Fig. 2. We will briefly present each part of this scheme:

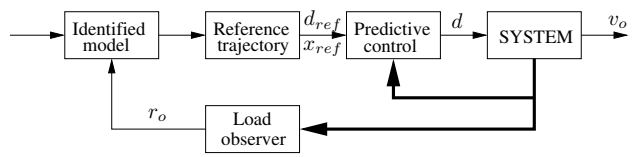

Fig. 2: Proposed control scheme

1) Generation of reference trajectory: This is the main contribution of our proposal, since we compute a reference trajectory which leads to the desired limit cycle behavior. Our task is to generate a reference x_{ref} and d_{ref} from the system (7) at the beginning of each period. This pair will be used as the input for the predictive control.

If the system (7) is periodic in steady state, then the duty cycle for the corresponding average model is constant:

$$d_{ref}^\infty = -\frac{v_{o,ref}}{\widehat{C}\widehat{A}^{-1}\widehat{B_1}}. \tag{15}$$

The duty cycle (15) allows to reach $v_{o,ref}$ in average. The corresponding state at the beginning of the period is:

$$x_{ref}^\infty = \left[\mathbb{I}_{2\times 2} - e^{\widehat{A}T_s}\right]^{-1} \widehat{A}e^{\widehat{A}T_s}\left[\mathbb{I}_{2\times 2} - e^{-\widehat{A}T_s d_{ref}^\infty}\right]\widehat{B_1}E.$$

The goal of the control is convergence to $(x_{ref}^\infty, d_{ref}^\infty)$. In order to obtain an optimal reference trajectory for the predictive control, we use a Newton algorithm to minimize a quadratic form of the error

$$\begin{aligned}\widetilde{x}_{ref}[(k+1)T_s] := x_{ref}[(k+1)T_s] - x_{ref}^\infty = e^{\widehat{A}T_s}\widetilde{x}_{ref}[kT_s] \\ - e^{\widehat{A}T_s(1-d_{ref}^\infty)}\widehat{A}^{-1}\left(e^{-\widehat{A}T_s\Delta d_{ref}[kT_s]} - \mathbb{I}_{2\times 2}\right)\widehat{B_1}E\end{aligned}$$

with respect to $\Delta d_{ref}[kT_s] = d_{ref}[kT_s] - d_{ref}^\infty$. This procedure ideally leads to a reference trajectory $(x_{ref}[(k+1)T_s], d_{ref}[(k+1)T_s])$ such that $\widetilde{x}_{ref} \to 0$.

2) Predictive control: Now, we search to track $(x_{ref}[(k+1)T_s], d_{ref}[(k+1)T_s])$ each period using a predictive model. As most of the predictive approaches, the structure of the control is composed of a prediction step and by an observation step in one period T_s [10], [11]. The prediction error criterion to be minimized is

$$\begin{aligned} G =& \|x_{pred}[(k+1)T_s] - x_{ref}[(k+1)T_s]\|_{Q_2}^2 \\ &+ \eta\left(y_{pred}[(k+1)T_s] - y_{ref}[(k+1)T_s]\right)^2 \\ &+ \gamma\left(\Delta d_{pred}[kT_s] - \Delta d_{ref}[kT_s]\right)^2, \end{aligned} \tag{16}$$

where η and γ are positive constants, Q_2 is a positive definite matrix, $\|x\|_{Q_2}^2 := x^T Q_2 x$, x_{pred} represents the prediction of the next state and y_{pred} is the output prediction. We use a one step Gauss-Newton iteration to minimize (16). If necessary, the duty ratio is adjusted to respect the current constraint.

3) Load observer: In this step we estimate the load r_o. This parameter appears in the matrices $\widehat{A}$, $\widehat{B}_1$ and $\widehat{C}$. In our scheme, we use a technique based on a least-square criterion:

$$\min_{r_o} \qquad (x - \widehat{x})^T Q (x - \widehat{x}). \tag{17}$$

The formulation (17) can be solved efficiently.

B. ETH: Model Predictive Control

Our controller is based on constrained finite-time optimal control (CFTOC) with a receding horizon policy, more specifically on Model Predictive Control (MPC) [12]. In the sequel, we assume that the input and output voltages v_s and v_o, respectively, and the inductor current i_ℓ can be measured. The output reference voltage $v_{o,ref}$ and the current limit $i_{\ell,max}$ are given by the problem setup.

The control model equations are augmented to include the system constraints on the control input, which is bounded by 0 and 1, and the current limit. In the case considered in this paper, the control problem is defined on a five-dimensional state-parameter space; this is given by the measured (scaled) converter state vector $x'[k]$, the previously used control input (duty cycle) $d[k-1]$, and the parameters of the control problem $p'[k] = [v'_{o,ref}\ i'_{\ell,max}]^T$, comprising the scaled output voltage reference and the scaled current limit.

To induce a steady state operation under a constant non-zero duty cycle, we introduce the difference between two consecutive duty cycles $\Delta d[k] = d[k] - d[k-1]$. Next, we define the penalty matrix $Q = \mathrm{diag}(q_1, q_2)$ with $q_1, q_2 \in \mathbb{R}^+$ and the vector $\varepsilon[k] = [v'_{o,err}[k]\ \Delta d[k]]^T$ with $v'_{o,err}[k]$ being an approximation of the average output voltage error, integrated over the k-th switching period. Finally, we consider the objective function

$$J(x'[k], d[k-1], p'[k], D[k]) = \sum_{\ell=0}^{N-1} \|Q\ \varepsilon(k+\ell|k)\|_1, \tag{18}$$

which penalizes the predicted evolution of $\varepsilon(k+\ell|k)$ from time-instant k on over the finite horizon N using the 1-norm. The control input at time-instant k is then obtained by minimizing the objective function over the sequence of control inputs $D[k]$ subject to the equations of the control model and the constraints on the duty cycle and the inductor current. This amounts to a CFTOC problem leading to the sequence of optimal duty cycles $D^*[k]$, of which only the first duty cycle $d^*[k]$ is applied to the converter.

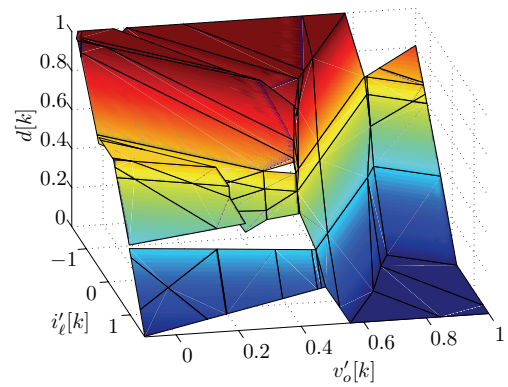

Fig. 3: State-feedback control law $d[k]$ for $d[k-1] = 0.6$, $v'_{o,ref} = 0.556$ p.u. and $i'_{\ell,max} = 1.667$ p.u.

To allow an implementation of the proposed controller despite the high switching frequency, the solution to the CFTOC problem needs to be explicitly pre-computed off-line. For this, the algorithm described in [13], [14] is used. The resulting state-feedback control law $d^*[k]$ is a PWA function of $[(x'[k])^T\ \ d[k-1]\ \ (v'_p[k])^T]^T$ defined on a polyhedral partition of the state-parameter space. Note that the normalization of the converter model over v_s allows one to avoid the introduction of the input voltage as a parameter in the control law, since any input voltage changes are translated to changes in the output voltage reference. For the converter PWA model derived for $\nu = 3$ with the model and control problem parameters considered in this benchmark, we compute the PWA state-feedback control law, which is defined on 633 polyhedral regions in the state-parameter space. Using the optimal complexity reduction algorithm [15], the controller is simplified to 121 regions. Fig. 3 depicts the control input $d[k]$ as a PWA function of $x'[k]$, where specific values are assigned to $d[k-1]$, $v'_{o,ref}$ and $i'_{\ell,max}$. By using this method an explicit MPC scheme for DC-DC buck converters was first presented as a novel control approach in [7].

In order to avoid introducing additional complexity to the CFTOC problem posed above, load variations are dealt with by using the state-feedback controller (derived for a time-invariant and nominal load), to which a loop comprising a Kalman filter [16] is added. For this, the reformulated (nominal) continuous-time model is augmented by a third state v'_e that tracks the output voltage error, and the Kalman filter is used to estimate it. In a last step, the output voltage reference $v'_{o,ref}$ is adjusted by the tracked voltage error.

C. KTH: Sampled-Data $\mathcal{H}_\infty$-Control

The control objective is to ensure robust asymptotic tracking. For robustness, the controller must ensure that the following $\mathcal{H}_\infty$ performance index

$$\|v_o - v_o^p\|_2^2 + \left\| \begin{bmatrix} qe_d \\ ru \end{bmatrix} \right\|_2^2 - \gamma^2 \|w\|_2^2 < 0 \tag{19}$$

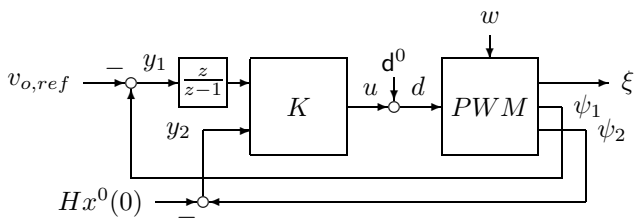

Fig. 4: Feedback Control Configuration, inner loop.

is satisfied for some $\gamma > 0$. Here $q > 0$ and $r \geq 0$ are design parameters, v^p is the nominal periodic solution, e_d and u are respectively defined as (d^0 is the nominal duty ratio)

$$e_d[k] := \sum_{i=0}^{k-1}(\psi_1[i] - v_{o,ref}), \quad u[k] := d[k] - \mathsf{d}^0.$$

The term e_d in (19) is introduced to penalize the integrator state and allows us to introduce integral action in the resulting controller. Finally, the inductor current i_l and the duty ratio should at all times satisfy the constraints

$$u + \mathsf{d}^0 \in [0,1],\ i_l \leq i_{\ell,max} \text{ where } i_{\ell,max} = 3\,p.u.. \quad (20)$$

The optimization problem involving the error dynamics and the constraints (19), and (20) is highly nonlinear and in general intractable for optimization. In the sequel we therefore consider the linearization of the state equation together with the quadratic approximation of (19). The constraints will be taken into account using an outer loop.

The inner loop contains a linear dynamic discrete time feedback regulator K. The controller K is designed to achieve robust asymptotic tracking for a small perturbation model of (9), (19), which is discussed in [9]. The structure of the inner feedback loop is described in Fig. 4.

The linear controller K is surrounded by an outer loop which, if necessary, will adjust the duty ratio computed by K. The outer loop is motivated by a number of reasons:

1) The state constraints (20) are not considered in the synthesis of K and need to be dealt with by some additional control structure.
2) The controller K has integral action and the presence of saturation suggests the need for an anti wind-up strategy.
3) The controller K is designed for a fixed nominal input voltage. Changes in the input voltage are handled by the integrator state, but the response can be made faster with feedforward control from the input voltage.

The outer loop can be implemented as a nonlinear map that remains inactive under normal operation, see [3].

D. LTH: Relaxed Dynamic Programming

Except for special cases, the computations required to solve a synthesis problem by means of exact dynamic programming are prohibitive. The only possibility is to resort to approximations. One such formulation was proposed in [17], see also [18] for examples. Using this formulation, different parameterization of the value function results in different algorithms. In this paper we will use the algorithm proposed by the author in [2]. This algorithm uses polynomials as parameterization. The computations are essentially a sequence of convex optimization problems and state and control constraints can be directly accounted for. The reader is referred to [2] for details.

The main control objective is to regulate the average output voltage to its reference $v_{o,ref}$, in presence of the constraints $d \in [0,1]$ and $i_l \leq i_{l,\max}$. To achieve this we define the step cost as

$$l(x, e, \hat{d}, d) = q_1|v_{o,ef} - g^T x|^2 + q_2|e|^2 + q_3|d - \hat{d}|^2, \quad (21)$$

where $\hat{d}$ is last control value and q_1,q_2 and q_3 are non-negative parameters chosen to reflect the relative importance of the different terms in l. The reason to introduce the extra state $\hat{d}$ is to avoid subharmonic oscillations at stationary conditions. We denote the state by $z = \begin{bmatrix} x^T & e & \hat{d} \end{bmatrix}^T$. Now, the optimal value function is defined by

$$V^*(z) = \min \sum_{k=0}^{\infty} l(z, d), \quad (22)$$

where the minimum is taken over $\{d[k]\}_0^\infty \in [0,1]^\infty$ such that $i[k] \leq i_{max}$. The algorithm in [2] can be used to compute an approximate convex value function $\hat{V}(z)$ which satisfies

$$\beta V^* \leq \hat{V} \leq \alpha V^*, \quad (23)$$

where $\beta \leq 1 \leq \alpha$ are constants. This function then defines the control law as,

$$d(z[k]) = \text{argmin}_{d\in[0,1]}\{\hat{V}(z[k+1]) + l(z[k], d)\}.$$

Note that the nominal closed loop system will be asymptotically stable on invariant subsets where inequality (23) holds. If the voltage source v_s is assumed to be measurable the response time of the closed loop can be improved considerably by using such measurements in a simple feedforward loop. If $v_{s,nom}$ is the nominal input voltage, a rescaling of the duty cycle to $\hat{d} = \frac{v_{s,nom}}{v_s} d$ implies that the feedback controller always sees the nominal gain, in fact the closed loop system dynamics will be independent of the source voltage.

VI. Simulation Results

The performance of the control approaches described above will be evaluated on four case studies. These represent different scenarios that are of interest in practical applications and pose performance challenges for any control scheme.

The output voltage reference is chosen to be $v_{o,ref} = 1$ and a current limit of $i_{\ell,max} = 3$ p.u. is imposed for all considered cases. The output regulation must be maintained with an accuracy of $\pm 1\%$ except when the current limit constraint is active in which case it may be lost.

1) The first case concerns the start-up of the converter from zero initial conditions. The initial state is given by $x(0) = [0,\ 0]^T$, the input voltage is $v_s = 1.8$ p.u.. During this start-up, the current constraint must be respected by the peaks of the inductor current.

2) In the second case, the response of the converter to input

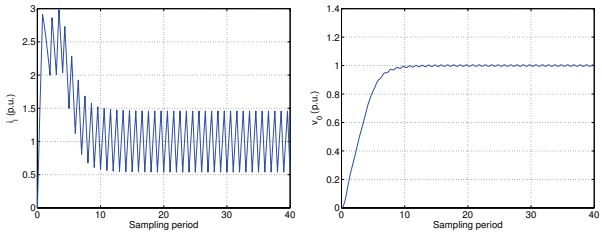

Fig. 5: CRAN: Closed loop step response from zero initial condition

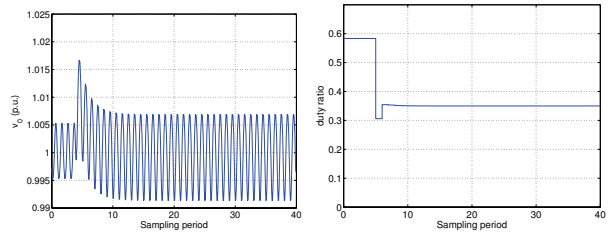

Fig. 6: CRAN: Closed loop step response to a step in the source voltage from $v_s = 1.8$ p.u. to $v_s = 3$ p.u.

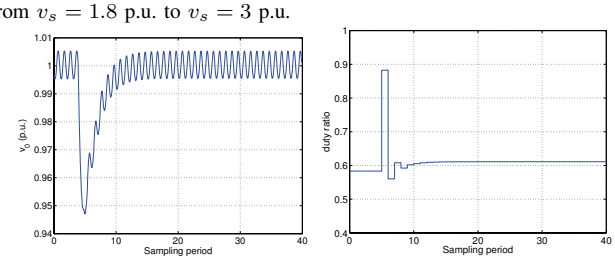

Fig. 7: CRAN: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.5$ p.u

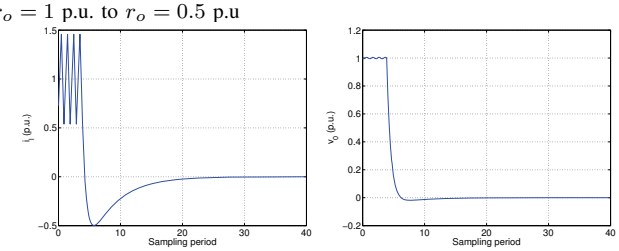

Fig. 8: CRAN: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.05$ p.u

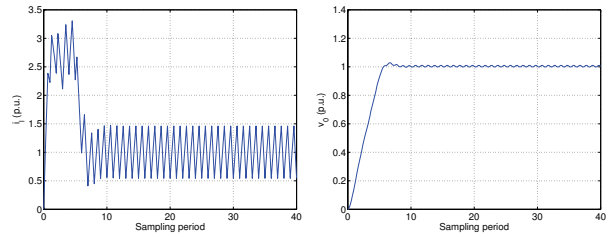

Fig. 9: ETH: Closed loop step response from zero initial condition

voltage variations is tested. The converter is initially at steady state when a step change in the input voltage from $v_s = 1.8$ p.u. to $v_s = 3$ p.u. is applied with $v_{o,ref} = 1$ p.u..
3) The third case examines the response of the converter to step changes in the output load. Starting from the steady state, the load drops from its nominal value to $r_o = 0.5$ p.u.
4) In the last case, we examine a crucial aspect of the controller operation, namely the system's protection against excessive load currents. The load drops from its nominal value to a very small one (namely to $r_o = 0.05$), almost creating a short circuit at the output. In this case, the controller must respect the current limit and force the output voltage to drop to the level that is needed in order to keep the current bounded.

Next we present a simulation study where each suggested control strategy is tested on the four test cases discussed above. All simulations are done using the same Simulink code. Additional plots and case studies can be found in [3].

1) CNRS-CRAN: Predictive control with load estimation: The simulation results are shown in Fig. 5-8. The first shows that the step to the desired limit cycle takes 10 sampling periods without any overshoot in the output voltage. The current limitation is respected.

Fig. 6 and Fig. 7 shows that the system recovers quickly from the input voltage step and the load resistance drop. We do not use a known value of r_o, but we make an estimation of the load by solving the problem (17). Finally, Fig. 8 shows the response when there almost is a short circuit.

A. ETH: Model Predictive Control

Regarding the optimal control scheme, the penalty matrix is chosen to be $Q = \text{diag}(4, 0.1)$, putting a rather small weight on the changes of the manipulated variable. In all simulations, the prediction horizon is set to $N = 2$. Based on this a PWA state-feedback control law is derived, which is shown in Fig. 3.

The simulation results for the four case studies are shown in Figs. 9-12. As can be seen, the current constraint is largely respected, and its small violations are due to the coarse resolution of the ν-resolution model. Moreover, one can observe in Fig. 11 a relatively large undershoot in the response of the system to a load resistance drop. This stems from the open-loop characteristics of the converter (relatively small output capacitor) and the fact that the worst-case scenario is examined here, where the disturbance is fed to the control scheme with the maximum time delay of one switching period.

B. KTH: Sampled-Data Control

The results to the four test cases are given in Fig. 13-16. The outer loop of our control structure is only active during the initial part of the step response and in the fourth test case when there almost is a short circuit at the output. It would be possible to tune the inner loop such that the current limit is satisfied using only the linear control but that results in slower responses. The feedforward from the input voltage improves the response to the input voltage disturbances but the integral action would be sufficient to ensure satisfactory performance. The inner loop is a dynamic controller that only uses the output voltage as a measurement.

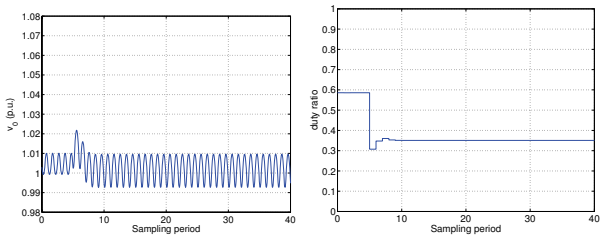

Fig. 10: ETH: Closed loop response to a step in the source voltage from $v_s = 1.8$ p.u. to $v_s = 3$ p.u

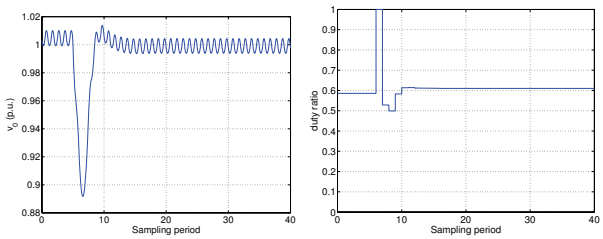

Fig. 11: ETH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.5$ p.u

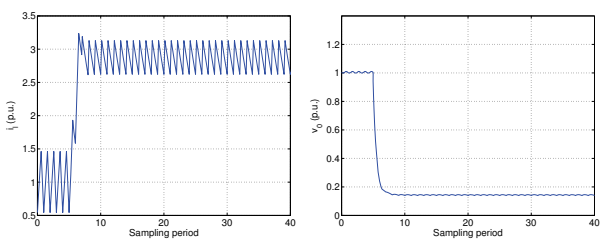

Fig. 12: ETH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.05$ p.u

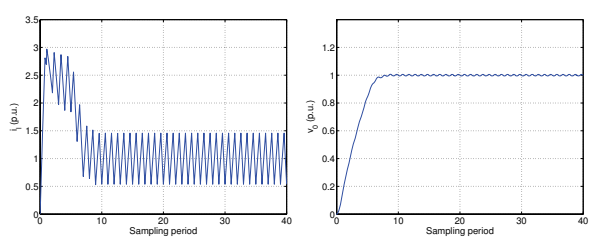

Fig. 13: KTH: Closed loop step response from zero initial condition

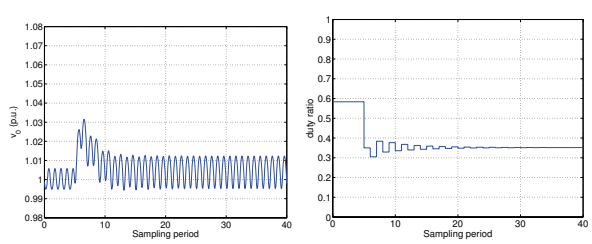

Fig. 14: KTH: Closed loop response to a step in the source voltage from $v_s = 1.8$ p.u. to $v_s = 3$ p.u

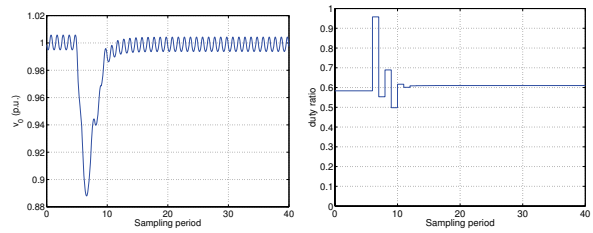

Fig. 15: KTH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.5$ p.u

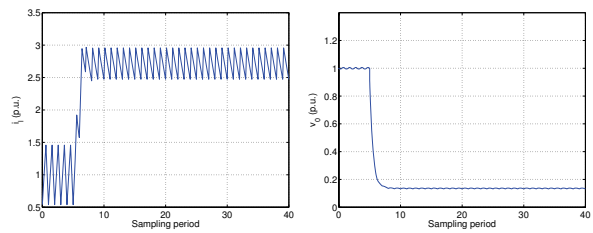

Fig. 16: KTH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.05$ p.u

C. LTH: Relaxed Dynamic Programming

Our simulations are shown in Fig 17-20. As can be seen the step response is very fast, it reaches its reference value after only 7% cycles. We used a relatively high value on q_1, as compared to q_2 and q_3. The current constraint $i \leq 3$ is respected during the step response simulations. To achieve this it was necessary to lower the bound to a value sightly less then 3. However, when the load drops, Fig. 20, from $r_o = 1$ p.u. to $r_o = 0.05$ p.u the current constraint is violated for a few cycles. This is not surprising since the controller was designed for nominal load. By lowering the bound further it would be possible to keep the current below the bound at the expense of a slower step response.

The quick response to an increase in the source voltage is due to a combination of integral action and feedforward, the response would remain acceptable if the feedforward was removed, see Fig. 18. The response to a 50% load drop is a bit slow, see Fig. 19, it takes approximately 30 cycles to get within 2% from the reference. It can be explained as a trade-off for fast step response.

VII. Comparison and Conclusions

The various control structures proposed in the paper are all based on digital control techniques where measurement

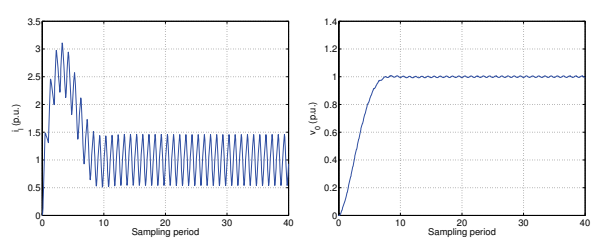

Fig. 17: LTH: Closed loop step response from zero initial condition

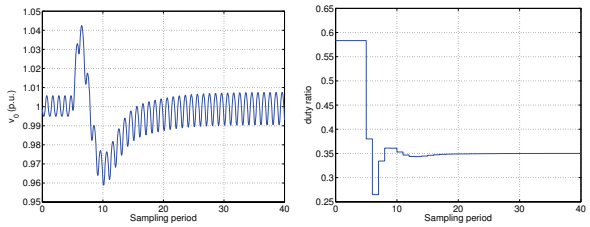

Fig. 18: LTH: Closed loop response to a step in the source voltage from $v_s = 1.8$ p.u. to $v_s = 3$ p.u

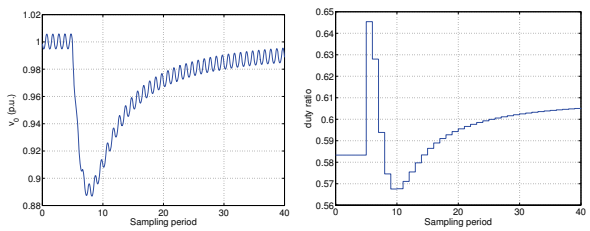

Fig. 19: LTH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.5$ p.u

and actuation takes place only at the sampling instances. The sampled data approach investigated by KTH is easy to implement and allows fast sampling rates to be considered. The model predictive control suggested by ETH and the relaxed dynamic programming approach by LTH allow a more systematic treatement of the nonlinear design constraints but may lead to increased yet manageable complexity of the resulting controller. The predictive control of CNRS-CRAN results in excellent performance but requires much more computation than the other approaches.

An important conclusion from this benchmark is that some nonlinear control action is necessary in order obtain a closed loop system that respects the state and control constraints without sacrificing too much in performance. Possible future directions would be to investigate how the methods can be extended to consider higher dimensional converter topologies and to investigate how they cope with parameter variations and dynamic uncertainties that appear under experimental conditions.

In Part 2 of this paper we investigate hybrid control strategies applied to a step-up (boost) converter. It is then necessary adjust the strategies discussed in this paper. For example, ETH reformulates their control problem as an

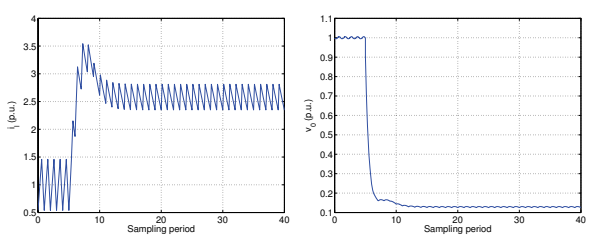

Fig. 20: LTH: Closed loop response to a step in the load resistance from $r_o = 1$ p.u. to $r_o = 0.05$ p.u

inductor current tracking scheme due to the non-minimum phase relation between output voltage and duty cycle. KTH uses a different cost function for the inner loop and designs the outer loop with the objective of improving the step response. LTH considers a different cost for their dynamic programming approach.

VIII. Acknowledgements

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