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Hellenbrand, Markus; Kilpi, Olli-Pekka; Svensson, Johannes; Lind, Erik; Wernersson, Lars-Erik

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Low-Frequency Noise in Nanowire and Planar III-V MOSFETs

Markus Hellenbrand*, Olli-Pekka Kilpi, Johannes Svensson, Erik Lind, Lars-Erik Wernersson

Department of Electrical and Information Technology, Lund University, Box 118, 221 00 Lund, Sweden

Abstract

Nanowire geometries are leading contenders for future low-power transistor design. In this study, low-frequency noise is measured and evaluated in highly scaled III-V nanowire metal-oxide-semiconductor field-effect transistors (MOSFETs) and in planar III-V MOSFETs to investigate to what extent the device geometry affects the noise performance. Number fluctuations are identified as the dominant noise mechanism in both architectures. In order to perform a thorough comparison of the two architectures, a discussion of the underlying noise model is included. We find that the noise performance of the MOSFETs in a nanowire architecture is at least comparable to the planar devices. The input-referred voltage noise in the nanowire devices is superior by at least a factor of four.

Keywords: III-V, Nanowire (NW), MOSFET, Low-Frequency Noise, Gate Oxide Defects, Border Traps

1. Introdution

The continuous improvement of the metal-oxide-semiconductor field-effect transistor (MOSFET) has been one of the major driving forces in electronics. In the future, further improvements of the MOSFET will require more innovative measures than the so far tremendously successful conventional geometrical scaling. Common suggestions include gate-all-around architectures and novel materials at the device level [1–4], and monolithic 3D integration at the system level [4, 5]. III-V nanowire (NW) MOSFETs, especially in a vertical architecture, can facilitate all these approaches at once and they have already demonstrated competitive or even superior performance in comparison with planar MOSFETs or FinFETs both in simulation [6] and in experiment [7–10].

In this paper we compare planar and NW III-V MOSFETs with similar channel and gate-oxide materials and investigate to what extent the change in architecture affects the low-frequency noise (LFN) of the devices, a property which is important as a technology quality metric at the device level, and for analog circuit performance at the system level [11]. Although LFN has been studied in both planar [12] and in NW [13] III-V MOSFETs, the two architectures have not yet been compared directly. The first part of the article describes the measured devices and the measurement setup. The comparison of the two MOSFET architectures comprises two metrics: the gate oxide defect density N_{bt} and the input-referred gate voltage noise power $S_{\mathrm{V_G}}$. In order to facilitate a detailed comparison of N_{bt}, its calculation is accompanied by a detailed discussion of the LFN model.

2. Devices and Measurement Setup

The following device descriptions focus on the channel and the gate stack as the two parts, which are most important for LFN. References are provided for further processing details.

For the vertical nanowire (vNW) devices, single nanowires were grown by metal-organic vapor-phase epitaxy on an n^+-InAs buffer layer integrated on Si. The nanowires were graded from intrinsic InAs on the source side to n^+-InGaAs on the drain side. During the InGaAs growth, an n^+-shell was formed around the InAs source to reduce the access resistance. After growth, the nanowires were covered with a top metal and a bottom spacer, so that the

*Corresponding author

Email address: markus.hellenbrand@eit.lth.se (Markus Hellenbrand)

channel area could be thinned down by digital etching (alternating surface oxidation and oxide etching) to form a recess gate. After digital etching, the 1 nm Al_2O_3/4 nm HfO_2 bilayer gate oxide (equivalent oxide thickness (EOT) $\approx$ 1.5 nm) and the 60 nm W gate metal were applied by atomic layer deposition (ALD) and by sputtering, respectively. A schematic of the device structure is provided in Fig. 1(a) and details about the processing can be found in [14]. Fig. 1(b) provides transfer curves representative of the vNW MOSFETs along with the gate lengths and the channel widths of the different measured devices. For the vNW MOSFETs, the channel width corresponds to the nanowire circumference.

For the planar reference devices, the channel consisted of not intentionally doped, 10-nm-thick InGaAs, which was grown by molecular beam epitaxy. In order to investigate differences between different gate oxides, three different ALD high-κ gate oxides were used in the planar devices: 5 nm Al_2O_3, 4 nm HfO_2, and 6.5 nm HfO_2. Evaporated Ti/Pd/Au was used as the gate metal. A schematic of the planar device structure is provided in Fig. 1(d) and details about the processing can be found in [15]. Fig. 1(e) provides a transfer curve representative of the planar MOSFETs along with the gate lengths and widths of the measured devices.

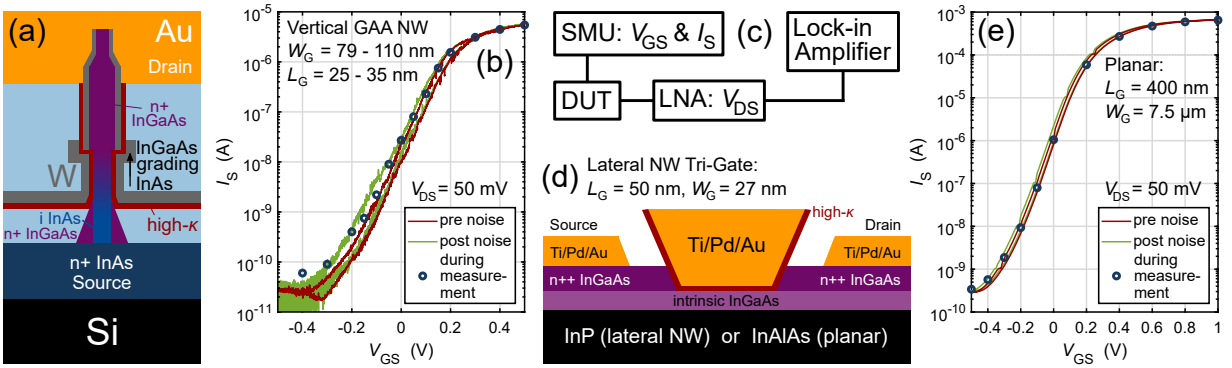

Figure 1: Schematics of the measured structures (a) & (d), the measurement setup (c), and representative transfer curves for the vertical (b) and the planar devices (e). Similar materials were used for the different devices and all devices exhibit good gate control with typically at least four orders of magnitude current modulation.

As an intermediate reference between the planar and the vNW MOSFETs, lateral NW MOSFETs from [16] are included in the analysis as well. Their structure was similar to that of the planar devices, although with a single lateral nanowire as the channel, formed by selective area growth, and with a gate oxide similar to that of the vNW devices. Prior to high-κ application, the nanowires were digitally etched, then sulfur-passivated and annealed in an N_2 atmosphere. Details about processing of the lateral nanowire devices can be found in [17] and their dimensions are included in Fig. 1(d).

Fig. 1(c) depicts the LFN measurement setup. The drain current of the device under test was measured by a low-noise amplifier (LNA), which also supplied the drain bias V_{DS} = 50 mV. The current noise power spectral density S_{I_D} was measured by a lock-in amplifier, which recorded the signal from the LNA. Gate and source bias were supplied by a Source/Measure Unit, which also measured the corresponding currents. For all measured devices, the gate current was at least one order of magnitude lower than the lowest source-drain current and in some cases it was below the measurement noise floor.

3. Results and Analysis

LFN in MOSFETs is typically explained as either number fluctuations, caused by gate oxide defects, or as mobility fluctuations, often described with the Hooge model [18]. The two mechanisms can be identified by the dependence of the measured S_{I_D} on the device current I_S. In the case of mobility fluctuations, S_{I_D}/I_S^2 is expected to be proportional to $1/I_S$, which was not observed for any of the measured devices. Instead, the measured S_{I_D} was roughly proportional to the transconductance squared (Fig. 2(b) and (c)), which identified number fluctuations as the dominant LFN mechanism. When measured as a function of the frequency f, LFN typically exhibits a $1/f^\gamma$ shape with $\gamma \approx 1$, where, in the case of number fluctuations, the value of γ depends on the spatial distribution of gate oxide defects. The $1/f^\gamma$

dependence was verified in Fig. 2(a), which presents a measurement for a vNW MOSFET, which is representative for the lateral NW and the planar devices as well.

In the case of number fluctuations, electrons from the MOSFET channel tunnel into and out of gate oxide defects with a certain time constant that determines the corresponding frequency component of S_{I_D}. The changing charge states in the oxide cause fluctuations in the flatband voltage and in carrier scattering, which then cause fluctuations in the device current. The two effects are called number fluctuations and correlated mobility fluctuations (CMF), respectively, and the relation between S_{I_D} and the gate oxide defect density N_{bt} can be derived as [19]

$$S_{I_D} = \frac{q^2 k_B T \lambda N_{bt}}{f^\gamma L_G W_G C_g^2}\left(1 + \frac{\alpha \mu_{eff} C_g I_S}{g_m}\right) g_m^2 = S_{V_{fb}}\left(1 + \frac{\alpha \mu_{eff} C_g I_S}{g_m}\right) g_m^2, \tag{1}$$

where g_m is the transconductance, q the elemental charge, k_B the Boltzmann constant, T the temperature, λ the tunneling attenuation length (calculated by the WKB approximation), L_G and W_G are the gate length and width, respectively, and C_g is the oxide capacitance in series with the quantum capacitance, which has to be taken into account for III-V MOSFETs. The prefactor including N_{bt} in the left term is the detailed expression for the power spectral density of the flatband voltage noise $S_{V_{fb}}$. For the term in parentheses, I_S is the device current, μ_{eff} the effective carrier mobility and α is the scattering parameter, which describes the change in mobility due to a change of charge in the gate oxide. To take into account screening due to charges in the channel, α decreases with increasing current. This can be expressed empirically as $\alpha = \alpha_0 - \alpha_1 \ln(N_q)$, where α_0 and α_1 are fitting parameters and N_q is the number of charges in the channel [20]. Here, instead of calculating N_q in detail, we express it as proportional to the device current I_S, which is an acceptable approximation, since $\ln(N_q)$ is multiplied by the fitting parameter α_1.

The derivation of (1), which relies on the assumption of elastic tunneling as the trapping/de-trapping mechanism, calls for a short side note. Evidence, in particular from reliability measurements [21], but also from some LFN measurements [22, 23], point towards inelastic rather than elastic tunneling as the charge exchange mechanism. However, since tunneling is still part of the inelastic mechanism, the assumption of elastic tunneling constitutes a lower limit of the inelastic model and it is as such that it was used in this study. This lower limit assumption especially affects the values for N_{bt}, calculated in the following, which thus also constitute a lower limit.

Results from different measurement techniques in literature [24–27] strongly suggest that N_{bt} varies with respect to energy with a minimum in vicinity to the InGaAs conduction band and increasing both above and below. Since different V_{GS} in the LFN measurement probe different energy levels in the gate oxide, N_{bt} is expected to vary with respect to the device current I_S. With two varying fitting parameters, N_{bt} and α, virtually arbitrary results could be obtained by fitting (1) to the measured data. Therefore, instead of choosing a random partitioning of the effects of a distributed N_{bt} and the CMF, we consider the two effects individually by studying the two "extreme" cases of (i) CMF with a constant N_{bt} and (ii) a varying N_{bt} without the influence of CMF (i.e. $\alpha = 0$).

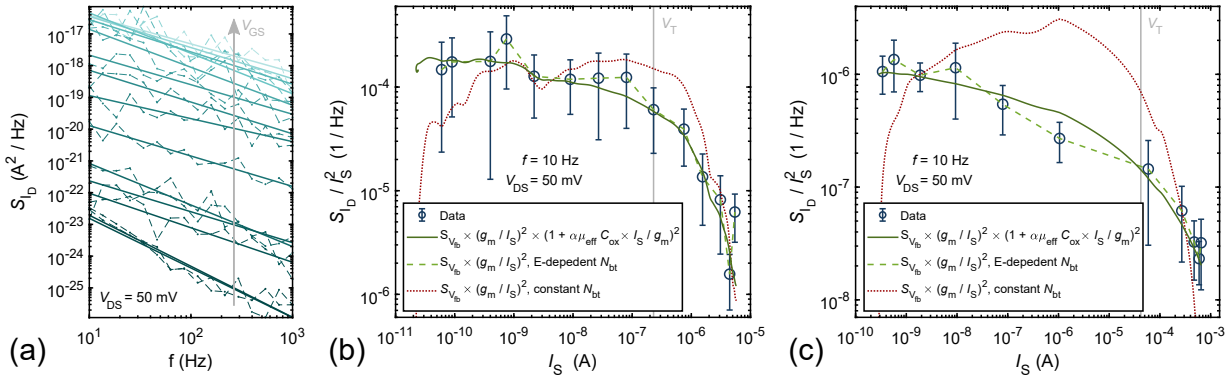

Figure 2: (a) Noise current power spectral density S_{I_D} as a function of the frequency for a vNW MOSFET. The $1/f^\gamma$ dependence with γ close to one is typical of LFN. (b) and (c) S_{I_D} at a fixed frequency of 10 Hz for a vertical and a planar device, respectively. Circles represent the measured S_{I_D} with the measurement standard deviation as error bars, lines represent different models with dependences according to the legend entries. Dark green, solid: Number and correlated mobility fluctuations with a constant N_{bt}. Light green, broken: Pure number fluctuations with an energy-dependent N_{bt}. Red, dotted: Reference for the assumption of pure number fluctuations with a constant gate oxide defect density N_{bt}.

Case (i) results in reasonable fits for the vertical and the planar devices, as demonstrated by the dark green, solid lines in Fig. 2(b) and (c). The corresponding constant N_{bt} are summarized in the inset of Fig. 3(a), where lines indicate the average N_{bt} for the respective architecture and shaded boxes indicate the standard deviation of the residuals. For the fits in Fig. 2(a) and (b), values of μ_{eff} = 1300 cm^2/Vs [13] and 3500 cm^2/Vs [28] were used for the vertical and the planar devices, respectively, C_g was typically about half the value of the geometrical oxide capacitance, and α typically varied between 2×10^4 and 10^3 Vs/C, which is in agreement with values from literature [11, 29, 30]. The simplest approach to (ii) is calculating N_{bt} pointwise from the measured S_{I_D} and (1) (with $\alpha = 0$). The resulting N_{bt} are presented in Fig. 3(a) and their shapes resemble the findings in literature. For both (i) and (ii), the values for the NW devices are comparable to those of the planar references and they are comparable to planar Si MOSFETs with HfO_2 gate oxides and a SiO_2 interface layer (EOT <2 nm, values adapted from [30] and [31]). In case (ii), the NW devices actually achieve lower values than both of the planar HfO_2 references. For the lateral NW MOSFETs, (i) did not properly model the measured data over the whole measurement range, whereas (ii) resulted in good fits, so that the lateral NW devices are not included in the inset of Fig. 3(a).

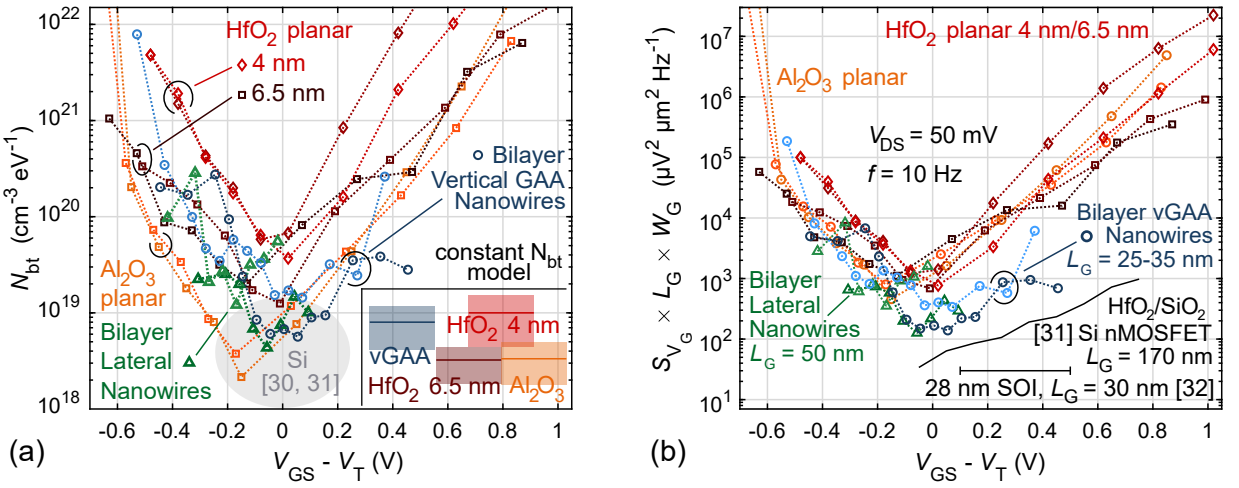

Figure 3: (a) Gate oxide defect density N_{bt} calculated with two models. (i) Inset: Constant N_{bt}, correlated mobility fluctuations. The lines represent the average values for all measured devices and the shaded boxes the standard deviation of the residuals. (ii) Main: Energy-dependent N_{bt}, no correlated mobility fluctuations. The differences between the two models are larger for the planar devices. Shaded oval as reference for HfO_2 on Si with a thin SiO_2 interface layer from [30] and [31]. (b) Input-referred voltage noise power spectral density S_{V_G} normalized with the gate area. Black lines as references for [31] as in (a) and commercial SOI [32]. The literature values from [30] and [31] are shifted with respect to V_{GS} so that they coincide with the measured minima. The metrics in both (a) and (b) reveal that MOSFETs in a (vertical or lateral) nanowire architecture are not degraded when compared with planar MOSFETs. Especially for the input-referred noise S_{V_G}, the nanowire devices actually achieve better values.

Although in most cases, both (i) and (ii) reproduced the measured data reasonably well, neither of the two models can be assumed to be sufficient on their own. (i) does not take into account the distributed nature of N_{bt}, while (ii) yields unphysical values for the highest and lowest V_{GS} (see Fig. 3(a)). Thus, a combination of both models is likely so that the actual N_{bt} resembles the shape of (ii), but with a shallower distribution and slightly lower overall values. Irrespective of the exact contribution of either model, it can be concluded that the mere change from a conventional planar to a NW architecture does not cause a degradation of the gate oxide in terms of LFN performance. In the comparison of the different high-κ gate oxides in the planar architecture, the HfO_2 oxides, especially the thinner ones, tend to exhibit higher values for N_{bt} than the Al_2O_3 oxides, when CMF are disregarded (i). Upon inclusion of CMF (ii), the differences are diminished, although the thin (4 nm) HfO_2 still tends to yield the highest values. These trends are most likely related to the ALD growth dynamics, but a more thorough investigation is beyond the scope of this study.

Since the differences in N_{bt} between (i) and (ii) are more prominent for the planar than for the NW devices (especially for HfO_2), it can be concluded that the relative contribution of CMF is stronger in the planar devices. This conclusion is supported by the comparison of the curves for (i) with the dark red, dotted reference curves in Fig. 2(b) and (c), which represent a constant N_{bt} without CMF. For the planar devices, it requires a larger contribution of CMF

to merge the two curves than it does for the NW devices. Since the effect of CMF was smaller or even negligible on both the vertical and the lateral NW MOSFETs, the influence of CMF seems to be related to the dimensions of the transistors rather than the lateral or vertical architecture. With large gate areas of L_G = 400 nm and W_G = 7.5 µm in the planar MOSFETs, mobility and scattering play an important role in carrier transport. With much shorter L_G = 25-35 nm (vertical) and 50 nm (lateral), the NW MOSFETs are governed by quasi-ballistic carrier transport [28] and they are approaching the one dimensional regime, which diminishes the influence of scattering. Furthermore, the larger surface-to-volume ratio in the nanowires is likely to entail a larger ratio of pure number fluctuations over correlated mobility fluctuations.

As a further comparison besides N_{bt}, Fig. 3(b) presents the input-referred gate voltage noise power spectral density $S_{V_G} = S_{I_D}/g_m^2$. This metric does not rely on a specific model, since it merely describes how much of a voltage fluctuation would be required at the gate terminal of a transistor without gate oxide defects to cause the same fluctuations in the device current that were measured for the actual transistor. Thus, S_{V_G} indicates the minimum size of a signal that could still be amplified by the transistor, if it was used e.g. as the input stage of an amplifier. Fig. 3(b) shows that in terms of S_{V_G}, the nanowire devices perform better than the planar references by typically at least a factor of four. For comparison with Si, Fig. 3(b) provides reference values for the same devices as Fig. 3(a) and furthermore for 28 nm silicon-on-insulator (SOI) MOSFETs, the S_{V_G} values of which were calculated from [32] and [33]. The values for the Si and the nanowire devices differ by only a factor three to five. With further optimization of the gate stack in the NW MOSFETs, it should be possible to overcome the remaining difference as well.

4. Conclusions

We measured and compared LFN in nanowire and in planar III-V MOSFETs. Number fluctuations were identified to dominate the LFN in both types of devices and two models were discussed in order to obtain values for the gate oxide defect distribution N_{bt}: number fluctuations with correlated mobility fluctuations for a constant N_{bt} and pure number fluctuations with an energy-dependent distribution of N_{bt}. The results for N_{bt} suggest that a combination of both is likely, where NW devices are less susceptible to correlated mobility fluctuations. Both models resulted in comparable values for N_{bt} in the NW and the planar architecture, which demonstrates that the change from a planar to a NW architecture does not deteriorate the gate oxide in terms of low-frequency noise. This, together with the lower values for the input-referred gate voltage noise in nanowire MOSFETs, demonstrates that the performance of the nanowire MOSFET architecture is not inhibited by low-frequency noise.

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