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High-Frequency III-V Nanowire MOSFETs

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1. Introduction

Scaling and miniaturization of transistors have been the enabler for the success of information technology. The decreased device dimension have not only lead to a larger device density as well as decreased power consumption, but has also allowed for higher device and circuit operation frequencies [1, 2]. Up till recently, this has mainly been achieved through scaling of planar Si-based metal-oxide-semiconductor field effect transistors (MOSFET)s, by the fabrication of very high performance CMOS circuits. The performance of planar III-V field effect transistors (FET)s and heterostructure bipolar transistors have also improved strongly through scaling, with maximum operation frequencies now exceeding 1 THz[3, 4]. High frequency electronics are of interest for many applications, including communication, computation and remote sensing. Higher device operation allows for active devices working at higher frequencies, but also reduced power consumption at lower frequencies, as well as better noise performance. The best device performance for low power mm-wave applications are today demonstrated by indium-rich III-V high electron mobility transistors (HEMT). These devices utilize a very high mobility quantum well channel and a large band gap gate insulator.

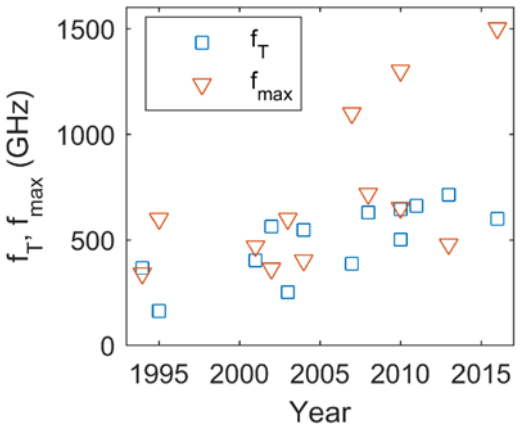

Figure 1. Evolution of high frequency perfomance for field effect transistors.

Figure 1 shows the evolution of the highest reported values for the maximum current gain frequency (f_T) and the maximum power gain frequency (f_{max}) for for InP-based high electron mobility transistors (HEMTs) for the last 20 years [3, 5-14]. Both f_T and f_{max} have improved strongly, with the current records of f_T=710 GHz [14] and f_{max}=1.5 THz [3]. This excellent performance has been achieved by aggressive device scaling: gate length reduction, decrease in the contact resistances and reduction in the gate to channel distance. Channel materials optimization, moving towards an InAs channel has been utilized for further improving the transport qualities.

While f_{max} has seen a strong improvement, f_T has only increased by ~25% since 2002. This is related to problems in scaling the planar HEMT, with minimum gate lengths having saturated at around 20 nm and barrier thicknesses at around 4-5 nm [1].

To improve on the device performance further, III-V MOSFETs utilizing high-k oxides are being explored [1]. The high relative dielectric permeability, and larger bandgap of high-k oxides, as compared with wide bandgap semiconductors, help improving the gate to channel distance and capacitance. A further, more radical approach is the utilization of nanowire structures for the transistor channel. A nanowire channel allows for tri-gate, or gate-all-around geometries which both have better scalability as compared with the traditional, planar counterpart. This can lead to development of transistors with better high frequency performance, which can lead to f_T exceeding 1 THz.

There are several methods for nanowire fabrication. They can broadly be classified into two categories: bottom up or top down[15] methods. The top-down approach most closely follows the traditional semiconductor fabrication route, where nanowire structures are etched out from a bulk semiconductor wafer. Hard-masks fabricated through lithography is used to define a local etch mask that is used for the pattern transfer into the semiconductor through typically a dry etch process[16, 17]. Both lateral (along the substrate) [17, 18] and vertical (parallel to the substrate) nanowires have been fabricated in this way [16].

The bottom up approach instead relies on epitaxy to locally grow the nanowires, using either selective area growth[19, 20] or catalytic particles in defining the nanowire position and size[21-23]. For selective area growth, openings in a hard-mask formed through lithography defines regions where epitaxy can take place on a substrate. For catalyst promoted growth, a metal particle deposited on a substrate defines the nanowire diameter. The epitaxial growth conditions are then adjusted to strongly promote epitaxial growth only below the metal particle, which allows for a nanowire to grow beneath the particle. The most common growth mode here is the vapor-liquid-solid (VLS) growth mechanism [24]. Again, both vertical and lateral nanowires can be fabricated for bottom-up nanowires.

In this review, we explore the results for III-V nanowire transistors that have demonstrated RF capabilities. For a general review of nanowire-type devices, see for example [2, 15, 25, 26]. Interestingly, while good DC device performance have been demonstrated for both bottom-up and top down fabricated nanowires, there are only reports in the literature for RF measurements utilizing bottom-up type of nanowires. This review is as follow. First, a brief review of RF metrics are introduced. The physics behind transistor and nanowire scaling are then presented. A basic ballistic nanowire modeling is then introduced. Finally, experimental RF results from lateral and vertical nanowire transistors are presented.

2. Review of RF metrics.

Nanowire FETs operate as thermionic devices with a gate electrode insulated from the channel. The resulting device model is thus very similar to the traditional three terminal HEMT or MOSFETs. It is thus possible to use the extensive knowledge from device modeling established from planar FETs, in understanding and modeling the nanowire FETs. Nanowire devices will be used in gate-all-around, or tri-gate configurations, where the effect of a body bias typically can be neglected. The device can then be described using a traditional, two-port small signal hybrid-π model, as shown in Figure 2 [27].

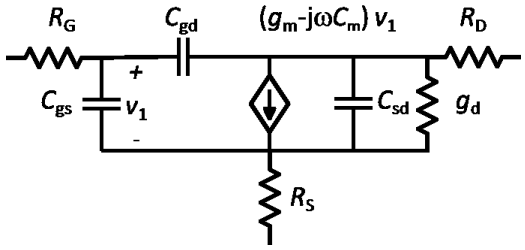

Figure 2 Small signal hybrid-π model describing a three terminal FET.

In figure 2, g_m is the device transconductance, and g_d the output conductance. R_G, R_D and R_s models the effective gate, source and drain resistances. R_G is here chosen to also include the effect of the channel resistance, R_i. This is reasonable for frequencies below the inverse channel transit time, and C_{gd}<<C_{gs}. The capacitances C_{gs}, C_{gd} and C_{sd} model the device displacement and charging currents, and include both the intrinsic device capacitances, as well as the extrinsic parasitic capacitances. C_m=C_{gd}-C_{dg} is the device mutual capacitance and ensures device charge conservation.

The intrinsic capacitances, mainly the total gate capacitance $C_{gg,i}$= $C_{gd,i}$+ $C_{gs,i}$, scales linearly with the total number of nanowires inside the device, and to first order also to the gate length. This capacitance is mainly reduced through decrease of the device gate length.

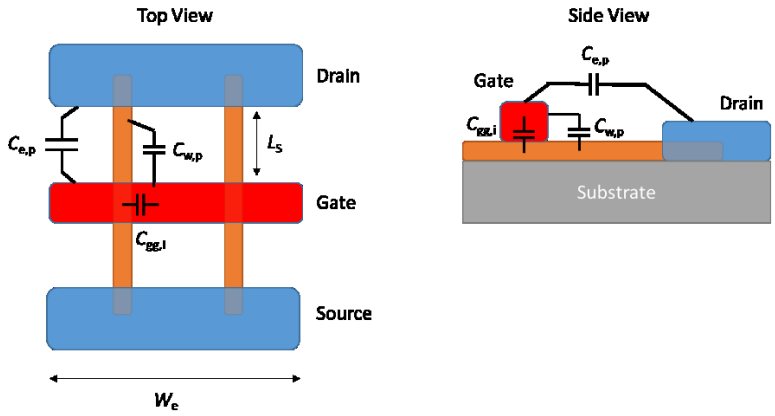

Figure 3. Top and side view for a lateral nanowire FET, with two nanowires constituting the channel. The main device intrinsic and parasitic capacitances are indicated. The side view plot only shows the gate-drain side of the wire for clarity.

For nanowire devices, special care has to be taken about the extrinsic, parasitic capacitances [28, 29]. Figure 3 shows a schematic layout of a lateral nanowire channel transistor, where a nanowire connect the source and drain electrodes, and charge modulation is performed through the gate electrode through $C_{gg,i}$. The device parasitic capacitances originates from the fringing electric field between the gate electrode and the source and drain reservoirs and ohmic contacts ($C_{e,p}$), as well as the fringing field between the gate electrode and the nanowire source and drain leads ($C_{w,p}$). The total gate parasitic capacitance C_p is then given by $C_p=C_{e,p}+C_{w,p}$, adding parasitic capacitance on between the gate-drain and gate-source terminals in the hybrid-π model. The parasitic capacitances depend on the geometry of the device, and scales directly with the total gate width W_e. For nanowire RF devices, the device channel typically consists of several nanowires in parallel in order to reach drive currents in the mA range. The key parameter to minimize the parasitic capacitances is the nanowire spacing [29, 30]. Dense nanowire arrays maximizes the number of nanowire per gate width, which improves the $C_{gg,i}$ to C_p ratio. Further, in a dense array, the electric field between the gate electrode and source/drain electrode is screened by the nanowires, which in part reduces the both $C_{e,p}$ and $C_{w,p}$. For nanowire FETs consisting of only a single nanowire, $C_{e,p}$ can become much larger as compared with $C_{gg,i}$ if very wide electrodes are used.

These parasitic constrains are the same as for lateral carbon nanotube based electronics, in also which dense arrays of nanotubes are needed for high device performance[30].

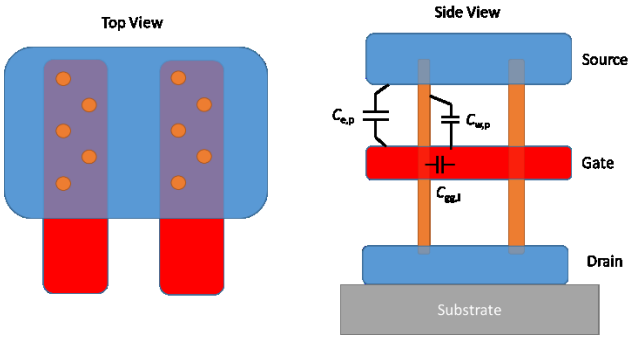

Figure 4. Top and side view for vertical nanowire FETs

For vertical nanowire FETs, similar parasitic capacitances exists, as show in Figure 4 [28]. Again, $C_{e,p}$ and $C_{w,p}$ is minimized by dense nanowire arrays. Also, removal of excess gate/drain/source metal overlap is of strong importance. This can otherwise leads to large parallel-plate like parasitic capacitances contributing to $C_{e,p}$. This can be achieved through lateral patterning of the gate, source and drain electrodes.
For RF applications, the most important metrics are the current gain, h_{21}, and power gain (MAG/MSG/U) [31].

The maximum current gain is defined from $h_{21}(f) = \frac{i_g}{i_{d_{v_d=0}}} = \frac{y_{21}}{y_{11}}$, where y_{xy} is the corresponding set y-parameters corresponding to Figure 2 [27]. The highest frequency where the transistor can amplify a current is called the transition frequency, f_T.

For the hybrid-π model shown in Figure 2, the single pole approximation gives $|h_{21}| \propto \frac{1}{\omega}$, which rolls off as -20dB/decade in a Bode plot. The corresponding f_T is then given from Eq. 1 as

$$f_T = \frac{1}{2\pi}\left(\frac{C_{gg,t}}{g_m} + (R_S + R_D)\left[\left(C_{gg,t}\frac{g_d}{g_m}\right) + C_{gd,t}\right]\right)^{-1}. \quad \text{Eq. 1}$$

$C_{gg,t}$ is the total gate capacitance including parasitic capacitances, and $C_{gd,t}$ the total gate-drain capacitance including the parasitic capacitances.
A large f_T thus requires a large value of g_m, large intrinsic voltage gain g_d/g_m, low source and drain resistances and low total capacitances. For comparison, the best planar InP HEMT have demonstrated f_T=710 GHz [14], and Si MOSFETs f_T = 485 GHz [32].

For any FET, as explained earlier the total capacitance can be divided into two parts – intrinsic capacitance and extrinsic capacitances, as shown in Eq. 2Eq. 3.

$$C_{gg,t} = C_{gg,i}(L_G) + C_{gg,p} \quad \text{Eq. 2}$$

$$C_{gd,t} = C_{gd,i}(L_G) + C_{gd,p} \quad \text{Eq. 3}$$

The intrinsic gate capacitance for a nanowire FET scales essentially linearly with the gate length $C_{gg,i} \sim L_G C'_G$, where C'_G can approximately be modeled as $\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{Cq} + \frac{1}{C_c}$.
C_{ox} models the oxide capacitance, C_q the quantum capacitance of the channel, and C_c the change centroid (or band bending) capacitance [33, 34].
For rectangular gate-all-around nanowire with an oxide thickness $t_{ox} << W_1, W_2$ [35],

$$C_{ox} \approx \frac{2\epsilon_{ox}\epsilon_0(W_1 + W_2)}{t_{ox}} + 2.232\epsilon_{ox}\epsilon_0. \quad \text{Eq. 4}$$

Where $\epsilon_{ox}$is the relative dielectric constant for the oxide, and ϵ_0 the vacuum permeability.
For a coaxial gate,

$$C_{ox} = \frac{2\pi\epsilon_{ox}\epsilon_0}{\ln\left(1 + \frac{r_{nw}}{t_{ox}}\right)} \quad \text{Eq. 5}$$

, where r_{nw} is the nanowire diameter [36].

For a rectangular nanowire, the charge centroid capacitance can be approximated from a series expansion of the solution of Poisson's equation, assuming a sinusoidal charge distribution. Keeping only the first term in the series expansion, and calculating the corresponding sub band shift from first order perturbation theory, one obtains the following approximate charge centroid capacitive term,

$$C_c \approx 6.94\epsilon_r\epsilon_0 \frac{(W_1^2 + W_2^2)}{W_1 W_2}. \quad \text{Eq. 6}$$

This expression is found to reproduce the sub band shifts within an error of around 25% for charge concentrations up to 5×10^{19} cm^{-3} as compared with results from effective mass Schrödinger-Poisson solver for a 10×10nm^2 nanowire.

The quantum capacitance $C_q = \frac{q\partial n_L}{\partial \psi_s}$, can be calculated from the device electrostatics and band structure, which is discussed in section 3 [33].

The transistor power gain corresponds to the capability to amplify the power from a source generator Z_S to a load Z_L. This is characterized by the transistor's maximum available gain (MAG) [31]

$$MAG = \frac{y_{21}}{y_{12}}\left(k - \sqrt{k^2 - 1}\right) \quad \text{Eq. 7}$$

where k is the stability factor [27]

$$k = \frac{2Re(y_{11})Re(y_{22}) - Re(y_{12}y_{21})}{|y_{12}y_{21}|}. \quad \text{Eq. 8}$$

Eq. 7 is defined for k<1 when the transistor is unconditionally stable. For k>1, the transistor is potentially unstable, and the corresponding figure of merit is the maximum stable gain (MSG), which is the maximum gain of the transistor that has been stabilized through shunt input/output resistors. MSG is obtained from Eq. 7 by setting k=1,

$$MSG = \frac{y_{21}}{y_{12}}. \quad \text{Eq. 9}$$

The maximum frequency when the transistor can supply power gain is called the maximum oscillation frequency, f_{max}. Depending on the exact transistor details, this will wither be set either by MAG or MSG, which leads to a non-analytical behavior of MSG/MAG, which makes extrapolation difficult.

For a transistor with a passive feedback network, implemented to make the transistor unilateral and thus stable as all frequencies, the corresponding maximum power gain is called Masons unilateral power gain, U [37].

$$U = \frac{|y_{21} - y_{12}|^2}{4\left(Re(y_{11})Re(y_{22}) - Re(y_{12})Re(y_{21})\right)}. \quad \text{Eq. 10}$$

This is valid for all frequencies, and for the hybrid pi model in Figure 1 one obtains $U \propto \frac{g_m^2}{4\omega^2}$ for high frequencies. The unilateral gain thus rolls off at -20 dB/decade, which can be used for extrapolation. f_{max} is obtain from the frequency when U=1.

If the source and drain resistances are small, one obtains [27]

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_G \left(C_{gd,t} + \frac{C_{gg,t} g_d}{g_m}\right)}}. \qquad \text{Eq. 11}$$

A large f_{max} thus requires a high f_T, low effective gate resistance R_G, low output resistance and a low $C_{gd,t}$. While not shown in Eq. 11, f_{max} is also degraded from R_D and R_S. Since a nanowire FET is expected to show a lower g_d as compared with planar FETs due to the better electrostatics, nanowire FETs can potentially be suitable for high values of power gain. The control of parasitic capacitances are of strong importance for the power gain. The intrinsic part of C_{gd} can be very small for a FET in saturation, which makes $C_{gd,t}$ dominated by the parasitic capacitances, and thus, the layout of the FET.

The best InP HEMTs have demonstrated f_{max}~1.5THz [3], and Si MOSFETs show f_{max}≈400 GHz [38] for L_G=32 nm.

In general, for RF applications f_{max} is the more important figure of merit, since it defines the maximum frequency where the power of a signal can be amplified. For circuit and noise design reasons, a well-balanced transistor with $f_T \approx f_{max}$ is usually of interest.

Finally, the minimum noise figure for a FET can approximately be shown to be (for f<<f_T)[39]

$$F_{min} \approx 1 + 2\sqrt{\gamma g_m (R_G + R_s)} \left(\frac{f}{f_T}\right) \qquad \text{Eq. 12}$$

Where γ models the effect of the channel thermal/shot noise. γ is 2/3 for a diffusive FET and larger (≈2) for a FET operating in velocity saturation [40]. The noise figure improves with a large f_T and low gate and source resistances.

3. Nanowire FET scaling for high RF performance.

A transistor suitable for RF applications should display a high f_T and a high f_{max}. This not only allows for circuit operation at high frequencies, but can also support low noise performance.

This is achieved by gate length scaling to reduce the capacitances and increase g_m, as well as controlled reduction of the parasitic capacitances and resistances.

Gate length scaling improves the transistor in two ways: reduction in the intrinsic gate capacitance and increase in the transconductance. The intrinsic gate (trans-)capacitances all essentially scale linearly with the gate length as shown in Eq. 2Eq. 6.

The transconductance can also improve as the gate length is scaled. For a long gate length device operation in the diffusive limit,

$$g_m = \frac{W C_g \mu_n (V_{GS} - V_T)}{L_G} \qquad \textit{Eq. 13}$$

Where μ_n is the electron mobility and V_{GS}-V_T the gate voltage overdrive. We directly obtain that g_m increases as L_g in scaled. For very short gate lengths, III-V transistors can operate close to the ballistic limit. For an ideal ballistic FET, the ballistic transconductance $g_{m,max}$ is independent of the gate length [41]. Scattering in the channel can however lower the transmission [42], resulting in a quasi-ballistic device and a lower transconductance, approximately given by $g_m \approx T \cdot g_{m,max}$, where T is the source-to-drain transmission probability. The transmission through a quasi-ballistic channel can be related to the mean free path, λ_0, as

$$T = \frac{\lambda_0}{\lambda_0 + L_G} \qquad \textit{Eq. 14}$$

Thus, as L_g decreases we expect T to increase towards unity, which will allow for device operation closer to the ballistic limit. Also for real, quasi-ballistic devices we expect g_m to increase as L_G is scaled, however slower as compared with a diffusive transistor.

However, as the gate length is scaled, the oxide and nanowire diameter also needs to be scaled to avoid short channel electrostatic effects. The distance from the source/drain electrodes that the channel potential is directly affected by the source/drain potential is described by the natural length scale, λ_n, of the transistor.
A simple expression for λ_n, valid around r_{nw}=t_{ox} for a cylindrical nanowire[43, 44] is

$$\lambda_n = \sqrt{\frac{\left(2\varepsilon_s r_{nw}^2 \ln\left(1 + \frac{t_{ox}}{r_{nw}}\right) + \varepsilon_{ox} r_{nw}^2\right)}{4\varepsilon_{ox}}}. \qquad \textit{Eq. 15}$$

r_{nw} is the nanowire radius, t_{ox} the oxide thickness, ε_s the semiconductor relative permeability and ε_{ox} the oxide relative permeability.

For good short channel control, we approximately require that

$$L_G \geq 5\lambda_n. \qquad \textit{Eq. 16}$$

In the limit of very thin nanowire channels, with t_{ox}>>r_{nw}

$$\lambda_n \approx \pi \frac{t_{ox} + r_{nw}}{2.4} \quad \textit{Eq. 17}$$

is a better approximation for λ_n then Eq. 15 [44, 45]. From Eq. 15 and Eq. 17 is it clear that λ_n decreases with r_{nw} and t_{ox}. As L_g is scaled to improve the device performance, t_{ox} and r_{nw} must to be simultaneously scaled. For Eq. 17, we obtain that $L_G \approx 6.5(t_{ox} + r_{nw})$. This can directly be compared with the expression for a ultra thin body planar FET[46],

$$\lambda_n \approx \pi(t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} t_w) \quad \textit{Eq. 18}$$

Which yields $L_G \approx 16(t_{ox} + t_w)$, assuming $\varepsilon_{ox} \approx \varepsilon_s$.
For a fixed L_G, a nanowire FET thus allows for usage of roughly 2-3 times oxide and body thickness as compared with a planar FET. This is the main electrostatic scaling advantage of a nanowire FET as compared with a planar FET. A device which does not fulfill Eq. 16 the non-ideal electrostatics will leads to a lower g_m, higher g_d as compared with the ideal device performance, both of which are strongly detrimental to the RF device performance.

The importance of the device channel thickness is related to the increased surface roughness scattering for thin body FETs. As shown in [47], the surface roughness limited low field mobility of a quantum well scales as

$$\mu_n \propto t_w^6. \quad \textit{Eq. 19}$$

The strong dependence on the quantum well thickness on the mobility can cause a rapid drop in the mobility. This can be the dominating scattering mechanism and limit the mobility as the quantum well is scaled to thicknesses below ~ 10 nm. The nanowire scaling advantage thus becomes important for transistors with gate lengths below around 50-35 nm. As a comparison, the Si industry introduced multi gate FinFets when going from the 28 nm node to the 22 nm node[48, 49]. Mobility is of importance also for quasi ballistic devices, since the mobility defines the mean free path [42].
In the non degenerate limit, a very simple relationship between the effective mobility and the mean free path is given by [33]

$$\lambda_0 = \frac{kT_L}{q} \frac{2\mu_n}{v_t} \quad \textit{Eq. 20}$$

where v_t is the thermal velocity and T_L the lattice temperature. A large mobility is thus essential in reaching quasi ballistic, device operation. The longer λ_n for a nanowire help to achieve this even for short gate length devices, due to the thicker body suppresses the surface roughness induced scattering.

This gives for a concise description of the interest for nanowire FETs for RF devices: the nanowire multi-gate geometry allows for usage of a thicker body thickness for nanowires as compared with planar FETs. For very short gate length lengths, where very thin body thickness are required according to Eq. 17 and **Error! Reference source not found.**, this can lead to a reduction in mobility and mean free path. Since the body of the nanowire FET can be about 2x thicker as compared with a planar FET, **Error! Reference source not found.** shows that the nanowire FET can show substantially higher mobility and mean free path.

4. Modeling of ballistic nanowire MOSFET.

To be able to quickly predict nanowire FET performance, simple and accurate modeling methods are of interest. From the nanowire FET scaling theory, we know that the nanowire diameter for highly scaled devices will be below around and below 10 nm. At these length scales, only a few 1D subband will be involved in the electron transport [50].

While effective mass models are accurate to nanowire diameters down to around 15-20 nm, accurate modeling of thinner nanowire requires the inclusion of non parabolic band structure effects [51]. It is expected that very short gate length III-V devices will operate close to the ballistic limit, modeling of ballistic transport is of importance. We here present a simple top-of-the-barrier model taking non parabolic effects into account. This model is expected to reasonable well determine the ballistic on-current. For more exact modeling, fully self-consistent quantum mechanical models should be used. Methods based on non-equilibrium Greens functions using atomistic tight binding [52], k·p[53] and effective mass models [54] have been used. Such models are especially of importance to accurately predict the source to drain leakage current for very short gate length devices [55].

To model the transistor performance, we use a simple 2-band k·p model which is reasonable accurate for direct bandgap III-V around the Γ-point, and apply it to rectangular nanowires with sides W_1 and W_2. The 3D non-parabolic dispersion is given by Eq. 21 [51, 56, 57].

$$E(1+\alpha E) = \frac{\hbar^2}{2m^*}\left(k_x^2 + k_y^2 + k_z^2\right) \qquad \textit{Eq. 21}$$

The parameter α models the degree of non-parabolicity for the material, and can be found from k·p theory to be [56]

$$\alpha \approx \frac{1}{E_g}\left(1 - \frac{m^*}{m_0}\right)^2. \qquad \textit{Eq. 22}$$

Where the bulk effective mass can be approximately be obtained from the bulk band gap as [58]

$$m^* \approx \frac{1}{1 + \frac{q20}{E_g}} m_0. \qquad \textit{Eq. 23}$$

To first order, the band structure of a direct bandgap III-V can thus be directly obtained from the bulk bandgap.

For a nanowire with hard wall quantization in the x and y direction, we require that $k_x = \frac{n\pi}{W_1}$ and $k_y = \frac{m\pi}{W_2}$ [51]. Eq. 21 then reduces to

$$E_{nm} = (\gamma_{nm} - 1)/2\alpha, \qquad \textit{Eq. 24}$$

With

$$\gamma_{n,m} = \sqrt{1 + \frac{2\alpha\hbar^2\pi^2}{m^*}\left[\frac{n^2}{W_1^2} + \frac{m^2}{W_2^2}\right]} = \sqrt{1 + 4\alpha E_{n,m}^p}, \qquad \textit{Eq. 25}$$

Where *n,m* corresponds to the different 1D subbands, and $E_{n,m}^p$ corresponds to the parabolic sub band energies.

By comparing to Eq. 21, each 1D subband can then be represented by an effective subband mass

$$m_{m,n}^* = m^*\gamma_{n,m} \qquad \textit{Eq. 26}$$

and an effective subband non parabolicity factor

$$\alpha_{n,m} = \frac{\alpha}{\gamma_{n,m}}. \qquad \textit{Eq. 27}$$

The effective subband mass increases with energy, and the effective non parabolocity factor decreases. The density of states for each 1D non parabolic subband can be evaluated to

$$D_{1D}(E) = \frac{\sqrt{2m_{n,m}^*}\left(1 + 2\alpha_{n,m}E\right)}{\pi\hbar\sqrt{E\left(1 + \alpha_{n,m}E\right)}} \qquad \textit{Eq. 28}$$

, with E given with respect to the subband minimum $E_{n,m}$. This reduces to the standard parabolic band expression if α_{nm}=0.

The total electron line concentration, given a fermi energy E_F can then be calculated from [33]

$$n(E_F) = \sum_{n,m} \int_{E_{n,m}}^{\infty} D_{1D}\left(E - E_{n,m}\right) f_{FD}(E_F - E)\, dE \qquad \textit{Eq. 29}$$

where f_{FD} is the Fermi-Dirac distribution function.

The semi-classical transistor current can now be calculated using the top-of-the-barrier model. First, we solve for the electrostatic potential E_0 at the top of the barrier [33],

$$E_0 = \alpha_D q V_{DS} + \alpha_G q V_{GS} - q^2 \frac{n(E_F - E_0) + n(E_F - E_0 - qV_{DS})}{2C_{eff}} \quad \text{Eq. 30}$$

α_D and α_G are empirical coefficients that model the short channel effects, which to first order can be obtained from solution of Laplace's equation, and $C_{eff} = C_{ox}||C_C$ from Eq. 4 and Eq. 6. For an ideal MOSFET, α_D=0 and α_G=1.

Since for 1D transport, the density of states and electron velocity cancels, the semi-classical ballistic current can be directly evaluated from

$$I_{1D} = \frac{2q}{h} \sum_{n,m} \left[\ln\left(1 + \frac{e^{(E_{FS} - E_{nm} - E_0)}}{kT}\right) - \ln\left(1 + \frac{e^{(E_{FS} - E_{nm} - E_0 - qV_{DS})}}{kT}\right) \right] \quad \text{Eq. 31}$$

where E_{FS} represents the source fermi level.

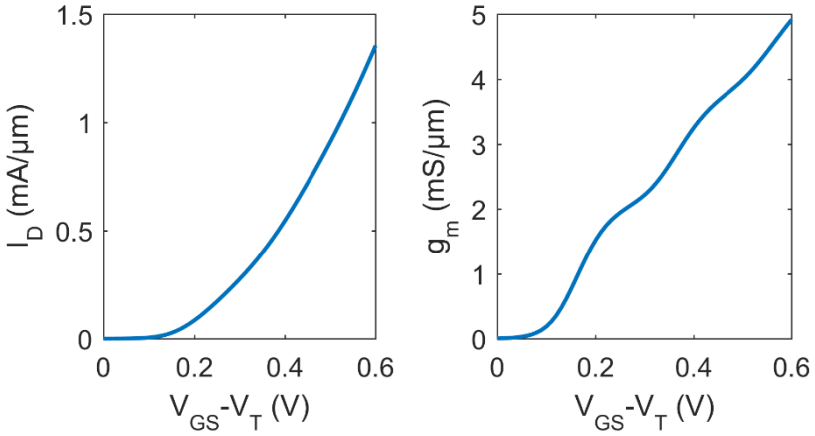

Figure 5. Simulated I_{on} and g_m for an InAs nanowire MOSFET. Normalization is performed using the total gated perimeter of the nanowire 2(W_1+W_2).

Figure 5. Simulated I_{on} and g_m for an InAs nanowire MOSFET. The used bulk bandgap is E_g=0.36 eV and bulk effective mass m^*/m_0=0.023. Figure 5 shows calculated I_D and g_m for a rectangular InAs nanowire with W_1=10 nm and W_2=8 nm, normalized to the total nanowire periphery, 2(W_1+W_2). t_{ox} is set to 3nm with a dielectric constant $\epsilon_{ox} = 20$. V_{DS} is set to 0.5V and V_T is choses at to achieve I_{off}=100 nA/μm at V_{GS}=0V. The shoulders in the g_m plot constitutes to separate subbands starting to conduct current.

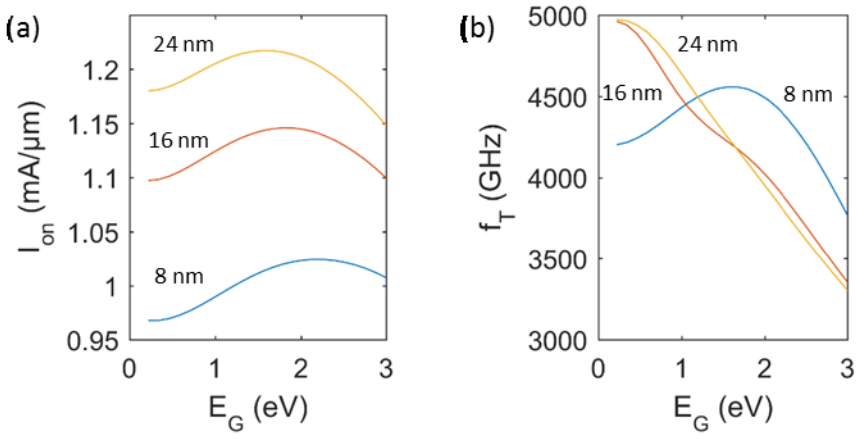

Figure 6. (a) Simulated I_{on} for different nanowire width W_2 and different bulk bandgaps E_G.(b) Simulated intrinsic f_T. A nanowire height W1=5nm is assumed for the different nanowires.

Figure 6 (a) shows the calculated I_{on} for a rectangular nanowire V_{DS}=V_{GS}-V_T=0.5 V, as a function of nanowire band gap as well as nanowire size, with W_1=5 nm and W_2=(8,16,24) nm for I_{off}=100 nA/μm. The gate length is assumed long enough that source-to-drain tunneling can be neglected. The calculated current is therefore a measure of the drive current capability. As E_G increases, the total density of states increases, but the injection velocity decreases, which leads to a complicated behavior with respect to I_{ON}. However, in the ballistic limit, the total current is fairly insensitive to the used band gap. There is a ~20% drop in the normalized on-current as the nanowire width is scaled to do 8 nm, originating from the reduced number of conducting sub bands for the smallest wire. The nanowires are thus expected to provide large on-currents for also for highly scaled devices. These numbers all compare favorably to the I_{on} for planar FETs, which are around 0.5 mA/μm [1]. Figure 6(b) shows a simulated approximate intrinsic $f_T \approx g_m/(2\pi C_{GG,i})$ for ideal L_G=20 nm device, ignoring 3D electrostatics effects. A constant electrostatic potential is assumed throughout the channel, so that the total channel charge (from which $C_{gg,i}$ can be calculated) is obtained as the top of the barrier charge as obtained from Eq. 29 and Eq. 30 multiplied by the gate length. An intrinsic f_T of a few THz can thus be achieved for a ballistic nanoscale nanowire transistor.

5. Experimental Lateral RF Nanowires

Lateral nanowire FETs are such that the nanowire constituting the channel is aligned along the substrate. These devices are thus similar to a traditional planar FET, and many of the fabrication techniques utilized for planar FETs can also be used for lateral nanowire FETs. The basic design idea for a lateral nanowire FET suitable for RF application requires: short gate lengths for high g_m, and low intrinsic capacitances, densely packed nanowire arrays for a large $C_{gs,i}/C_{gg,p}$ ratio and high quality, source and drain ohmic contacts for low access resistances. The same device designs is also applicable to lateral carbon nanotube devices.

Two type of nanowire device fabrication routes have been used for demonstration of lateral nanowire based device RF performance. First, direct growth of nanowire devices on the host substrate. Secondly, growth of nanowires on a different host substrate, which are then subsequently transferred to the device substrate. The first approach allows for a better control of nanowire placement and support of dense arrays, whereas the second allow for a greater freedom in nanowire growth as well as type of device substrate, where for example semiconductor nanowire FETs have been implemented on flexible substrates. Fabrication of dense nanowire arrays are however more difficult.

Transferred lateral nanowires.

The first compound semiconductor nanowire RF measurements were performed on a single vapor-liquid-solid (VLS) grown InAs nanowire that was mechanically transferred to a host substrate [59, 60]. First, 30-nm-diameter InAs nanowires were grown on a InAs substrate using colloidal Au-seed particles as catalysts. InAs nanowire were then randomly mechanically transferred to a semi insulating GaAs substrate covered in SiN_x.

To form a FET, electron beam lithography and lift off was used to locally form Ti/Au source and drain contacts on a single nanowire. 30 nm of chemical vapor deposition (CVD) deposited SiN_x were deposited as the gate dielectric. Electron beam lithography and lift off were used to locally deposit a Ti/Au gate electrode, with source/drain overlap. The gate used gate length was 1.4µm, with a Ω-type of gate. Figure 7 show a scanning electron microscope image of the device after fabrication. The large gate-source/drain overlap is visible.

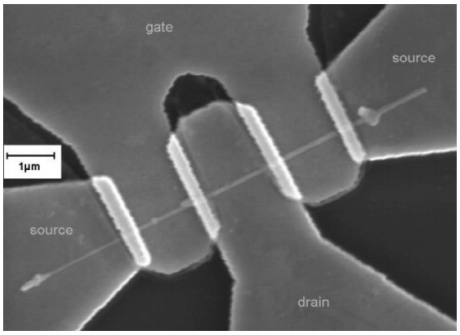

Figure 7. SEM micrograph of an lateral single nanowire InAs MOSFET. From [59].

The device thus consisted of a single nanowire, with large source/drain overlaps. A DC transconductance was extracted to 45 µS (normalized 0.64 mS/µm from the wire diameter). S-parameter measurements were performed on the single nanowire device, as well as on reference pads and open devices. The pad-pad capacitance was extracted to be around 8 fF, and the overlap capacitance to around 8-13 fF. The intrinsic gate capacitance was estimated from field simulations to be around 0.4 fF. The large difference between the overlap and pad capacitance limited any accurate extraction of the high frequency parameters of the device. An f_{max} of 15 GHz was extracted after removal of both pad and overlap capacitances. The calculated f_T before pad/overlap removal was a 0.2 GHz. While it is possible to measure S-parameters on single devices, the accuracy can be low.

A similar method has been applied to a AlGaN/GaN nanowires [61]. First, GaN nanowires are grown using the VLS method, and subsequently core-shell growt is utilized to form an AlGaN shell on the wires. The wires are then mechanically transferred to a sapphire substrate. LIfto-off based formations of ohmic contacts, and a 20-nm-thick SiN_x layer is deposited by chemical vapor deposition as a gate insulator. Finally, a 500-nm-wide gate metal is formed by electron beam lithography (EBL)-based lithography. The device shows a peak g_m=0.078 mS/µm at V_{DS}=10V. S-parameter measurements show f_T=5GHz and f_{max}=12 GHz after pad and electrode de-embedding.

A larger density of transfer nanowire [62] has been realized using a transfer printing method [63], which has been demonstrated RF devices on flexible substrates.
First, arrays of randomly positioned 30 nm diameter InAs nanowires were grown on a Si/SiO_2 substrate. By sliding a polyamide coated handling wafer across the growth wafer, the grown nanowires are transferred in an aligned fashion onto the polyamide layer. A lift-off technique was applied to locally transfer arrays on nanowires to the polyamide layer. Contact optical lithography was used for deposition of Ni source/drain electrodes, with a source-to-drain spacing of 1.5 µm. An 8-nm-thick Al_2O_3 layer was deposited as a gate oxide using atomic layer deposition (ALD). Contact optical lithography and lift-off was used for gate formation, producing a gate length of around 1.4 µm. The nanowire density was in total 4 NW/µm, with an estimated 2 NW/µm that cross the source/drain electrodes, with a total gate width of W=200 µm. After the device fabrication, the polyamide layer with the fabricated FETs was removed from the substrate, yielding RF compatible devices on a flexible substrate.

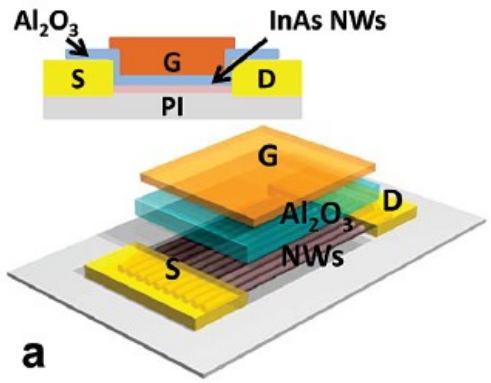

Figure 8. (a) Schematic image of the printed InAs nanowire FET. From [62].

A peak transconductance of 11 µS/µm as normalized to the complete gate finger width, corresponding to g_m=76 mS/mm from the total gated nanowire area was obtained at a V_{DS}=2.5 V. An intrinsic voltage gain of g_m/g_d=8 was obtained from the measurements.
After S-parameter measurements and open/short-pad deembedding, a peak f_T=1 GHz and peak f_{max}=1.8 GHz was obtained [62]. The pad-deembedding can be accurately performed, since the pad capacitance is substantially smaller as compared with the transistor device capacitances.

Higher values of f_T and f_{max} are expected by increasing the nanowire density in the printing process. While the transition frequency is not very high, this demonstrates the possibility of the transfer processes in fabricating devices on host substrates that are very different from the material of the nanowires, as well as the nanowire growth substrate.

VLS Epitaxial Nanowires

A method have developed for lateral VLS-type of nanowire growth, so called selective lateral epitaxy[64-66]. Au seed particles are deposited on a (001) or (110) substrate, typically GaAs. Using metal-organic chemical vapor deposition (MOCVD) growth, GaAs and InAs nanowires can be grown along the GaAs substrate. The nanowires randomly grow in the [0-11] or [01-1] direction on a (001) substrate, while unidirectional growth has been demonstrated on the (001) direction.

For RF compatible devices, GaAs nanowires with a width around 60 nm and a height of 75 nm were first grown. $Al_{0.3}Ga_{0.7}As$/GaAs HEMT type of nanowire devices were fabricated by embedding the GaAs wires with an n-type doped 50-nm-thick $Al_{0.3}Ga_{0.7}As$ layer followed by an n^+ GaAs contact layer. The GaAs n^+ layer was removed from the gate region using a recess etch. Devices with gate lengths between 150-300 nm and a nanowire density of around 1.5 NW/µm were fabricated [65]. EBL-based lift-off techniques were utilized to form source, drain and gate contacts. Figure 9 shows a scanning electron microscope (SEM) image after device fabrication.

The devices demonstrate a peak g_m=0.35 mS/µm at V_{DS}= 1-3V and V_{GS}= 0.6V for a L_g=150 nm device, in a tri-gate geometry. Due to the fairly large nanowire diameter and doped large bandgap barrier, these FETs operate similar to a planar AlGaAs/GaAs HEMT with a channel being formed at the heterojunction interface.

Small signal S-parameters show a peak f_T= 33 GHz and peak f_{max}=75 GHz, after pad parasitic removal for a L_G=150 nm device. The intrinsic parts of C_{gs} and C_{gd} is found to increase linearly with L_g. Figure 9(b) shows the measured and modeled microwave gains.

Detailed fits to the small signal measurements show that the parasitic capacitances contribute roughly 2/3 of the total gate capacitance, with $C_{gs,p}$~1.3fF/µm. Reduction in the parasitic capacitances can be achieved through a larger nanowire density [66].

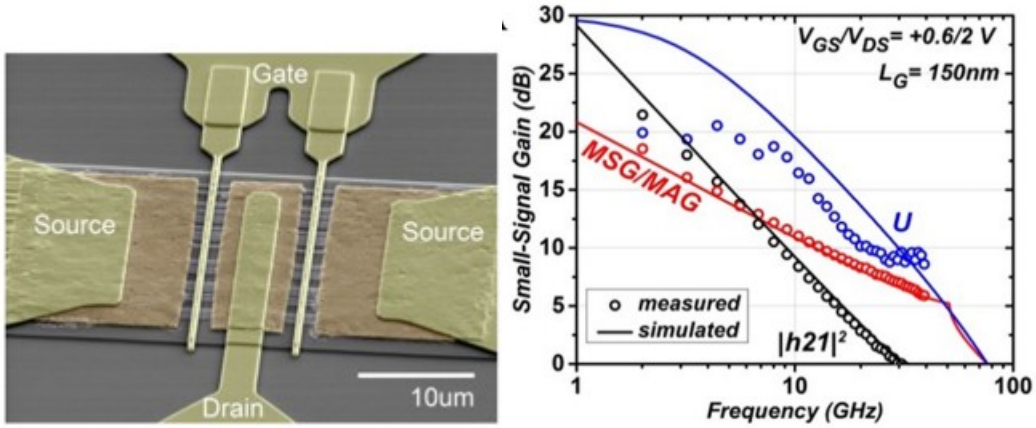

Figure 9. (a) False color SEM image of a lateral VLS GaAs NW FET. (b) Measured and modeled microwave gains. From [65].

InAs nanowire MOSFET devices in a gate all around geometry have also been fabricated using the SLE method, using Al_2O_3 as the gate oxide. For a 30 nm diameter nanowire with a gate length of 350 nm and oxide thickness 6 nm, a peak g_m=0.22 mS/µm has been reported at V_{DS}=0.5V [64].

A similar device fabrication methodology has been presented for GaN/Ga_2O_3 nanowires[67, 68]. Here GaN nanowires are grown on a (0001) Sapphire substrate from Au seed particles using the VLS growth method. The nanowires are found to grow in the $[11\bar{2}0]$ direction in contact with the sapphire substrate with a triangular shape defined by $\{1\bar{1}0\bar{1}\}$ side facets. A photon enhanced chemical oxidation process was applied to form a Ga_2O_3 gate oxide with a thickness around 6 nm. EBL defined lift-off of Ni/Au gate metal and Ti/Al/Ti/Au source and drain metal contacts. The used source-drain spacing was 1 µm with gate lengths between 50-500 nm. The devices show a peak g_m=0.78 mS/µm at V_{DS}=4V [67]. S-parameter measurements from devices consisting of a single nanowire were performed. After de-embedding of the pad and electrode capacitances, a peak f_T=150 GHz was obtained, with an uncertain extraction of f_{max}=180 GHz, both for an L_G=50nm. The nanowire density if fairly low, with >>1 NW/µm, implying that a substantial part of the total nanowire device capacitance is removed from the de-embedding.

Selective Area Growth

Selective area growth using hard masks have been implemented for high density arrays of nanowires on InP substrates [69-71]. Using electron beam lithography to expose a hydrogen silsesquioxane (HSQ) resist, SiO_2-like hard masks are formed on an InP S.I. substrate.

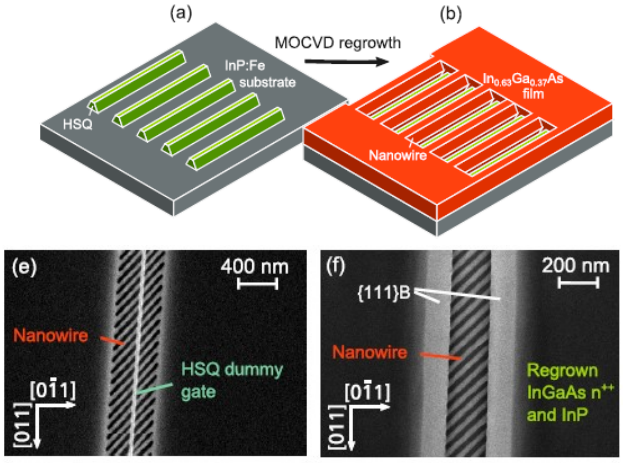

Figure 10.(a) and (b) Schematic illustration of lateral nanowire formation. (c) and (d) shows dumym gate formation and raised source/drain growth. From [70].

By patterning these lines into stripes, masks for nanowire growth are fabricated. MOCVD-growth is then used to selectively grow InGaAs nanowires in between the HSQ masks, as illustrated in Figure 10. The density and sizes of the nanowires are adjusted through HSQ line separation, as well as digital etching from ozone oxidation and wet etching. Nanowire widths down to W=25 nm and heights H=11 nm have been demonstrated. A high nanowire density of 14 NWs/µm have been realized.
The composition of the nanowires are set by the MOCVD growth, but with a larger In-concentration in the wires as compared with the 2D film outside of the wires. Nanowires with $In_{0.8}Ga_{0.2}As$ have been demonstrated.
N^{++} source and drain contacts are formed by depositing a HSQ dummy gate, followed by a second growth step, where a 40-nm-thick InGaAs n^+ layer is grown. The gate length of the devices are set by the width of the dummy gate, with demonstrated devices down to Lg=32 nm. The dummy gate process and regrowth is illustrated in Figure 10.
High-k Al_2O_3/HfO_2 gate oxide is deposited using ALD. Lift-off based fabrication of T-gates and self-aligned source and drain contacts, as well as coplanar probing pads finishes the process. The source/drain spacer thickness is here set by only the high-k oxide thickness, leading to a fairly large parasitic gate-electrode capacitance, $C_{e,p}$.

The RF compatible devices have demonstrated a peak DC g_m=1.8 mS/µm at V_{DS}=0.5 V. DC only devices consisting of only a single nanowire have demonstrated a very high g_m=3.3 mS/µm at V_{DS}=0.5 V, showing promising device performance [72].

S-parameter measurements show peak f_T=285 GHz and a peak f_{max}=350 GHz at V_{DS}=1V, after pad capacitance de-embedding for an L_g=32nm device. Small signal modeling of the devices are used to extract the V_{GS} and V_{DS} behavior of the intrinsic device metrics. $C_{gg,i}$ found to be around 2fF, whereas the total parasitic capacitance C_p is measured to 12fF [70]. The device performance is thus to a large extent limited by the parasitic capacitances, which is mainly dominated by the large $C_{e,p}$. Introduction of side wall spacers are suggested to decrease the parasitic capacitances, as well as increase of the nanowire density.

6. Vertical RF Nanowire MOSFETs.

Vertical nanowire FETs are constructed such that the nanowires constitution the transistor channel is perpendicular to the substrate. This is the typical geometry of VLS-grown nanowires. While the vertical transistor technology is more advanced as compared with the previously discussed planar technologies, vertical devices has a number of advantageous properties as compared with the lateral nanowire technologies. For high density device integration, the gate length and source/drain contacts lengths does not directly influence the transistor cell size [2]. The nanowires can be directly processes as grown, which removes the mechanical transfer processes used for other VLS-grown wires. This allows for accurate device placement and direct integration of tightly spaced nanowire devices.

In the vertical geometry, the source, gate and the drain are fabricated on top of each other along the growth direction of the nanowire, which makes this kind of device processing different as compared with the planar processing for the lateral nanowire devices [19, 23, 73-75]. Of importance is to separate the gate, drain and source electrodes, as well as minimize the electrode overlap [28]. The gate placement is respect with source and drain doping inside the wire most also be well controlled, in order to minimize access resistance.

Vertical nanowire InAs MOSFETs suitable for RF performance have been demonstrated on both InP and Si substrates [76, 77].

First, Au-seed particles are formed on a substrate using EBL and lift-off. The seed particles defines the nanowire positions and diameters. RF compatible devices have been demonstrated on either (111) S.I. InP substrates as well on a 300-nm-thick InAs buffer layer grown on highly resistive (111) Si substrates [78].

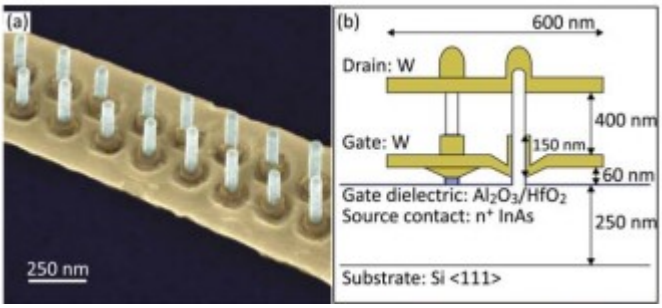

Figure 11. (a) A row of vertical nanowires after gate formation. (b) Schematic side view of a vertical InAs nanowire FET. From [76].

Using the VLS growth method, nanowires with lengths around 500-1 µm are grown, with typical diameters around 20-40 nm. The explored device geometry usually consists of zig-zag rows of nanowires, with a nanowire pitch of 100-300 nm [76]. The presented RF devices utilize a non-self-aligned gate process, but recently also DC performance of self-aligned gates have been demonstrated [79]. After growth, the wires are coated in high-k oxides using ALD, typically an Al_2O_3/HfO_2 type of dielectrics. The devices with the best demonstrated RF performance used a 1.4 nm EOT consisting of 10 cycles of Al_2O_3 and 50 cycles of HfO_2. The gate is separated from the source contact using a spacer layer. Organic spacers and SiN_x inorganic layers have been utilized for RF devices to separate the bottom source contact

To minimize the parasitic electrode capacitance, the gate and drain electrodes are preferably patterned to remove any excess metal. Figure 11(a) shows a SEM micrograph of the vertical nanowire FET after gate formation, as well as a schematic image of a vertical FET in (b).

The best presented RF device show a peak DC g_m=0.7 mS/µm at V_{DS}=0.8 V (normalized to the total gated nanowire circumference) for an L_G=150 nm device, with a total nanowire density of 10 NWs/µm. These wires are fabricated using a Si substrate [76].

From S-parameter measurement, and extrapolated f_T=104 GHz and f_{max}=155 GHz for device with EBL-patterned source and drain contacts. For these devices, only the pad capacitance are de-embedded. Device without patterned gate and drain electrodes, demonstrate f_T=25 GHz and f_{max}=100 GHz. The large difference in f_T is due to the strong decrease in the

electrode parasitic capacitance $C_{e,p}$ with elimination of excess electrode area. The f_{max} difference is smaller, since the patterned gate electrode have a larger R_G as compared with the large area gate electrode. This can be mitigated through use of different electrode layout, where the full 3D layout of the vertical nanowire structures are used to minimize both the electrode capacitances as well as the gate resistance. The peak f_T measured for these devices is f_T=141 GHz, but with a lower f_{max} = 61 GHz [80].

7. Summary and Conclusions

Tables 1-2 summaries the presented data for the highest presented III-V nanowire FETs in various embodiments. The selective area growth In-rich nanowires have demonstrated the highest g_m and f_T/f_{max}. RF compatible devices on flexible and different host substrates have also been demonstrated, which is showing possibility for nanowire-based electronics on various substrates. Nanowire FETs have further been epitaxially implemented in vertical geometries on Si substrates, with demonstrated f_T>100 GHz.

Table 1. Record lateral nanowire RF FETs

FET fabrication	Nanowire Material	g_m (mS/µm)	f_T (GHz)	f_{max} (GHz)	Ref.
Mechanical Transfer	GaN	0.078	5	12	[61]
Printer Transfer, Flexible substrate	InAs	0.076	1.18	1.53	[62]
Lateral VLS growth	GaAs	0.35	33	75	[65]
Lateral VLS growth	GaN	0.7	150*	180*	[67]
Lateral, selective area	InGaAs	1.8	285	350	[70]

(*) After electrode capacitance removal.

Table 2. Record vertical nanowire RF FET

FET fabrication	Nanowire Material	g_m (mS/µm)	f_T (GHz)	f_{max} (GHz)	Ref.
VLS, Si substrate	InAs	0.7	105	155	[76]

For nanowire devices to approach the RF performance of HEMTs, two main objectives need to be fulfilled. The nanowire gate length, oxide thickness and nanowire diameter needs to be scaled in order to increase the intrinsic transconductance and minimize the intrinsic capacitances. The nanowire packing density needs to be increases in order to minimize the effect of the parasitic wire and electrode capacitances. Further, optimization of the source/drain electrodes need to be performed to reduce the contact and access resistances.

A wide variety of integration routes for nanowire devices have been investigated in the literature. The DC nanowire performance have demonstrated excellent performance, with highly competitive device performance. The RF nanowire performance have improved very rapidly during the last few years, with transitions frequencies increasing from a few GHz in 2010 up to close to 300 GHz in 2014. This shows promise for implementation of future very high performance nanowire devices for RF applications.

An overview of nanowire FET devices for RF applications have been presented. The electrostatic advantage for nanowires as the gate length is scaled below 30 nm over traditional planar FETs have been demonstrated, highlighting the reduced effect of the surface roughness induced scattering due to the thicker body. A simple scheme for calculating the ballistic current nanowires including non-parabolic effects have been introduced. An overview of the demonstrated RF compatible III-V nanowire devices have then been performed.

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