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First InGaAs Lateral Nanowire MOSFET RF Noise Measurements and Model

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The first radio frequency (RF) noise measurements on lateral nanowire metal-oxide-semiconductor field-effect transistors (MOSFETs) and a noise model are presented. We have characterized the RF noise and scattering parameters of an indium gallium arsenide (InGaAs) device. A fitted model yields extrapolated $f_t = 316$ GHz current gain cutoff and $f_{\max} = 166$ GHz maximum oscillation frequency. This device technology is being developed for millimeter wave circuit implementations, targeting a 94 GHz carrier frequency. The modeled intrinsic $F_{\min} < 1$ dB minimum noise figure obtained promises performance at the target band, given reduction of gate parasitics. In any wireless system, noise and bandwidth limits the performance. Understanding of RF noise in nanowire MOSFET devices is thereby key for realization of future radar and communications systems.

Device Fabrication and Measurements

The lateral nanowire MOSFET is similar to a previous device [1]. However, it has air spacers and a line gate as shown in Fig. 1. Semi-insulating (iron (Fe) doped) indium phosphide (InP) is used as substrate. Nanowires were regrown by metal organic chemical vapor deposition (MOCVD) of InGaAs through a hydrogen silsesquioxane (HSQ) mask. The 200 nanowires of the MOSFET are approximately 25 nm wide and 10 nm high with sloping facets. An HSQ mask is then used in MOCVD contact regrowth of n^+ In_{0.63}Ga_{0.37}As. Mesa isolation by wet etching, nanowire ozone/ wet digital etching, atomic layer deposition (ALD) of high- κ gate dielectric, and repeated lift-off patterning with titanium (Ti)/ palladium (Pd)/ gold (Au) is used to finalize the devices. The gate dielectric, approximately 1 nm equivalent oxide thickness (EOT), is hafnium oxide (HfOx) with a thin interface layer of aluminum oxide (AlOx).

Output and transfer dc characteristics of the $L_g = 50$ nm gate length and $W = 7$ μ m gate width lateral nanowire MOSFET is shown in Fig. 2(a)-(b). This indicates a $g_m = 1.0$ mS/ μ m dc transconductance peak and a $I_{DS} = 2.2$ mA/ μ m drive current; both are evaluated at $V_{GS} = 1.25$ V gate bias and $V_{DS} = 1.50$ V drain bias. Noise and scattering parameters were analyzed from 100 MHz to 50 GHz. Measured scattering parameters are presented in Fig. 3, as well as small signal modeled parameters and optimum source reflection coefficient, Γ_{opt} . The measured and modeled noise figure (50 Ω source and load) is shown in Fig. 4, as well as modeled minimum noise figure.

Small-Signal Noise Model

A small-signal model that includes noise sources, shown in Fig. 5, is fitted to the measured characteristics. This has a brute force minimized relative error to (open short deembedded) the measured admittance parameters, available and current gain, as well as system referred noise figure. Thermal noise in the effective channel resistance, $r_i \propto 1/g_m$, and the output noise current spectral density, $S_i(f)$, are intrinsic noise sources.

The intrinsic noise sources are well defined for a diffusive device but less so for the quasi-ballistic nanowire MOSFET studied here. In this model, the intrinsic gate noise from the channel resistance, $r_i = 38 \Omega = 1/(1.4g_m)$, translates to noise at the input and a correlated term at the output. The output noise current spectral density, $S_i(f) = S_{i,f}(f) + S_{i,th}$, is modeled in two parts. Flicker noise, $S_{i,f}(f)$, is included to fit the lower frequency range of the measured noise figure. This includes interactions between oxide trap states and charges in the channel region. Thermal noise, $S_{i,th} = 4k_B T g_m \gamma$, is described here by a quasi-ballistic excess noise factor, $\gamma = 2/3$, assigned to the transconductance [2]. This model indicates $NF_{\min} = 4.8$ dB minimum noise figure at 94 GHz, limited by gate resistance.

One simplification is to compress the intrinsic RF noise into an equivalent electron channel temperature, $T_{\text{ec}} = T(1 + \gamma g_m/g_{ds} + r_i g_m^2/g_{ds}) = 3755$ K, assigned to the output conductance [3]. Introduction of a T-gate process and proper device scaling is expected to make available a value closer to the modeled $NF_{\min} \approx 1$ dB observed at lower frequencies. These initial results show potential for millimeter-wave amplifiers with high gain and low noise figure.

Acknowledgment

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[1] C. B. Zota, et al., IEEE-TED, vol. 61, no. 12, p. 4078, (2014). [3] M. W. Pospieszalski, IEEE Microw. Mag., vol. 11, no. 6, p. 61, (2010).
[2] C. Enz, IEEE-TMTT, vol. 50, no. 1, p. 342, (2002).

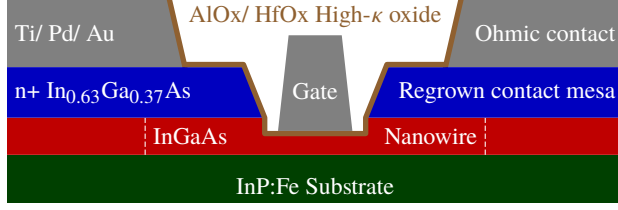


Fig. 1: Schematic cross-section of the regrowth and lift-off defined InGaAs lateral nanowire MOSFET technology.

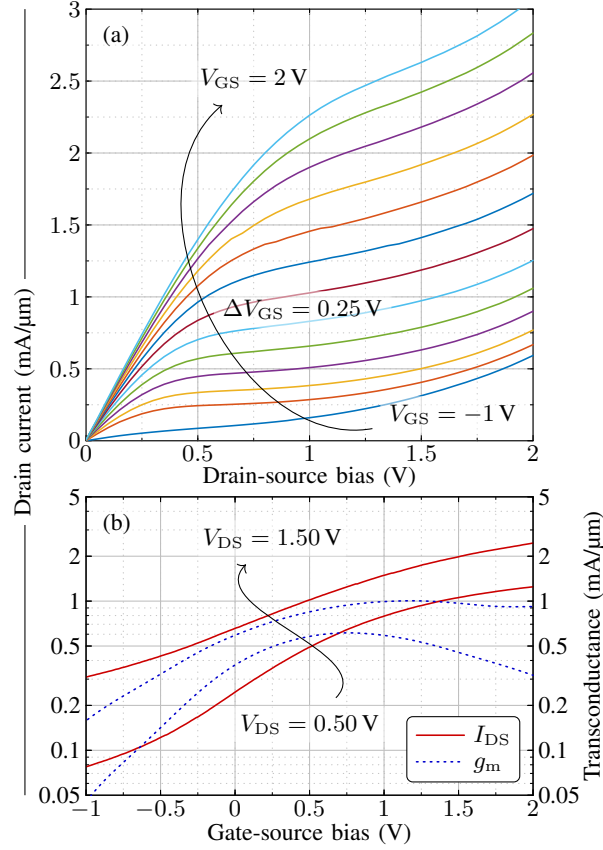


Fig. 2: (a) Output and (b) transfer dc characteristics of the $L_g = 50$ nm gate length and $W_g = 7 \mu\text{m}$ wide measured lateral nanowire MOSFET device.

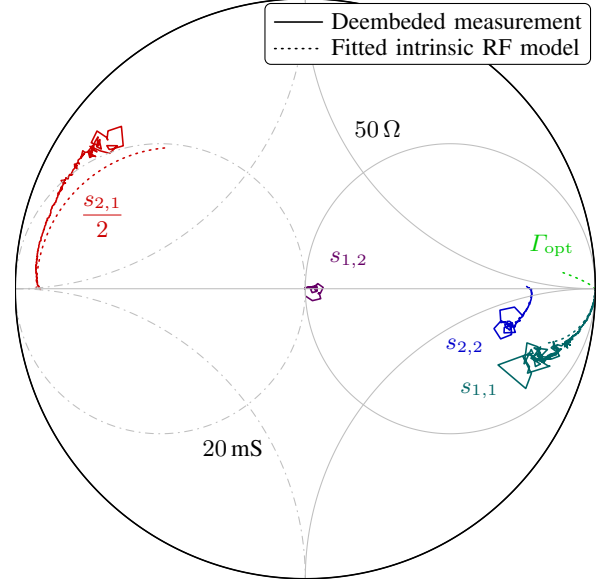


Fig. 3: Measured and modeled scattering parameters, as well as modeled optimum source reflection coefficient.

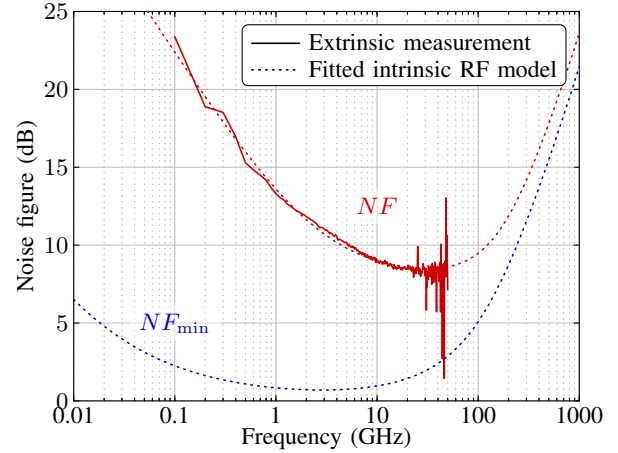


Fig. 4: Measured and modeled noise figure, as well as modeled minimum noise figure.

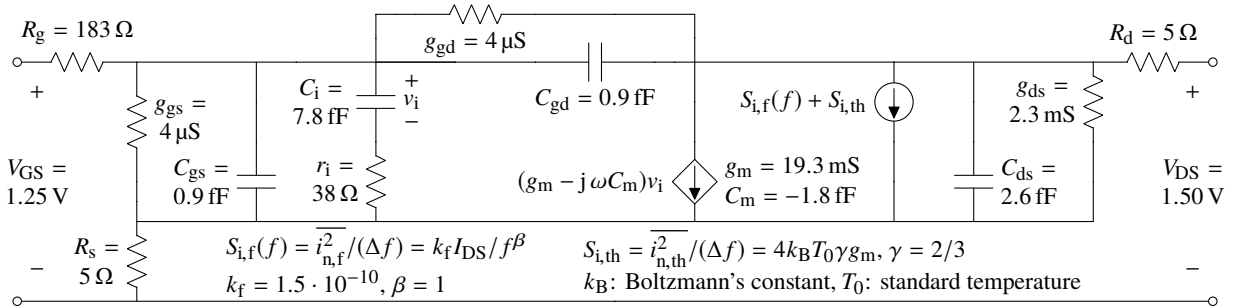


Fig. 5: Small-signal RF noise model fitted to the deembedded admittance, gain, and measured noise parameters. The bias point is input $V_{GS} = 1.25$ V and output $V_{DS} = 1.50$ V, consuming $I_{DS} = 16.8$ mA for the measured device.