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Published in:
Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon-ULIS, EUROSOI-ULIS 2017 - Proceedings

DOI:
10.1109/ULIS.2017.7962611

2017

Document Version:
Peer reviewed version (aka post-print)

Properties of III-V Nanowires: MOSFETs and TunnelFETs

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***Abstract*—This paper describes the properties and performance status of vertical III-V nanowire transistors. The development of key process modules has advanced the vertical fabrication technology and competitive device performance is reported for InAs MOSFETs and TunnelFETs. Besides the benefits in electrostatic control and the ease in integration on Si substrates, the vertical transistors offers a path towards 3D device integration as demonstrated by the stacked track-and-hold circuit where a capacitor is integrated on top of the vertical transistor for area reduction.**

Keywords—III-V nanowires; III-V MOSFETs; InAs; InAs//GaSb; TFETs

I. INTRODUCTION

The properties of III-V nanowire transistors have shown a dramatic increase in performance that last few years. Part of this improvement is related to the advantageous intrinsic transport properties of III-V materials, but part is also related to the continuous refinement of the processing technologies, what enables the transistor fabrication. The small nanowire volume makes the transistors not only susceptible to surface effects such as scattering, but the structures are also sensitive to contact formation and high-*k* integration in the non-planar geometry. It is hence essential to address these technological challenges and to establish processing techniques supporting the transistor evolution.

In this paper, we will present an approach to optimize various processing technology modules for vertical III-V nanowires including ohmic contact formation, high-*k* integration, and a gate-last technology. The evaluation and optimization is performed in a vertical process flow, what makes the technology directly compatible with the transistor fabrication. These process modules are used to fabricate vertical MOSFETs and TunnelFETs with competitive performance on Si substrates.

II. PROCESSING MODULES

A. Ohmic Contact Formation

Transmission line measurements are a well established approach to characterize ohmic contacts to semiconductors. However, the conventional technique applied to lateral structures is hardly applicable for vertical nanowire structures, since it requires that the contact distance can be changed in a systematic way. Spin-coating and other deposition methods typically results in uniform thickness across the wafers, what limits the usefulness of a single step. Recently, spin-coating of hydrogen silsesquioxane (HSQ) and subsequent electron beam exposure has been developed for vertical nanowire structures as a way to control the spacer layer thickness within the structures [1]. It allows for fabrication of layers with a systematic and well-controlled change of the thickness, and hence the contact spacing, on the same sample, what is required for contact evaluation.

The method has been applied to Ni/W/Au contacts to vertical InAs nanowires with a diameter of about 20 nm. The data show that a low specific contact resistance of 0.6 $\Omega\mu m^2$ and a contact transfer length of about 50 nm can be achieved for these vertical structures [2]. The data is encouraging as it suggests that sufficiently low contact resistance can be achieved also for these comparably thin vertical structures.

B. High-k Integration on Vertical Nanowires

The integration of high-*k* dielectrics on III-V materials is challenging due to the complex nature of the interface oxides and the thermal instability of the sub-oxides. III-V nanowires naturally consists of a multitude of different facets with corners and edges, what may affect the binding of the oxide to the semiconductor. Furthermore, the nanowires are resistive what affects the measured frequency-dependent capacitance and may easily lead to misinterpretation about the material properties.

The RF-properties of InAs/HfO_2 vertical nanowire capacitors were studied for structures with air-bridge finger gates to reduce the parasitic capacitance towards the substrate [3]. Capacitors based on InAs nanowires grown with different growth conditions and with different doping levels were measured to evaluate the influence of the crystal quality and the surface properties on the InAs/HfO_2 interface. The data show a D_{it} minimum around the InAs conduction band edge with minimum levels evaluated to be below 10^{12} $eV^{-1}cm^{-2}$ for samples grown under optimized conditions [4]. Furthermore, doping of the nanowire top segment is found to influence the interface properties on the nanowire side walls, possible due to parasitic growth on the facets. Optimization of the growth conditions was found to be effective in reducing the influence of the doping on the side facets what is critical to reduce the D_{it}.

C. Vertical Gate-Last Technology

Processing of the layers in a vertical geometry typically starts with deposition of the bottom layers followed by the subsequent layers towards the top of the device. However, due to the high resistance in thin nanowires and the challenging ohmic contact formation, a self-aligned, gate-last process was developed [5]. In this flow, a sacrificial HSQ-mask is first applied at the bottom of the nanowire while the nanowire top is covered by the ohmic contact. A recess gate is formed by local etching of the nanowire to trim the diameter after removal of the fist mask. The gate stack is then deposited and the gate-length defined by removal of the gate stack on the top of the nanowire. This process allows for multiple gate lengths on the same sample as it is defined by the edge of the top contact that is controlled by the initial HSQ exposure dose.

III. Applications

A. Vertical III-V MOSFETs

The gate-last processing modules developed have been used to fabricate vertical InAs MOSFETs. Transistors (L_g=190 nm) with I_{on} of 140 µA/µm for I_{off}=100 nA/µm have been demonstrated based on a subthreshold swing of 90 mV/dec. The highest transconductance reported for these transistors were g_m=1.6 mS/µm. Substantial increase in performance is expected as these transistor still are limited by the top contact access resistance, what may be minimized by the optimized ohmic contact scheme described above. These vertical transistors may find applications for CMOS at scaled nodes, where the vertical direction is used to provide more space for gates and separation layers as compared to lateral transistors, what saves power [6]. Evaluation has also shown that these transistors may show competitive performance at millimeter wave frequencies, once the parasitics are controlled [7].

B. 3D Device Integration

The vertical nanowire geometry naturally allows for vertical device stacking where individual transistors and other components are connected in the vertical direction. This approach saves space on the substrate although it requires demanding processing as well as layout considerations to identify the best options for the device integration. As a first step towards a 3D device integration scheme, a capacitor was integrated on top of a vertical InAs nanowire MOSFET forming the basis for a track-and-hold circuit [8]. This circuit was selected since it requires quite a large capacitor to match the input in the subsequent circuit blocks. The capacitor was wrapped around the transistor top contact and the functionality of the track-and-hold circuit demonstrated. Evaluations showed that 10*x* capacitor area saving can be achieved for 400 nm long nanowires when places at 100 nm spacing.

C. III-V TunnelFETs

The possibility to grow nanowire heterostructures offers a wide range of possibilities to design structures suitable for TunnelFET fabrication. For nanowire TunnelFETs, the electrostatic control is essential and hence the diameter needs to be scaled to about 20 nm or below [9]. InAs/GaSb nanowire TunnelFETs have shown very high current levels as the broken band alignment provides little resistance at the heterojunction. However, no subthreshold swing below 60 mV/decade was detected [9]. Adjusting the material composition at the heterojunction to InAs/GaAsSb/GaSb improves the device transfer characteristics to below 60 mV/decade operation [10]. Still, comparably high I_{on}=10 nA/µm was measured at V_{ds}=0.3V. The data suggest that indeed TunnelFETs with competitive performance can be realized and there is no reason to believe that the performance can not be increased further by improved heterostructure design and enhanced electrostatics.

IV. Summary

This work describes the recent advancement in processing technology for vertical III-V nanowire MOSFETs and TunnelFETs, including ohmic contact formation, gate-stack formation, and gate-last processing. These modules are essential for the realization of transistors with competitive performance both for digital and millimeter wave applications.

Acknowledgment

This work was supported by the Swedish Foundation for Strategic Research, the Swedish Research Council, and the EU projects INSIGHT (688784) and E2Switch (619509).

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