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High-Mobility GaSb Nanostructures Cointegrated with InAs on Si

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ABSTRACT

GaSb nanostructures integrated on Si substrates are of high interest for p-type transistors and mid-IR photodetectors. Here, we investigate the MOCVD growth and properties of GaSb nanostructures monolithically integrated onto silicon-on-insulator wafers using template-assisted selective epitaxy. A high degree of morphological control allows for GaSb nanostructures with critical dimensions down to 20 nm. Detailed investigation of growth parameters reveals that the GaSb growth rate is governed by the desorption processes of an Sb surface, and in turn is insensitive to changes in material transport efficiency. The GaSb crystal structure is typically zinc-blende with a low density of rotational twin defects and even occasional twin-free structures are observed. Van der Pauw/Hall measurements are conducted on 20 nm thick GaSb nanostructures, revealing high hole mobility of 760 cm^2/Vs, which matches literature values for high-quality bulk GaSb crystals. Finally, we demonstrate a process that enables cointegration of GaSb and InAs

nanostructures in close vicinity on Si, a preferred material combination ideally suited for high-performance complementary III-V MOS technology.

KEYWORDS

GaSb, Template-Assisted Selective Epitaxy, Hole mobility, Cointegration, InAs, Si

The continued miniaturization of complementary metal-oxide-semiconductor (CMOS) circuits has in recent years demanded alterations of the standard processes such as the incorporation of strained Si/SiGe channels, high-*k* metal gate stacks and non-planar device architectures to improve performance and maintain low power consumption. To be able to continue this progress beyond the 7 nm node, a shift from Si to III-V semiconductor materials is being considered because of their high bulk carrier mobilities and injection velocities. However, to become a viable option, III-V semiconductors have to be fully integrated with standard Si CMOS platforms and processes. Recently, InGaAs n-type MOS field effect transistors (MOSFETs) integrated with Si CMOS were successfully demonstrated.[1–3] For p-type MOSFETs, GaSb is considered a feasible alternative to Si and SiGe[4] because of its large hole mobility (750-1000 cm^2/Vs at 300 K) and higher receptivity to strain.[5] Ga(In)Sb has also been proposed as a potential single material for both p- and n-channel in III-V CMOS[6] which would allow for a unified device process for both p- and n-devices. In addition, GaSb is an important material for mid-infrared optoelectronics. At the interface to InAs, GaSb forms a broken type-II band alignment, successfully utilized as low-noise photodetector arrays in the mid-IR spectrum.[7] The GaSb/InAs heterojunction is also considered optimal for high-performance tunnel-FETs,[8,9] devices which may become the successors of MOSFETs in ultra-low-power electronics. Recently there have been reports of GaSb-on-insulator (-OI) p-MOSFETs by direct wafer bonding[10] and epitaxial layer transfer,[11] but these methods remain costly due to the limited sizes of available III-V substrates. The adoption of p-type GaSb in large-scale III-V CMOS

circuits calls for a scalable monolithic integration approach that also allows for cointegration with high performance n-type materials like InAs and InGaAs. High-quality III-V nanowire devices have been grown directly on Si(111) substrates by the vapor-liquid-solid and selective area metalorganic chemical vapor deposition (SA-MOCVD) methods.[12–16] However, a recent work clearly points out that the surface energetics of the antimonide materials pose a fundamental challenge for realizing well-controlled nanowire-like morphology with small diameter.[17] In this article, we investigate epitaxial growth of horizontal p-type GaSb-OI nanostructures on Silicon-OI (SOI) wafers, using a method called Template-Assisted Selective Epitaxy (TASE), based on SA-MOCVD.[18–20] Within TASE, control of the GaSb crystal shape is maintained by confining its growth within pre-defined oxide templates. Moreover, a high III-V material quality is assured by minimizing the size of the Si/III-V heterojunction, avoiding both dislocation threading and anti-phase boundary defects. Electrical characterization of GaSb nano-scale Hall devices reveal a hole mobility which is on par with bulk values. Finally, we show that the developed GaSb process can be used for cointegration of GaSb with InAs nanowires on the same wafer, tightly packed right next to each other.

Results and Discussion

Figure 1a displays a scanning electron microscopy (SEM) image of an exemplary array of GaSb nanostructures after completed epitaxy, still covered by the oxide templates in which they were grown. A high tilt-angle SEM image of GaSb nanostructures after template removal is displayed in Figure 1b. The GaSb crystals are in intimate contact with the Si fins on which endpoint they nucleated. The shape of the GaSb nanostructures has been defined by the template inner walls, and cross-sectional dimensions down to 20 nm are routinely achieved. The amount of unwanted GaSb growth on the mask is typically minute even at the lowest growth temperatures studied.

However, at V/III ratios of 0.6 and below, large (>5 µm diameter) round Ga-rich crystallites deposit on the mask outside the templates (Supporting information). The exposed front GaSb surface, at which the crystal grows, typically forms a large {111} facet often with two smaller and opposing {110} facets (see Figure 1c-d) similar to the case of InAs TASE.[20] Because of the polar nature of the GaSb zinc-blende crystal structure, non-equivalent 180° rotations of the crystal lattice can occur upon nucleation on the non-polar Si. This results in two distinct orientations of the growth facets as illustrated in Figure 1d. It is through growth on these facets that the GaSb nanostructures fill up the length of the oxide template. In many cases a more varied range of growth front morphologies are observed, as exemplified in Figures 2a-b. Such growth fronts also correlate with a higher growth rate. In particular, a roughly 18° in-plane inclination of the growth front is often observed, corresponding to the orientation of a {112} facet. Facets of higher angles such as 45° (Figure 2b) are common as well. In extreme cases the GaSb only partially fills up the template. The prevalence of these alternative facet morphologies is correlated with a low nominal V/III ratio (Figure 2c), suggesting that it may be the consequence of a partial Ga-enrichment on the growth surface, leading to a local growth rate enhancement and thus the formation of higher-index facets to accommodate the uneven evolution of the growth front. As shown in Figure 2b and S2, even Ga-droplet assisted vapor-liquid-solid (VLS) growth is observed.[15,21] Notably, in extreme cases of Ga-droplet-mediated growth the oxide template still guides the GaSb crystal and therefore still enables a precisely defined GaSb morphology.

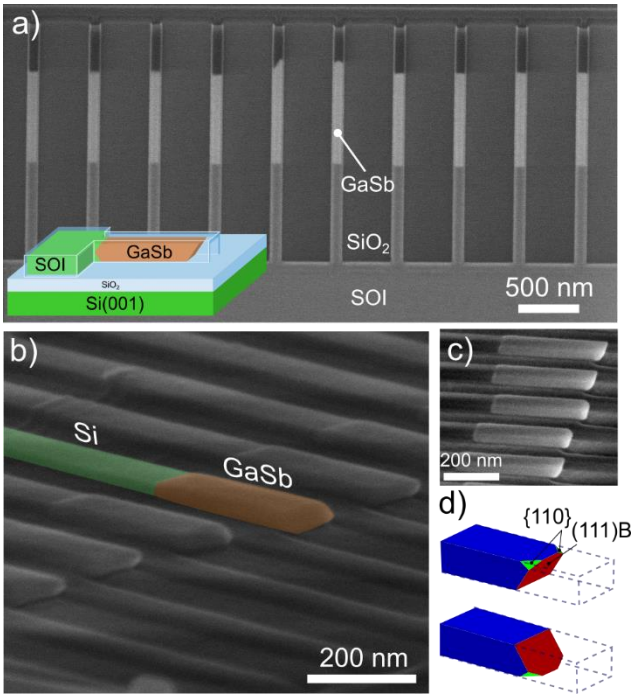

Figure 1. (a) SEM image of an array of horizontal GaSb nanostructures grown at 550 °C integrated co-planar with a SOI layer using TASE. The inset shows an illustration of the layer structure. (b-c) SEM images taken at 75° tilt angle of GaSb nanostructures grown at 550 °C. (d) Schematic illustration highlighting the typical faceting observed at the growth front of the GaSb crystals.

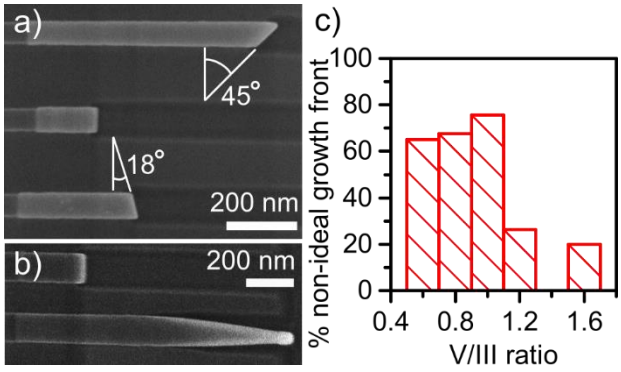

Figure 2. SEM images of GaSb nanostructures exhibiting variations to the typical growth front, (a) with an angle to the growth direction, (b) pointy end which only partially fills up the

template. (c) Percentage of fins exhibiting "non-ideal" growth fronts as a function of nominal growth V/III ratio.

We observe that the yield of GaSb nucleation in the oxide templates strongly depends on the nominal V/III ratio, as displayed in Figure 3a. Furthermore, the nucleation yield at a growth temperature of 550 °C has been compared for the case of nucleation directly on the Si seed with GaSb nucleation after first growing a short InAs segment. At low V/III ratio the nucleation yield is essentially 100%, such that there is GaSb crystal growth in all templates. For nucleation directly on Si the yield drops quickly to zero around V/III ratios of 1. When a short InAs segment (<20 nm long) was grown first, the GaSb nucleation yield decreased much more slowly with increased V/III ratio, and even at V/III ratios above 3 the yield is still around 25%. It is very likely that the much lower lattice-mismatch between InAs and GaSb (0.5%) compared to Si and GaSb (12%) significantly reduces the energy barrier for nucleation.

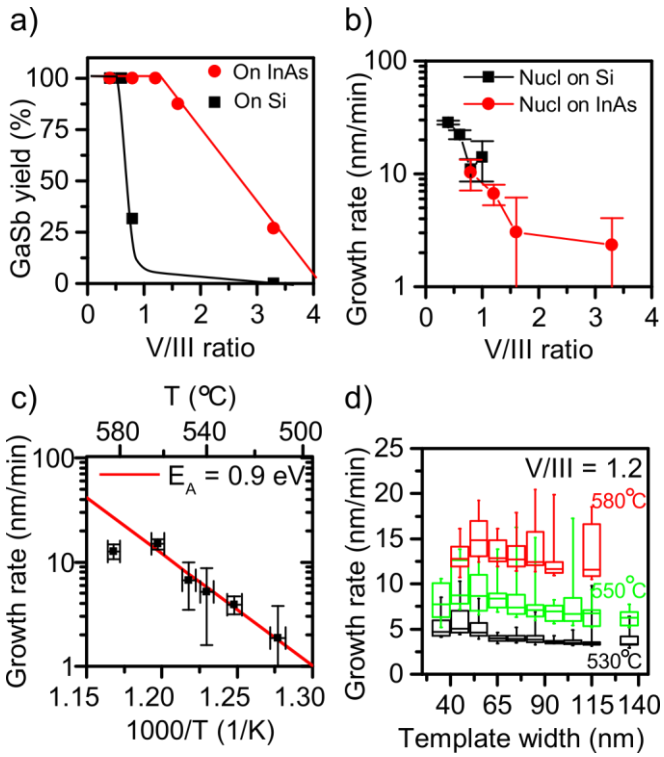

Figure 3. (a) Yield of successful GaSb nucleation on Si and InAs as function of nominal V/III ratio. (b) GaSb axial growth rate as function of V/III ratio. Error bars originate from the standard deviation of the length measurement. (c) Arrhenius plot illustrating the temperature dependence of the GaSb growth rate. Using the slope of the data below 600 °C, an activation energy of 0.9 eV could be extracted. (d) GaSb growth rate dependence as function of template width for different growth temperatures. The middle line of each box corresponds to the median value, the top and bottom box edges to the 90% limits and the arms to the minimum and maximum values for each data set.

The growth rate along the direction of the template tube (<110>) was studied as a function of V/III ratio and is found to decrease exponentially with increased V/III ratio up to a V/III ratio of 1.5, as displayed in Figure 3b. A decrease in growth rate with increasing V/III ratio was previously observed for MOCVD of GaSb(100) under Sb-rich conditions,[22] although the effect was much weaker. The strong decrease in growth rate observed here indicates that excess Sb may strongly interfere with the GaSb growth within the templates. Sb is a well-known surfactant[23] and has a much lower vapor pressure than other group V species such as P and As.[24] Thus, we hypothesize that excess Sb forms a surface layer on the exposed GaSb surface, thus occupying the surface sites and hindering adsorption of Ga. If this effect is strong enough the growth rate will be governed by the rate at which Ga adsorption sites free up, *i.e.* by the rate of Sb desorption from the GaSb surfaces. Possibly, a similar Sb surface layer in the initial phase of growth could account for the reduced nucleation yield observed for higher V/III ratios (Figure 3a).

To investigate this hypothesis further the temperature dependence in the range from 510 °C to 585 °C of the GaSb growth rate was studied at relatively high V/III ratio (1.2). An Arrhenius plot of the resulting data is displayed in Figure 3c. Experiments were also conducted at 605 °C but in most

templates no growth was observed at this high temperature, and in others non-epitaxial Ga-mediated growth was observed (Supporting Information) indicating that the effective V/III ratio had become too low. The temperature dependence is evidently exponential up to 565 °C and an activation energy of 0.91 eV (± 0.09 eV) is extracted from the slope of these data points. The metalorganic precursors for GaSb growth in this work were trimethylgallium (TMGa) and trimethylantimony (TMSb). We note that the activation energy for homogeneous TMSb decomposition in a mixture with TMGa, 1.45 eV[25], and the activation energy for TMGa decomposition in H_2 ambient, 2.5-2.6 eV,[26] are both much higher than what is found here and can therefore be ruled out as being the limiting processes, although such high activation energies have been reported by others (1.45 eV[25], 1.56 eV[22]) for GaSb epitaxy. There are also reports of activation energies for GaSb growth close to the value observed here; 0.83 eV,[27] 0.84 eV,[28] 0.87 eV,[29] 0.88 eV,[30] although no attempt to identify the underlying mechanism was made. Importantly, Maeda and Watanabe[31] have measured the activation energy for Sb desorption from GaSb (100) surfaces and found two competing desorption processes with different activation energies, 0.71 and 0.90 eV, covering this same range. This supports the hypothesis that Sb desorption from the GaSb surface in fact governs the GaSb growth rate in TASE for the conditions investigated here. It is expected that the Sb surface coverage on the (111)B facet can be particularly high because of the intrinsic Sb termination of that facet. As a large GaSb{111} growth facet is typically observed in the templates, especially under Sb-rich conditions, this is a strong indication that this facet is in fact a (111)B facet.

The dependence of the growth rate on a variation of template width contains information on the mechanisms of the material transport to the GaSb growth surface. In Figure 3d such data is displayed for growths performed at growth temperatures of 530, 550 and 580 °C. For all

investigated temperatures, the growth rate varies only very weakly with template width, in contrast to InAs TASE for which the growth rate increases linearly with increasing template widths (widths < 140 nm).[20] This effect was attributed to a decreased As species supply in narrow tubes in accordance with reduced transmission probability for Knudsen diffusion in the vapor.[32] For GaSb, the weak width dependence can be attributed to the high surface coverage of Sb, such that a variation in material supply will have only a minor effect on the growth rate if any at all. However, one might distinguish a slight tendency towards higher growth rates at smaller widths compared to larger from the data in Figure 3d. This could be an indication that the effective V/III ratio in narrow templates is somewhat reduced, thus causing an increased growth rate (compare with Figure 3b).

Crystal structure

Characterization of the crystal structure of grown GaSb nanostructures was performed *via* scanning transmission electron microscopy (STEM) after sectioning by focused ion beam (FIB). Similarly to previous work on GaAs and InAs TASE[33] we do observe an array of misfit dislocations at the Si/GaSb heterojunction, but no dislocations or antiphase boundaries extending away from the junction. Of particular interest, however, is to investigate the presence of planar defects (stacking faults and rotational twins) which in the semi-polar III-V semiconductors often form on {111} planes.[34] Figure 4a displays an atomically resolved high-angle annular dark-field (HAADF) STEM image along the [-110] viewing direction of a GaSb crystal grown at a V/III ratio of 0.4 at a temperature of 550 °C. The GaSb crystal grows along the [110] direction, and (111) rotational twin and stacking faults are observed edge-on at a lower density (0.2 defects/nm) compared to what is commonly observed in GaAs and InAs TASE (> 1 defects/nm).[33] In a close-up image (Figure 4b) a region, highlighted by dashed lines, can be seen containing additional atoms

in between the expected dimer rows. This imaging effect is the result of additional twinning on the {1-11} or {-111} type planes which are inclined with respect to the [-110] viewing direction.

In Figure 4c a GaSb nanostructure grown with V/III ratio of 1.2 is displayed, which exhibits significantly less defects (0.07 defects/nm) than at V/III ratio of 0.4. We have also observed several nanowires where no planar defects are observed, such as displayed in Figure 4d. Due to the extensive sample preparation required for TEM analysis, the statistical sample is small, and a trend cannot be established with certainty. We do, however, note a lower incidence of planar defect formation at Sb-rich growth conditions, in accordance with studies in other III-V materials.[35] It is very likely that other parameters such as the growth temperature may also affect the formation of twin defects and stacking faults.

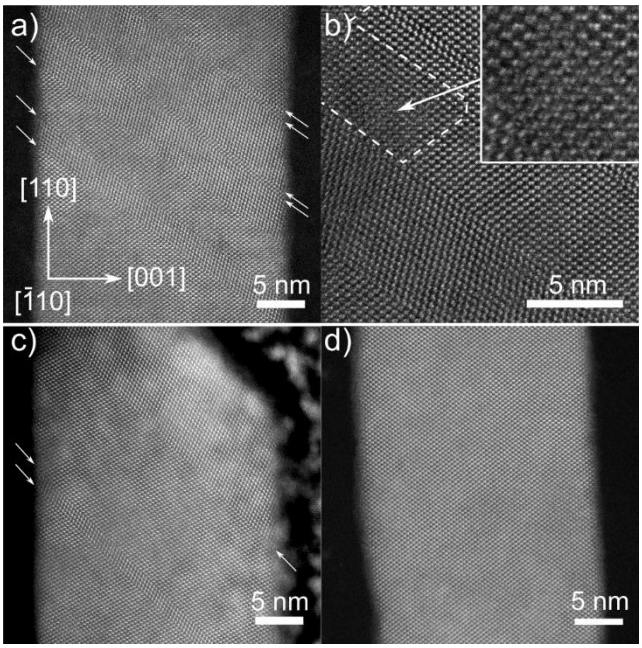

Figure 4. HAADF-STEM images GaSb nanostructures grown at V/III ratio of (a-b) 0.4, (c) 1.2 and (d) 0.6 and growth temperature of 550 °C. Edge-on oriented (111) planar defects are

indicated by white arrows. The dashed line, inset and arrow in (b) indicates a region of rotational twins that are inclined with respect to the [-110] viewing direction.

Electrical properties

For characterization of the electronic properties of our GaSb-OI materials, Van der Pauw/Hall test structures were fabricated, 20 nm thick and 500 nm by 1000 nm wide (Figure 5a). Note that here a single GaSb nucleus was created on a small Si seed surface (left part of structure in Figure 5a), which was further grown to fill up the predefined shape of the oxide template. Van der Pauw measurements were performed on 19 devices from which consistent sheet resistance values could be extracted as displayed in the histogram of Figure 5b. The average sheet resistance value of 15.3 kΩ/□ corresponds to a resistivity of 31 mΩcm, assuming a device thickness of 20 nm. This is significantly lower than reported resistivity values for non-intentionally doped Au-seeded GaSb nanowires (~200 mΩ-cm[36,37]). Complementary Hall measurements were conducted on several devices at room temperature in an evacuated cryostat with a variable magnetic field in the range of ± 6 T. The resulting Hall resistance as function of magnetic field is displayed for a typical device is shown in Figure 5c. The positive slope of this curve indicates hole carrier transport, as expected for unintentionally doped GaSb. From the value of the slope the sheet carrier concentration can be extracted, for the particular device in Figure 5c being 4.8 x 10^{11} cm^{-2} (2.4 x 10^{17} cm^{-3} at 20 nm thickness). Together with the corresponding sheet resistance data the hole mobility (μ_H) can be calculated. From Figure 5d is becomes clear that most devices have similar sheet carrier concentration with an average hole mobility of 760 cm^2/Vs. Our attained mobility value is higher compared to previous reported values for GaSb nanostructures (μ_{FE} < 400 cm^2/Vs),[38] and compares well to values reported for thick epitaxial GaSb films (μ_H ~ 500-950 cm^2/Vs).[27,39,40] Notably, the mobility is high despite that the thickness of the devices is only around

20 nm, indicating that surface scattering may be of minor importance for these GaSb devices which are still covered by the template oxide and are thus protected from oxidation. It is further noteworthy that such high mobility values are obtained despite the likely presence of isolated planar defects in the devices, which one may expect to act as scattering centers. Interestingly, such isolated defects have previously been shown to have little or no impact on the resistivity of zinc-blende InAs nanowires.[41] We also observe two devices which exhibit considerably higher hole mobilities than the others, close to 1300 cm^2/Vs (Figure 5d). To the authors' knowledge a hole mobility above 1000 cm^2/Vs in GaSb has only been reported once before, in >10 µm thick GaSb heteroepitaxial layers grown on GaAs(100) substrates by molecular beam epitaxy.[42]

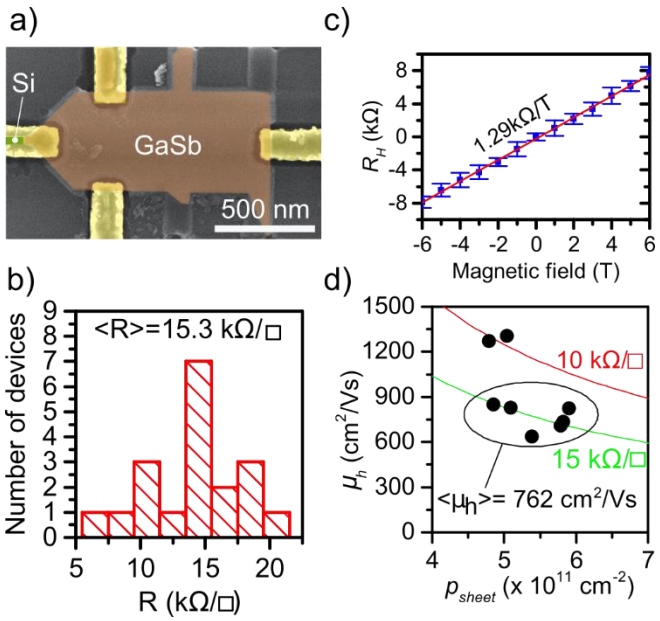

Figure 5. *(a) SEM image of a GaSb Hall device, 500 nm wide and about 20 nm thick. The GaSb is still covered by the oxide template in which it was grown. (b) Histogram showing the distribution of measured sheet resistance values from distinct devices by the Van der Pauw method. (c) Hall resistance versus magnetic field for a representative device. (d) Graph*

illustrating the relationship between hole sheet carrier concentration and hole mobility for the measured devices. Indicated are also two constant sheet resistance lines as well as the mean mobility value for the main group of devices.

Cointegration of multiple III-Vs on Si

Finally, we investigate the cointegration of multiple III-V compounds on Si by sequentially combining the GaSb growth process reported here with the similar InAs growth reported previously[18] in separate templates on the same wafer. These two materials constitute a preferred material combination ideally suited for high-performance III-V CMOS technology.[16] A test pattern was realized where one set of nanowire templates was formed interlaced with another that could be opened from the adjacent direction. The first set of templates was opened and InAs was grown (Figure 6a), similar to as reported previously.[18] The InAs structures were then protected by the deposition of SiO_2, after which the second set of templates were opened and back-etched to grow GaSb (Figure 6b). The detailed process is described in the Supporting Information (Figure S3). A SEM image of the resulting test structure is shown in Figure 6c, where InAs and GaSb nanowires are interlaced with only 250 nm pitch in between. In this cointegration process, an additional important aspect of the oxide templates is to suppress decomposition of the InAs nanowires during GaSb growth, with the template being be a diffusion barrier for volatile As species. The chemical distinction and structural uniformity of the resulting final cointegrated GaSb and InAs nanomaterials was obtained by acquiring X-ray energy-dispersive spectroscopy (EDS) spectrum images across several InAs and GaSb nanowires (Figure 6d). The colored map in Figure 6d is generated using pink for In and As, and orange for Ga and Sb. Detailed investigation of the InAs crossection by EDS reveal no visible material degradation, and Hall measurements confirm that the electron mobility in co-integrated InAs devices is unaffected by the cointegration process

(Supporting Information, Figure S4 and S5). The co-planar and dense cointegration shown here is a particular feature of TASE which can be extended also to other material systems, even other than III-V, without significant alterations.

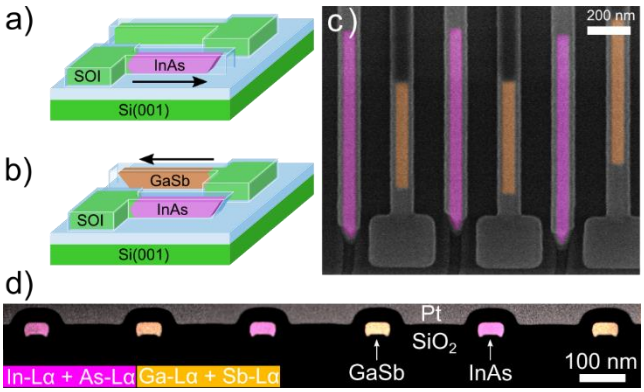

Figure 6. *Dense cointegration of GaSb and InAs nanostructures on SOI wafer. (a-b) Schematic illustration of the two sequential (a) InAs and (b) GaSb growth steps in two separate sets of templates opened from opposite directions. The arrows indicate the growth directions. (c) Top view SEM image of the finished interlaced nanowires. The nanowires are false-colored to match the color of the schematics. (e) Cross-sectional colored map generated from an EDS spectrum image using pink for In-Lα + As-Lα , and orange for Ga-Lα + Sb-Lα.*

Conclusions

In conclusion, we have investigated monolithic integration of high-mobility horizontal GaSb nanostructures on SOI, and showed that the developed GaSb process is suitable for dense cointegration of GaSb with InAs nanostructures on the same chip. We found, that the GaSb growth is governed by excess Sb present on the GaSb surface, leading to a strong growth rate dependence on V/III ratio and temperature. HAADF-STEM investigations of the crystal structure of the GaSb nanostructures indicate a low twin defect density when grown at V/III ratio below one, which is further reduced by raising the nominal V/III ratio above one. Very high average hole mobility,

similar to bulk GaSb crystals, were extracted by resistivity and Hall measurements from nanoscale GaSb-OI devices integrated on Si. The high degree of morphological control together with the exceptional electrical quality of the GaSb nanostructures, as well as the possibility for GaSb cointegration with other III-V materials on Si provides a perfect basis for a wide range of electronic and mid-IR optoelectronic applications integrated with Si CMOS.

Methods

Horizontally oriented SiO_2 nanotube templates were fabricated along the [110] direction on (001)-oriented SOI substrates as described previously by Schmid *et al.*[18] In short, a SOI device layer was structured into horizontal fins or more complex structures by inductively coupled plasma reactive ion etching (HBr chemistry) and covered by SiO_2 by plasma-enhanced atomic layer deposition. The oxide was removed at one end of the fins after which the Si is partly back-etched through wet chemical etching to create a horizontal empty oxide tube with well-defined dimensions and with a Si seed surface at the deepest point. For this study the templates had a height of 20-30 nm and widths varying between 10 nm and 500 nm. The depth of the tubes was typically around 1 µm. No impact of tube depth on the GaSb growth rate was observed, thus the growth rate was assumed constant throughout a run.

GaSb growth was conducted in a Veeco P150 MOCVD system run at 60 torr pressure with H_2 carrier gas, and trimethylgallium (TMGa) and trimethylantimony (TMSb) as precursors for GaSb growth. Prior to loading, the substrates were briefly etched in dilute HF to remove the native oxide on the Si seed surface within the templates. After loading, the reactor was heated to above 700 °C under flow of tertarybutylarsine (TBAs) before ramping down to the growth temperature (510-610 °C), at which TMGa and TMSb were introduced at TMGa molar flow in the range 13 - 48 µmol/min and V/III ratio between 0.4 and 13. Typical growth times were between 20 and 90 min.

After completed GaSb growth the temperature was ramped down to room temperature while flowing only H_2 gas. In some growth runs a 5 min InAs nucleation step was made (20 nm length) to improve the GaSb nucleation yield. Trimethylindium (TMIn) and TBAs were then used as precursors for InAs, at a V/III ratio of 160 and a five second purge step under TBAs flow was introduced in-between the InAs and GaSb growth steps.

The lengths of GaSb nanowires with constant width were measured after growth by inspection in a Hitachi SU8000 SEM. For each data point in this work the length of at least 20 structures were measured. Displayed data points in this work correspond to the median values of the data set, and error bar length to one standard deviation.

Samples for TEM were prepared along the GaSb nanostructures by means of a FEI Helios Nanolab 450S FIB. The HAADF-STEM and EDS data was acquired with a double spherical aberration-corrected JEOL JEM-ARM200F microscope operated at 200 kV, and equipped with a JEOL Dry SD100GV silicon drift detector with 100 mm^2 detection area for EDS. A probe semiconvergence angle of 25.3 mrad was set yielding a probe size of about 80 pm. The annular semidetection range of the annular dark-field detector was calibrated at 90-370 mrad. Elemental maps were calculated from the EDS spectrum image from the Lα peaks of Ga, As, In and Sb. The multiple linear least squares fitting routine was used to decompose the partially overlapping Ga-As and In-Sb peaks.

Van der Pauw/Hall devices were fabricated from long and wide GaSb structures (>1 µm long, 300-500 nm wide), of around 20 nm thickness. These devices were contacted patterning PMMA resist by electron beam lithography, locally etching away the template oxide in the contact areas and defining Ni/Au contacts by electron beam evaporation and lift-off. Prior to evaporation, the samples were immersed in buffered HF for a few seconds, followed by 10 min surface

passivation in 0.1% $(NH_4)_2S$ solution, and directly transferred to the evaporation chamber after rinsing in deionized water. The specific contact resistivity is measured to be 400 $\Omega\mu m^2$. Hall measurements were conducted at room temperature in an evacuated cryostat with a variable magnetic field up to 6 T. The GaSb sheet resistivity was determined by the Van der Pauw method and compared to four-probe and transmission line measurement results for consistency. From the measurement method and spread in the data we estimate the relative error of the sheet resistance to be maximum ± 12 %. The relative error of the carrier concentration obtained from the Hall measurement is ± 6 %. Uncertainty in the device thickness does not impact the hole mobility determination as only sheet hole concentration and sheet resistance enter into the equation.

ASSOCIATED CONTENT

Supporting Information. Additional information on parasitic growth on the mask, resulting GaSb morphology for growth above 600 °C, details on the cointegration process, and details of InAs material evaluation after GaSb growth.

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Author Contributions

M.B., H.S., K.E.M. and H.R. conceived the experiments, M.B., D.C. and M.K. processed template substrates. MB performed the GaSb growth and analyzed the results. M.B. processed Hall devices, and M.B., J.G. and S.W. did electrical measurements. M.D.R. and N.B. performed scanning transmission electron microscopy. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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