Comparison of Low-Frequency Noise in Nanowire and Planar III-V MOSFETs

Hellenbrand, Markus; Kilpi, Olli-Pekka; Svensson, Johannes; Lind, Erik; Wernersson, Lars-Erik

2019

Document Version:
Peer reviewed version (aka post-print)

Link to publication

Citation for published version (APA):
Hellenbrand, M., Kilpi, O.-P., Svensson, J., Lind, E., & Wernersson, L.-E. (2019). *Comparison of Low-Frequency Noise in Nanowire and Planar III-V MOSFETs*. Paper presented at Insulating Films on Semiconductors (INFOS), Cambridge, United Kingdom.

Total number of authors:
5

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Comparison of Low-Frequency Noise in Nanowire and Planar III-V MOSFETs

M. Hellenbrand, O.-P. Kilpi, J. Svensson, E. Lind, and L.-E. Wernersson
Department of Electrical and Information Technology, Lund University, Box 118, SE-221 00 Lund, Sweden
E-mail address of corresponding author: markus.hellenbrand@eit.lth.se

1. Summary

We compare III-V nanowire (NW) metal-oxide-semiconductor field-effect transistors (MOSFETs) in a vertical gate-all-around (GAA) as well as a lateral tri-gate architecture with planar reference MOSFETs and reveal that the NW geometry does not deteriorate the low-frequency noise (LFN) performance. In fact, with gate oxides deposited at the same conditions, the NW structures show potential to achieve better metrics due to slightly lower border trap densities N_{bt}. The normalized LFN in transistors with a higher number of NW can degrade due to averaging effects between individual nanowires within the same device.

2. Introduction

The IEEE International Roadmap for Devices and Systems [1] predicts nanowire transistors to play an important role in the future of electronics. Here, we investigate in how far the change in geometry from planar reference structures to highly scaled NW transistors affects the LFN properties of the devices, metrics that are especially important for low-noise amplifiers and detectors and as such monitor the maturity level of the technology.

3. Experimental Setup

Schematics of the device structures are presented in Fig. 1(a) and Fig. 2(b) alongside transfer curve examples for a vertical and a planar device at $V_{\mathrm{DS}} = 50$ mV in Fig. 1(b) and Fig. 2(c). All types of devices exhibit good gate control with at least five orders of magnitude current modulation. For the planar reference structures, three different high-κ gate oxides were used (5 nm $\mathrm{Al_2O_3}$, 6.5 nm $\mathrm{HfO_2}$, and 5 nm $\mathrm{HfO_2}$) to possibly reveal corresponding differences. All NW transistors used a 0.5 nm $\mathrm{Al_2O_3}$/4.5 nm $\mathrm{HfO_2}$ bilayer gate oxide and all gate oxides were deposited under the respective same conditions. Details about the device processing can be found in [2-4] and [4] also provides more details about the measurement of specifically the lateral NW devices. A schematic of the LFN measurement setup is provided in Fig. 2(a): The current noise spectral density $I_{\mathrm{N}} = \sqrt{S_{\mathrm{ID}}}$ was measured with a lock-in amplifier after the device current was amplified by a low-noise amplifier, which also supplied the $V_{\mathrm{DS}} = 50$ mV. LFN was measured as a function of V_{GS} and the frequency (Fig. 3(a)) as well as at a fixed frequency of 10 Hz as a function of V_{GS} (Fig. 3(b)).

4. Results and Discussion

The current noise power spectral density S_{ID} in all measured devices exhibited a clear $1/f^{\gamma}$ dependence (Fig. 3(a)) with γ close to one, which is characteristic of a large number of gate oxide defects [5]. The dominant noise mechanism can be identified by plotting S_{ID} normalized by the device current I_{S} squared as a function of I_{S}, as illustrated in Fig. 3(b). For all measured transistors, number fluctuations were the dominant noise mechanism, which was revealed by the proportionality of $S_{\mathrm{ID}}/I_{\mathrm{S}}^2$ to the transconductance as $g_{\mathrm{m}}^2/I_{\mathrm{S}}^2$, and which describes the capture and emission of electrons in and from gate oxide defects.

To compare the LFN performance of NW and planar devices for circuit applications, the intrinsically generated noise of the transistors can be transferred to the gate as the input of the devices as $S_{\mathrm{VG}} = S_{\mathrm{ID}}/g_{\mathrm{m}}^2$. In the case of number fluctuations, S_{VG} turns out to be the same as the flat-band voltage noise power spectral density S_{Vfb}, which is proportional to one over the gate area. Correspondingly, Fig. 3(c) compares the gate-area-normalized S_{VG} of the measured devices and reveals that the highly scaled NW transistors (single-nanowire devices) exhibit equal or slightly better performance than the planar reference structures. (Commercial SOI [6] included for further reference.) The defect densities N_{bt} in Fig. 4(c) are rather similar for all devices, but the minimum N_{bt} values are consistently achieved by the NW devices. These minima coincide well with the minima in S_{VG}, which is consistent with the assumption of number fluctuations as the dominant noise mechanism, and straightforwardly reveals low N_{bt} values as a requirement for low device noise.

If not processed carefully, NW transistors with NW arrays instead of single NWs can exhibit deteriorated LFN performance (Fig. 4(a)) due to averaging effects between individual NWs within the same device. These averaging effects are revealed by the lower normalized transconductances of the same array devices in Fig. 4(b). With careful processing, however, averaging effects can be kept at a minimum, which was demonstrated in e.g. [7], where the highest $g_{\mathrm{m}}/W_{\mathrm{G}}$ values were achieved for array devices. LFN characterization of those well-behaved arrays will be part of our future work as well as a more detailed identification of the exact capture/emission mechanism that leads to LFN.

5. Conclusion

Vertical nanowire transistors achieve similar or improved LFN metrics when compared with planar reference structures with similarly deposited gate oxides, which indicates that LFN does not constitute a roadblock on the path towards nanowire transistors.

Acknowledgments

This work was supported in part by the Swedish Research Council, in part by the Swedish Foundation for Strategic Research, and in part by the European Union Horizon 2020 Program INSIGHT under grant agreement number 688784.

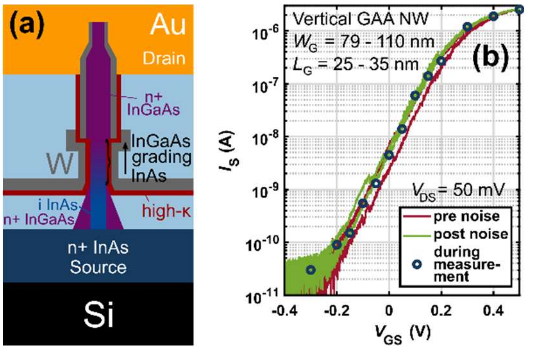

Fig. 1: (a) Schematic and (b) example transfer curve for vertical gate-all-around nanowire transistors. ('i' for materials denotes intended intrinsic carrier concentration.)

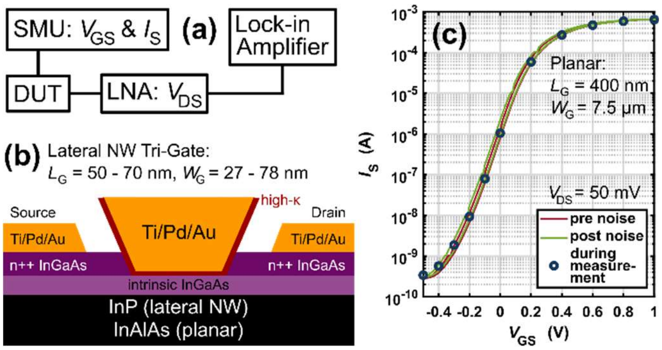

Fig. 2: Schematics of (a) the measurement setup and (b) the lateral tri-gate NW as well as the planar reference device structure. In this side view, both look the same, although with different NW/channel thicknesses of 7.5 nm and 10 nm, respectively. (c) Representative transfer curve for a planar device.

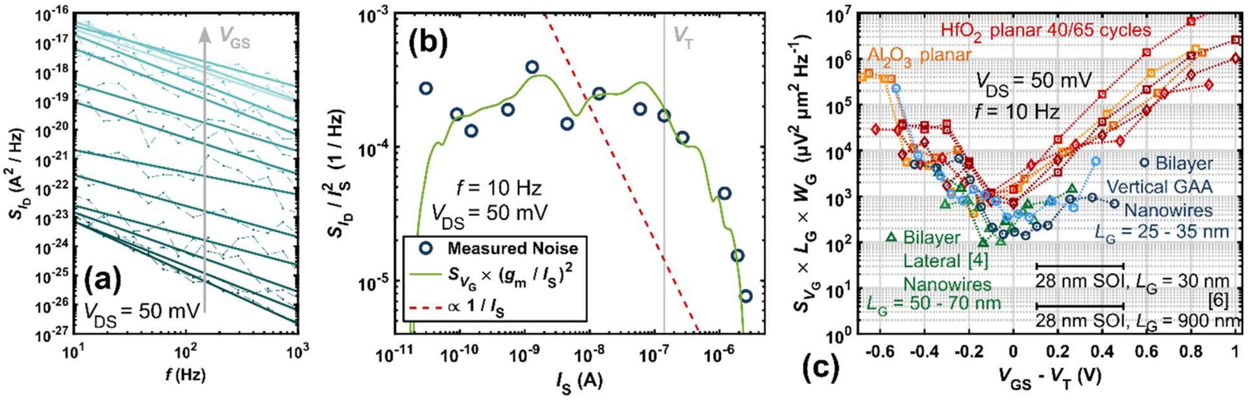

Fig. 3: (a) Measurement of the current noise power spectral density S_{ID} at different frequencies and at different V_{GS} to identify the 1/f behavior. (b) S_{ID} normalized with the source current at a fixed frequency of 10 Hz to identify number fluctuations (solid green line) as the dominant noise mechanism. Mobility fluctuations (broken red line for reference) are not observed. Example for a vertical nanowire transistor with one nanowire. (c) S_{VG} normalized with the gate area. The NW transistors (blue circles for vertical, single NW, green triangles for lateral tri-gate single NW) achieve similar or even slightly better values than the planar reference structures (orange and red squares/diamonds). Reference values for commercially produced highly scaled SOI MOSFETs are only about one order of magnitude lower.

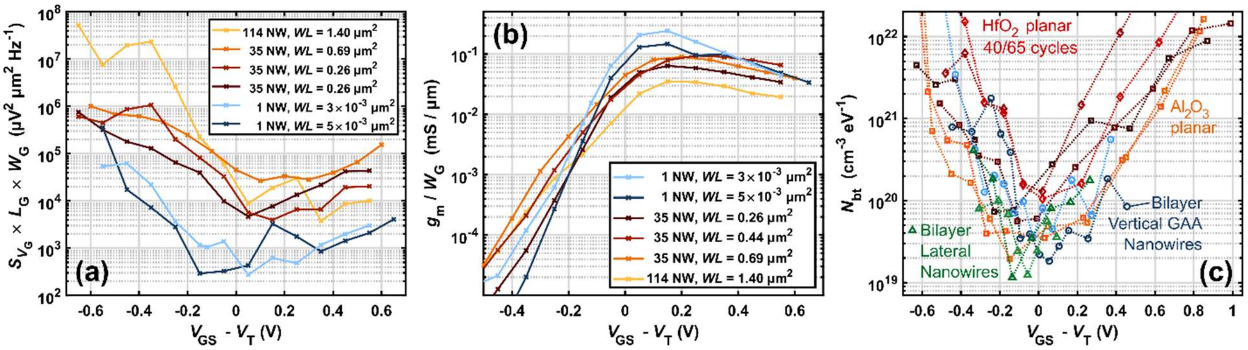

Fig. 4: (a) $S_{VG} \times L_G \times W_G$ for nanowire transistors with different numbers of nanowires is not independent of the gate area, as would be expected. (b) Comparing g_m/W_G for the same transistors as in (a) reveals V_T shifts between the individual nanowires within the same transistor as the explanation for the observation in (a). (c) Comparison of the gate oxide defect density N_{bt} for the different device structures. The values are comparable, while the minimum N_{bt} values are consistently achieved by NW devices. The N_{bt} minima coincide with the S_{VG} minima, which is consistent with the assumption of number fluctuations as the dominant noise mechanism. It also reveals low N_{bt} as a requirement for low LFN.

References

[1] https://irds.ieee.org/
[2] Kilpi et al., Nano Lett., 2017, 17 (10), 6006–6010
[3] G. Roll et al., Appl. Phys. Lett., 2015, 106 (20), 203503
[4] Möhle et. al., Microelec. Eng. 178 (2017) 52–55
[5] M. v. Haartman, 2007, doi: 10.1007/978-1-4020-5910-0
[6] Ioannidis et al., IEEE IEDM, 2011, 18.6.1–18.6.4
[7] A. Jönsson, IEEE EDL 39 (2018), 935–938