III-V Nanowires for High-Speed Electronics

Lindelöw, Fredrik

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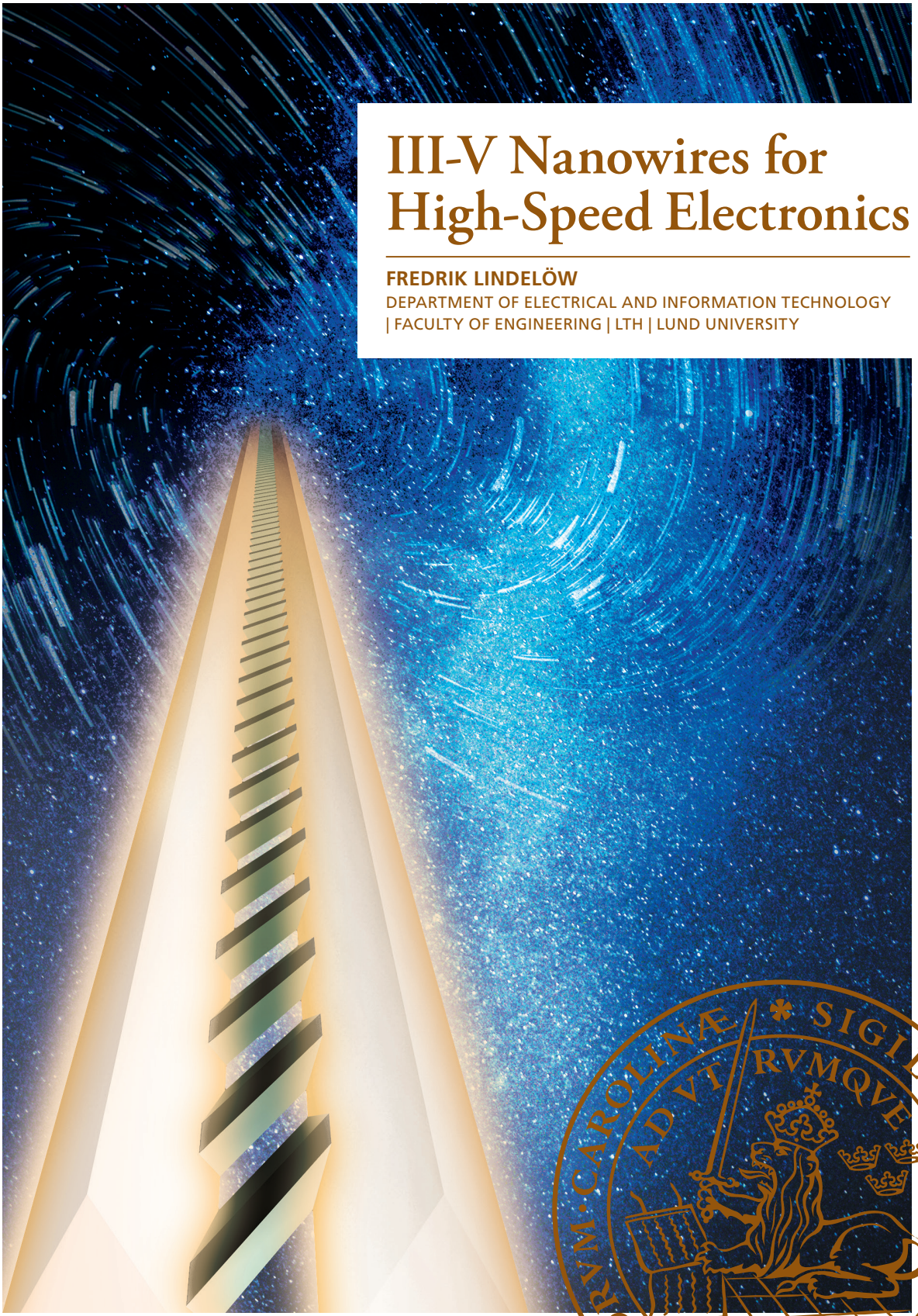

III-V Nanowires for High-Speed Electronics

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Abstract

III-V compound materials have long been used in RF applications in high-electron-mobility-transistors (HEMTs) and bipolar-junction-transistors (BJTs). Now, III-V is also being viewed as a material candidate for replacing silicon in the n-channel in CMOS processes for increased drive currents and reduced power consumption in future nodes. Another alternative to increase the drive current is to use nanowire channels, where the increased electrostatic control can be utilized for scaling the gate length even further. In this thesis, we have characterized III-V nanowires with Hall-measurements to quantify the carrier concentration and optimize growth parameters. We have fabricated nanowire transistors for both digital and analog applications. Digital transistors made of a single nanowire show state-of-the art performance with low subthreshold slope and simultaneously high transconductance and high on-current. For RF applications, the nanowire technology faces several challenges, mainly due to its inherent higher parasitic capacitance since the filling factor is less than 1. To adapt the DC processing scheme to RF measurements, we have implemented T-gates, two-finger devices, 100 nanowires in parallel with tight pitch and we have developed novel spacer schemes with capacitances almost as low as recessed HEMT devices. These schemes consists of for instance modulation doped InP spacers as well as self-aligned air-spacers. To make the RF nanowire MOSFETs even more competitive, the transoncductance of RF devices needs to be optimized to match that of DC devices.

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III-V Nanowires for High-Speed Electronics

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Doctoral Thesis
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Coverphoto showing 100 lateral nanowires with two Λ-ridge spacers, illustrated by Linus Kandefelt and Fredrik Lindelöw

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Abstract

III-V compound materials have long been used in RF applications in high-electron-mobility-transistors (HEMTs) and bipolar-junction-transistors (BJTs). Now, III-V is also being viewed as a material candidate for replacing silicon in the n-channel in CMOS processes for increased drive currents and reduced power consumption in future nodes. Another alternative to increase the drive current is to use nanowire channels, where the increased electrostatic control can be utilized for scaling the gate length even further. In this thesis, we have characterized III-V nanowires with Hall-measurements to quantify the carrier concentration and optimize growth parameters. We have fabricated nanowire transistors for both digital and analog applications. Digital transistors made of a single nanowire show state-of-the art performance with low subthreshold slope and simultaneously high transconductance and high on-current. For RF applications, the nanowire technology faces several challenges, mainly due to its inherent higher parasitic capacitance since the filling factor is less than 1. To adapt the DC processing scheme to RF measurements, we have implemented T-gates, two-finger devices, 100 nanowires in parallel with tight pitch and we have developed novel spacer schemes with capacitances almost as low as recessed HEMT devices. These schemes consists of for instance modulation doped InP spacers as well as self-aligned air-spacers. To make the RF nanowire MOSFETs even more competitive, the transoncductance of RF devices needs to be optimized to match that of DC devices.

Populärvetenskaplig sammanfattning

Mycket av de saker som vi tar för givet i vårt moderna samhälle, så som datorer, smarta mobiltelefoner och internet har möjliggjorts av den enorma utvecklingen av transistorer under de senaste 70 åren. Den första transistorn tillverkades i halvledarmaterialet germanium, men sedan dess har mycket av utvecklingen av transistorer gjorts i kisel. Kisel visade sig vara ett väldigt lämpligt material att använda på grund av dess goda ledningsförmåga samt dess elektriskt isolerande oxid, SiO_2. Transistorer kan användas både för att stänga av och på strömmar, för att representera 0:or och 1:or i digitala kretsar samt som en förstärkare av signaler i analoga kretsar. Ett exempel på en tidig analog krets var transistorradion som revolutionerade lyssnandet av musik innan modernare portabla koncept var utvecklade. Det visade sig att genom att göra transistorerna mindre och mindre så kunde beräkningarna i datorer utföras snabbare och med mindre energiförbrukning. Denna utveckling har beskrivits av Moores lag där antalet transistorer per yta på ett kretskort dubblas vartannat år. Idag har dock kurvan börjat avta på grund av att energin per ytenhet har blivit enormt hög och det har blivit betydligt mer komplext att tillverka de minsta beståndsdelarna i transistorn som är långt mindre än ljusets våglängd. Ett annat sätt att förbättra transistorn utan att nödvändigtvis göra den mindre är att använda nanotrådar samt andra material än kisel. I halvledarmaterialet indium-gallium-arsenid kan elektronerna färdas snabbare än i kisel, dessutom med en lägre pålagd elektrisk spänning. Genom att minska spänningen, alternativt behålla samma som för kisel, kan antingen energiförbrukningen minskas eller prestandan förbättras.

I denna avhandling har vi studerat hur man kan förbättra nanotrådstransistorer gjorda av InGaAs både för digitala och analoga applikationer, där storleken på nanotrådarna är ungefär i samma storlek som ett coronavirus. Att tillverka en transistor påminner om konsten att laga mat. Det finns säkra recept att följa steg för steg vilket man vet kommer att ge en god måltid. Men vill man skapa något nytt och bättre så måste man våga experimentera och komma på nya tekniker. Ifall resultatet

blir dåligt, får man kasta sin kreation i komposten för att ta nya tag och komma på bättre lösningar. För att förbättra transistorns prestanda har vi utvecklat en teknik där atomernas förmåga att växa i speciella kristallriktningar har utnyttjats, lite liknande hur atomerna i natriumklorid bildar kristaller i flingsalt. Genom att utnyttja olika kristall-riktningar kan transistorns prestanda optimeras och kapacitanser som saktar ner transistorn kan minskas. Just minskning av kapacitanser har varit ett stort fokusområde för avhandlingen, där många nya processtekniker har föreslagits, varav vissa gav bland de lägsta kapacitanserna av alla transistorteknologier i världen. Transistorerna har visat prestanda nära de teoretiska fysikaliska gränserna, och i vissa avseenden presterar de till och med bättre än kisel-transistorer tillverkade av stora miljard-företag. Arbetet kan bli betydelsefullt för framtida utveckling av energieffektiva och prestandakrävande applikationer inom 5G, bilradar, internet of things samt gest-igenkänning.

Acknowledgments

There have been so many people involved in making this thesis a reality. First, I would like to thank my main supervisor Erik Lind. Erik, it has been a pleasure working with you during these years. We have shared so many great (and maybe not so great) ideas. Your door has always been open and you have guided me through the semiconductor technologies with great enthusiasm. Lars-Erik, you have been a great group leader and shown me how to set-up great research environments and how to initiate collaborations and in giving a broader view on industry and education in general. Mattias, thanks for all the inspiration and for guiding me through all aspects of III-V technology, from atoms to systems.

Cezar, a big thanks for introducing me to the lateral nanowire processing and characterisation, my work wouldn't have been possible without all your efforts. Navya and Lasse, thanks for the countless hours you have spent working in the lab to help our common projects. Stefan, thanks for always being there helping out with processing and setting up RF measurements, and introducing me to all aspects regarding circuits. Anna and Josefine, thanks for help developing the transistor technology, and for your great patience and perseverance. Thanks to Olof and Magnus for introducing me to device technology and to the Lund Nano Lab, which made it possible for me to pursue my career in academia.

Olli-Pekka, Adam, Markus, Sebastian, Elvedin, Karl-Magnus, Lars, Johannes, Aein, Guntrade, Jun, Martin, Kristofer, Patrik, Saketh, Heera, Robin, Anton, Gautham, Zhongyunshen and Abinaya, you have made these years a pleasure and make working with all of you has been a joy.

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I would like to thank all personnel at EIT, especially Daniel, Elisabeth, Anne and Linda for always helping out when I am lost.

Mum and dad, thanks for all your support and love. Thanks for always taking the time and answering my questions about how things worked growing up. Eva, thanks for being a great sister and friend in life and for helping your younger brother through school in younger years!

I would like to thank my friends and extended family for always caring and providing good times and laughter. Linus, thank you so much for the help with cover photo and images.

My daughter Alma, you are an inspiration in your daily quest to understand how the world works, and you make time fly. Louise, you are the love of my life and my true inspiration, both in personal life as well as in research. You encourage me to try new things and if it wasn't for you, I wouldn't have had the courage to start my PhD in the first place.

List of Papers

This thesis is based on the following six papers which are included at the back of the thesis.

I F. Lindelöw, C. B. Zota, E. Lind, ”Gated Hall effect measurements on selectively grown InGaAs nanowires”, *Nanotechnology,* 2017

I designed the Hall bar structures, performed all fabrication steps except growth, did both Hall measurements and resistivity measurements and analyzed the measured data. Finally, I also wrote the paper.

II F. Lindelöw, N. Sri Garigapati, L. Södergren, M. Borg, E. Lind, ”III-V nanowire MOSFETS with novel self-limiting Λ-ridge spacers for RF applications”, *Semiconductor science and technology,* 2020

I developed the novel process of Λ-ridge spacers including fabrication and validation of all involving process steps. I co-fabricated the actual device that was published and were involved both in DC and RF measurements. I did the data analysis and wrote the paper.

III C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz”, *Electronic Letters,* 2016

I collaborated in developing processing scheme with a focus on spacer implementation, and co-fabricated devices, as well as contributed to DC and RF measurements and data analysis.

IV C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”InGaAs tri-gate MOSFETs with record on-current”, *2016 IEEE Int. Electron Devices Meetings (IEDM),* 2016

I collaborated in device processing, especially in lithography, deposition and digital etching. I also collaborated in electrical characterization and data analysis.

V C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”InGaAs nanowire MOSFETs with I_{ON}= 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V”, *Symposium on Very Large Scale Integrated Circuits and Technology (VLSI)”,* 2016

I collaborated in developing the process and in the processing of the device itself, especially in digital etching and device passivation. I also collaborated in electrical characterization and data analysis.

VI F. Lindelöw, M. Heurlin, G. Otnes, V Dagyte, D. Lindgren, O. Hultin, K. Storm, L. Samuelson, M. Borgström , ”Doping evaluation of InP nanowires for tandem junction solar cells”, *Nanotechnology,* 2016

I performed all device processing of the Hall-contacts on the nanowires. I performed the Hall measurements and resistivity measurements. I did the majority of the data analysis and I wrote the paper.

The following papers are not included in the thesis, but summarize related work that I have contributed to.

VII F. Lindelöw, C. B. Zota, E. Lind, ”Low capacitance InGaAs nanowire MOSFETs for high-frequency applications”, *Compound semiconductor week,* 2018

VIII F. Lindelöw, C. B. Zota, L.-E. Wernersson and E. Lind, ”High transconductance InGaAs nanowire MOSFETs ”, *GigaHertz,* 2016

IX L. Ohlsson, F. Lindelöw, C. B. Zota, M. Ohlrogge, T. Merkle, L.-E. Wernersson, E. Lind, ”First InGaAs lateral nanowire MOSFET RF noise measurements and model”, *75th Annual Device Research Conference (DRC),* 2017

X S. Andric, L. Ohlsson Fhager, F. Lindelöw, O.-P. Kilpi, L.-E. Wernersson, ”Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs”, *Journal of Vacuum Science & Technology B,* 2019

XI C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, “High-performance field-effect transistors using selectively grown lateral InGaAs nanowires”, *Nanowire week,* 2017

XII T. Haggren, G. Otnes, R. Mourao, V. Dagyte, O. Hultin, F. Lindelöw, M. Borgström, L. Samuelson, ”InP nanowire p-type doping via zinc indiffusion”, *Journal of crystal growth,* , 2016

XIII F. Lindelöw, L. Södergren, E. Lind,, ”III-V nanowire MOSFETs for high-frequency applications”*,* IVC 21, 2019

Abbreviations and Symbols

ABBREVIATIONS

$(NH4)_2S$ diammonium sulphide

Al aluminum

Al_2O_3 aluminum oxide

ALD atomic layer deposition

Au gold

BOE buffered oxide etch

BCB benzocyclobutene

CMOS complementary metal-oxide-semiconductor

DOS density of states

DUT device under test

EOT effective oxide thickness

FDSOI fully depleted silicon on insulator

FinFET fin field-effect transistor

FET field-effect transistor

GAA gate-all-around

GaAs gallium arsenide

H_2O_2 hydrogen peroxide

H_3PO_4 phosphoric acid

HCl hydrochloric acid
HEMT high-electron-mobility-transistor
HF hydrofluoric acid
HfO_2 hafnium oxide
HSQ hydrogen silsesquioxane

InGaAs indium gallium arsenide
InP indium phosphide

LED light emitting diode

MAG maximum available gain
MSG maximum stable gain
MOCVD metal organic chemical vapor deposition
MOVPE metal organic vapor phase epitaxy
MOSFET metal-oxide-semiconductor field-effect transistor

Ni nickel

Pd palladium
PMMA poly(methyl methacrylate)

QCL quantum capacitance limit

RF radio-frequency

S.I. semi-insulating
S/D source and drain
Si silicon
SiO_2 silicon dioxide

Sn tin

SS inverse subthreshold slope

TMAH tetramethylammonium hydroxide

Ti titanium

TiN titanium nitride

VLS vapor-liquid-solid

VNA vector network analyzer

GREEK SYMBOLS

μ mobility

λ mean free path

κ dielectric constant

$\varepsilon(0)$ top of the barrier energy

ρ resistivity

σ conductivity

LATIN SYMBOLS

C_C charge centroid capacitance

C_{OX} oxide capacitance

C_Q quantum capacitance

D_n diffusion constant

E_F Fermi level

f_{max} maximum oscillation frequency

f_T cut-off frequency

g_d output conductance

g_m transconductance

I_{OFF} off-state current

I_{ON} on-state current

k wavevector

k stability factor

L_g gate length

m^* effective electron mass

n carrier density

q electric charge

R_g gate resistance

R_{ON} On-resistance

T_L crystal lattice temperature

V_{DD} drive bias

V_T threshold voltage

Table of Contents

1 Background

In 1947, Bell laboratories invented the first point-contact transistor and it was made in the semiconducting material germanium [1]. The transistor allowed a very small signal to control a much larger current flow, effectively turning the transistor on and off as a switch. About a decade later, in 1959, the first experimental demonstration of a metal-organic-semiconductor field-effect transistor (MOSFET) made out of silicon was fabricated. It turned out that the native oxide that naturally forms on silicon, SiO_2, was a good electrical insulator to use underneath the gate contact in order to achieve small gate leakage currents but also a high capacitive coupling between the gate electrode and the channel. Silicon is also a material with a high density of states and a good electron mobility, which all together made the realization of well performing transistors. In parallel to the evolution of the silicon MOSFET, III-V semiconductor materials were researched due to their direct band gap, enabling optical semiconductor devices and due to the superior electron mobilities. However, these III-V materials do not have as good native oxide as silicon [2], and their superior electron velocity was primarily used for oxide-less high-electron-mobility-transistors (HEMTs) [3] and bipolar-junction-transistors [4]. As the silicon transistor size was scaled down according to the laws of Dennard scaling [5], the speed of the transistor also increased, one reason being a lower resistance in the shorter channel. This allowed for smaller, faster and more energy-efficient computing for every new node, which Gordon Moore famously predicted in what is called Moore's law; the transistor density approximately doubles every two years [6]. In order to scale the MOSFET transistor even further, the thickness of the insulating oxide barrier had to be thinner as well to maintain a good electrostatic control of the channel potential. However, this made the gate leakage increase and therefore, research of different oxides than the native SiO_2 was conducted and eventually, the SiO_2 was replaced with HfO_2 in Intel's 45 nm node, where the capacitive gate coupling could be high while having a thicker oxide due to the higher κ-value[7]. This eliminated one of the intrinsic benefits that silicon had over III-V materials, as HfO_2 and Al_2O_3 have been shown to perform well on III-V semiconductors when self-cleaning pulses in atomic layer deposition (ALD) is used

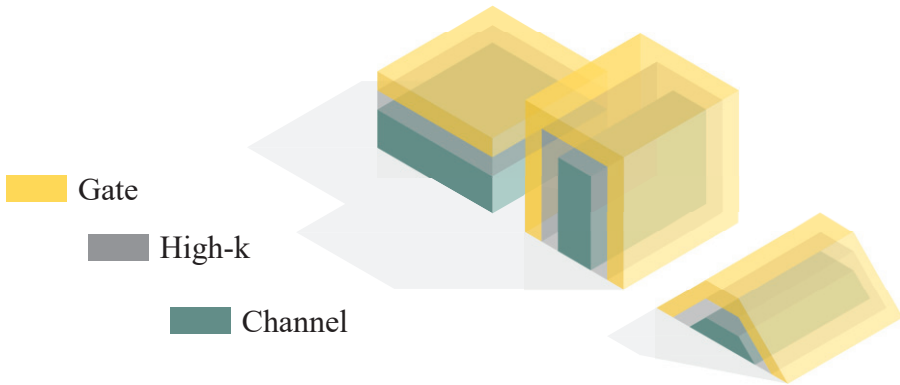

Figure 1.1: Schematic illustrations of three important device architectures, planar MOSFET, FinFETs and nanowire MOSFET also called Tri-gate or nanosheet architecture that has been used in this thesis.

to remove native oxide[8-10]. Similar scaling problems also arose for III-V HEMTs, where the scaled devices with thin semiconductor barriers underneath the gate also gives increased gate leakage [11]. Therefore, MOSHEMTs with high-k barriers on top of $In_xGa_{1-x}As$ channels are currently researched, with expected increase in drive currents and high-frequency performance[12]. However, the reliability of high-k oxides on III-V materials is still a challenge and needs to be solved before III-V transistors with gate oxide will be implemented in commercial devices. After the invention of high-k MOSFETs, another important technology shift was the move to three-dimensional channels rather than planar two-dimensional in high-performance digital circuits [13]. Three dimensional channel transistors as FinFETs and nanowire transistors, as seen in figure 1.1, give a performance boost from increased electrostatic control due to that the gate can control the potential in the channel from multiple sides, reducing the detrimental short channel effects.

The evolution of silicon transistors has in many ways been driven by the digital circuits, where the demand of digital chips have increased many fold since the first silicon MOSFET was invented. However, the demand for RF devices is also large and it is expected to increase as we are transmitting ever more data wirelessly in the modern society. From the 2G and 3G technology, which used only a few frequency bands to transmit signals, to the modern 4G technology which can use up to 40 bands, the amount of analog transistors in a smartphone is increasing and requirements on well-performing amplifiers are high [14]. Future applications in 5G where massive multiple-input multiple-output applications are likely to be implemented, as well as radar applications in the automotive industry, will make the

demand of RF transistors increase even further [15]. Generally, low-noise-amplifiers and power amplifiers in smartphones have been based on GaAs or InP technology, while devices for routing of analog signals, such as switches, have been made in silicon. Chips where analog and digital functions can be combined is expected to decrease delay and energy consumption. There have been a lot of research recently by for instance IBM Zurich and IMEC on how to integrate different semiconductors on silicon to combine for example standard complementary-metal-oxide-semiconductor (CMOS) technology with III-V to be able to take advantage of the improved speed or optical capabilities [16-18].

Up until now, the industry have made many studies on logic performance of silicon nanowires for scaled process nodes, but the RF capabilities are less researched. The work in this thesis have been aimed at improving the field of III-V nanowires with special emphasis on nanowire MOSFETs for high-frequency applications, where spacer technologies for reducing the inherently higher parasitic capacitances has been the main focus.

1.1 Optical applications

III-V materials have been used for opto-electronics due to their direct band gap and favorable electron mobility. The direct band gap allows for development of light-emitting diodes (LEDs) and lasers which has led to significant improvements in growth and characterization of III-V semiconductors [19, 20]. GaAs and InP also have a band gap near the optimum for a single junction solar cell for maximum energy conversion [21]. The possibility to fine-tune band gap and lattice constant with composition of ternary III-V compounds, opens up the possibility to do tandem junction solar cells with several different band gaps to absorb more of the incoming energy from the sun. Recently, researchers at NREL demonstrated a GaAs based 6 junction solar cell with world record efficiency of 47.1% under 143 suns concentrated light [22]. The drawback however, is the increased price for III-V semiconductors compared to silicon, especially in such large area applications as solar cells. Research to limit the amount of III-V material needed is currently ongoing by using nanowires with substrate reuse, or by using nanowires grown with aerotaxy without a substrate [23, 24]. If the nanowire array is engineered so that the diameter and pitch of the nanowires are similar to the wavelength of light, the nanowire can actually absorb a larger portion of the incoming light than its own cross section [25].

2 Transistor theory

In this section, the most important aspects of electrical transport and characterization, with a focus on transistors, will be presented.

2.1 Transistor operation

A transistor is a three-terminal device, where a voltage bias is applied between source, gate and drain contacts enabling a current to flow between source and drain. The third terminal, the gate contact, turns this current on or off with applied gate bias. The transistor can either operate as a switch or as an amplifier of applied signals. For a switch, which for instance is used in CMOS technologies that perform the calculations in almost all computers and smartphones, the most important metrics regarding the off-state are off-current (I_{OFF}), inverse subthreshold slope (*SS)*, drain-induced barrier lowering (DIBL) and threshold voltage (V_T) while for the on-state important metrics are transconductance (g_m), output conductance (g_d) and on-resistance (R_{ON}) and on-current (I_{ON}). Transfer characteristics for off-state and on-state can be seen in figure 2.1 with logarithmic and linear scale respectively. For a transistor that is used as an amplifier, the off-state is not as important, since the transistor will in general operate in the on-state. The most important metrics for a transistor in an analog application is all metrics regarding on-state as mentioned before, but also gate capacitance and gate resistance, as well as transistor gain. Compared to planar silicon transistors, III-V nanowire structures can in theory enable steeper inverse subthreshold slope and higher drive currents at the cost of increased parasitic capacitances.

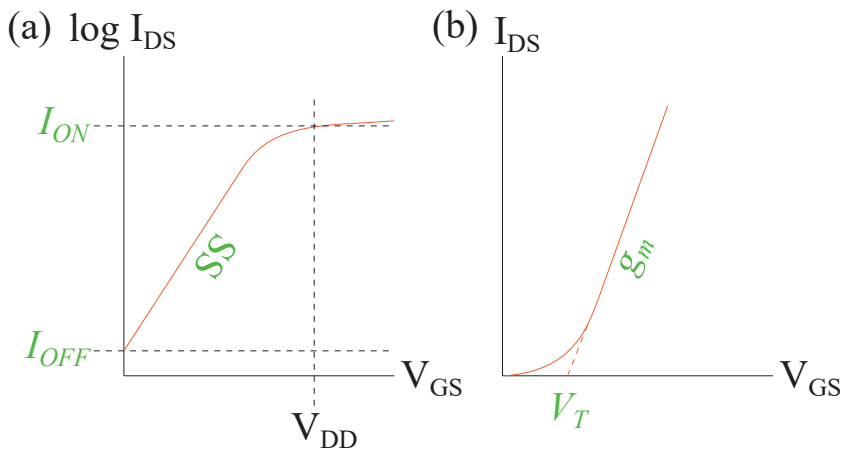

Figure 2.1: Off-state(a) and on-state (b) of a MOSFET transistor with a few relevant metrics highlighted.

2.2 Classical transport

For semiconductor devices with large dimensions and low electric fields, and low carrier concentration, the transport through the semiconductor can be described with the classical transport of drift and diffusion[26].

$$J = qn\mu\varepsilon + qD_{\mathrm{n}}\frac{dn}{dx} \tag{2.1}$$

The current originating from drift is proportional to the mobility μ, carrier concentration n, and the applied electric field ϵ. In general, III-V materials have a high electron mobility, since it is inversely proportional to the effective mass m^*, but a smaller intrinsic carrier concentration than silicon, due to the density of states being smaller, also due to the lower effective mass.

$$\mu = \frac{q\tau_{\mathrm{c}}}{m^*} \tag{2.2}$$

As the devices are scaled in dimensions, the applied electric fields become very large, and eventually, the electron velocity is not proportional to the applied electric

field but saturates at a finite value called velocity saturation [27]. The current originating from drift can then be rewritten, by inserting the constant ε_c which is the critical electric field

$$J = \frac{qn\mu\varepsilon}{1 + \frac{\varepsilon}{\varepsilon_c}} \tag{2.3}$$

Diffusion current is also proportional to the mobility, but more importantly to the gradient in carrier concentration in the material.

2.3 Channel capacitance

As transistor dimensions have been scaled over the years, the short channel effects also increased. According to Dennard scaling, in order to maintain good electrostatic control of the channel, the thickness of the insulating oxide should also decrease[5]. The surface potential at the top of the barrier in the channel is set by the difference between applied gate overdrive voltage and the voltage drop over the oxide. In order to have a high coupling between the gate and the channel, the voltage drop over the oxide should be minimized, which corresponds to an increased gate oxide capacitance according to equation (2.4)

$$C_{\mathrm{ox}} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox}} \tag{2.4}$$

The total gate capacitance to the channel is three capacitors in series, the oxide capacitance C_{ox}, the quantum capacitance C_{q} and the charge centroid capacitance C_{c} [28].

$$C_{\mathrm{G}} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{1}{C_c}\right)^{-1} \tag{2.5}$$

For a two dimensional field effect transistor, the quantum capacitance can be written as

$$C_q = \frac{q^2 m^*}{\pi \hbar^2} \tag{2.6}$$

and is the effect of the limited density of states in the semiconductor, which results in accumulation of electrons in the channel. Once there are carriers inside the channel, this will in turn lead to an upward shift of the energy bands due to repulsive interactions between electrons. This can be described by another capacitance in series with the quantum capacitance, and is called charge centroid capacitance, and can be calculated by quantum mechanical perturbation theory.

$$C_c = \frac{\varepsilon_s \varepsilon_o}{0.36 t_{\mathrm{w}}} \tag{2.7}$$

The quantum capacitance is not fixed for all different channel materials, but it depends on the effective mass of the electron. For a classical silicon transistor, the effective mass and quantum capacitance is relatively large and therefor the C_q^{-1} can be neglected in equation (2.5) as long as the thickness of the insulating gate oxide is not too small. This is called the MOS limit for gate capacitance**.** For a III-V transistor, with a very small effective mass and a scaled oxide thickness, $C_{ox} \gg C_q$ and the term C_{ox}^{-1} can be neglected in equation (2.5). This limit is called the quantum capacitance limit (QCL) and this means that the applied gate overdrive bias would directly control the potential in the top of the barrier in the channel. In devices where $C_{ox} \gg C_q$, the transistor performance would not continue to improve with reduction of oxide thickness, but rather saturate at some finite value.

2.4 Ballistic transport

For a nanowire MOSFET with high electron mobility and very narrow dimensions, including width, height and gate length shorter than the mean free path, the transport through the channel can be modelled with 1D ballistic transistor theory. This means that the carriers are confined in two dimensions, and can only propagate in the third dimension. The analysis follows work developed by Lundstrom [29].First, we use the effective mass approximation and assume simple parabolic band structure, where only the first sub-band is conducting.

$$\varepsilon_1(k) = \varepsilon_1(0) + \frac{\hbar^2 k^2}{2m^*} \tag{2.8}$$

Here $\varepsilon_1(0)$ is the minimum of the bottom sub-band, also called the top of the barrier, which for a well-designed one dimensional transistor with insignificantly small influence of drain and source bias, is set by

$$\varepsilon_1(0) = -qV_G{}' + \frac{q^2 n_{s,(\varepsilon_1(0))}}{C_{ox}} \tag{2.9}$$

The electron velocity is proportional to the derivative of the energy, $v_x = \hbar^{-1} dE/dk$. The charge can be calculated by integrating the product of the 1D density of states and the probability that each state is occupied, which is described by the Fermi-Dirac distribution.

$$n = \int_{E_c}^{\infty} D(E) f_0(E) dE = \int_{E_c}^{\infty} \frac{D(E) dE}{1 + e^{(E-E_f)/k_B T}} \tag{2.10}$$

Where the density of states for 1 dimension is:

$$D_{1D}(E) = \frac{\sqrt{2m^*}}{\pi\hbar} \sqrt{\frac{1}{E - E_c}} \tag{2.11}$$

The charge can be divided into two parts, carriers with positive and negative k-states travelling in opposite directions. The solution to the integral in (2.11) is seen below, where N_{1D} is the effective density of states and $F_{-1/2}$ is the Fermi Dirac integral of order -1/2.

$$n_L^+(0) = \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F) \tag{2.12}$$

With the constant $\eta_F = \frac{(E-E_c)}{k_B T_L}$, where $N_{1D} = \frac{\sqrt{2m^* k_B T_L/\pi}}{\hbar}$ is the effective density of states and $F_{-\frac{1}{2}}(\eta_F) = \frac{2\eta_F^{1/2}}{\sqrt{\pi}}$ is the Fermi Dirac integral of order -1/2. For negative k-states, the drain bias has shifted the drain fermi-energy downwards, why U_D is added to the expression.

$$n_L^-(0) = \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F - U_D) \tag{2.13}$$

$$U_D = \frac{qV_{DS}}{k_B T_L} \tag{2.14}$$

Next to, obtain the current, we calculate the sum of all k-states and start with the positive k-vectors.

$$I^+ = \frac{1}{L}\sum_{k>0} qv\, f_0(E_F) \stackrel{\text{def}}{=} qn_L^+(0)v^+(0) \tag{2.15}$$

This can be remade into an integral, if taking into account that each k-state occupies a length of 2π/L.

$$I^+ = \frac{2q}{2\pi\hbar}\int \frac{dE}{dk} f_0(E(k), E_F)dk = \frac{2q}{h}\int_{E_c}^{\infty} f_0(E(k), E_F)\, dE \tag{2.16}$$

Here it is seen that the ballistic current is not dependent on effective mass, due to that the terms regarding effective mass in the density of states and electron velocity cancels for 1D transport. The solution to the equation is

$$I^+ = \frac{qk_B T_L}{\pi\hbar} F_0(\eta_F) \tag{2.17}$$

$$F_0(\eta_F) = \ln(1 + e^{\eta_F}) \tag{2.18}$$

By combining equation (2.15) with equation (2.12) we can also get an expression for the velocity for the carriers with positive momentum

$$v^+(0) = v_T \frac{F_0(\eta_F)}{F_{-1/2}(\eta_F)} \tag{2.19}$$

where the v_T is expressed as: $v_T = \sqrt{2k_B T_L/\pi m^*}$. The same reasoning can be done for the negative k-states, and current, with the velocity:

$$v^-(0) = v_T \frac{F_0(\eta_F - U_D)}{F_{-1/2}(\eta_F - U_D)} \tag{2.20}$$

Next we calculate the total current:

$$I = I^+ - I^- = \frac{2qk_B T_L}{h}\{F_0(\eta_F) - F_0(\eta_F - U_D)\} \tag{2.21}$$

If we assume that the bands are degenerate, $\eta_F \gg 1$ as they often are for III-V semiconductors, and the top of the barrier is below the fermi-level on both source and drain side, i.e. small drain biases, the equation above simplifies to

$$I_D = \frac{2q^2}{h} V_{DS} \tag{2.22}$$

In the QCL limit, where $C_Q \ll C_{ox}$ equation (2.21) turns into equation (2.23) which is independent of material parameters.

$$I_D = \frac{2q^2}{h} (V_{GS} - V_T) \tag{2.23}$$

2.5 Two-port measurements

The transistor is a three-terminal device, but when the transistor is biased in common-source configuration, the source terminal is grounded and the transistor can be measured in a two-port measurement with AC-signals supplied to the gate and drain contacts. In an S-parameter measurement, incident electromagnetic power waves a_i are applied at the two ports and the reflected power waves b_i are measured. From this, the scattering matrix S consisting of reflection coefficients S_{11} and S_{22} and transmission coefficients S_{21} and S_{12} can be calculated[30].

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.24}$$

The benefit of measuring S-parameters compared to the more intuitive Y- or Z-parameters is that the former only require 50 Ω termination in the vector network analyzer (VNA) while the two latter requires perfect open and short terminations which is difficult to achieve in a high-frequency environment, effectively reducing the measurement accuracy [31].

2.6 Small signal modeling

For optimization of the high-frequency performance of a MOSFET, it is very important to be able to quantify the performance limiting aspects of the transistor. A small-signal hybrid-π model can be used to make a physical representation of the transistor [32]. To extract the different elements of the model, the measured S-parameters are first deembedded (more information section 2.8) and then transformed into impedance parameters Z. Next, estimated source and drain resistances R_s and R_d are subtracted from the Z-parameters before the parameters are transformed to Y-parameters, which is the basis of the parameter extraction. The small signal elements can be extracted according to equations (2.25) to (2.31) and the small-signal model can be seen in figure 2.2.

$$g_m = Re(Y_{21})|_{\omega^2=0} \tag{2.25}$$

$$g_{ds} = Re(Y_{22})|_{\omega^2=0} \tag{2.26}$$

$$R_g = \frac{Re(Y_{11})}{Im(Y_{11})^2} \tag{2.27}$$

$$C_{gd} = \frac{-Im(Y_{12})}{\omega} \tag{2.28}$$

$$C_{gs} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega} \tag{2.29}$$

$$C_{dg} = \frac{-Im(Y_{21})}{\omega} - g_m R_g (C_{gs} + C_{gd}) \tag{2.30}$$

$$C_{sd} = \frac{-Im(Y_{22})}{\omega} - C_{gd} - g_m R_g C_{gd} + \omega^2 C_{gd} C_{dg} (C_{gs} + C_{gd}) {R_g}^2 \tag{2.31}$$

When all parameters of the model have been extracted, the modeled Y-parameters can be calculated, and subsequently the modeled Z-parameters with added source and drain resistances R_s and R_d. This way, the transistor behavior can be modeled up to higher frequencies, based on measurements up to relatively low frequencies. This model agrees with the transistor behavior fairly well, but none ideal effects can be added to make the model match the device under test. For instance, at high drain

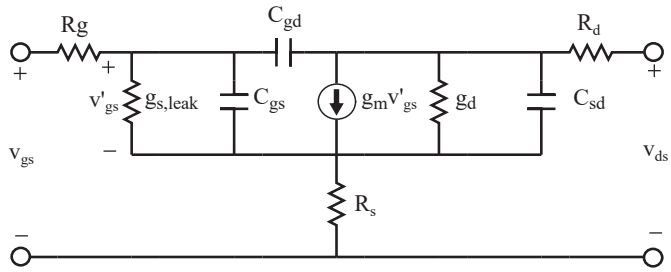

Figure 2.2: A small signal hybrid-π model used to model the RF devices in this thesis. Here Rg is the effective gate resistance with the channel resistance included.

bias, impact ionization and band to band tunneling effects can be added as current sources [33] and time dependent effects as oxide traps can be added as frequency dependent conductance [34].

2.7 RF metrics

A transistor working as an analog device to amplify a signal needs to have gain, otherwise the signal on the output would be smaller than the input and noise would be added. Gain can be defined in several ways, where the most common ones are current gain and power gain. The current gain of the device can be calculated from the measured Y-parameters.

$$h_{21} = \frac{i_2}{i_1}\bigg|_{V_1=0} = \frac{Y_{21}}{Y_{11}} \tag{2.32}$$

Reactance in the transistor will behave as short circuits at very high frequencies, and the transistor will no longer have current gain, leading to that the AC gate leakage current will be as large as the source drain current. The maximum current gain frequency f_T is defined as the frequency where the ratio of these two currents are unity, and can be estimated by plotting $|h_{21}|^2$ in a semi-log plot up to the measured frequency limit and then extrapolating with a slope of -20 dB/decade. The other approach is to report the value that the y-parameters from the small-signal model predicts. This can give a slightly higher result, as the small signal modeled gain often deviates from -20 db/decade slope at higher frequencies.

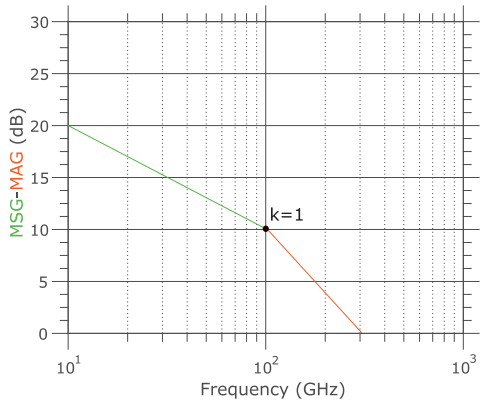

Figure 2.3: Maximum stable gain and maximum available gain where the intersection is the k-point for an arbitrary transistor. The gain of the transistor quickly drops after this point.

An approximate value of f_T can also be obtained from the parameters of the small signal model.

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.33}$$

Optimizing for large f_T, which is important for low RF noise, means that the transistor should have a high transconductance and small parasitic capacitances. The other important gain of the transistor is the power gain. Maximum available gain is defined as

$$MAG = \frac{Y_{21}}{Y_{12}}(k - \sqrt{k^2 - 1}) \tag{2.34}$$

Where the stability factor k is defined as.

$$k = \frac{2Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{12})}{|Y_{12}Y_{21}|} \tag{2.35}$$

When $k > 1$, the transistor is unconditionally stable and the circuit designer can optimize gain without worrying about the stability. If $k < 1$, the transistor is conditionally stable and then the maximum stable gain is defined as.

$$MSG = \frac{Y_{21}}{Y_{12}} \tag{2.36}$$

MSG can also be approximated with small signal model elements as seen in equation (2.37).

$$MSG(f) \approx \frac{1}{f}\frac{g_m}{2\pi\, C_{gd}} \tag{2.37}$$

When $k = 1$, MSG = MAG and this frequency is called the k-point. In order to increase the power gain at frequencies below the k-point, for instance at 5 and 20 GHz, where many communication important frequencies are, all aspects of optimizing for f_T applies, but with special emphasis on low drain capacitance $C_{gd.}$. At frequencies above the k-point, the gain drops quickly and it can therefore be useful to increase the k-point as much as possible, see figure 2.3. For a transistor with a passive feedback network, the corresponding maximum power gain of the transistor is called Mason's unilateral power gain U and can be calculated as

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(Re(Y_{11})Re(Y_{22}) - Re(Y_{12})Re(Y_{21}))} \tag{2.38}$$

The frequency at which the power gain U is unity is called maximum oscillation frequency f_{max} and for small source and drain resistances, f_{max} can be approximated

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_G(C_{gd} + \frac{C_{gg}g_d}{g_m})}} \tag{2.39}$$

This means that high f_T usually also leads to a higher f_{max} but in order to maximize f_{max}, the gate resistance, output conductance and especially drain capacitance needs to be low. Due to the gate resistance entering the equation, peak f_{max} typically occurs at smaller device width than peak f_T.

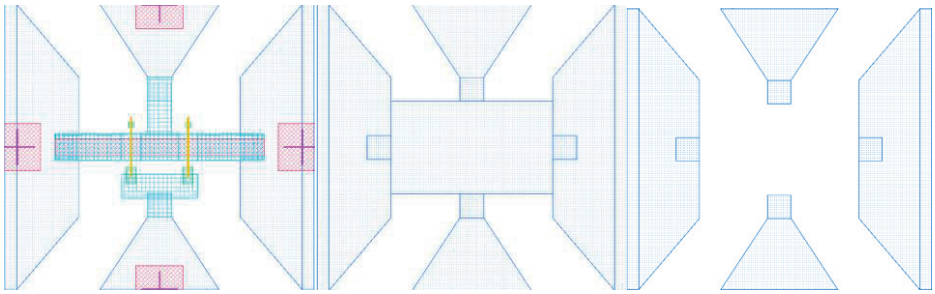

Figure 2.4: Schematic images for device under test as well as short and open deembedding structures.

2.8 Calibration and de-embedding

In an RF measurement of a transistor, the measured parameters from a VNA is not only dependent on the device under test, but also pads, probes, cables and connectors. However, when designing an amplifier, it is important to know the performance of the device itself, otherwise device modeling will be incorrect and matching networks of the device will be flawed. Therefore two things are necessary to perform in order to know the real performance of the device. First, the VNA must be calibrated to move the reference point from the connectors of the VNA, to the tip of the probes with LRRM calibration (line, reflect, reflect match) using an impedance standard substrate (ISS) [35]. Next, in order to not let admittance and impedance in probes and pads affect the modeling of the device under test, the reference plane must be moved from the probe tips to the edge of the transistor. This is done with open and short deembedding [36]. The open and short reference structures are fabricated simultaneously with the transistor on the substrate and measured with the VNA. Layout of device under test (DUT), open and short deembedding can be seen in figure 2.4. First, the measured S-parameters of open, short and device under test are transformed into Y-parameters. To eliminate the capacitance from the open structure, the measured open Y-parameters, Y_O, is subtracted from both the short, $Y_{S-O} = Y_S - Y_O$ and the device under test $Y_{DUT-O} = Y_{DUT} - Y_O$. Next, in order to remove the inductances of the short reference, the subtracted Y-parameters are transformed into Z-parameters, and the Z-parameters of the short reference structure is subtracted from the device under test to give the deembedded Z parameters, $Z_{DE} = Z_{DUT-O} - Z_{S-O}$. Finally, the de-embedded Z-parameters can be transformed into S-parameters again for further analysis.

3 Semiconductor crystals and doping

This section covers two important aspects of semiconductor manufacturing that greatly affect the performance and characteristics of III-V electronic devices, namely doping of the semiconductor crystals, and the effect of facets in the crystal lattice.

3.1 Doping

Doping of a semiconductor was first realized by John Robert Woodyard in 1950, and has led to a rapid evolution in the semiconductor industry[37]. Doping a semiconductor with very small portions of another material, with either surplus or deficit of valence electrons gives rise to n-type or p-type doping, drastically changing the conductivity of the material. P-n junctions, where both type of doping are used in sequence, is the fundamental building block of most types of solar cells, LEDs, as well as in bipolar junction transistors, in order to create electric fields forcing electrons and holes to either separate or recombine [38]. In CMOS technology, for an n-type and p-type device conducting current with electrons or holes respectively. A few of the most common dopants for III-V semiconductors used in high-speed devices are Si, Sn and S for n-type dopants and Zn for p-type dopants, while Fe is used to insulate III-V substrates. Both silicon and tin are group IV elements. This means that they can act either as donors or acceptors depending on if they occupy the group III or V position in the lattice. N-type doping with group IV atoms can thus autocompensate and saturate at high doping levels due to occupancy of group V sites. This also makes the free carrier concentration levels with group IV atoms dependent on V/III ratios during growth[39].

3.1.1 Hall measurements

There are many techniques available to determine the carrier concentration of electron and holes in a nanowire, for instance photoluminescence [40],

cathodoluminescence [41], field-effect measurements as well as recently Hall measurements [42]. Although optical measurements is not inducing any damage in the nanowire, most times it requires that the nanowires are broken off and moved to a specific measurements substrate. This is however difficult if the nanowires are lateral and grown into the substrate itself. Another drawback is the fairly low spatial resolution obtainable. Field-effect measurements does not require that the nanowires are transferred to another substrate, but is difficult to estimate the capacitance between the gate and the channel due to the occurrence of semiconductor capacitance and oxide capacitance, the latter suffering from uncertainties in density of interface traps affecting the capacitance. Hall measurements is another way of determining the carrier concentration in a semiconductor and at the same time obtaining the mobility of the carriers. In 2012 Storm et al published the first spatially resolved Hall measurements on nanowires, where the doping profile along the nanowire could be established [43]. However, evaporating contacts on each side of the nanowire with a sufficient spacing is a challenge for nanowires of small dimensions. The selective area growth of lateral nanowires has the possibility of simultaneous growth of semiconductor contacts to the nanowire in the same growth step as the nanowire itself, which then can be contacted with larger metal contacts in a subsequent step.

An electron moving with a velocity in a simultaneous electric and magnetic field is exposed to a force, called the Lorentz force.

$$F = q(\boldsymbol{E} + v \times \boldsymbol{B}) \tag{3.1}$$

In a Hall measurement setup, the electron moves in x-direction due to an applied electric field, and a magnetic field is applied in z-direction. Then equation (3.1) can be simplified.

$$F_z = 0 \tag{3.2}$$

$$F_y = q v_x B_z \tag{3.3}$$

$$F_x = q E_x \tag{3.4}$$

This means that compared to standard drift current, the electrons also exhibits a force in y-direction, causing the electrons path to diverge, giving an accumulation of electrons on one side and a depletion on the other, generating a voltage that is called the Hall voltage. The force from the electric field in y-direction, the Hall field, generated from the Hall voltage will at steady state cancel out the force from the applied magnetic field.

$$\frac{qV_H}{w} = qv_xB_z \tag{3.5}$$

The Hall voltage can then be calculated from the width, velocity in x-direction and the applied magnetic field.

$$V_H = wv_xB_z \tag{3.6}$$

The current in x-direction is also dependent on thickness of the semiconductor and can be written as

$$I_x = qtnwv_x \tag{3.7}$$

Inserting this into equation (3.6), the Hall voltage can finally be written as equation.

$$V_H = \frac{I_xB_z}{qtn} \tag{3.8}$$

The Hall voltage is thus proportional to the applied magnetic field and current, and inversely proportional to the electron charge, thickness of the semiconductor and importantly the carrier concentration. By also measuring the resistivity of the semiconductor, the mobility of the charged carriers can be calculated as:

$$\mu = \frac{1}{qn\rho} \tag{3.9}$$

For a cylindrical nanowire as in paper VI, with thickness and width being equal to the diameter, with metal contacts directly in contact with the nanowire that cannot be regarded as point contacts, the extracted carrier concentration can differ slightly from the true carrier concentration. We therefore extended the equations to allow

for electric fields existing in all three directions, x, y and z, and modeled the electric fields and Hall voltage in a finite element method program called COMSOL Multiphysics. The drift current $J_{n,drift} = \sigma E$, can be modeled with the three dimensional conductivity tensor according to

$$\sigma = \sigma_0 \begin{pmatrix} \frac{1}{1+(\frac{q\tau}{m^*}B)^2} & \frac{\frac{q\tau}{m^*}B}{1+(\frac{q\tau}{m^*}B)^2} & 0 \\ \frac{-\frac{q\tau}{m^*}B}{1+(\frac{q\tau}{m^*}B)^2} & \frac{1}{1+(\frac{q\tau}{m^*}B)^2} & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{3.10}$$

where $\sigma_0 = (\frac{q^2\tau n}{m^*})$ [26]. More information on Hall measurements on nanowires can be found in [43].

3.1.2 Modulation doping

One way to decrease the resistivity in a semiconductor is to dope it, with very small portions of donor atoms. However, the doping leaves ionized donor atoms behind, which will reduce the electron mobility in the doped material due to increased amount of scattering events. In 1977, Bell labs developed a scheme where the doping was performed in a wide band gap material just next to a narrow band gap material [44]. Due to the difference in band gap, the free carriers will fall into the narrow band gap material, as the electrons strive to lower its potential energy, effectively separating the carriers from its ionized donors. This gives a high amount of carriers in the narrow channel material, while still maintaining a high mobility.

3.2 III-V semiconductor crystal

III-V compounds typically forms crystals in zincblende structure, but III-V nanowires can also be wurtzite, where the inclusion of one of them inside the other one is called a stacking fault. One common substrate is the (100) zincblende which

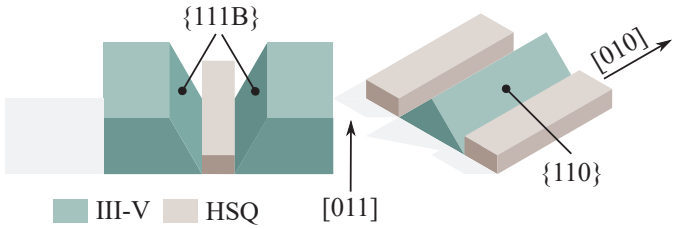

Figure 3.1: Depending on alignment of HSQ growth mask in [011] and [010], different facets of the semiconductor is obtained, {111}B or {110} with an angle of 54.7° and 45° towards the top {100} facet respectively.

been used for the selective area growth in this thesis. Depending on the alignment of the SiO_2 growth mask, semiconductor structures bound by {110} and {111} side walls can be obtained which can be seen in figure 3.1. In figure 3.2, the positions of the atoms for four different kind of low order facets is illustrated, {100}, {110}, {111}A and {111}B planes. Each atom in the lattice, has four electrons to bind to neighboring atoms of the other atomic type. {100} facets are consisting of a single group of atoms, either group III or V, and there are two dangling bonds at the surface. Since the crystal is symmetric in this direction, there is no separation between A and B type. {110} planes have equal amount of group III and V atoms at the surface, and there is one dangling bond per atom. {111} planes are however different, as they can be either A or B, depending on if the surface is group III or V terminated respectively. Typically, the growth rate of {111} planes are slower than {100} due to fewer dangling bonds giving rise to an increased diffusion length of ad atoms, making it possible for atoms to diffuse to the (100) top facet during growth. Mask openings aligned in [011] directions give {111}B facets that are especially technologically important as these facets slope away from the growth mask, avoiding mask overgrowth. [01-1] aligned mask openings give {111}A facets that are typically less stable than {111}B facets and grow faster in MOVPE growth which typically leads to upward facing {111}A facets and simultaneously downward facing {111}B facets, overgrowing the growth mask. This effect can also be beneficial, although not used in this thesis, if self-aligned spacer schemes is to be employed, although it requires very careful planning of the thicknesses of epitaxial layers and mask layers. The reason for these growth rates is linked to the fact that MOVPE is usually growth with high V-III ratios, where we have a surplus of group V atoms at the surface, and the growth rate is limited by the supply of group III atoms.

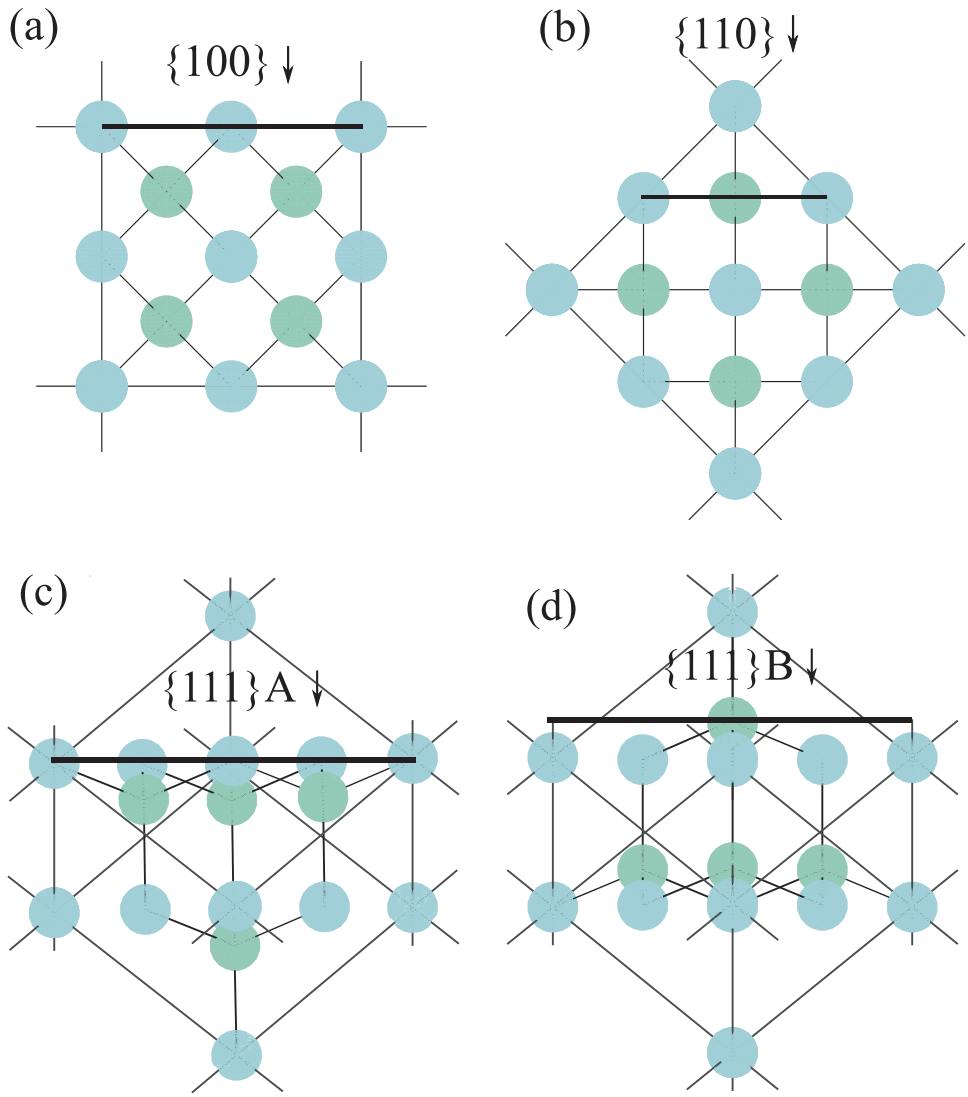

Figure 3.2: Unit cube of zincblende atomic structure where each mentioned plane is pointing upwards. The lines between blue atoms outlines the unit cube, and the lines between blue and green atoms indicate atomic bonds. (a) {100} plane consists of a single atom type, (b){110} plane consist of equal amount of group III and V, (c) {111}A and (d) {111}B plane is group III or V terminated respectively.

When a layer of group V atoms has been grown at the {111} facet, on a {111}A facet, there are three dangling bonds per atom attracting group III atoms to the growth site, while for a {111}B facet, there is only one dangling bond available. Similarly, the etch rate of {111}A facets are typically slower due to that the group V atoms sitting just below the surface are pulling the electrons away from the surface, making it harder to form redox pairs. The anisotropy of wet-etching is especially noticeable when etching InP with HCl as {211} etch stop facets can stop the etching if careful attention is not taken.

4 RF transistors

In this section, the main competitors to high speed nanowire MOSFETs for RF applications are highlighted and the important aspect of spacers are discussed in detail.

4.1 HEMTs

The high-electron-mobility transistor was invented in 1979 [45].The device architecture utilizes the high-electron mobility of buried III-V channels, with wide band gap semiconductors acting as the insulating layer between the gate and the channel. This is based on the Schottky contact between the semiconductor and the gate metal, and the gate overdrive voltage is therefore often limited to maximum 0.5 V, to avoid too high gate currents. Metamorphic buffers is commonly used to allow for different lattice constant in channel and substrate. Narrow band-gap HEMTs is a mature technology that has shown excellent high-frequency performance and gain at 1 THz was achieved already in 2007 [46]. But the performance have typically not improved over the last years, mainly due to that scaling of the transistors has led to increased parasitic capacitance compared to intrinsic capacitance and increased gate leakage. The transconductance has settled around 3 mS/μm, while the parasitic capacitances is hard to lower as many device schemes already employ modulation doping and recessed air-spacers.

4.2 MOSHEMTs

The saturation of HEMT performance at scaled dimensions have started the research of MOSHEMTs. The idea is to take all the knowledge from the HEMT devices, but thinning the semiconductor barrier and applying a thin oxide layer at the top, thereby

increasing the capacitive gate coupling and reducing the gate leakage. However, this approach is not quite as straight forward as it may seem. The inclusion of high-k inside the air-spacers will increase the parasitic capacitances of the device. The III-V MOS interface needs to be of very good quality not to lower the electron mobility, and to worsen the reliability of the devices. Another aspect is that the ALD of high-k oxide is typically performed above 200 °C, making it necessary to replace the initial organic resist that was used as a mask for the etching of gate openings.

4.3 Planar RF CMOS

Since the digital silicon CMOS devices have constantly improved over the years, also considerable efforts have been invested in adjusting the devices for analog applications. The major drawbacks of silicon RF devices are the lower electron mobility, making long spacer regions too resistive, and the high density of states, making the intrinsic gate capacitance large. Silicon does not have as good material candidates that are lattice matched for use in wide-band gap modulation doped schemes and barriers for HEMT type devices. Another constraint is the CMOS processing flows, where all contacts are sitting extremely tight, effectively increasing the parasitic capacitances, and reducing the high-frequency gain. Lift-off is also seen as incompatible with the silicon industry, why T-gate schemes is much more complicated to achieve, and high gate resistance for small nodes and narrow gate lengths is a big challenge for high power gain. Although all of these constrains exist, planar silicon transistors has still been able to deliver good RF performance with f_T of 445 GHz in the 32 nm node already in 2010[47].

4.4 FDSOI

FDSOI is a development of planar silicon transistor technology where the channel is sitting directly on top of a buried oxide. It has the advantage of lower parasitic capacitance, and a less complicated process scheme than FinFETs, with a smaller mask cost. The threshold voltage can also be tuned, making the same transistor suitable for various applications. RF FDSOI is especially important since the parasitic capacitance to the underlying silicon substrate can be reduced. The RF modes in the substrate can also be suppressed with the oxide box underneath the channel. So far, the supply of SOI chips has been a bottle neck as the IP-rights owner

Soitech is ramping up its production, going from 200 mm wafers to 300 mm wafers, something that should improve the RF performance of the analog devices. Global foundries have reported f_T and f_{max} of 375 and 290 GHz respectively for their 22 nm technology [48].

4.5 RF FinFETs

The main advantages of RF FinFETs compared to conventional CMOS, FDSOI and HEMT devices are the improved electrostatic control originating from the three-dimensional gate structure. This leads to a very low output conductance and a high voltage gain $A_v = g_m/g_d$, beneficial for RF applications. The devices also have very low drain induced barrier lowering, making RF modelling easier as drain bias has a reduced effect on off-state. The advantages over FDSOI is especially in terms of higher voltage gain but the increased parasitic capacitance in the areas between the fins will have a large negative impact. The width dependence of RF FinFETs is not as easy to model as for conventional planar devices, due to that the gate resistance has a large vertical component along the fins, making the gate resistance nonlinear in width dependence. Typically, peak $f_{\max}$ occurs at very narrow device widths, approximately 10 fins, which is small for analog applications [49]. Intel, Samsung, Globalfoundries and TSMC have all shown RF performance of silicon FinFETs. Samsung has demonstrated 14 nm RF CMOS with FinFETs capable of f_T of 252 GHz at a low gate overdrive of 0.2 V [50]. Globalfoundries has shown that their 14 nm FinFET technology outperforms their 28 nm planar technology in both DC and RF metrics due to increased transconductance [51]. An interesting effect of the high aspect ratio of the fins with a tight pitch is that the effective gate width (the gated circumference of the fin) often is larger than the physical width of the gate itself. This means that current lost due to spacing between fins can be compensated by the height of the fins, making the fin height and pitch important parameter for RF optimization. In order to mitigate short-channel-effects in scaled devices, higher and thinner fins have typically been used. But due to surface scattering, mobility quickly degrades, and fins narrower than 5 nm are likely to be dominated by the surface scattering, making scaling beyond 5 nm node challenging.

4.6 RF Nanowire FETs

The next generation CMOS devices to extend the scaling path to smaller nodes is believed to be the nanowire FETs, also called nanosheets. The benefit of nanowire FETs is that the gate can have an even better electrostatic control of the channel potential than FinFETs, due to that the gate can be made gate-all-around. This gives increased resilience against short-channel effects, and scaling to even shorter gate-lengths with healthy transistor performance can be made. For digital applications both vertical nanowires and lateral nanowires are of interest for pitch reduction and increased drive currents. The possibility to vertically stack lateral nanowires enables increasing currents for high performance without increasing the area of the chip, giving a large benefit over FinFET technology. However, the largest benefit of nanowire FETs is also what makes them most challenging from a RF perspective; namely the increased capacitances, both intrinsic and extrinsic. Therefore, nanowires horizontally stacked instead of vertically can be a trade-off for reduced capacitance and gate resistance in an RF adopted scheme. Spacer deposition is also an aspect that will need to be optimized for the technology to be a viable option in RF applications. Nanowire MOSFETs for digital applications have been shown by most major manufacturers [52, 53], but the RF publications has so far been made by different universities.

4.7 Spacers

Spacers are a very important part of high-performance MOSFETs for both logic and analog applications. For logic devices, the spacers can be employed to induce strain in the channel material, but it is also important for avoiding short-circuits in the devices and to reduce the capacitance between connections in order to have a low power delay product. For high speed analog applications, it is especially important for reduction of gate capacitances, to achieve a high gain at high frequencies, but also as passivation to ensure a good reliability in the devices. For a parallel-plate capacitor, the capacitance is proportional to the area of the plates A and the dielectric constant of the spacer material κ, and inversely proportional to the distance between the plates d.

$$C = \kappa \epsilon_o \frac{A}{d} \tag{4.1}$$

In general, employing a spacer between the gate and the drain and source contacts, effectively creates a larger separation between contacts. This means that the capacitance will go down but the transistor resistance will also increase, especially if the area underneath the spacer is undoped [54]. This is a delicate balance and a trade-off that needs to be perfectly implemented in order not to deteriorate the device performance. One way to circumvent a large increase of resistance when implementing a spacer is to use modulation doped layers. This means that a wide band gap semiconductor on a narrow band gap channel is doped. The free charge carriers generated from the doping will leave static ionized donors, but the carriers themselves will fall into the channel of the narrow band gap material, giving rise to smaller capacitance in the depleted doped layer and larger electric currents in the channel itself.

When choosing suitable spacer material, several considerations needs to be taken into account. The optimal spacer material should have a low dielectric constant, low leakage currents, withstand high temperatures, high-etch resistance towards process important chemicals and a good structural integrity [55]. It should preferably also be able to be removed without damaging surrounding materials. For passivating layers, good adhesion, resistant to moisture penetration and low stress is also favorable qualities. In table 4.1 dielectric constant of a few spacer material and high-k oxides are shown.

Table 4.1: Dielectric constant for a few important oxides and spacer materials.

Material	$\boldsymbol{\kappa}$
BCB	2.7
SiO_2	3.9
Si_3N_4	7
Al_2O_3	9
HFO_2	25

4.7.1 Silicon oxide spacers

The most common interlayer dielectric material that have been used since the beginning of spacer technology, is silicon oxide which is thermally stable up to very high temperatures [56]. Silicon oxide processing is very mature in the CMOS technology platforms, and can easily be thinned down with chemical mechanical polishing (CMP). It has a very good structural integrity and can have a low surface roughness. The drawback is that the dielectric constant is not that low, and that removal of silicon oxide with buffered oxide etch (BOE) can simultaneously remove high-k gate oxide material. Deposition methods range from PECVD, evaporation and ALD. EBL exposure of HSQ resist also forms silicon-oxide like structures with possible low dielectric constant due to the hydrogen content in the film [57]. The thickness can be controlled with dilution, spin-speed and exposure dose.

4.7.2 Silicon nitride spacers

Silicon nitride is commonly used as spacer between gate and source drain contacts to lower the parasitic gate capacitance. Especially for ALD of SiN, the possibility to finely control very narrow spacer regions has been realized [58]. SiN has also been used as passivation in HEMTs and as a simultaneous dry-mask for gate openings, due to the possibility of very precise dry-etching[59]. It is also good at mitigating moisture and can be deposited with a moderate stress level. One important parameter of SiN deposition is the amount of hydrogen in the film. If the SiN should be able to withstand BOE etches, the hydrogen content needs to be very low, as the etch rate increases exponentially with increasing hydrogen content [60].

4.7.3 Air spacers

The theoretically best spacer is the air or vacuum spacer. The main benefit is the low dielectric constant, making very low capacitance schemes possible, which has been utilized in the recessed spacer area of HEMTs and as gate encapsulations [61, 62]. However, implementing air spacers is difficult, and not something that is common in CMOS technology. Air-spacers is typically created by selective etching of a sacrificial layer, with a different material above. The drawback of the approach is that it sets physical constraints on the materials above, as there is a risk for collapsing structures. If the air-pockets are not sealed, the performance in front-end-of-line (FEOL) and back-end-of-line (BEOL) can vary drastically, if the air-pockets are filled in BEOL with the used interlayer dielectric.

5 Lateral nanowire transistor fabrication

The transistor process used in this work, is a replacement metal gate – high k scheme. This means that the channel material is first processed, then a sacrificial gate is exposed where the real gate will later be placed. This allows for the high-k and gate metal deposition to take place late in the transistor process, assuring a high-quality MOS interface. In this section, some of the most important process steps are described, although the order of the steps can vary between device generations.

5.1 Selective area growth and resist masking

To avoid any effect of parasitic substrate transistors, it is important that the substrate conducts as little current as possible. Since the lateral nanowire transistors are fabricated directly on the substrate, semi-insulating Fe doped InP substrates are used which is lattice matched to $In_{0.53}Ga_{0.47}As$ and more Indium rich InGaAs can also be grown with a certain degree of strain in the film. For selective area growth, a growth mask consisting of SiO or Si_3N_4 is most common [63]. For the selective area growth of InGaAs nanowires in this thesis, the growth mask used is hydrogen silsesquioxane (HSQ) resist that has been exposed and developed by tetramethylammonium hydroxide (TMAH), which makes the HSQ form into a SiO_x-like material. For RF compatible layout, the HSQ process has been optimized for HSQ adhesion, small line edge roughness and narrow HSQ lines in order to increase the nanowire density. The adhesion to InP substrates is known to be poor for HSQ resist, while for silicon it is generally higher. Due to this, the HSQ resist is baked at 200 °C to make sure that there is no loss of lines during the development phase. Unfortunately, this leads to less contrast during the exposure. To reduce the line width, the HSQ is diluted to 1.5 % and spun to a thickness of approximately 20 nm in order to reduce the effect of backscattering during EBL exposure [64]. The HSQ exposure is made with single pixel lines where each line is exposed several

times after each other to reduce the effect of shot noise in the electron beam [65]. To optimize the line edge roughness, which transfers into nanowire roughness, we develop the exposed areas at 40 °C, as higher development temperatures generally increases HSQ contrast [66].

To remove native oxides present at the InP surface, the sample is annealed at high temperature in the MOCVD chamber. The nanowire growth itself is initiated by growth of a very thin InP buffer, followed by growth of intrinsic $In_{0.63}Ga_{0.37}As$ layer at a growth temperature between 500 °C and 600 °C. Due to interactions with the HSQ mask, the nanowire layer becomes more indium rich compared to the planar growth [67]. We have seen from Hall measurements that the growth at 500 °C with no intentional doping yielded a carrier concentration at around 1e19 cm^{-3} [68]. Increasing the growth temperature to 600 °C decreased the background doping by an order of magnitude. However, problems with poor off-state have arisen occasionally, and attempts to reduce the conductance in the InP wafer and to improve the nanowire quality is under investigation, for instance by improving the switching between gas phases during growth, and optimization of pre-cleaning steps before MOVPE growth.

5.2 Regrowth of highly doped contacts

Next the growth mask is removed, and a HSQ dummy-gate is exposed [69]. The dummy gates sets the separation between the highly doped contact regions and effectively sets the gate length of the device. This makes it possible to vary the gate length across a sample with little extra effort. Generally, the contact layer is composed of approximately 30 nm thick Sn doped InGaAs and with or without sacrificial intrinsic InP spacer layer, both grown at 500 °C.

5.3 Mesa etching

In order to avoid short circuits between different parts of the transistor that should be isolated from one another, it is common to perform device isolation etching. The isolation mask for the wet etching of mesa-structures, has either been EBL defined HSQ or UV defined S1813 resist. The benefit of EBL-defined mesa is that it is easy to set an exact width of the device and the alignment accuracy is high. The big

drawback of EBL defined HSQ mask is the writing time and that HCl etching can compromise the adhesion of the mask to the substrate. UV-masks, on the contrary, has relatively poor alignment accuracy, but an improved adhesion. Throughout this work, the InGaAs layers have been wet etched with H_3PO_4:H_2O2:H_2O (1:1:25) and InP layers with HCl:H_2O (1:1). The wafer tends to change color for every layer of the semiconductor stack that is etched away, making it easier to ensure correct etching times. The etch selectivity is also close to 100% for both acid mixtures, allowing for over etching without damaging the layers below. During the switching of gases between InP growth and InGaAs, thin layers of $In_xGa_{1-x}As_yP_{1-y}$ can arise, that potentially is harder to remove with the two etch chemistries.

5.4 Source and drain metallization

In this work, source and drain metals most commonly used are Ti/Pd/Au as it has been shown to give an ohmic contact with low contact resistivity to the underlying InGaAs contact layer [70]**.** The thin titanium layer is known to create a good adhesion to III-V materials, the palladium acts as a barrier for gold diffusion in case of annealing of the device, and gold has a low resistance, limiting parasitic resistances to the device. In figure 5.1, the contact resistivity as a function of length of the n+ contact layer is shown for a 7 μm wide mesa. The intersection with the y-axis represents the contact resistance including probe resistance of approximately 10 Ω.

5.5 Insulating gate oxide and gate contact

In order to passivate the dangling bonds on the InGaAs surface, the sample is put into an ammonium sulfide mixture for 20 minutes just before ALD deposition. The purpose is to reduce the density of interface traps otherwise present in the oxide – semiconductor interface. The ALD process is initialized with several cycles of aluminum pulsing which is known to have a self-cleaning effect, removing the native oxide present at the surface [10]. Next, a bilayer of Al_2O_3 and HfO_2 is deposited with an equivalent oxide thickness (EOT) off approximately 1 nm.

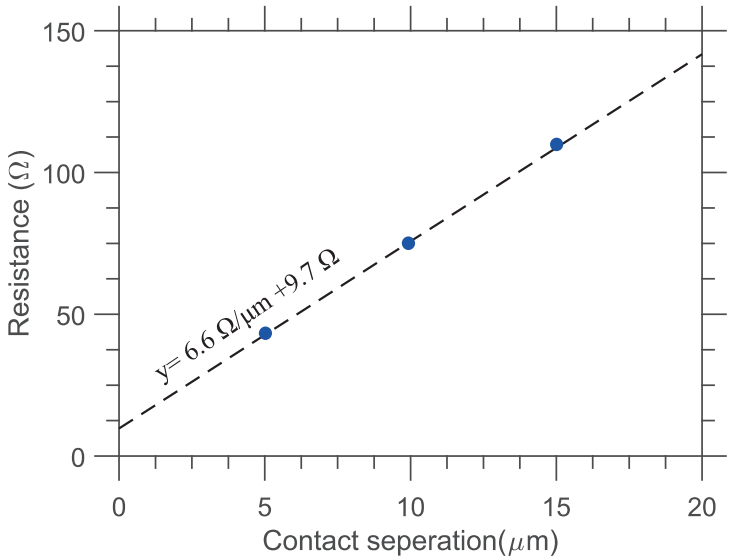

Figure 5.1: Transmission line measurement of highly doped n^+ contact layer with Ti/Pd/Au metal contacts, giving a sheet resistance of 50 **Ω**.

$$EOT = t_{high-k}\frac{k_{SiO2}}{k_{high-k}} \tag{5.1}$$

The bilayer is chosen due to that Al_2O_3 is known to create a low D_{it} with InGaAs, which should give a high electron mobility [71]. The thicker part of the oxide is HfO_2 due to the higher dielectric constant, increasing the gate to channel capacitance, giving an improved electrostatic control. Next PMMA resist is exposed where the gate contact will be. The gate is usually composed of Ti/Pd/Au or Ni/Pd/Au where the second has a better tolerance to BOE. We have also developed a bi-layer resist process where a more electron sensitive resist is deposited on top of PMMA resist. After development and exposure, the developed region will be wider in the top resist, effectively creating a T-shape in the evaporated metal. This allows for a bilayer based gate with the same resistance as the single layer resist gate, but with a reduced parasitic capacitance. An example of the T-gate can be seen in figure 5.2 on top of nanowires for illustrative purposes.

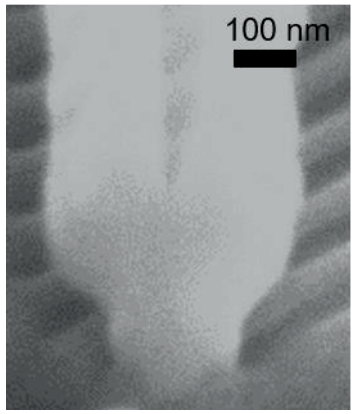

Figure 5.2: Cross-sectional SEM image of a T-gate made with the double layer resist and evaporation. In this case the gate is deposited on a nanowire device without regrown contacts for illustrative purposes.

5.6 High-frequency adapted processing schemes

During this thesis work, four different processing schemes have been used to fabricate spacers in high-frequency adopted MOSFET layouts. Besides spacer schemes, the major differences between our RF devices and digital devices, is that the RF devices consists of 2 gate fingers with many nanowires in parallel, whereas DC devices usually consists of a single nanowire. The layout of contacts have been optimized for small parasitic capacitances and to enable measurements with ground-signal-ground RF probes. Gate contacts in RF-schemes has generally been made with a large cross-section for low gate resistance, but also with T-gate shape to keep parasitic gate capacitances low. Schematic images of generation I, II, III and IV RF devices can be seen in figure 5.3. Due to that the nanowires are rotated 45° compared to the gate contact, the nanowire shape can be seen in the cross-section looking into the gate contact. Electrical characterization of each generation can be seen in section 6.3.

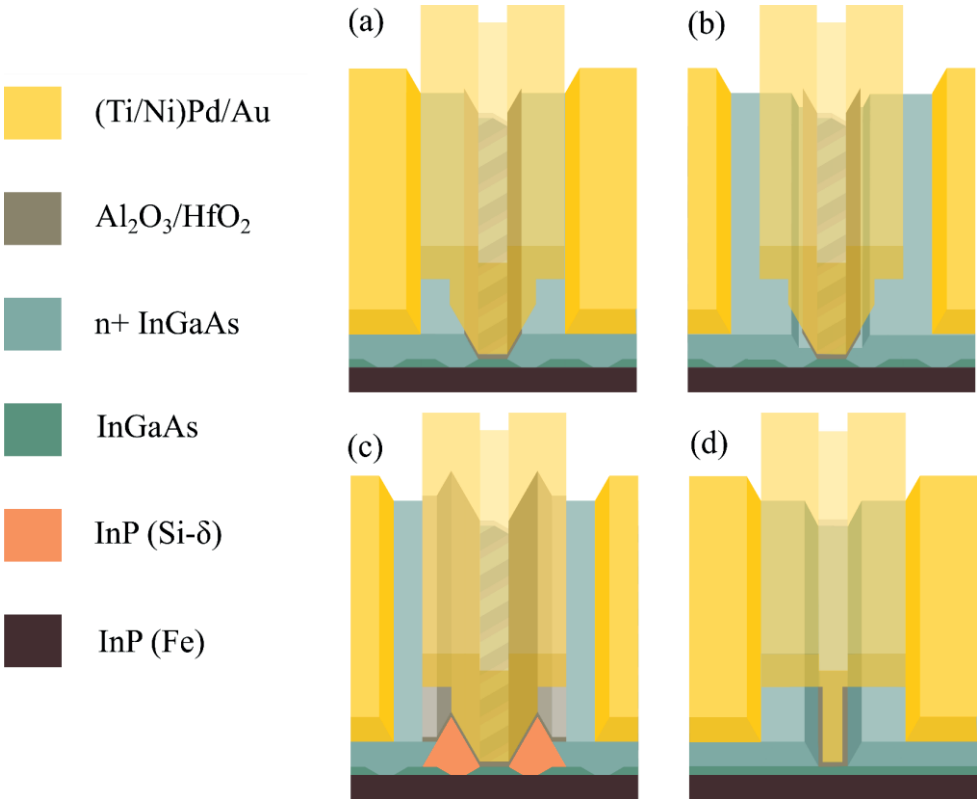

Figure 5.3: Schematic images of generation I (a), II (b), III (c) and IV (d) RF MOSFETs. Generation I with partial air-spacers, generation II with an InGaAs n^+ ledge, generation III with modulation doped InP Λ-ridge spacers and generation IV with self-aligned air-spacers.

5.6.1 Generation I

Generation I of our device scheme employed a sacrificial InP spacer, grown on top of the highly doped n+ contacts in the same MOVPE step. The benefits were that the InP could be selectively etched away after gate deposition, leaving an air-spacer between the T-gate and the top surface of the InGaAs contact area. However, there was still an overlap between the gate and the {111}B surface of the InGaAs contacts, yielding a capacitance that was limiting the high-frequency performance[72]. SEM image of the nanowires and contact layer as well as cross-sectional schematic image can be seen in figure 5.4.

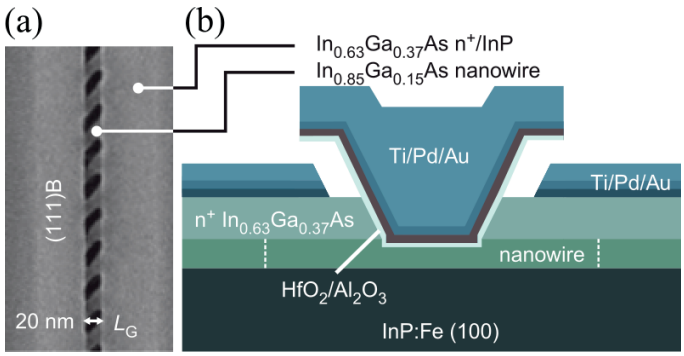

Figure 5.4: SEM image and schematic image of a generation I device.

5.6.2 Generation II

In generation II devices, we investigated a scheme to employ highly doped ledges and air-spacers, to try to create a device with low capacitance and low access resistance. After growth of n+ contacts, the width of the dummy gate was thinned down by diluted HF (generation II A), or the dummy gate was replaced with a narrower dummy gate (generation II B). Next, a thin n+ InGaAs ledge was grown, followed by sacrificial InP. The benefit of the first approach was that the spacer alignment was self-aligned, and not limited by EBL alignment. However, one of the drawbacks, which was improved by the second approach, was the inability to set different spacer width across the sample. Another drawback of the first approach was that the yield was far from ideal. Narrow dummy gates could collapse when trying to do longer back-etching for long spacer lengths and sometimes the ledge could grow in between the nanowires in the channel due to insufficient HSQ adhesion after the HF etch. The second approach however, was limited by the alignment of our EBL equipment, giving poor yield. The benefit of generation II devices were that an air-spacer could be introduced, while still having low access resistance due to the n+ InGaAs ledge. However, since the ledges were very narrow, it was often difficult to assess whether sufficient etching of the sacrificial InP was performed to really give an air-spacer. Improvements to this scheme would be to use modulation doped InP in the spacer region, but it was incompatible with the sacrificial InP removal. An important parameter to optimize in this type of transistor scheme, is the thickness of the n+ InGaAs ledge. Simulations of the capacitance as a function of ledge length and height is shown in figure 5.5 (a) for a planar channel [73]. If the ledge is made too thick, it resembles the standard n+ contact more than a ledge, replicating the layout of generation I devices with too high capacitance. If

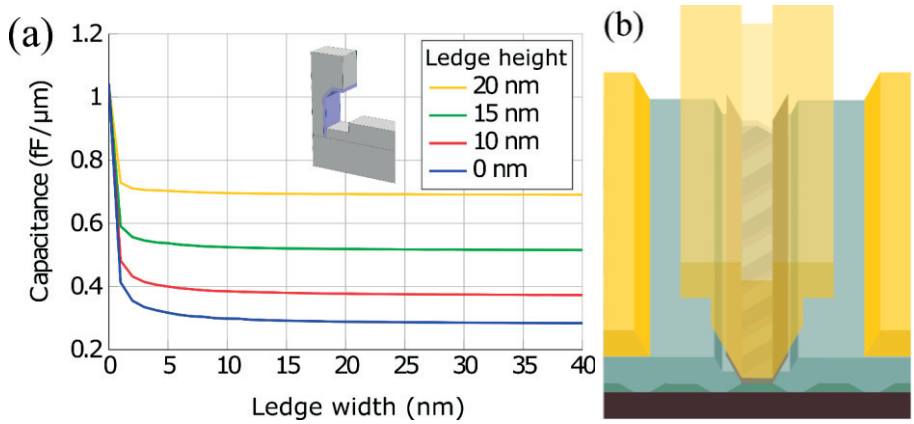

Figure 5.5: (a) Comsol modelling of capacitances for device generation II, where the thickness and length of InGaAs ledge is varied. (b) Schematic image of a generation II RF device with an InGaAs ledge and air spacer.

too thin, the access resistance would be similar to ungated nanowire spacers, and access resistance would degrade.

5.6.3 Generation III

In generation III, a novel Λ-ridge process was introduced, where we aimed at high spacer design flexibility and self-alignment with the implementation of modulation-doped InP spacers that the generation II devices did not have. After nanowire growth, a dummy gate was exposed while simultaneously masking the contact regions, just leaving a void in the growth mask that will form the Λ-ridge spacer. The HSQ exposure was followed by growth of intrinsic InP Λ-ridges with a Si-modulation doped layer sequence in the bottom, see figure 5.6 (a). Due to that the Λ-ridges were bound by {111}B facets with very slow InGaAs growth rates, the subsequent growth of n+ contacts would be self-aligned as long as the second HSQ dummy gate was aligned within the outer boundaries of the InP Λ-ridges. Due to the use of modulation doped spacer regions, a low access resistance while simultaneously low capacitances were achieved. The benefits of generation III devices were that the spacer lengths of the devices could be set independently over the substrate, the process scheme was close to self-aligned, relaxing the constraints on EBL alignment. The drawback is the three epitaxial steps as well as a bit too high sensitivity to dose variations in the Λ- ridge HSQ exposure step, making narrow spacer regions difficult. With generation III we showed that the performance of a

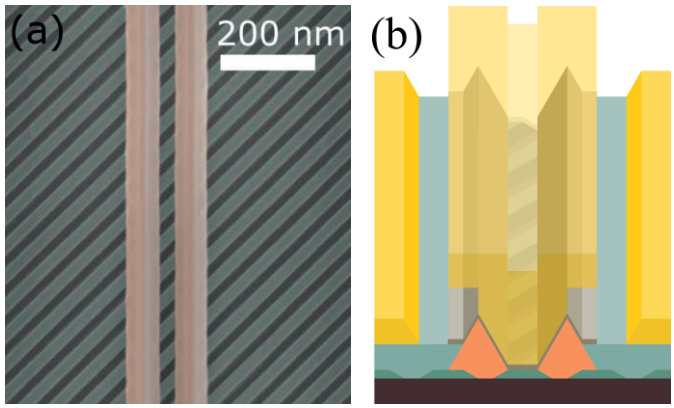

Figure 5.6: (a) False-colored SEM image after spacer growth and (b) schematic image of finalized transistor of a generation III RF device with a novel modulation doped InP Λ-ridge spacer region seen in orange and grown nanowires in green.

Λ-ridge device with large gate overlap could match that of a spacer less device with a gate that was aligned almost exactly at the edge of n+ contacts, something is difficult to achieve repeatedly[74].

5.6.4 Generation IV

In generation IV, we reinvented generation I devices with inspiration from RF-CMOS processing schemes. Due to lack of CMP equipment, alternative approaches were introduced. After unsatisfying tests with spacer materials as SiN, SiO and HSQ due to spacer loss during dummy-gate etching, a sacrificial spacer material was selected with high etch selectivity between the spacer, dummy-gate, gate metal and III-V material. This allowed for both dummy-gate removal and spacer removal without damaging surrounding structures. Due to problems with HSQ resist exposure and HSQ delivery at the time, generation IV has so far only been implemented on planar InGaAs devices, but there is nothing foreseeable that should inhibit the process scheme to be implemented on nanowire MOSFETs as well.

After growth of the highly doped contact regions, the dummy-gate is left in place, instead of being removed as it was in generation I devices. The dummy-gate will act as a template for the sacrificial spacer placement to come. After PECVD deposition of the sacrificial spacer, the dummy gate will be buried, and needs to be accessed in order for the gate to be placed at the channel in later steps. In CMOS processing, the dummy-gate is accessed with CMP but we have instead developed a scheme

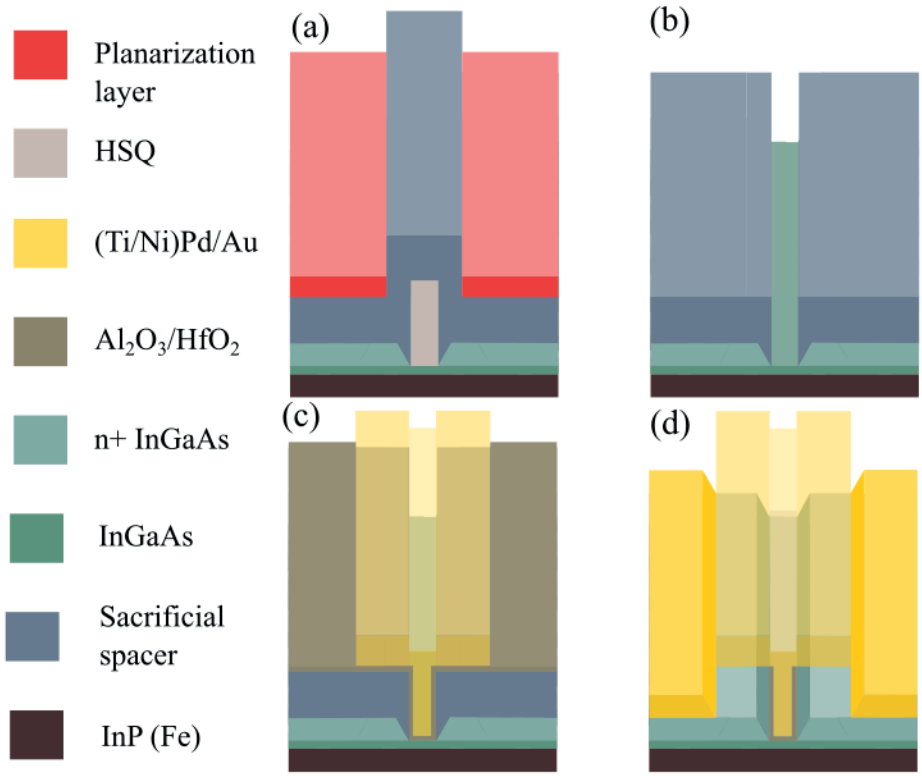

Figure 5.7: Schematic images of generation IV RF device with air spacer and a gate not overlapping the {111}B facet of the InGaAs n+ contact. (a) Deposition of spacer with the HSQ dummy gate as mask with a thinned down planarization layer. (b) Dry-etching of spacer on top of dummy gate and removal of dummy gate and planarization layer. (c) ALD of high-k oxide and metal evaporation. (d) Removal of oxide, sacrificial spacer and deposition of source drain contacts.

where an organic planarization layer is spin coated and then thinned down to reveal the top of the dummy gate with spacer material on top, see figure 5.7(a). The spacer material on top of the dummy gate is then dry etched away until the top of the dummy gate itself is visible. The planarization layer is removed, and the dummy gate can be etched away by BOE, figure 5.7 (b). After gate stack deposition and lift-off, figure 5.7 (c), the high-k oxide outside the gate is removed and the sacrificial spacer material can be etched away, leaving an air-spacer between the gate and the n+ InGaAs contacts. The T-gate can then also be used as a shadow mask for very tight source-drain spacing, see figure 5.7 (d).

Table 5.1: Simplified process-flow of generation I, IIB, III and IV RF devices.

Process steps	Gen I	Gen IIB	Gen III	Gen IV
1st EBL - nanowire	X	X	X	-
1st MOCVD - channel	X	X	X	X
2nd EBL – dummy gate	X	Wider	+ Spacer area	X
2nd MOCVD	InGaAs + InP	InGaAs	InP	InGaAs
Dummy gate removal	X	X	X	-
3rd EBL – dummy gate	-	Narrower	X	-
3rd MOCVD	-	InGaAs ledge + InP	InGaAs	-
Spacer deposition	-	-	-	X
Dummy gate removal	-	X	X	X
High-k and gate	X	X	X	X
Spacer etching	X	X	-	X
Mesa etching	X	X	X	X
Source, drain, pad	X	X	X	X

This scheme has utilized all benefits of generation I devices, that is self-aligned gate, low access-resistance, air spacer, but with the additional improvement of a gate that is separated from the {111}B facet of the contact layer for smaller parasitic capacitance.

The high yield of generation IV devices, together with the self-alignment of the spacer scheme, allowed us to do the largest device scaling study so far of our III-V MOSFETs. With both gate length and width variation, we could quantify the intrinsic and parasitic properties of our devices, which is beneficial for future circuit implementations.

5.6.5 Summary of RF process flows

The four RF device generations above share a lot of similarities, but also differ in a few key aspects. Table 5.1 compares the process flow for generation I-IV RF devices, with the main processing steps highlighted. Different generations vary in the amount of MOCVD steps and EBL steps, depending on the process complexity.

6 III-V device characterization

In this thesis, we have performed electrical characterization of III-V nanowires and MOSFET devices aimed at low-power applications as well as analog RF applications, showing the very high potential of the material system for future electrical circuits.

6.1 Hall measurements

In this thesis, two papers regarding Hall measurement on nanowires are included, paper I and paper VI. Hall measurements on small nanostructures has been challenging to perform due to the high-accuracy alignment required for measuring on nanowire devices. Vapor-liquid-solid (VLS) growth of vertical nanowires, as well as the fine-tuning of growth parameters with complementary Hall measurements is important both for optoectronic devices as well as vertical nanowire transistors, both being thoroughly researched at Lund University. In paper VI, we characterized vertical InP nanowires grown with VLS growth to see how far we could increase the Sn-doping in the nanowires while still ensuring a high nanowire quality, see figure 6.1 [75]. The analysis linked growth rates and doping incorporation in the nanowires, with a special emphasis on spatial resolution in the measurements, as Hall-contacts were fabricated on three separate locations along the nanowire. The measured carrier concentration for different TMIn flow during the MOVPE growth is shown in figure 6.1(b). There is a clear trend with increasing carrier concentration with lowered TMIn flow due to increased TESn/TMIn ratios, until the value saturates around 1e19 cm^{-3}. We observe that the nanowires grown with relatively higher TMIn flow has a decreasing growth rate at the top of the nanowires, most likely due to less In atoms diffusing along the nanowire to the top, where it incorporates into the gold-particle. This could also explain why the Hall measurements indicate a higher carrier concentration in the top for these TMIn flows, due to the possible reduced Indium supply along the wire, yielding an increased group IV-III ratio. Interestingly, the carrier concentration is reversed for

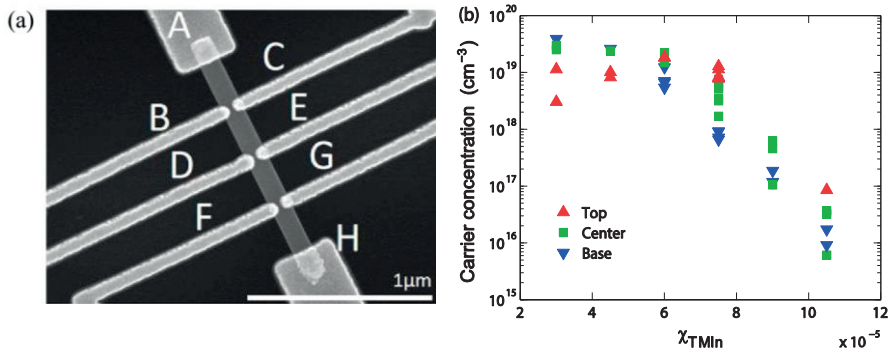

Figure 6.1: (a). SEM image of Hall contacts on a VLS grown Sn doped InP nanowire where the carrier concentration can be measured in pairs along the nanowire. (b) Carrier concentration as extracted from Hall-measurements for varied molar fraction of TMIn.

relatively lower carrier concentrations, where also the growth rate difference between bottom and top is less pronounced. One possibility is that the lowered TMIn flow has affected the diffusion lengths of dopants and In-adatoms, giving a decreased group IV-III ratio along the wire.

With the knowledge gained from Hall measurements in paper VI, in paper I, we revised the Hall-fabrication process to be compatible with selective-area-grown lateral nanowires, similar to those used in the transistor process in the rest of the papers [68]. Instead of metal contacts in direct contact with the nanowire, which is suitable for nanowires wider than 100 nm, the nanowires in this paper were grown in a Hall-bar structure, enabling Hall-measurements of nanowires with width as small as 50 nm. From the measurements we concluded that the carrier concentration in the nanowires were surprisingly high, around 1 x 10^{19} cm^{-3} as seen in figure 6.2, even though the nanowires are non-intentionally doped. We could see a slight decrease in carrier concentration with decreasing width, but more importantly, the effect of surface scattering increased significantly for narrower widths, clearly decreasing the mobility.

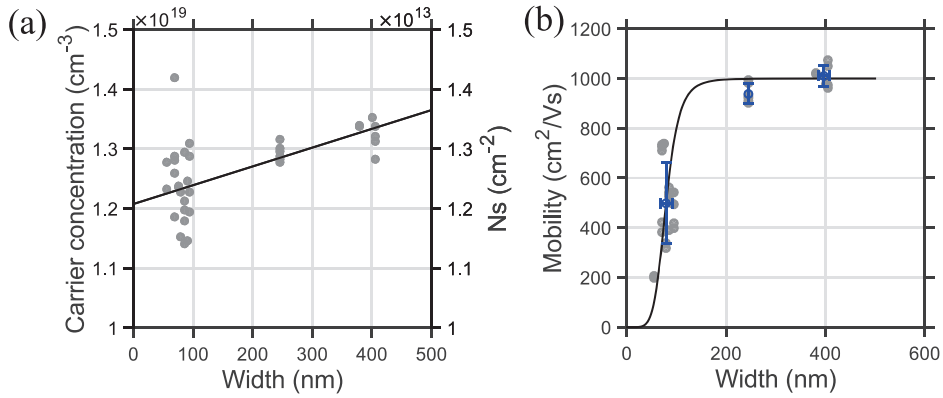

Figure 6.2: Carrier concentration (a) and mobility (b) as extracted from Hall bar structures made of selective area growth of InGaAs nanowires with varying width.

Due to the relatively high carrier concentration, we investigated the effect of growth temperature on carrier concentration for planar structures. We could see a large decrease in carrier concentration with increasing growth temperature, as well as increased mobility, see figure 6.3. This made us use an increased growth temperature of 600 °C for generation III and IV RF devices.

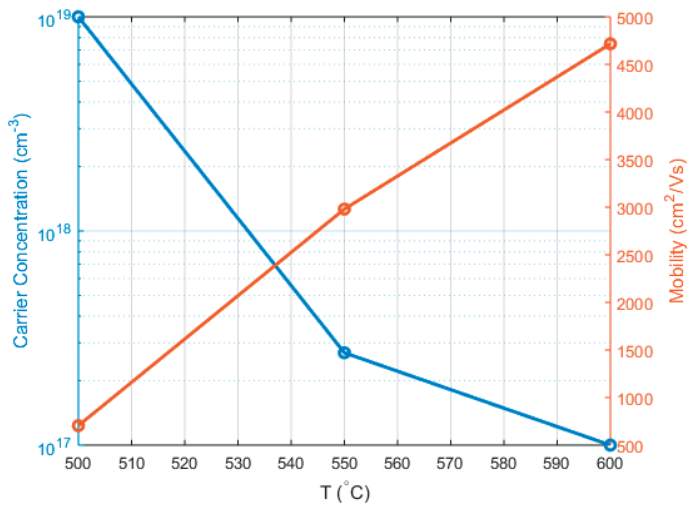

Figure 6.3: Carrier concentration and mobility from Hall measurements on planar InGaAs layers with varied temperature during MOVPE growth.

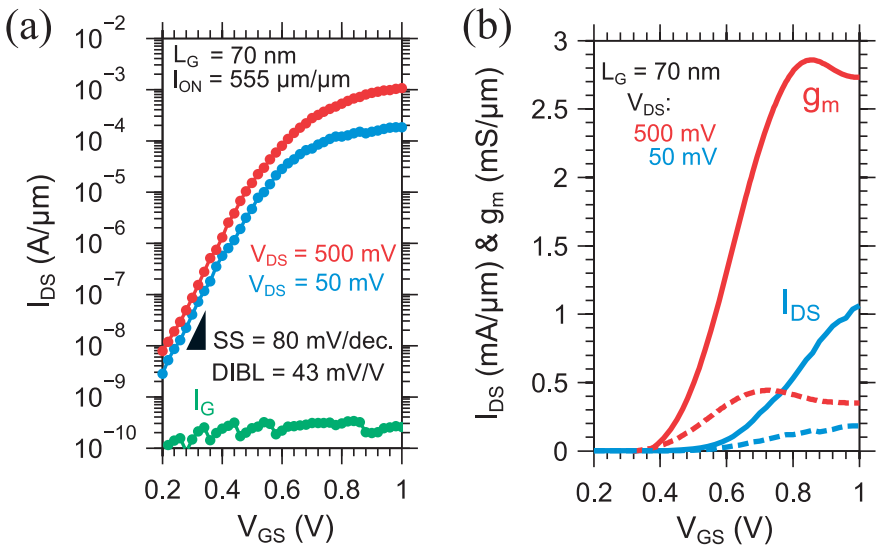

Figure 6.4: Off-state (a) and on-state (b) for VLSI adopted nanowire MOSFET with 555 µA/µm on current at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm from paper V.

6.2 III-V nanowire MOSFETs for low-power digital applications

III-V nanowires are interesting for logic applications due to the increased electron velocity in narrow band gap semiconductors and for the improved electrostatic control coming from the three dimensional gate structure. In paper V, we investigated DC performance of selective area grown indium rich $In_{0.85}Ga_{0.15}As$ single nanowire MOSFETs in tri-gate geometry [76]. For a fairly long gate length of 70 nm, the devices showed a high transconductance of 2.85 mS/µm, still maintaining a well performing off state with SS = 80 mV/decade, giving I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V which was record performance at the time, see figure 6.4. Another device with a better off-state had SS = 65 mV/decade and g_m = 2.65 mS/µm giving a high Q value of 40. Scaling of nanowire dimensions showed significant improvement in SS with decreasing nanowire width, while still maintaining a well performing off-state at the smallest gate length of 40 nm.

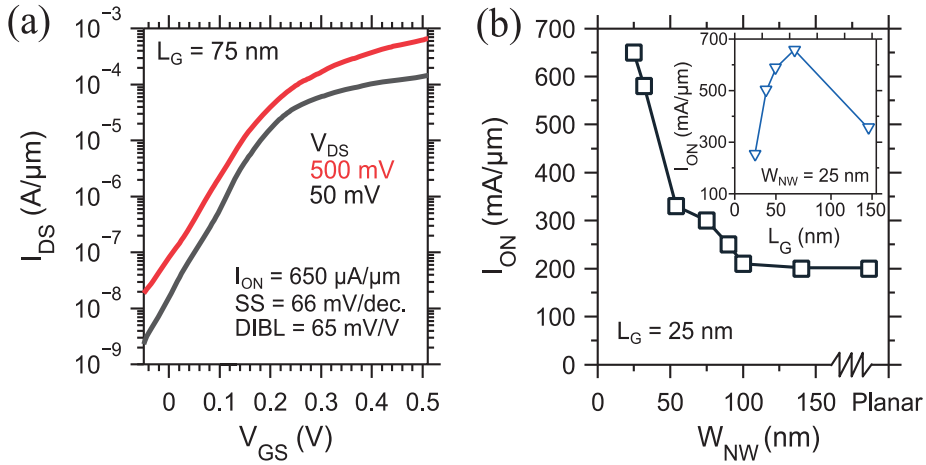

Figure 6.5: (a) Offstate of a VLSI adapted transistor in paper IV with sub threshold swing close to the thermal limit of 60 mV/decade and record I_{ON} . (b) Nanowire width influence on I_{ON} indicating the improved electrostatic control with reduced nanowire width.

In paper IV, we were able to improve the DC performance even further, simultaneously enabling g_m = 3 mS/µm and SS = 66 mV/decade, giving the highest reported I_{ON} to date at 650 µA/µm, see figure 6.5 (a) [77]. The optimum of I_{ON} is for narrow nanowire width and a gate length of 70 nm where the best slopes are obtained with a high transconductance still. This was achieved with an improved surface passivation scheme prior to ALD gate oxide deposition, lower EOT of the gate dielectric, and the inclusion of an InP pillar etch which allows the gate to give a better electrostatic control in the bottom edges of the nanowires.

6.3 MOSFETs for high-frequency applications

Building on our platform of digital nanowire transistors consisting of single nanowires, we have adjusted the transistor layouts for improved high-frequency performance, with hundreds of horizontally stacked nanowires with a tight pitch, including spacer schemes for low capacitances, and transistor layout suitable for RF measurements. We have also demonstrated the first noise measurements on our RF platform, as well as BEOL processing and initial circuit demonstrations. We have also varied the transistor dimensions, both gate length and gate width to quantify the intrinsic and parasitic performance of our devices.

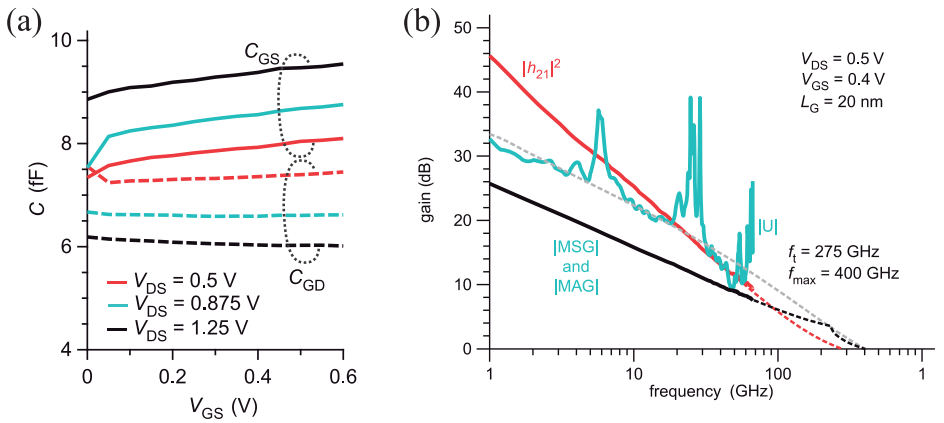

Figure 6.6: (a) Capacitance and (b) gain of generation I RF devices with a sacrificial InP spacer creating a seperation to the contact layer.

In paper III, generation I of our RF devices were published [72]. The devices consisted of 2 fingers with 100 nanowires per finger with a very short gate length of 20 nm. The devices had a partial air-spacer and self-aligned source-drain contacts, giving a low access resistance. The short gate-length and narrow nanowires also gave a low intrinsic capacitance, with a total gate capacitance C_{GG} = 1.10 fF/µm. High f_T and especially f_{max} was delivered, due to high transconductance and fairly low capacitances as seen in figure 6.6.

In order to try to improve the performance of generation I devices, generation II devices that was presented at the conference Compound Semiconductor week (paper VII, not included in the thesis) [78], had a highly doped ledge and attempt on airspacer with the aim of separating the gate from the {111}B facets of the n+ doped contact. Generation II A with a back-etched HSQ dummy gate, and 5 nm ledge length showed f_T of 180 GHz and f_{max} of 200 GHz where the gain plot is seen in figure 6.7 (b). The capacitances was unfortunately not decreased from generation I devices with C_{GG} = 1.2 fF/µm, figure 6.7 (a), most likely due to insufficient InP etch, wider nanowires and longer gate length. With the aim of lowering the capacitance, we developed generation II B devices, with 10 nm ledge length, aligned by EBL. The increased spacer length achieved a reduction of the capacitances to C_{GG} = 1.0 fF/µm in the on-state as seen in figure 6.7 (c) but due to worse transconductance than generation I, f_T and f_{max} remained at around 100 GHz.

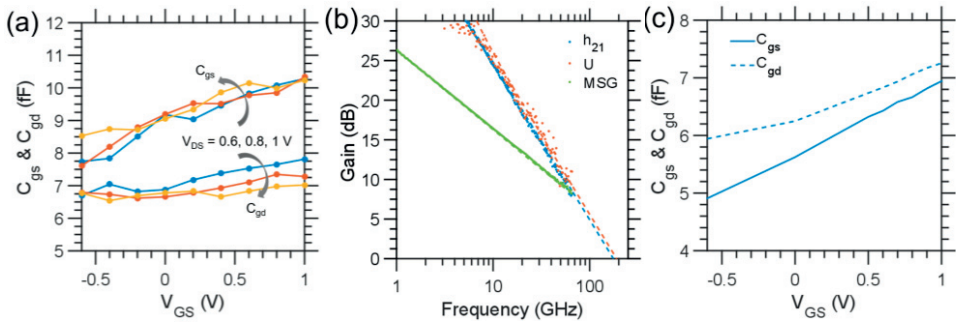

Figure 6.7: Capacitance of generation II A self-aligned 5 nm length n+ ledge device and gain. Capcitance of generation II B device with 10 nm n+ ledge EBL aligned, showing a drop in the measured capacitances.

Generation III-devices in paper II, was implemented with a novel approach on modulation doped InP spacers [74]. The devices were not dependent on InP-sacrificial layer etching which had been a limiting factor on yield and device variation in previous generations. The novel approach was inspired by work from Santa Barbara where an InAs MOSFET with InP spacer had shown high performance on planar structures with f_T of 357 GHz [79]. The introduction of novel Λ-ridge InP spacers in generation III devices eliminated the need for InP underneath the n^+ contacts, possibly lowering the access resistance compared to the processing scheme utilized in [79]. The influence of gate overlap capacitance was reduced compared to spacerless devices, as we have modeled in figure 6.8. The introduction of modulation doped layers could keep the access resistance fairly low even with the introduction of 80 nm spacer for a 40 nm gate length device. This lead to that the performance of devices with large spacer, and relaxed gate alignment requirements with a large gate overlap of 40 nm, could almost match performance of devices without a spacer with an EBL aligned gate with minimal overlap of approximately 5 nm, something that cannot be reproduced with a high accuracy in our university lab. The spacer scheme allowed for a small reduction of capacitances compared to generation I devices and matched generation IIB devices at C_{GG} = 1.0 fF/μm. However, due to relatively poor transconductance in both spacer less devices and devices with spacer f_T and f_{max} was 70 GHz and 100 GHz respectively.

Building on the platform developed in generation I devices together with spacer processing from CMOS compatible III-V FINFET devices [80], our generation IV devices had a completely self-aligned air-spacer scheme. Due to the self-aligned nature of the processing scheme, high yield of devices were achieved, and variations

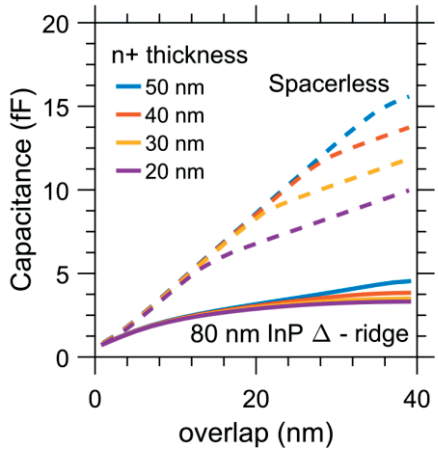

Figure 6.8: Modelled gate overlap capacitance for direct contact with n+ InGaAs contacts and with an 80 nm wide InP Λ-ridge spacer from generation III RF devices.

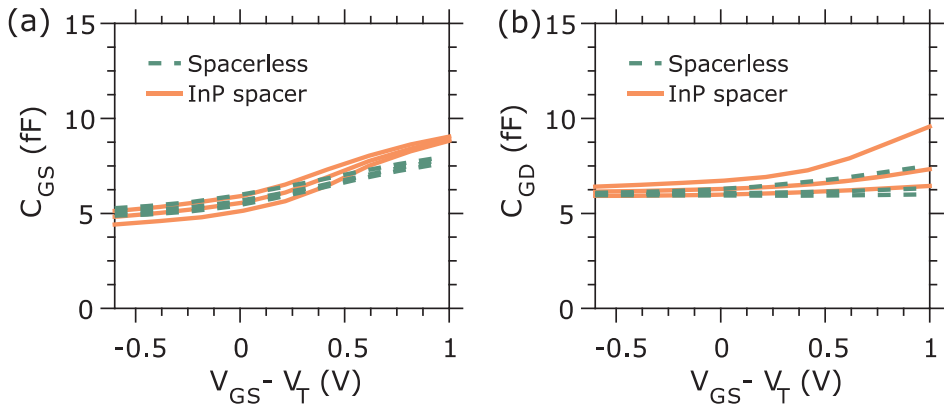

Figure 6.9: Experimental capacitances of 2 x 7 µm finger generation III devices with a self-alinged modulation doped processing scheme. Devices with InP spacer and a large gate overlap matches capacitances from a EBL demanding 5 nm gate overlap spacerless device.

in gate length and gate width enabled extraction of intrinsic and parasitic capacitances in a planar channel device. Due to problems with EBL exposure at our university lab, the devices were fabricated with a planar device channel, and source-drain contacts as well as pads were fabricated with UV lithography, with an alignment accuracy of the order of 2 µm. To be sure to actually align the devices correctly, the source drain metal had 2 µm extensions on each side outside the mesa

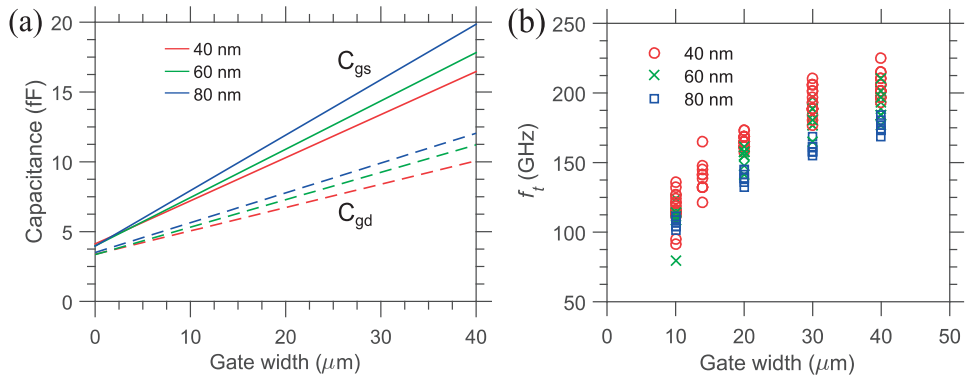

Figure 6.10: (a) Fitted capacitance from approximately 160 planar devices in the self-aligned generation IV device, with gate length in legend. Data from on-state at V_{GS} = 0.5 V and V_{DS} = 0.5V. (b) Influence of gate width and gate length on unity current gain frequency showing the improved transistor performance with increased gate width due to reduced influence of parasitic pad capacitances.

structure, adding a significant part to the parasitic capacitance. We also believe that the large separation between gate fingers of 24 µm has contributed to adding a long parallel plate capacitor between gate pad and drain contact of approximately 1-2 fF that especially reduces performance for narrow device widths. Even though the devices had increased parasitic capacitances due to UV exposures, the capacitances were the lowest measured so far in any of our device generations. 160 devices with different gate length and width were measured in RF, and the linear fitting of 40 nm gate length as a function of gate width gave C_{gd} = 0.17 fF/µm + 3.4 fF, C_{gs} =0.31 fF/µm + 4.1 fF and C_{gg} = 0.48 fF/µm + 7.5 fF. This highlights the large influence the pad capacitances have on especially small gate width device. Figure 6.10 (b) shows f_T dependence on gate length and width. The highest f_T was 225 GHz, measured for a 40 nm gate length, 2 x 20 µm finger device with C_{gg} = 0.62 fF/µm, comparable to high performance HEMTs [81]. The reason for increasing f_T with increasing gate width is the decreased influence of parasitic pad capacitance.

6.4 Benchmarking of RF performance

In this section, we benchmark the RF performance of our III-V MOSFETs for the most important high-frequency metrics against other competing technologies as III-V HEMTs, III-V MOSHEMTs, planar MOSFETs and FinFETs.

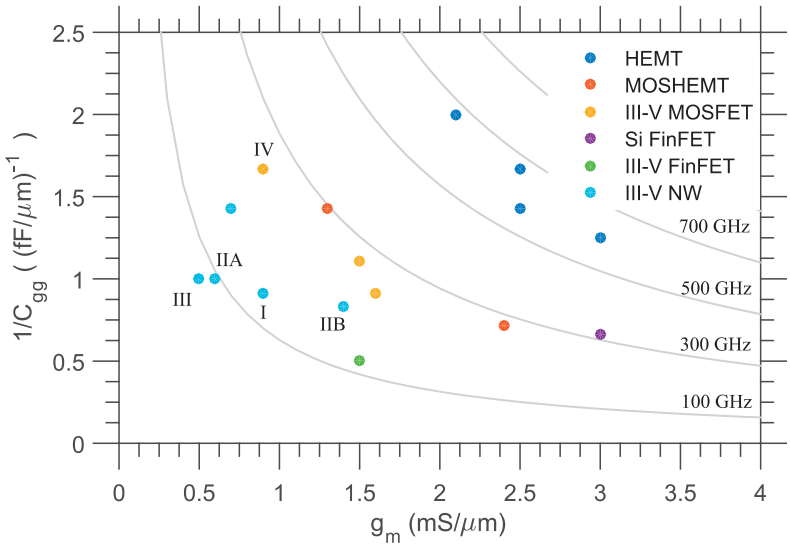

Figure 6.11: Total gate capacitance as a function of transconductance for different RF technologies, showing that both high transconductance and low capacitance is needed for high-performance at high frequencies. $f_T \approx \frac{g_m}{2\pi C_{gg}}$ is indicated in grey lines. Some variations between reported f_T and relationship to grey lines will occur depending on if reported g_m is the intrinsic or extrinsic value.

In table 6.1, information about technology, gate length, transconductance, total gate capacitance f_T and f_{max} as well as year published is presented. In some cases, the total gate capacitance is not written in the paper, therefore, it has been approximated from transconductance and f_T as $C_{gg} \approx \frac{g_m}{2\pi f_T}$. It is clear that still HEMT devices are the best in terms of high-frequency performance, but not much improvement has occurred over the last years. In RF CMOS, where logic technology is also available, Si FinFETs are competitive to planar architectures, mainly due to improved transconductance, however, capacitances and cost are limiting factors. In this work, single III-V nanowires have shown very high DC transconductance, and low-capacitance RF schemes have also been demonstrated. Still, both obtained at the same time is needed for both vertical and lateral nanowire MOSFET to be really competitive in RF domain. In figure 6.11, the inverse of C_{gg} is plotted against transconductance with the formula $f_T \approx \frac{g_m}{2\pi C_{gg}}$ shown in grey lines. It can be seen that generation I-III devices beats both the reference III-V FinFETs and Si FinFET in terms of capacitances, but the transconductance needs to be improved for higher f_T. Generation IV planar MOSFET is also very comparable with state of the art HEMT technologies in terms of capacitances, but again the transconductance must be increased to reach the performance of HEMT devices.

Table 6.1: RF performance of various high-speed transistor technologies, with metrics taken from papers. If C_{gg} not presented, an approximation from $C_{gg} \approx \frac{g_m}{2\pi f_T}$ has been used. Generation I-IV devices are normalized to gate width, and not gated circumference of nanowires to make for a better comparison of capacitances with planar technologies.

Technology	Year	L_g (nm)	g_m (mS/μm)	C_{gg} (fF/μm)	f_T (GHz)	f_{max} (GHz)	Ref
III-V HEMT	2008	35	2.5	0.7	556	-	[62]
III-V HEMT	2011	20	2.5	0.6	660	-	[82, 83]
III-V HEMT	2013	60	2.1	0.5	710	438	[83]
III-V HEMT	2015	25	3.0	0.8	610	1500	[84]
III-V MOSHEMT	2017	30	1.3	0.7	306	380	[85]
III-V MOSHEMT	2019	20	2.4	1.4	275	640	[12]
III-V MOSFET	2018	30	-	-	400	100	[86]
III-V MOSFET	2018	20	1.5	0.9	370	310	[87]
III-V MOSFET	2018	30	1.6	1.1	410	357	[79]
Bulk CMOS	2010	26	-	-	445	-	[47]
SOI	2012	32	-	-	430	400	[88]
FDSOI	2016	20-28	-	-	375	290	[48]
Si FinFET	2014	34	-	-	180	-	[89]
Si FinFET	2017	30	-	-	252	-	[50]
Si FinFET	2017	32	-	-	230	284	[49]
Si FinFET	2017	14	3.0	1.5	314	180	[51]
III-V FinFET	2018	20	1.5	2.0	120	60	[80]
III-V FinFET	2018	-	-	-	150	150	[87]
Vertical III-V NW	2014	150	0.7	0.7	141	155	[90]
III-V NW	2016	20	0.9	1.1	275	400	g. I[72]
III-V NW	2018	40	1.4	1.2	180	200	g. II[78]
III-V NW	2018	40	0.6	1.0	100	85	g. II[78]
III-V NW	2020	32	0.5	1.0	70	100	g. III[74]
III-V MOSFET	2020	40	0.9	0.6	225	130	g. IV

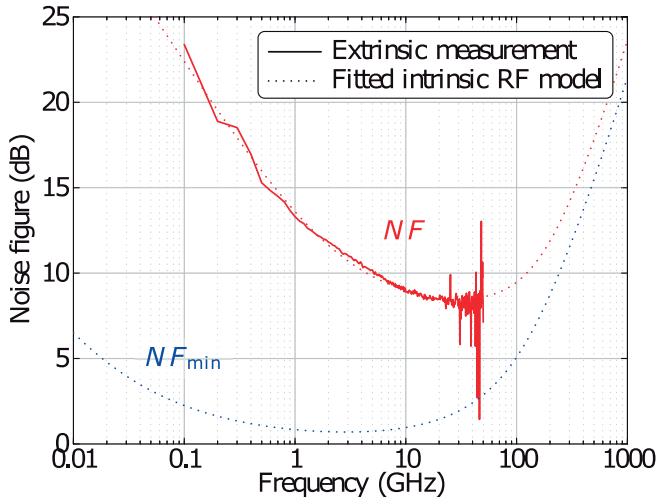

Figure 6.12: Measurements of the minimum noise figure for a nanowire transistor with 50 nm gate length and 2 x 7 µm gate width.

6.5 Initial circuit efforts

This section indicates a few highlights of initial circuit activities that the author has contributed to, although performed mainly by colleagues, on the lateral nanowire transistors. As part of the EU project Insight, the RF noise was measured for one of our transistors as can be seen in figure 6.12 [91]. Minimum noise figure was fitted to be approximately 5 dB at 94 GHz, with the lowest value of approximately 1 dB around 5 GHz. The technology lacked implementation of T-gate, why the gate resistance was high, limiting the noise performance.

After generation I devices, the development of FEOL transistors was combined with efforts in developing a low-temperature BCB based BEOL in-house, performed by colleagues in our research group. The influence of BEOL on the DC properties of our lateral nanowire MOSFETs to determine if transistor performance was deteriorated due to the increased amount of processing post transistor finalization [92]. It was concluded that no such negative effect could be seen, only drawback was slightly higher off-current as seen in figure 6.13. Actually, the transconductance increased slightly due to the annealing of the contacts.

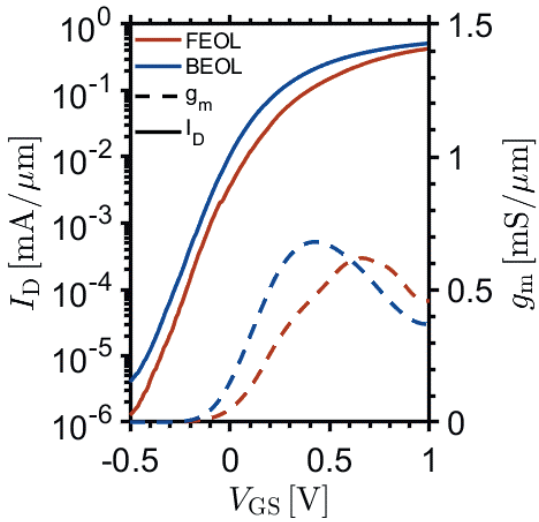

Figure 6.13: DC performance of a 2 finger, 200 parallell nanowire transistor before and after back-end-of-line processing.

In the BEOL, also matching networks were designed for the lateral nanowire transistor with the aim of achieving gain at 60 GHz. In figure 6.14, the S-parameters is plotted for a frequency range of 50 to 70 GHz, with S_{21} showing a gain of approximately 4 dB at 60 GHz.

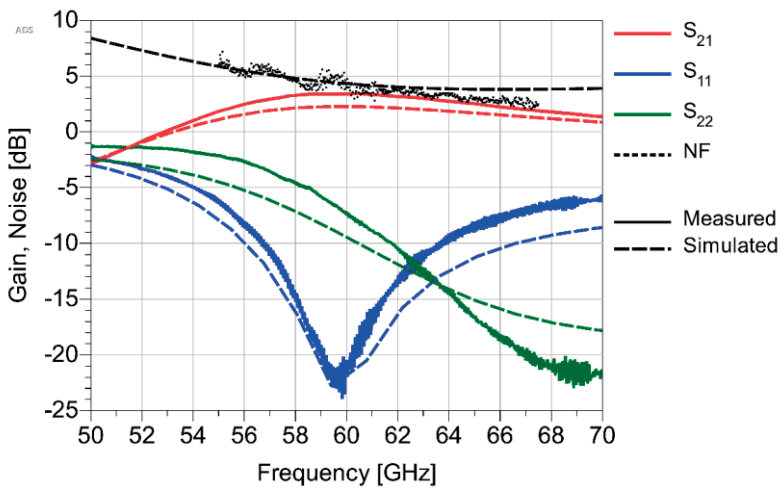

Figure 6.14. Gain for a single transistor, 2 x 7 µm gate width, 40 nm gate length, generation I device, with input matching network and output bias tee performed in BEOL.

7 Conclusions and outlook

This thesis highlights the progress made in III-V nanowire technology for electronic devices. The papers included in the thesis spans all the way from Hall measurements of the carrier concentration in the nanowire crystal, to implementation of record performance VLSI devices as well as transistors adopted for high-frequency applications. The n-type tri-gate nanowire transistor for VLSI applications show world-record I_{ON} at 650 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, higher than any silicon transistor to date. The SS = 66 mV/decade and g_m = 3 mS/µm indicates a well performing transistor in both off-state and on-state. RF-adopted transistors consisting of several hundred nanowires with tight pitch show f_T and f_{max} of 275 and 400 GHz respectively. Efforts in making the RF transistors ready for circuit applications have been initiated with small signal parameter modelling of up to 160 devices, enabling extraction of both intrinsic and parasitic performance, crucial for future circuit applications based on the nanowire technology. The author has also contributed to, although not included in the selected papers of the thesis, initial RF noise measurements, BEOL integration and first demonstration of a RF nanowire transistor with matching network showing gain at 60 GHz.

One of the main focuses has been on implementing spacer technology for the RF nanowire transistors. Many of the processing schemes presented in this thesis have shown a low capacitance, comparable to the state of the art HEMT devices, something very important to make nanowire technology competitive also in the RF-domain. In order to improve the high-frequency performance further, the quality of the nanowire layer must be improved, so that transconductance and output conductance of the RF devices can match that of DC devices demonstrated early on during the thesis work. Ongoing work is analysis of different pre-treatments before growth, annealing studies and In-content in the nanowire layer. Possibly, further optimization of EBL exposure of the HSQ growth mask for RF devices could yield smoother nanowire side walls with an increased mobility. So far, generation IV processing scheme, with self-aligned air spacers, have not been processed on nanowires, which together with an improved nanowire quality could potentially yield even higher RF performance. During the thesis work, T-gate structures have

been developed, however with thickness in the order of 100 nm. To improve the power gain of the transistors, possible tri-layer resist T-gate processes should be developed for gate thickness in the order of 200-300 nm. Future work also focuses on implementation of low-noise-amplifiers in the BEOL, where significant modelling has already been initiated. Finally, optimizing the pad layout with smaller separation between fingers and increased drain to gate pad separation could reduce the parasitic capacitances with a few fF more.

To summarize, lateral nanowire MOSFETs with world-record performance have been manufactured in this thesis, and as far as we can see, lateral nanowires are the main candidate of replacing FinFETs, most likely already in the 3 nm node, although implemented in silicon and with a gate-all-around technology. If the improved speed of III-V channels will be enough to replace Si for logic and if nanowire technology will be implemented in commercial RF devices still remains to be seen.

A. Appendix A

A.1 Lateral nanowire RF process

This section describes the lateral nanowire MOSFET for RF applications, based on generation IV self-aligned process scheme with nanowire processing added.

A.1.1. Nanowire masking and growth

Sample preparation

Cut (100) InP:Fe (S.I) into 10 x 12 mm pieces

Sample cleaning

5 min acetone, 2 min isopropanol (IPA)

8 min ozone cleaning, 500 sccm O_2 flow

Resist deposition

2 min on 200 °C hotplate demoisturizing bake

Dilute 6 % HSQ to 1.5% with methyl isobutyl ketone (MIBK) and spin coat on sample 60 s 6000 rpm

Bake resist 2 min on 200 °C hotplate to promote HSQ adhesion to the InP substrate.

EBL 1: NW growth mask exposure

Expose single pixel lines with 2 nm step size, 30 µm aperture, 50 kV exposure voltage and 300 pA current.

Development

Heat TMAH 25% to 40 °C. Develop 1 min 30 s, 2 min H_2O, 30s IPA.

MOCVD 1: Nanowire growth

Growth of 12 s InP buffer and 12 s $In_{0.63}Ga_{0.37}As$ (~ 12 nm) u.i.d. at 600 °C with surface cleaning at 690 °C in PH_3 over-pressure.

Growth mask removal

3 min BOE 10:1, 1 min H_2O 30 s IPA

A.1.2. HSQ dummy gate mask exposure and contact regrowth

Resist deposition

2 min on 200 °C hotplate demoisturizing bake

Spin coat 6 % HSQ on sample 60 s 3000 rpm (~100 nm)

Bake resist 2 min on 200 °C hotplate.

EBL 2: HSQ dummy gate exposure

Expose dummy gate features, 8 nm step size, 40 μm aperture, 50kV exposure voltage and 600 pA current.

Development

2 min TMAH 25%, 2 min H_2O, 30 s IPA.

MOCVD 2: Contact regrowth

Growth of 30 nm $In_{0.63}Ga_{0.37}As$ at 500 °C with Sn doping, with surface cleaning at 590 °C in AsH_3 over-pressure.

A.1.3. Sacrificial spacer deposition and dummy gate removal

Spacer deposition

~75 nm PECVD of spacer layer

Organic planarization layer deposition

2 min on 180 °C hotplate demoisturizing bake

Spin coat S1805:PGMA 2:3 on sample 45 s, 5000 rpm (~120 nm)

Bake resist 10 min on 180 °C hotplate.

Thinning of planarization layer

O_2 RIE at 300 mTorr, 50 W. Etch until top of HSQ dummy with spacer on is visible

Dry-etch of spacer material to open up HSQ dummy

SF_6/N_2, 25/25 sccm, 20 W, approximately 30 s, until HSQ dummy is visible.

Planarization layer removal

20 min, 50 °C, alternatively O_2 RIE at 300 mTorr, 50 W.

Dummy gate removal

4 min BOE 10:1, 1 min H_2O 30 s IPA

A.1.4. Gate dielectric and gate metal deposition

High-k deposition and surface passivation

8 min ozone cleaning, 500 sccm O_2 flow

10 min $(NH_4)_2$, 7 s H_2O.

Atomic layer deposition: 5 cycles of TMAl precleaning, 6 cycles of Al_2O_3 at 300 °C, 36 cycles of HfO_2 at 125 °C.

Resist deposition

2 min on 180 °C hotplate demoisturizing bake

Spin coat PMMA 950 A5, 4500 rpm, 45 s

Bake resist 2 min on 180 °C hotplate

EBL 3: Gates and gate anchors

Expose gate features, 8 nm step size, 40 µm aperture, 50kV exposure voltage and 600 pA current.

Development

1 min 30 s MIBK/IPA 1:3, 30 s IPA

Metallization 1: Gate

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

Thermal evaporation of 5/10/150 nm Ni/Pd/Au, rotating sample

30 min acetone 50 °C lift-off

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

A.1.5. Sacrificial spacer removal and device isolation

High-k removal outside gate

2 min BOE 1:10, 1 min H_2O, 30s IPA

Dry-etch of spacer material to form air-spacer

SF_6/N_2, 25/25 sccm, 10 W, 45 mT, approximately 60 s, until sacrificial spacer is removed underneath T – shape in gate.

Resist deposition

2 min on 120 °C hotplate demoisturizing bake

Spin coat S1813, 4000 rpm, 60 s

Bake resist 2 min on 180 °C hotplate

UV-1: Mesa etch mask

Hard contact 5.5 s

Development

Continued stirring

Bake resist 10 min at x °C

Mesa etching

40 s in H_3PO_4:H_2O_2:H_2O 1:1:25, 1 min H_2O, 30 s IPA, to make sure InGaAs is removed underneath gate outside active device area

7 s in HCl H_2O 1:1, 1 min H_2O, 30 s IPA, to make sure InP is removed underneath gate outside active device area

Resist stripping

20 min acetone 50 °C S18 removal

60 s at 5 mbar O_2 pressure in oxygen plasma etcher

A.1.6. Source – drain contacts deposition

Resist deposition

2 min on 120 °C hotplate demoisturizing bake

Spin coat maN, 4000 rpm, 60 s

Bake resist 2 min on 180 °C hotplate

UV-2: Source and drain contacts

Hard contact 5.5 s

Development

Continued stirring

Bake resist 10 min at x °C

Metallization 2: Source and drain

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

10 s HCl:H_2O, 1:10, 10 s H_2O native oxide etch

Thermal evaporation of 5/5/30 nm Ti/Pd/Au using the T-gate as a shadow mask

30 min acetone 50 °C lift-off

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

A.1.7 Pad deposition

Resist deposition

2 min on 120 °C hotplate demoisturizing bake

Spin coat maN, 4000 rpm, 60 s

Bake resist 2 min on 180 °C hotplate

UV-3: pads

Hard contact 5.5 s

Development

Continued stirring

Bake resist 10 min at x °C

Metallization 3: pads

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

Thermal evaporation of 5/10/300 nm Ti/Pd/Au using the T-gate as a shadow mask

30 min acetone 50 °C lift-off

30 s at 5 mbar O_2 pressure in oxygen plasma etcher

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PAPERS

Paper I

Paper I

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Gated Hall effect measurements on selectively grown InGaAs nanowires

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Abstract

InGaAs nanowires is one of the promising material systems of replacing silicon in future CMOS transistors, due to its high electron mobility in combination with the excellent electrostatic control from the tri-gate geometry. In this article, we report on gated Hall measurements on single and multiple $In_{0.85}Ga_{0.15}As$ nanowires, selectively grown in a Hall bridge geometry with nanowire widths down to 50 nm and thicknesses of 10 nm. The gated nanowires can be used as junctionless transistors, which allows for a simplified device processing as no regrowth of contact layer or ion implantation is needed, which is particularly beneficial as transistor dimensions are scaled down. The analysis shows that the InGaAs layer has a carrier concentration of above 10^{19} cm^{-3}, with a Hall carrier mobility of around 1000 cm^2 V^{-1} s^{-1}. The gated Hall measurements reveal an increased carrier concentration as a function of applied gate voltage, with an increasing mobility for narrow nanowires but no significant effect on larger nanowires.

Keywords: Hall effect, InGaAs, nanowire, carrier concentration, MOSFET, Hall bridge, junctionless

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor nanowires (NWs) are an attractive device geometry for the production of LEDs [1], sensors [2], photo detectors [3, 4] and solar cells [5]. The nanowire geometry also allows for heterogeneous integration of various III–V [6] compounds as well as Si. Nanowire field effect transistors (NWFETs) is an additional key area where nanowires provide advantages, due to the improved electrostatic control of the channel potential arising from the gate all-round geometry [7]. To produce high performance devices, it is important to measure and understand the charge carrier concentration and mobility. Hall measurements of vapor–liquid–solid (VLS) grown nanowires have previously been performed [8, 9]. In this case, the vertical NWs were broken off and placed on a measurement substrate. However, with this technique it is difficult to align metal contacts with high enough precision and sufficient space between adjacent Hall probes on NWs with a diameter smaller than 100 nm.

Selective area growth of NWs offer several advantages. For instance, nanowires can be formed lateral to the substrate, which is compatible with standard complementary metal oxide semiconductor (CMOS) fabrication. Moreover, template assisted growth allows us to design Hall bridge geometries and measure the carrier concentrations (n_{NW}) on nanowires with dimensions down to 50 nm.

In recent years, InGaAs nanowires have received increased attention for CMOS applications due to the improved electron mobility of InGaAs compared to silicon [10]. Higher electron mobility leads to increased drive currents which effectively allow the supply voltages as well as the power consumption to be reduced.

In this work we present a processing scheme as well as gated Hall measurements of selectively grown lateral InGaAs NWs. This approach requires no NW transfer, or top-down etching to define the NWs hence the sidewalls are defined by crystal facets rather than etched surfaces.

The use of gated nanowires in combination with Hall bridge geometry enables us to control and measure the channel carrier concentration n_{NW} as the gate voltage is varied, as well as the Hall mobility. The fabricated gated Hall bar device is

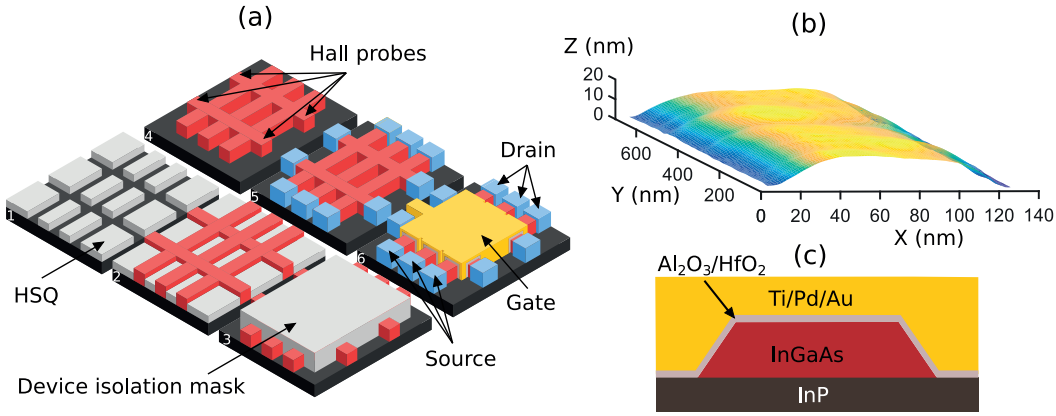

Figure 1. (a) Schematic image of the fabrication process for our regrown InGaAs nanowire transistors in Hall bridge geometry. Step 1: HSQ patterned into a growth mask for the selective area regrowth of InGaAs in step 2. Step 3: HSQ patterned as an etch mask for the subsequent device isolation in step 4. Step 5: Ti/Pd/Au contacts evaporated to source and drain regions as well as Hall contacts. Step 6: Final processing step of ALD (10 cycles of Al_2O_3/150 cycles of HfO_2) followed by gate evaporation of Ti/Pd/Au. (b) AFM image showing the cross section of a 110 nm wide fin. Observe that the scale of the y-direction is different from X and Z. (c) A cross-sectional schematic image of the substrate, channel material and oxide as well as gate metal. Note that figures 1(a) and (c) are not to scale.

essentially a realization of a junctionless transistor. Junctionless transistors, which typically employ uniform high doping through the contacts and the channel, have seen increased research interest recently due to their simplified fabrication process that does not require any ion implantation in the source and drain regions [11]. We have previously demonstrated the potential of this material system in combination with regrown contact regions. For example, we have measured quantized conductance in nanowire channels and excellent transistor performance with high on-currents [12, 13].

2. Experimental

The process starts with spin coating a semi-insulating InP:Fe substrate with the negative electron beam lithography (EBL) resist hydrogen silsesquioxane (HSQ) (1.5%) followed by a baking step at 200 °C. The resist is EBL exposed and developed by tetramethylammonium hydroxide (TMAH) where the HSQ partially transforms into SiO_2 (figure 1, step 1). The SiO_2 acts as a growth mask for the subsequent MOCVD selective area growth of lateral [011] $In_{0.85}Ga_{0.15}As$ nanowires (step 2) with nanowire widths varying from 50 to 410 nm. While the NWs are grown not intentionally doped, the low growth temperature of 500 °C facilitates high background doping. We have fabricated transistors with both single wires and with three nanowires in parallel to increase the current, and effectively reducing the signal-to-noise ratio. The nanowires have a higher In-content than the planar growth areas, arising from interactions with the HSQ mask [12]. The NW's faceting structure depends on their orientation on the substrate. In this work, we utilize NWs with (111)B sidewalls, as seen in figure 2(c) for thicker reference NWs. In contrast to the reference, the growth is terminated at a nanowire height of 15 nm, rendering a flat (100) top facet, as can be seen in the AFM image in figure 1(b). The SiO_2 growth mask is subsequently removed by buffered oxide etch (BOE) (10:1). The devices are isolated through EBL exposure of an HSQ (6%) mask (step 3) followed by a mesa etch with H_3PO_4:H_2O_2:H_2O for 25 s. The schematic image of the Hall-bar after device isolation and HSQ removal is shown in figure 1 (step 4). We perform 4 cycles of digital etches to trim down the nanowire height, from 15 nm as seen in figure 1(b) to a final thickness of 10 nm, through ozone oxidation for 8 min followed by 15 s of HCl:H_2O (1:5). Next, the devices are contacted through EBL exposure of PMMA and evaporation and lift-off of Ti/Pd/Au (100/100/800 Å) (step 5). The transistor channel is passivated with a $(NH_4)_2S$ (10%) solution and gate oxide is deposited through ALD (10 cycles of Al_2O_3 and 150 cycles of HfO_2) with an EOT of 4 nm where the Al_2O_3 acts as an interface layer to reduce interface roughness and decrease density of interface traps (D_{it}) [14]. The relatively thick gate oxide has been selected to decrease the gate leakage in order to obtain as stable a Hall voltage signal as possible. The transistor is completed with gate definition through EBL, evaporation and lift-off of gate metal, Ti/Pd/Au (100/100/800 Å) (step 6) creating a tri-gate geometry. Figure 1(c) shows a cross-sectional schematic image, and top view SEM images of finalized transistors can be seen in figures 2(a) and (b) for multiple and single nanowire devices, respectively. All data presented from gated devices in this paper have gates overlapping the source and drain contacts to reduce the resistances in the transistors, figure 2(d) shows a zoomed out top view image with the layout of measurement pads for Hall measurements. From AFM measurements seen in figure 1(b) we have measured the root mean square roughness of the top facet to 1 nm and the side wall roughness to 5 nm.

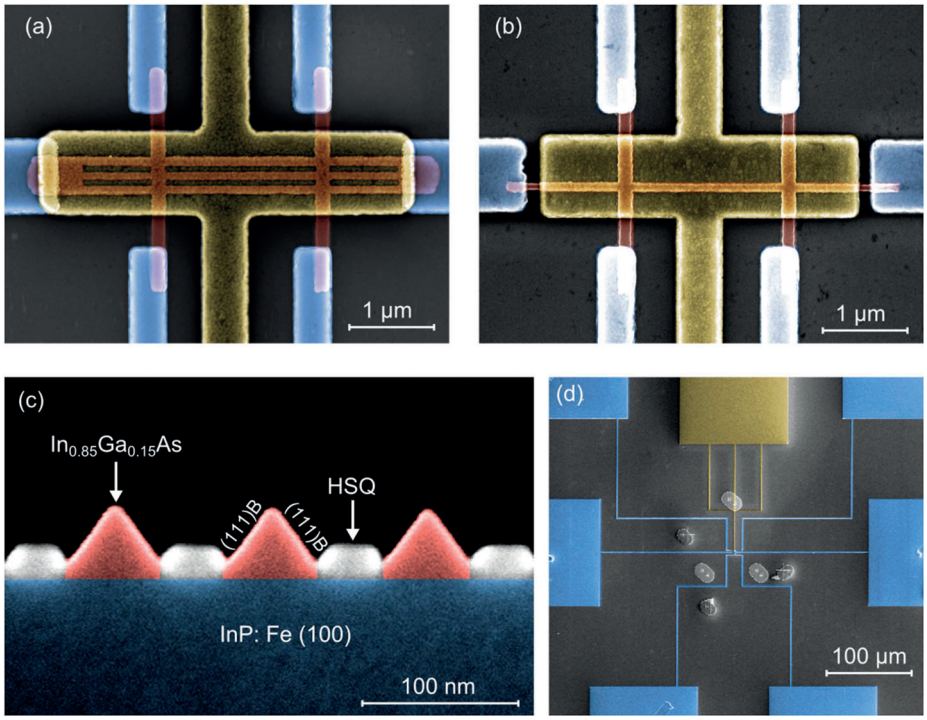

Figure 2. (a) Top view SEM image of finished gated nanowire Hall bar with gate length of 4 μm with three nanowires in parallel and for a single wire (b). (c) A cross-sectional SEM image of InGaAs nanowires from a reference sample with thicker nanowires, showing the (111)B planes that make up the side walls. (d) A SEM image of the finalized device showing measurement pads as well as alignment marks for the two metallization steps. The images have been false colored to highlight different device areas.

3. Results and discussion

The electrical measurements are performed at room temperature with a Hall effect measurement setup using 4 source-measure units and a 2.5 Tesla electromagnet. In order to measure the intrinsic resistivity and to reduce the effect of contact resistance and the resistance in the metal probes (0.5 Ω/μm length) we have performed 4-probe measurements where the source-drain voltage (V_{DS}) is swept from 0 to 0.2 V generating a current through the nanowire. From the linear fitting of the voltage drop measured between the inner contact pairs on one side of the device, plotted against the current, the intrinsic resistance, and hence the resistivity, ρ, is calculated as:

$$\rho = \frac{R \cdot w \cdot t}{L_c} \tag{1}$$

where R is the resistance, w is the width of the nanowires, t is the thickness and L_c the length between Hall contacts on the same side of the device. Here we take into account a factor of 3 for the nanowire width if a device with three nanowires is analyzed. For the Hall measurements, V_{DS} of 0.5 V is sourced and a magnetic field of -2 to 2 T in steps of 1 T is applied perpendicular to the substrate. The subsequent Hall voltage, V_h, is measured as the voltage difference between two opposing Hall contacts to extract the carrier concentration, n_{NW}:

$$n_{NW} = \frac{iB}{V_h q t} \tag{2}$$

where i is the current measured between source and drain, B the applied magnetic field and q is the elementary charge. We calculate the carrier concentration from a linear fitting of the Hall voltage as a function of the five different magnetic fields. The measurement of the Hall voltage is performed for both Hall pairs in a device with good correlation of the extracted carrier concentration. Finally, the electron mobility, μ_n, is calculated from measurements of resistivity and Hall carrier concentration:

$$\mu_n = \frac{1}{q n_{NW} \rho} \tag{3}$$

We have studied the carrier concentration and the mobility both before and after gate deposition. After the gate is applied, the measurements are repeated for gate voltages, V_{GS} of -0.5 to 0.5 V in steps of 0.1 V with the resistivity measurements repeated for every gate voltage. In figure 3(a), the extracted n_{NW} from Hall measurements prior to gate deposition is plotted

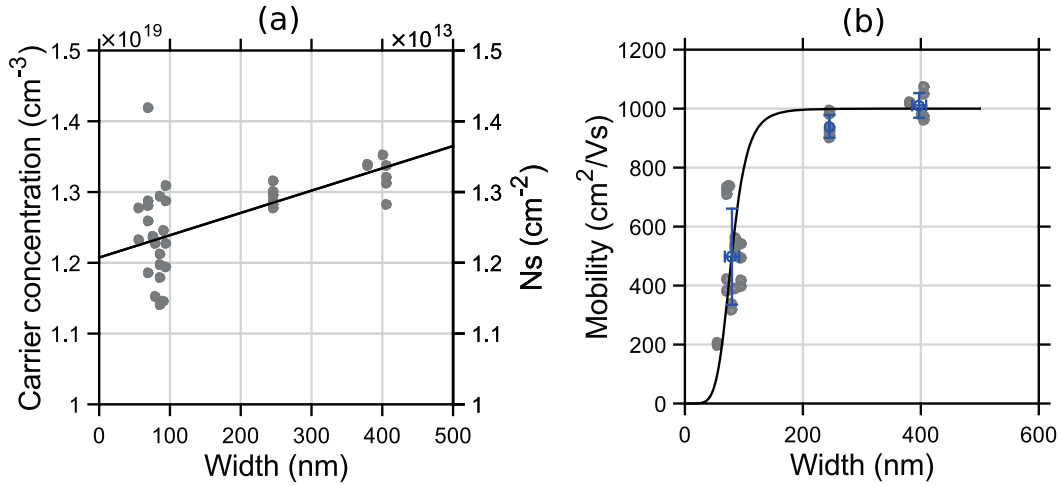

Figure 3. Measured Hall carrier concentration (a) and Hall mobility (b) as a function of nanowire width for ungated devices. The blue crosses marks the standard deviation for width and mobility for the different nanowire sizes. Black lines represent fittings to the measured data points.

as a function of the nanowire width, w_{NW}. Each data point represent a single Hall pair on a device. A linear fit gives $N_D = 3.6 \times 10^{15} \times w_{NW} + 1.2 \times 10^{19}\,cm^{-3}$. The measured devices with a single nanowire and three nanowires in parallel show consistent carrier concentration and mobility. In(Ga)As is known to have surface pinning of the Fermi level, attracting charge close to the surface [15], either on the NW side walls or on the top facet. If Fermi level pinning on the side walls is the dominating effect, we would expect the carrier concentration to drop as the nanowire width, and thus volume, increases while surface pinning at the top facet or bulk doping would yield a constant carrier concentration with increasing width, which is similar to what is measured here. We have previously seen that the nanowires have a higher In-content than the corresponding thin film, most likely caused by local change in growth kinetics due to the HSQ mask [12]. A correlation between the In-content and background doping could explain this trend.

In figure 3(b), the mobility extracted from the carrier concentration and the resistivity is plotted as a function of the width. The mobility can be analyzed using Matthiessen's rule, where the effective mobility is set by the dominating scattering mechanism:

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{planar}}} + \frac{1}{\mu_{NW}} \tag{4}$$

where μ_{planar} is the mobility of the widest device, limited by bulk and top surface roughness scattering, and μ_{NW} is mobility limited by side wall surface roughness scattering. μ_{NW} can be approximated as $\mu_{NW} = k * w^6$ as suggested in [16] and [17] where w is the width of the nanowire and k is a fitting constant For the narrow nanowires, the mobility is primarily limited by scattering from the side walls but as the nanowire width is increased, the impact of the side wall roughness is less and the mobility saturates around $1000\,cm^2\,V^{-1}\,s^{-1}$ due to the top facet scattering and possible ionized impurity scattering. The highest mobility measured is comparable to values measured at the same sheet carrier concentration in InGaAs [18] and is ten times higher than silicon of similar carrier concentration [19]. The large effect of nanowire width on mobility highlights the importance of obtaining as smooth nanowire side walls as possible with low surface roughness.

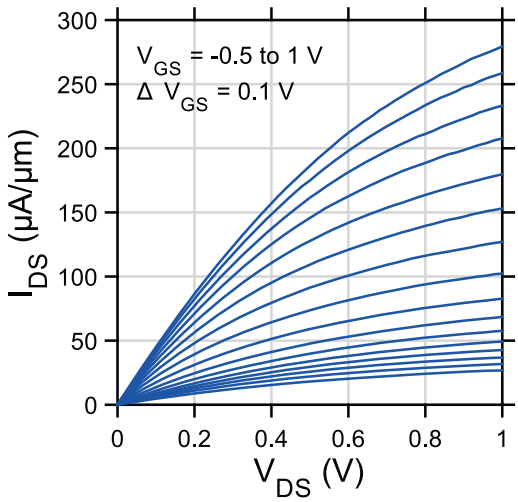

Figure 4. Output characteristics of a transistor with nanowire width of 70 nm with a gate length of 4 μm.

Figure 4 shows the output characteristics of a gated 70 nm wide nanowire with a gate length of 4 μm. The fabricated transistor has a peak current of 270 $\mu A\,\mu m^{-1}$ for V_{DS} of 1 V and V_{GS} of 1 V, normalized to the total gated periphery, which is in line with other reported values for InGaAs with similar transistor dimensions [18, 20]. Due to the high carrier

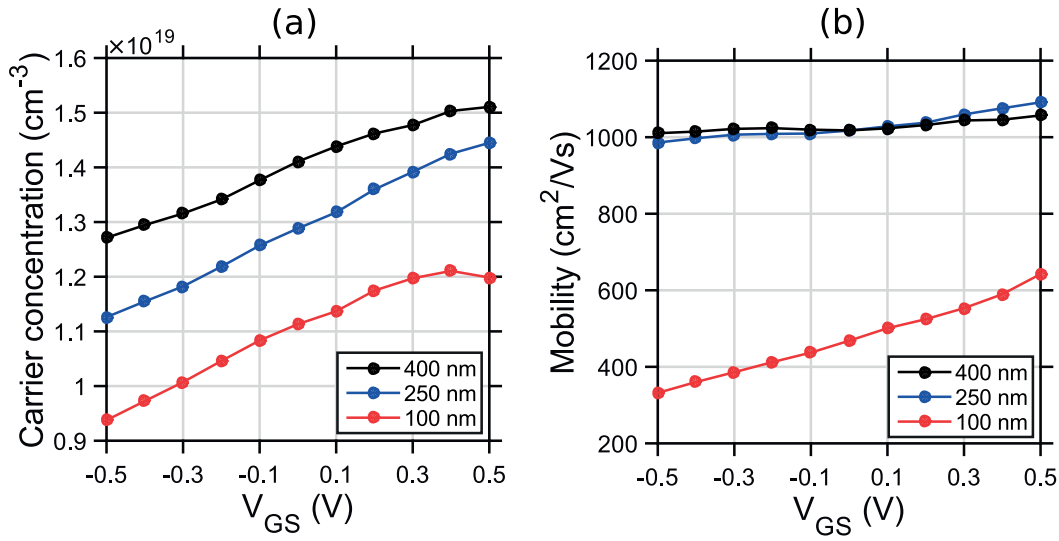

Figure 5. (a) Measured carrier concentration from Hall measurements as a function of applied gate voltage (V_{GS}) with a fixed source-drain voltage (V_{DS}) of 0.5 V for different nanowire widths. (b). Calculated Hall mobility as a function of applied gate voltage.

concentration, together with slightly too thick nanowires, we have not been able to fully deplete the nanowires.

In figure 5(a), the carrier concentration as a function of applied gate voltage is studied. The carrier concentration increases with gate voltage for all widths, until it stabilizes at values similar to the ungated measurements. Also in agreement with the ungated measurements, the carrier concentration exhibits a minor w_{NW} dependence. From the difference between the ideal and measured slope of $\Delta n(V_{gs})$ we can extract an average interface defect density of around 6–10 $\times$ 10^{12} cm^{-2} eV^{-1}. In figure 5(b) we can see that the mobility of the wider nanowires remains in the saturated regime for all gate voltages, but the increase in mobility with gate voltage is strong for the narrow nanowires. One possible explanation for the increasing mobility for the W = 100 nm wires with respect to V_{GS} can be different interface defect profiles (D_{it}) for the different facets. The 100 top surface is expected to have a lower D_{it} as compared with the rougher 111B surface, which would lead to a stronger electron accumulation close to 100 as compared to 111B, which in turn will result in an average increase in mobility with V_{GS}. This effect will decrease with nanowire width since the influence of the side walls on total mobility is less. An increase in carrier concentration has also been suggested to minimize back scattering for quantum wells and nanowire structures, due to a diminishing scattering matrix element for large Fermi wave vectors [21]. Decreased mobility for decreasing carrier concentrations have previously been measured for gated InGaAs MOSHEMTs of similar channel thickness [22, 23], allocated to reduced screening of coulomb scattering. The field effect mobility extracted from transistor measurements is around 500 cm^2 V^{-1} s^{-1}, without any clear dependence on width and gate voltage.

4. Conclusions

We have presented a processing scheme to fabricate selectively grown nanowires with a width down to 50 nm in a Hall bridge geometry, allowing the carrier concentration and mobility to be analyzed as a function of applied gate voltage. From Hall measurements, we obtain a nanowire width-dependent carrier concentration of $N_D = 3.6 \times 10^{15} \times w_{NW} + 1.2 \times 10^{19}$ cm^{-3} and a maximum electron mobility of 1000 cm^2 V^{-1} s^{-1} in 200 nm wide nanowires. For thinner nanowires the mobility is found to be reduced from process induced surface roughness. We believe that a fully optimized EBL process for NW definition would reduce the side wall roughness and have a positive effect on electron mobility for most scaled device dimensions as well as allowing fabrication of gated nanowires substantially smaller than 50 nm in width.

Acknowledgments

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Paper II

Paper II

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III-V nanowire MOSFETs with novel self-limiting Λ-ridge spacers for RF applications

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Abstract

We present a semi self-aligned processing scheme for III-V nanowire transistors with novel semiconductor spacers in the shape of Λ-ridges, utilising the effect of slow growth rate on {111}B facets. The addition of spacers relaxes the constraint on perfect alignment of gate to contact areas to enable low overlap capacitances. The spacers give a field-plate effect that also helps reducing off-state, and output conductance while increasing breakdown voltage. Microwave compatible devices with L_g = 32 nm showing f_T = 75 GHz and f_{max} = 100 GHz are realized with the process, demonstrating matched performance to spacer-less devices but with relaxed scaling requirements.

Keywords: Nanowire, MOSFET, RF, spacers, InGaAs, InP

1. Introduction

III-V materials such as InGaAs has been widely used in HEMTs for mmWave applications due to its high electron mobility[1-3]. In recent years, high-performance digital MOSFETs made of III-V materials have also been reported and are candidates for replacing Si in order to maintain a high on-current while reducing the supply voltage[4-8]. Another way of improving the performance of CMOS devices is to use nanowires or nanosheets due to the improved electrostatic control gained by surrounding the channel with gates from multiple sides, allowing more aggressive gate length scaling[9, 10]. III-V nanowire MOSFETs and FinFETs have also been studied for RF applications[11, 12] and is an interesting candidate for future mixed applications where analogue and digital function is placed close to each other, for instance in system on Chip (SoC) used in 5G telecommunication and above. One limiting factor for RF MOSFETs is the parasitic capacitance between the highly doped contact regions and the gate contact which increases compared to HEMT devices due to the high-k oxide. Lowering the parasitic capacitances is especially important for nanowire MOSFETs since there is space in between the nanowires that contribute with a parasitic capacitance but not with current or transconductance[13]. This makes the requirement on alignment accuracy very high since any gate overlap on contact regions results in increased parasitic capacitances.

In this paper we propose a novel semi self-aligned InGaAs nanowire MOSFET with self-limited growth of InP ridges with triangular cross-section (Λ-ridges) acting as spacers for use in RF applications. The introduction of InP spacers can reduce the effect of gate-drain and gate-source overlap on transistor performance, while keeping the increase in access resistance small due to the introduction of modulation-doped Si layer in the Λ-ridges[14]. The process also allows for low access resistance due to a lack of wide bandgap heterojunction between the ohmic contact and nanowire channel.

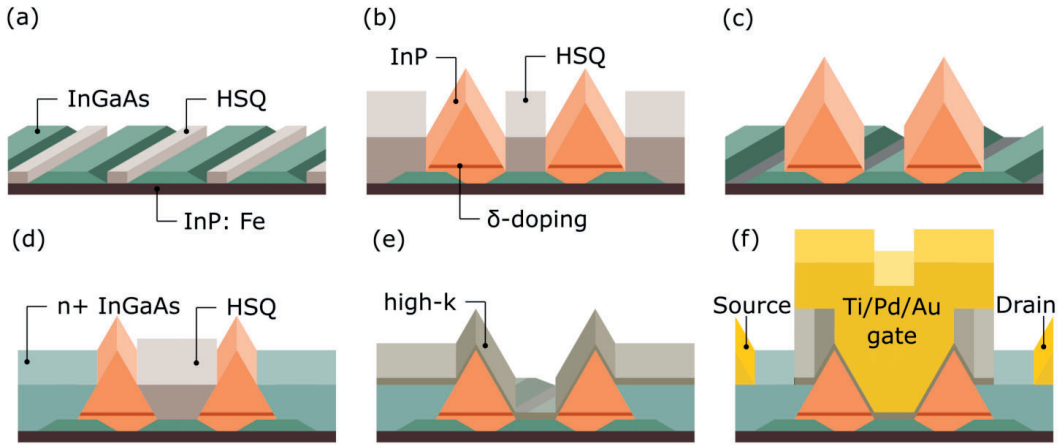

Figure 1. Schematic illustrations of the RF nanowire MOSFET device with InP Λ-ridge spacers. (a) HSQ exposure and MOCVD growth of InGaAs nanowires. (b) Dummy gate and spacer exposure followed by growth of modulation doped InP self-limiting Λ-ridge bound by {111}B facets. (c) Device after stripping of the HSQ resist. (d) Second HSQ dummy gate exposure and contact regrowth. (e) Resist stripping and high-k deposition. (f) T-gate and source drain evaporation.

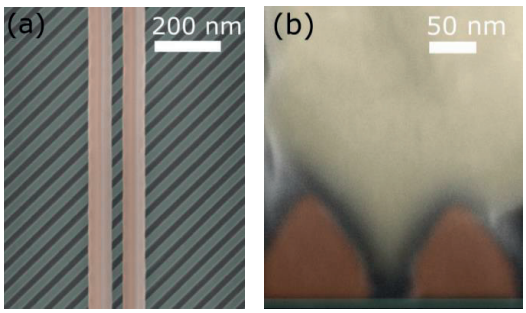

Figure 2. (a) False coloured SEM image of a nanowire device after growth of 80 nm wide InP Λ-ridge spacers, separated by 40 nm, corresponding to figure 1(c). (b) Tilted cross-sectional SEM image of the same device after high-k and gate deposition, corresponding to figure 1(f).

2. Device fabrication

The processing starts with e-beam exposure and development of hydrogen silsesquioxane (HSQ) resist to form a SiO-like template for the selective area metalorganic chemical vapor deposition (MOCVD) growth of 7 nm thick and 30 nm wide $In_{0.85}Ga_{0.15}As$ nanowires on a semi-insulating (100) InP:Fe substrates, figure 1(a). The HSQ lines sets the width and pitch of the nanowires while the growth time sets the thickness. The lines are aligned in the [100] direction, forming nanowires bound by {110} side walls with 45° inclination relative to the (100) top facet. Next, a second HSQ exposure is performed to create a 40 nm dummy gate and 80 nm wide spacer openings aligned in the [011] direction, which will later set the gate length of the device. This is followed by growth of the InP self-limiting Λ-ridges with a layer sequence of 4 nm i-InP, 4 nm Si-modulation doped layer ($N_D = 5x10^{18}$ cm^{-3}) and 60 nm thick i-InP. Due to the 45° rotation of the dummy gate compared to the nanowires, the InP ridges are defined by slow growing {111}B facets with 54.7° inclination relative to the (100) top facet, as seen in figure 1(b)[15]. Most of the atoms impinging on the {111}B facets either migrate to the top (100) facet or reevaporate. As the growth proceeds the (100) becomes smaller due to the minimal growth rate on the {111}B facets. In the limit the (100) facet disappears, leading to a ridge with height determined by the width of the base. The width of the Λ-ridge continues to expand by growth on the {111}B facets at a near negligible growth rate, which means that for all practical purposes the process can be viewed as being self-limited. Importantly, the gate length and spacer length is set by the separation and width of the Λ-ridges simultaneously and independently of each other, making the spacer placement self-aligned. After a second HSQ dummy gate has been exposed to avoid growth in the channel region, 20 nm thick Sn-doped $In_{0.63}Ga_{0.37}As$ contact regions ($N_D = 5x10^{19}$ cm^{-3}) are grown, figure 1(d). This second dummy gate must be same width or wider than the initial dummy gate, but not wider than the dummy-gate plus the two spacer regions for

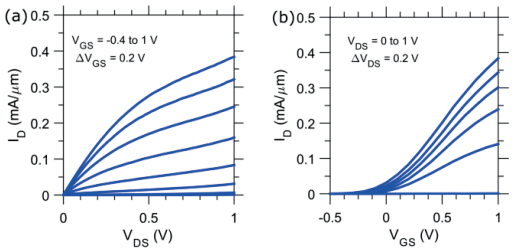

Figure 3. Output (a) and transfer (b) characteristics of a nanowire MOSFET device with 32 nm gate length and 80 nm InP Λ-ridge spacers, consisting of 2x100 nanowires with total gated circumference of 7 μm which have been used for the normalization.

the scheme to work. InGaAs is known to have negligible growth rate on {111}B facets in MOCVD, however, we cannot exclude some minor InGaAs growth due to roughening of the facets by the processing done between growth runs[15, 16].

To finalize the transistor, mesa-isolation, ALD high-k oxide (7 cycles Al_2O_3 and 37 cycles HfO_2) figure 1(e), and TiPdAu T-gate and source drain metals are evaporated, figure 1(f). Figure 2 shows a top-view SEM image of a device after InP ridge growth (figure 2(a)) and a tilted cross-sectional SEM image after the device is completed. In a similar process, we have also fabricated reference spacerless devices without InP ridges. The gate contact will here have a 10 nm overlap against the source and drain n+ regions.

The reason for using the InP Λ-ridge spacers are two-fold. First, separating the n+ contact region and the gate could potentially reduce the parasitic gate-drain and gate-source capacitance. Secondly, the inclusion of a field-plate region in the drain-side has been shown to increase the breakdown voltage and reduce the output conductance of MOSFET devices, due to the reduced maximum electric field at the drain side, minimizing band-to-band tunnelling and short-channel effects. However, including the InP underneath the n+ contact regions as in [14] adds a series resistance in the access regions, which the novel Λ-ridge layout avoids.

The second consideration comes to self-alignment. In a spacer-less layout, the gate should ideally be placed perfectly between the two n+ contact regions without any overlap. By using the Λ-ridges, the requirement on perfect alignment can be relaxed and the gate can on purpose be designed wider than the opening between the spacers and overlap the side walls without a significant loss in overlap capacitance. The limitations of this design is that the second HSQ dummy gate must be aligned to the first one. However, due to that the spacers have {111}B sidewalls, with very limited growth rate, as long as the edges of the second dummy gate is inside the two Λ-ridges, the n+ contacts will start to grow at the (100)

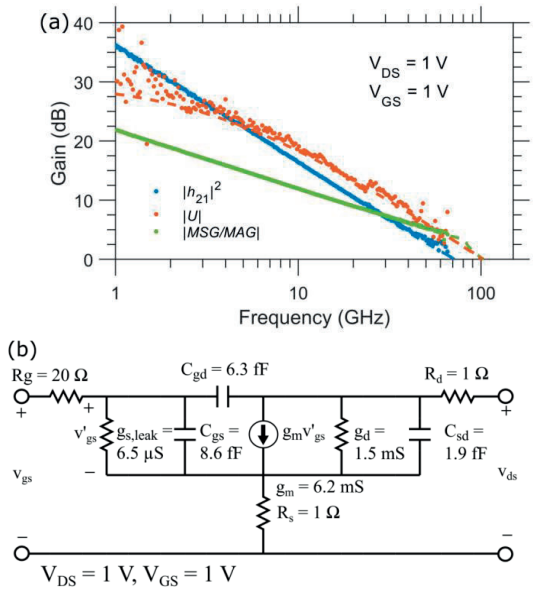

Figure 4. Measured and modeled gain of the same device as in figure 3, with V_{DS} = 1 V and V_{GS} = 1 V with f_t = 70 GHz and f_{max} = 100 GHz. (b) Small signal model used to fit the data in figure 4(a).

surface on top and between the nanowires outside the channel region. This allows for a misalignment equal to approximately the half of the spacer width, easily accomplished with high-resolution lithography techniques.

3. Results and discussion

We have successfully fabricated nanowire MOSFETs with Λ-ridges InP spacers utilising very limited growth on {111}B facets. In figure 3(a) output and 3(b) transfer characteristics of a 32 nm gate length device with 80 nm InP spacers are shown with peak transconductance of 300 $\mu S\mu m^{-1}$, consisting of 2 fingers with 100 nanowires in parallel per finger, giving a total gated nanowire circumference of 7 μm and a total device width of 14 μm. Due to the use of the InP spacers, the device exhibits excellent pinch off at high drain bias up to V_{DS} = 1 V and low gate bias. This is an improvement from our earlier work where the output conductance was considerable already at V_{DS} = 0.75 V for the same gate length [17]. The transistor has a minimum off-current at 100 $nA\mu m^{-1}$, with a subthreshold slope of 400mV/decade, which is a slight reduction compared to a spacer-less reference device with gate length of 52 nm at 500 mV/decade. The output conductance of the two devices at 1 V V_{DS} and 1 V gate overdrive is 200 $\mu S\mu m^{-1}$ even though the gate length is shorter for the device with spacer, indicating the positive

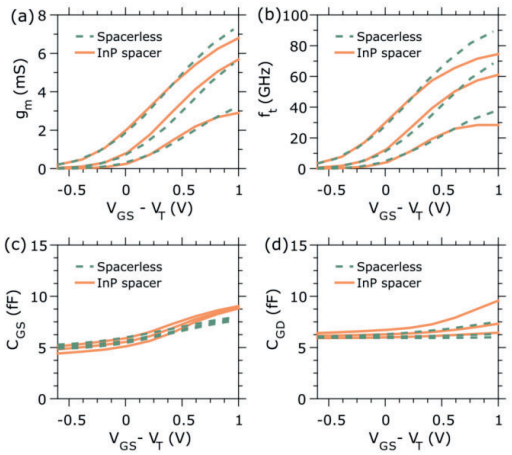

Figure 5. RF behavior for V_{DS} = 0.2, 0.6 and 1 V of a device with 80 nm InP Λ-ridge spacers (gate overlap 40 nm) and a spacerless device where the spacerless device has been optimized for small gate overlap on the source and drain regions. (a) RF transconductance, (b) current gain (c) gate-source capacitance and (d) gate-drain capacitance as extracted from small-signal model.

effect of the InP spacer. In order to evaluate the high frequency performance of the device, we have measured the transistor RF-gains from 100 MHz up to 67 GHz. Off-chip LRRM calibration and pad deembedding on open/short structures have been performed. In figure 4(a) the RF gain of the transistor with V_{DS} = 1 V and V_{GS} = 1 V is shown. Linear fitting with -20db/decade gives f_T = 70 GHz and f_{max} = 100 GHz. From the measured y-parameters we have fitted a small signal model seen in figure 4(b). The device current and unilateral gain show a roll-off of 20db/decade and the frequency dispersion in transconductance is less than 10%, indicating that the high-k oxide has a minor effect on the high-frequency device performance.

To be able to extract the parasitic capacitances of the device, we have measured the RF as a function of V_{GS}. For negative biases below V_T, the obtained capacitances are mainly due to the parasitic capacitance, since at this points the channel is depleted of carriers. The equivalent of the small-signal model is shown in figure 5 for the analysed device in figure 3 and 4 as well as a reference spacer less device with gate length of 52 nm. The spacerless device has been optimised for small gate overlap, with approximately 10 nm gate overlap on each side of gate towards the n+ contact regions, this in comparison with the Λ-ridge device, where the overlap is approximately 40 nm per side. Both devices show similar transconductance around 300 μSμm^{-1} even though the InP Λ-ridge spacers ads a 80 nm access region, thus the addition of modulation doped InP

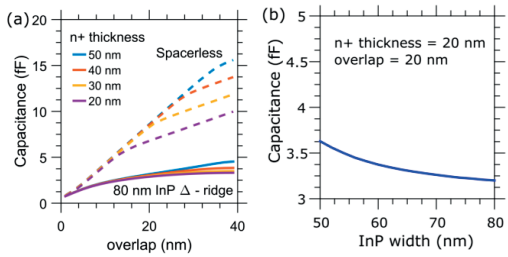

Figure 6. (a) Modeled influence on gate overlap on parasitic gate-source/drain capacitance for varying contact thickness, for both 80 nm InP spacer and for a spacerless layout. Device is 2x100 nm with total gated circumference of 7 μm. (b) Gate-source capacitance for a fixed thickness of 20 nm and a gate overlap of 20 nm with varying InP spacer width.

spacers does not add significantly to the access resistance. At higher gate overdrive, the spacer-less device performs slightly better, possibly due to source-starvation in the Λ-ridge device. Source starvation can limit the transconductance at high gate overdrive due to a lack of carriers in the source-access region[18]. We obtain a parasitic gate capacitance from V_{GS} - V_T = -0.55 V of $C_P \approx$ 5.0 fF for the ridge device, and C_P = 5.5 fF for the spacer less device. Even though the device with the Λ-ridge has a gate overlap which is substantially larger, both C_{GS} and C_{GD} is very comparable to the spacer-less device with minimal overlap, up until high-gate overdrive where the charging in the InP spacers starts to play a significant role. To compare and verify the proposed device architecture, we have modelled the parasitic capacitance between the gate and the n+ InGaAs, InGaAs channel and the InP Λ-ridge spacers using a 2D electrostatic model in COMSOL multiphysics. A similar device width of W = 14 μm as the fabricated devices is used in the model. The quantum capacitances of the channel quantum well and n+ source regions are taken into account in the model as a distributed capacitance. In the model, we have compared the gate overlap capacitance for 80 nm Λ-ridge InP spacers and for a spacerless layout with varying contact layer thickness. In figure 6(a) it is seen that the influence of gate overlap is drastically reduced with the InP spacer, as compared to the spacerless device. However, a small overlap in a spacerless device can yield similar capacitances as a larger overlap in a Λ-ridge device, as we have seen experimentally. For the spacerless device, we obtain a good agreement with the measured value of the parasitic capacitance at an overlap of 10 nm. For the InP ridge, a parasitic capacitance of 3.7 fF is modelled. The higher value of 5.0 fF can originate from a slightly too high delta-doping in the ridge leading to remaining carriers in the spacer, which increases the parasitic capacitance. In figure 6 (b), we have studied the influence of the width of the pyramid on overlap capacitance for a fixed overlap of 20 nm and n+ contact thickness of 20 nm.

Increasing the spacer width lowers the capacitance, but the effect is fairly small since most of the fringing capacitance occur very close to the overlap between the gate and the spacer.

4. Conclusion

We have successfully fabricated InGaAs nanowire MOSFETS with a processing scheme utilizing the faceting of MOCVD grown InGaAs and InP to include Λ-ridge spacers in a semi self-aligned process. We have shown that utilizing this scheme, the gate can overlap the spacer regions without a significant loss in overlap capacitance, compared to a non-self-aligned spacerless approach, which considerably relaxes the alignment requirements in the gate definition. The scheme also opens up possibilities to vary the gate length and spacer length independently over the wafer and it is even possible to fabricate asymmetric spacers with larger gate-drain separations for improved f_{max}. The self-limiting Λ-ridge scheme is not limited to nanowires and can also be implemented for planar MOSFETs.

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Paper III

Paper III

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz”, *Electronic Letters,* 2016

High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz

C.B. Zota✉, F. Lindelöw, L.-E. Wernersson and E. Lind

Extremely scaled down tri-gate RF metal-oxide-semiconductor field-effect transistors (MOSFETs) utilising lateral nanowires as the channel, with gate length and nanowire width both of 20 nm are reported. These devices exhibit simultaneous extrapolated f_t and f_{max} of 275 and 400 GHz at $V_{DS} = 0.5$ V, which is the largest combined f_t and f_{max}, as well as the largest f_{max} reported for all III–V MOSFETs.

Introduction: Tri-gate (or non-planar) metal-oxide-semiconductor field-effect transistors (MOSFETs) for RF applications are motivated by that the use of a high-k oxide, rather than a semiconductor barrier (as in high electron mobility transistors (HEMTs)) allows for higher gate capacitance in the MOSFET [1, 2]. Furthermore, the tri-gate architecture improves short-channel effects, allowing for shorter gate length, L_G, without degradation of performance due to short-channel effects. Both these points enable higher ideal transconductance, g_m, in MOSFETs compared with HEMTs, assuming similar electron mobility. In fact, state-of-the-art III–V MOSFET devices exhibit g_m larger than that of record HEMTs, although they presently do not allow RF-compatible device designs [3–5].

In this Letter, we present RF-compatible tri-gate $In_{0.85}Ga_{0.15}As$ MOSFETs utilising lateral nanowires (NWs) as the channel. Compared with our previous work, we have here further scaled down device dimensions, L_G and NW width, W_{NW} [6]. This enables higher g_m at $V_{DS} = 0.5$ V, which significantly improves f_t/f_{max} from 220/305 to 275/400 GHz. The combined f_t and f_{max}, as well as the f_{max} of these devices represent the highest reported values for all III–V MOSFETs.

Fabrication: The device fabrication process is similar to what has been described elsewhere [7]. The device channel consists of 200 lateral $In_{0.85}Ga_{0.15}As$ NWs, formed by selective area MOCVD growth on (100) InP:Fe (S.I.) substrate, split over two gate fingers. The NW width is 20 nm, and the height is 11 nm. The S/D highly doped regions are formed by a second MOCVD growth step of 40 nm n^+ $In_{0.63}Ga_{0.37}As$/100 nm InP with in-situ Sn doping ($N_D = 5 \times 10^{19}$ cm^{-3}) in the doped layer (Fig. 1*a*). Subsequently, 1 nm/5 nm Al_2O_3/HfO_2 is deposited by atomic layer deposition and Ti/Pd/Au by thermal evaporation, forming the gate stack. The regrown 100 nm InP is selectively etched by an HCl solution leaving a T-gate. S/D and pad metallisation of Ti/Pd/Au completes the process (Fig. 1*b*).

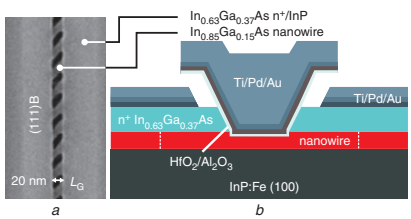

Fig. 1 *Device fabrication and device materials and design*

a SEM image of device after contact regrowth, L_G is defined as distance between n^+ contacts. (111)B denotes crystal facet of contact layer

b Schematic figure of fabricated device

Results: Fig. 2*a* shows transfer characteristics of a device with $L_G = 20$ nm measured at DC with a Keithley 4200 semiconductor characterisation system. All data are normalised to the total gated periphery of the NWs (7 µm). At $V_{DS} = 0.5$ V, peak g_m is 2.1 mS/µm. Fig. 2*b* shows the scaling behaviour of peak g_m and on-resistance R_{on} versus L_G. R_{on} reaches 220 Ω µm at $L_G = 20$ nm. The total access resistance is estimated to 130 Ω µm from transmission line measurements.

RF measurements were performed at 40 MHz to 67 GHz with an Agilent E8361A vector network analyser. On-chip pad de-embedding as well as off-chip two-port load-reflect-reflect-match calibration was performed. The total pad capacitances were ~20 fF.

A small-signal model was determined from the measured *S*-parameters, with a good fit to the measurement data [8]. Fig. 3 shows measured and modelled (dashed traces) unilateral power gain $|U|$, current gain $|h_{21}|^2$ and maximum available/stable gain (|MAG| and |MSG|) for a device with $L_G = 20$ nm. Extrapolated cut-off frequency f_t is 275 GHz and maximum oscillation frequency f_{max} is 400 GHz.

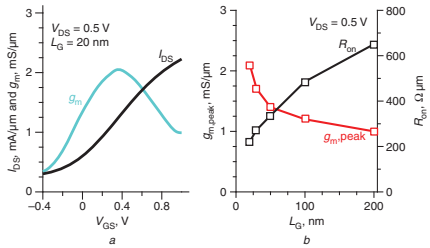

Fig. 2 *Device characteristics at DC*

a Transfer characteristics of a $L_G = 20$ nm device

b Scaling behaviour of peak g_m and R_{on} versus L_G

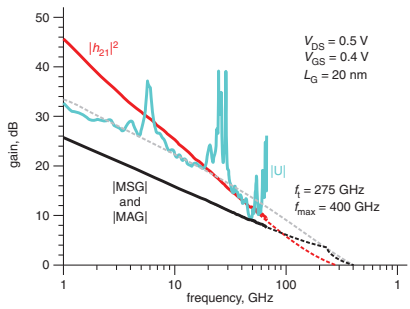

Fig. 3 *Measured and modelled (dashed traces) gain of $L_G = 20$ nm device at $V_{DS} = 0.5$ V*

The small-signal model, which is similar to that in [6], includes both the effect of border traps in the oxide, and impact ionisation. Border traps are modelled using the distributed border trap model in [9]. Border traps introduce a frequency dependency to g_m and g_d, as well as a frequency-dependent oxide loss, and explain the −10 dB slope of $|U|$ versus f [10]. Fig. 4*a* shows $g_{m,peak}$ for an $L_G = 20$ nm device extracted from the small-signal model at DC and 67 GHz (RF). $g_{m,peak}$ increases by ~13% in the latter case, to a maximum of 2.9 mS/µm at $V_{DS} = 1.25$ V, which is attributable to that trap responses are partially disabled at high frequency.

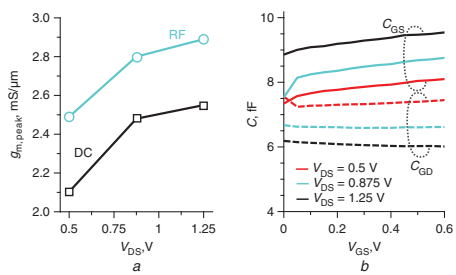

Fig. 4 *Peak g_m and capacitances*

a Peak g_m measured at both 40 MHz (DC) and 67 GHz (RF), for an $L_G = 20$ nm device

b Gate-to-source, C_{GS}, and gate-to-drain, C_{GD}, capacitances measured at different V_{DS}

The effective gate resistance is ~5 Ω, and the source and drain resistances are ~2 Ω. The gate-to-source and gate-to-drain capacitances, C_{GS}

and C_{GD}, are shown in Fig. 4*b*. At $V_{DS} = 0.5$ V, the total gate capacitance $C_{GS} + C_{GD}$ is 15 fF at peak g_m. This includes both the parasitic capacitance from the source and drain gate overlaps, and the intrinsic gate capacitance. The latter is estimated as $C_{gg,int} = (2/3)WLC_{ox}/(C_q + C_{ox})$, with the quantum capacitance $C_q = q^2 m^* / \pi\hbar^2$, which is ~2 fF with $m^* = 0.04m_0$. Thus, RF performance is primarily limited by the parasitic overlap capacitance, which can be lowered by implementation of source and drain spacers.

Fig. 5 shows a benchmark of f_t, f_{max} and the geometric mean $\sqrt{f_t \times f_{max}}$ (dashed traces) for state-of-the-art III–V MOSFETs [11–18]. The geometric mean is 330 GHz for these devices, which is the highest reported value for a III–V MOSFET. Squares show planar devices, and triangles show non-planar devices.

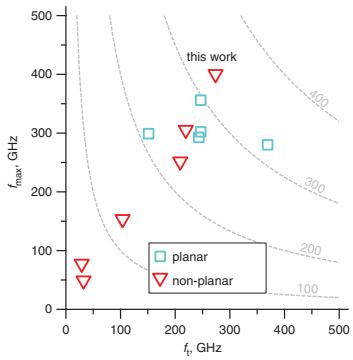

Fig. 5 *Benchmark of RF performance for III–V MOSFETs*

Squares show planar devices, triangles show non-planar devices. V_{DS} and L_G vary between devices, but are 0.5 V and 20 nm, respectively, for this work. Dashed traces show geometric mean

Conclusion: We have demonstrated $L_G = 20$ nm $In_{0.85}Ga_{0.15}As$ tri-gate MOSFETs with high-frequency performance, $f_t = 275$ GHz and $f_{max} = 400$ GHz, recorded at $V_{DS} = 0.5$ V.

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One or more of the Figures in this Letter are available in colour online.

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Paper IV

Paper IV

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”InGaAs tri-gate MOSFETs with record on-current”, *2016 IEEE Int. Electron Devices Meetings (IEDM),* 2016

InGaAs Tri-gate MOSFETs with Record On-Current

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***Abstract*—**We demonstrate InGaAs tri-gate MOSFETs with an on-current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, enabled by an inverse subthreshold slope of *SS* = 66 mV/decade and transconductance of g_m = 3 mS/μm, a Q-factor of 45. This is the highest reported I_{ON} for both Si-based and III-V MOSFETs. These results continue to push III-V MOSFET experimental performance towards its theoretical limit. We find an improvement in *SS* from 81 to 75 mV/dec. as the effective oxide thickness (EOT) is scaled down from 1.4 to 1 nm, as well as improvements in *SS*, g_d and DIBL from reducing the nanowire width. We also find that electron mobility remains constant as the width is scaled to 18 nm.

I. Introduction

An important path for reducing the power density in CMOS technology has been to lower the supply voltage V_{DD}. To maintain sufficient drive current, innovations are required, such as strained channels, novel channel materials and 3D device architectures [1]-[14]. For this purpose, high indium $In_xGa_{1-x}As$ is an attractive channel material due to its excellent electron transport properties, i.e. high electron mobility μ_e and long mean free path λ [6]. While the relatively low DOS of indium-rich $In_xGa_{1-x}As$ is predicted to limit I_{DS} in highly scaled devices, compared to competing technologies such as Si and Ge, this may be offset by the gain from the long λ and high μ_e of $In_xGa_{1-x}As$ [15]. Since this technology likely will be implemented in a 3D channel architecture, such as FinFETs or NWFETs, a further question concerns the dependence of λ on the channel dimensions, i.e. the influence of surface roughness on device performance.

In this work, we demonstrate tri-gate MOSFETs utilizing an $In_{0.85}Ga_{0.15}As$ nanowire (NW) as the channel. By gate oxide scaling, improvements of the surface passivation process and optimization of device dimensions, we achieve a drive current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm. This is a record value for both III-V and Si MOSFETs. We also show that, as the NW width, W_{NW}, is scaled down, electrostatic properties significantly improve, while g_m and λ do not degrade. These results continue to push the limits, as well as explore the potential, of III-V FETs.

II. Device Fabrication

The process flow and schematic images of the device are shown in Fig. 1(a)-(f). The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask, as described elsewhere [4]. Each device consists of a single NW. The composition of the NW is $In_{0.85}Ga_{0.15}As$, as determined by optical characterization [15]. Fig. 1(g) shows an SEM image of an NW with W_{NW} = 90 nm, with the {110} sidewall facets denoted [15]. The inset of Fig. 1(h) shows a schematic figure of the NW cross-section. 30 nm highly doped $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) is subsequently grown by MOCVD as the contact layer, utilizing HSQ as a dummy gate [Fig. 1(h)]. After mesa isolation, the InP in the channel is etched by HCl (10%) in order to form a ~30 nm tall plateau, with the purpose of improving the gate coverage along the bottom of the sides of the NW. 4 cycles of surface oxidation by ozone and diluted HCl etching (digital etching) are performed to reduce the dimensions of the NW. The final height of the NW is H_{NW} = 8 nm, as determined from AFM. Subsequently, Ti/Pd/Au contact metal is evaporated and patterned by lift-off. Surface passivation, by ozone cleaning and $(NH4)_2S$ (10%) for 20 min, is followed by deposition of Al_2O_3/HfO_2 gate oxide (5/35 cycles and EOT ≈ 1 nm, unless otherwise stated). A 12 hour post-deposition anneal step at 100 °C in N_2 atmosphere is performed in-situ. Thermal evaporation and patterning by lift-off of 30/10/150 nm Ni/Pd/Au as the gate metal complete the process [Fig. 1(i)].

III. Results

Fig. 2 shows transfer characteristics of a tri-gate MOSFET with L_G = 75 nm and W_{NW} = 25 nm. All normalization is done to the total gated NW periphery, i.e. the three sides of the tri-gate. Peak transconductance is $g_m \approx 3.0$ mS/μm at V_{DS} = 0.5 V. Subthreshold characteristics of the same device are shown in Fig 3. At V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, I_{ON} = 650 μA/μm. The gate current is I_G < 1 nA/μm. Minimum inverse subthreshold slope *SS* reaches 66 mV/decade (Fig. 4) at V_{DS} = 0.5 V, and 61 mV/decade at V_{DS} = 0.05 V. The drain-induced barrier-lowering (DIBL) is 65 mV/V, measured at I_{DS} = 1 μA/μm. The on-resistance of this device is R_{ON} = 175 Ω·μm at V_{GS} = 1 V. Output characteristics for W_{NW} = 90 and W_{NW} = 25 nm devices with L_G = 75 nm are shown in Fig. 5 and 6, respectively. The output conductance of these devices is g_d = 0.45 and 0.25 mS/μm (voltage gain is 5.5 and 10) at $V_{GS} - V_T = V_{DS}$ = 0.5 V.

Minimum *SS* versus L_G is shown for W_{NW} = 25 nm and W_{NW} = 90 nm devices at V_{DS} = 0.05 and 0.5 V (Fig. 7). The reduced W_{NW} offers improved resilience against short channel effects (SCEs), but at L_G = 25 nm, *SS* is degraded (110 mV/decade) even at W_{NW} = 25 nm. Minimum *SS* versus W_{NW} is shown in Fig. 8 for L_G = 75 nm devices at V_{DS} = 0.5 V. Average minimum *SS* improves from approximately 95 mV/dec. for W_{NW} > 90 nm to *SS* < 70 mV/dec. for W_{NW} < 30 nm due to enhanced electrostatic control. The lowest *SS* of a device at this bias is 64 mV/dec. The theoretical values

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indicate *SS* obtained from a solution of Laplace's equation modeling the full 3D structure of the nanowire using COMSOL. To improve performance at short L_G, W_{NW} must be further reduced. Scaling of H_{NW} will improve *SS* but reduce the aspect ratio (AR), which is undesirable. Moreover, the implementation of a wider band gap back-barrier, such as InAlAs or a BOX layer, is also expected to improve resilience to SCEs. Fig. 9 shows median (crosses) and mean (squares) minimum *SS* for four samples with L_G = 75 nm and W_{NW} = 25-30 nm at both V_{DS} = 0.05 and 0.5 V (~40 devices each). Sample D has 5/50 cycles Al_2O_3/HfO_2. Sample C has 5/45 cycles Al_2O_3/HfO_2. Sample B and A have 5/35 cycles Al_2O_3/HfO_2. In addition, samples D, C and B where passivated with $(NH_4)_2S$ (10%) produced by Merck, while sample A was passivated with $(NH_4)_2S$ (10%) produced by Sigma-Aldrich. Fig. 10 shows mean minimum *SS* of samples D to B versus EOT (1 cycle = 1.1 Å, κ = 18 and 9 for HfO_2 and Al_2O_3). These results indicate an improvement both from oxide scaling (average *SS* improves from 81 to 75 mV/dec. for EOT from ~1.4 nm to ~1 nm), and from optimization of the surface passivation parameters (mean *SS* improves from 75 to 70 mV/dec. for sample B to A). The trend indicates that *SS* may be further improved by scaling of the EOT. We do not observe a clear trend of g_m versus EOT.

Fig. 11 shows g_d versus W_{NW} at V_{DS} = 0.5 V and $V_{GS} - V_T$ = 0.5 V for L_G = 75 nm devices. Average g_d is reduced from 0.5 mS/µm at W_{NW} = 90 nm to ~0.2 mS/µm at W_{NW} = 25 nm. The DIBL measured at 1 µA/µm is shown in Fig. 12. It is similarly reduced from 170 mV/V at W_{NW} = 90 nm, to 38 mV/V at W_{NW} = 25 nm. The threshold voltage (V_T) defined at I_{DS} = 1 µA/µm increases in narrow NWs (Fig. 13). The trend approximately follows calculated values from an effective mass quantum wire model, indicating that the V_T increase is due to quantum confinement.

Fig. 14 shows g_m versus W_{NW}. The highest g_m observed in these devices is ~3.3 mS/µm (SS_{sat} = 90 mV/dec.) at V_{DS} = 0.5 V and L_G = 50 nm. g_m increases as W_{NW} is scaled down to approximately 35 nm from planar architecture (W_{NW} = 1 µm). This may be explained by that narrow NWs are more Indium-rich, due to interactions with the HSQ mask during MOCVD growth, which may improve mobility as well as change the D_{it} distribution [15]. This shows that the improvement of g_d with W_{NW}, is in fact due to improved electrostatics. The inset of Fig. 15 shows average values of g_m versus L_G for W_{NW} = 25 nm. Dashed traces show an analytical quasi-ballistic model with λ = 140 nm fitted to the measured data.

I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm is shown in Fig. 15 versus both W_{NW} and L_G (inset). I_{ON} increases from 200 to 650 µA/µm as W_{NW} goes from 1 um (planar) to 25 nm, due to the simultaneous improvements of *SS* (100 to 66 mV/dec.) and g_m (1.1 to 3 mS/µm). I_{ON} peaks at L_G = 75 nm, which is explained by the degraded *SS* (Fig. 7) and that g_m only improves slightly (Fig. 14) for shorter L_G.

These devices exhibit quantized conductance at 10 K due to subband splitting in a 1D channel (inset of Fig. 16). From the conductance steps, the transmission is obtained. The device in Fig. 3 shows a transmission of T = 0.67, which indicates quasi-ballistic transport. Fig. 16 shows electron mobility μ_e and λ for NWs with W_{NW} = 18 – 32 nm calculated from quantized conductance. To obtain μ_e, we use the Einstein relation and a correction factor of 1.6 to account for degeneracy [15]. We note that this method is not strongly influenced by D_{it}. No dependency versus W_{NW} is observed, which correlates with g_m versus W_{NW} with W_{NW} < 35 nm, explained by small surface scattering. Since g_m is temperature-independent, the same is true for μ_e.

A benchmark of the I_{ON} (at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm) for state-of-the-art III-V planar and non-planar MOSFETs is shown in Fig. 17. The value of 650 µA/µm presented in this work is the record value of both categories. The same is true for the quality factor Q = g_m/SS, which is 45 in this work (Fig. 18). Fig. 19 compares I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm for various technologies. $I_{DS,surface}$ is I_{ON} normalized to the gated channel periphery, while $I_{DS,chip}$ is normalized to the chip surface width including the specified pitch size. $I_{ON,chip}$ in our devices is lower than that of 14 nm FinFET (570 compared to 650 µA/µm for a pitch of 42 nm), which demonstrates the importance of high AR in 3D channels, but we observe a two-fold increase in $I_{ON,surface}$ over 14 nm FinFET technology, which is due primarily to the high μ_e of $In_xGa_{1-x}As$ [16].

IV. Conclusion

We have demonstrated $In_xGa_{1-x}As$ tri-gate MOSFETs with a record on-current of 650 µA/µm at V_{DD} = 0.5 V and I_{ON} = 100 nA/µm, *SS* = 66 mV/decade and g_m = 3.0 mS/µm. From data versus NW width, we observed improvements in *SS*, DIBL and g_d for scaled down NWs. Furthermore, we observed improvements both from oxide scaling the surface passivation process. From low-temperature measurements we obtain μ_e and λ, which remain high, 2750 cm^2/Vs and 150 nm, respectively, even in scaled NWs.

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V. References

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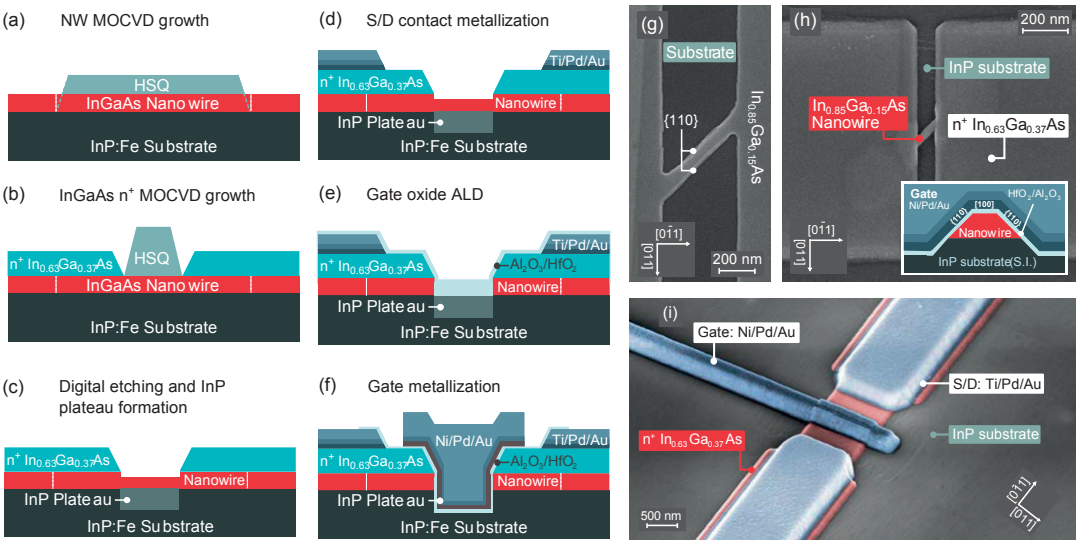

Fig. 1: Schematic figures SEM images of the device fabrication process. (a) NW formation utilizes selective area MOCVD growth with an EBL-defined HSQ hard mask. (b) Contacts are defined using an HSQ dummy gate and MOCVD regrowth of n^+ $In_{0.63}Ga_{0.37}As$. (c) NW is scaled down using "digital etching". (d) S/D metal is deposited by evaporation and lift-off. (e) A bilayer of Al_2O_3/HfO_2 is used as the gate oxide. (f) Ni/Pd/Au is evaporated as the gate metal. (g) SEM image of a 90 nm wide NW with the {110} side facets denoted. (h) The device after contact regrowth. Inset shows a schematic cross-section of the NW in the finished device. (i) False-color SEM image of the finished device. The NW is located at the center of the 1 µm wide mesa.

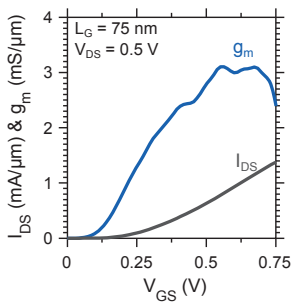

Fig. 2. Transfer characteristics for a device with W_{NW} = 25 nm.

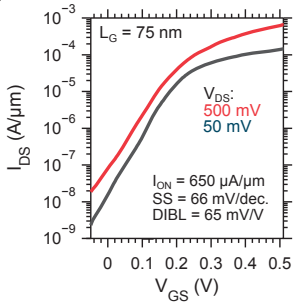

Fig. 3: Subthreshold characteristics for the same device as in Fig. 2.

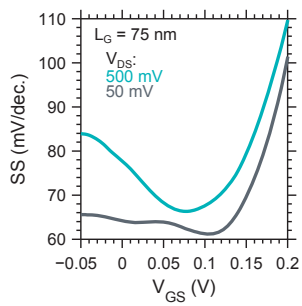

Fig. 4: Subthreshold slope versus V_{GS} for the same device as in Fig. 2.

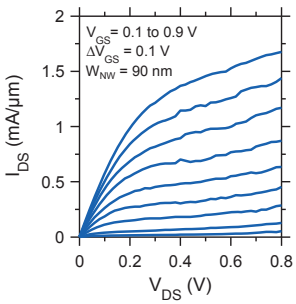

Fig. 5: Output characteristics for a device with L_G = 75 nm and W_{NW} = 90 nm.

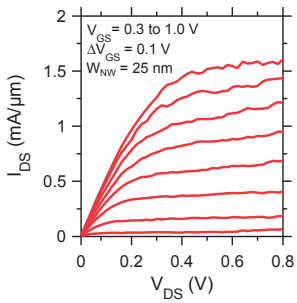

Fig. 6: Output characteristics for a device with L_G = 75 nm and W_{NW} = 25 nm.

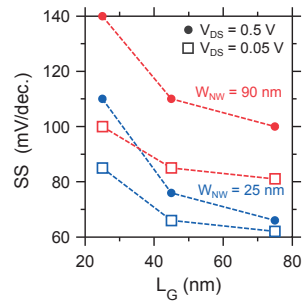

Fig. 7: Subthreshold slope for devices with different W_{NW} and L_G.

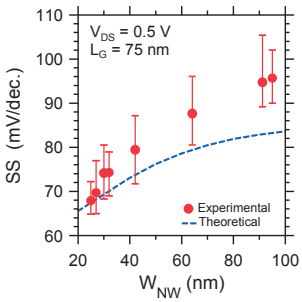

Fig. 8: Subthreshold slope versus W_{NW} at V_{DS} = 0.5 V and L_G = 75 nm.

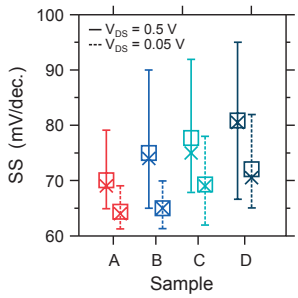

Fig. 9: Mean (squares) and median (crosses) *SS* for different samples.

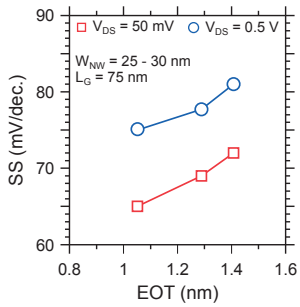

Fig. 10: Average subthreshold slope (each point is ~40 devices) versus EOT.

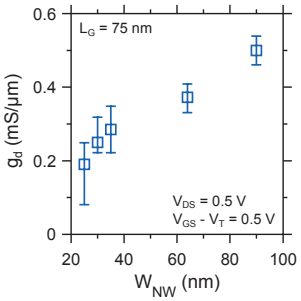

Fig. 11: Output conductance versus W_{NW}, measured at $V_{DS} = V_{GS} - V_T = 0.5$ V.

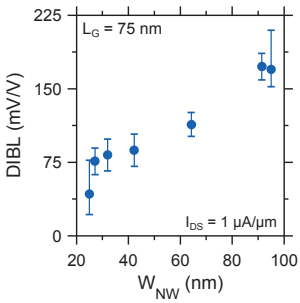

Fig. 12: DIBL versus W_{NW} measured at I_{DS} = 1 μA/μm.

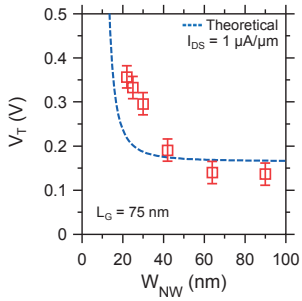

Fig. 13: Threshold voltage versus W_{NW}. Dashed traces show a QW model.

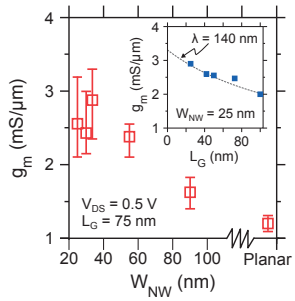

Fig. 14: Peak g_m versus W_{NW} and (inset) L_G, all measured at V_{DS} = 0.5 V.

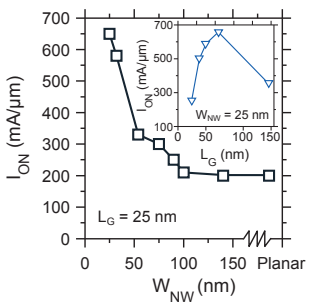

Fig. 15: I_{ON} versus W_{NW} and L_G at I_{OFF} = 100 nA/μm.

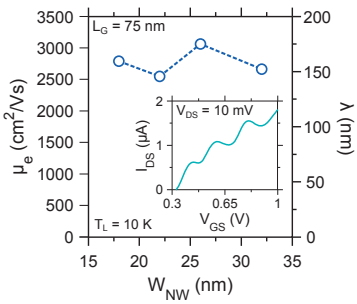

Fig. 16: μ_e and λ, measured from quantized current (inset), versus W_{NW}.

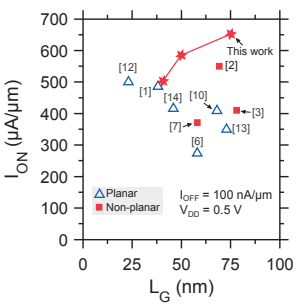

Fig. 17: Benchmark of I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm.

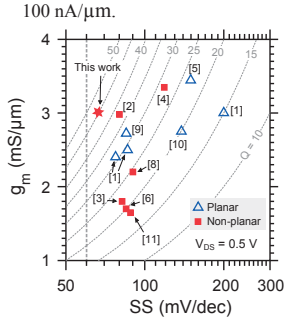

Fig. 18: Benchmark of the quality factor g_m/SS at V_{DS} = 0.5 V.

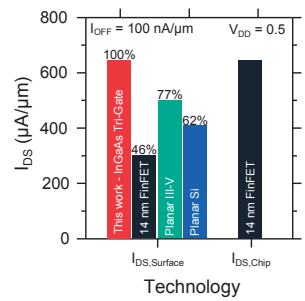

Fig. 19: Benchmark of various technologies.

Paper V

Paper V

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, ”InGaAs nanowire MOSFETs with I_{ON}= 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V”, *Symposium on Very Large Scale Integrated Circuits and Technology (VLSI)”,* 2016

InGaAs Nanowire MOSFETs with I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V

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Abstract

We report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs (NWFETs) with record performance in several key VLSI metrics. These devices exhibit I_{ON} = 555 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), I_{ON} = 365 µA/µm (at I_{OFF} = 10 nA/µm and V_{DD} = 0.5 V) and a quality factor Q ≡ g_m/SS of 40, all of which are the highest reported for a III-V as well as silicon transistor. Furthermore, a highly scalable, self-aligned gate-last fabrication process is utilized, with a single nanowire as the channel. The devices use a 45° angle between the nanowire and the contacts, which allows for up to a 1.4 times longer gate length at a given pitch.

Introduction

$In_xGa_{x-1}As$ MOSFETs are expected to deliver high on-currents at a reduced V_{DD} of 0.5 V, making them suitable for VLSI applications [1]-[17]. This is due to their high mobility, which enables increased transconductance g_m at a given L_G. For instance, we have recently demonstrated $In_{0.85}Ga_{0.15}As$ NWFETs with g_m = 3.3 mS/µm, surpassing that of all other III-V and silicon transistors, including HEMTs [4]. However, to achieve high I_{ON} at a specified I_{OFF} and V_{DD} = 0.5 V comparable to state-of-the-art silicon technology, the subthreshold slope must be near 60 mV/decade. This is challenging in III-V technology due to the oxide interface quality and narrow band gap, causing e.g. band-to-band-tunneling in the off-state. Recently, planar InAs MOSFETs with I_{ON} matching or surpassing that of silicon technology were reported [12]. In this work, we report on NWFETs with a new record of I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V.

Device Fabrication

Fig. 1 shows a schematic of the fabricated device, and the process flow [17]. The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask. The composition of the nanowire layer is $In_{0.63}Ga_{0.37}As$, while the nanowire is $In_{0.85}Ga_{0.15}As$, as determined by optical characterization. Fig. 2(a)-(c) demonstrate the scalability of the selective growth process. A high-density nanowire-cluster with nanowire spacing of <10 nm is shown in fig. 2c. In this work, we characterize single-nanowire devices. The highly doped $In_{0.63}Ga_{0.37}As$ (N_D = 5 × 10^{19} cm^{-3}) contact layer is formed from a subsequent MOCVD growth step using HSQ as a dummy gate [Fig. 2(d)]. A 45° angle between the nanowire and the contacts is chosen in order to obtain optimal crystal facets. At a given pitch, this will also improve electrostatic control by allowing a longer gate length. After mesa isolation, Ti/Pd/Au is patterned and evaporated as the contact metal. The InP in the channel region is etched by HCl (1:1), in order for the metal to properly cover the sides of the nanowire. Several cycles of surface oxidation by ozone and diluted HCl etching is performed in order to reduce the dimensions of the nanowire. Surface passivation, by $(NH4)_2S$ (1:1) for 20 min, is followed by deposition of Al_2O_3/HfO_2 (EOT ≈ 1.5 nm) by ALD at 300/100°C. Subsequently, an in-situ 12 hour post-deposition annealing step at 100°C in N_2 atmosphere is performed. Ni/Pd/Au gate metal patterning and evaporation completes the process.

Results

Fig. 3(a)-(c) show subthreshold, transfer and output characteristics of an L_G = 70 nm NWFET with nanowire width and height W_{NW}/H_{NW} = 25/7 nm. The peak transconductance is $g_{m,peak}$ = 2.85 mS/µm at V_{DS} = 0.5 V. The subthreshold characteristics for the same device are shown in Fig. 4. The subthreshold slope (SS) is 80 mV/decade at both V_{DS} = 0.5 V and 50 mV. The drain-induced barrier-lowering (DIBL) is 43 mV/V at I_{DS} = 1 µA/µm. The device exhibits I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, which is the highest reported value for a MOSFET. The quality factor Q ≡ g_m/SS is 35 for this device. The on-resistance is R_{ON} = 177 Ωµm. The specific contact resistivity is $\rho_C = 7\times10^{-8}$ Ωcm^{-2} and the sheet resistance of the n^+ $In_{0.63}Ga_{0.37}As$ contact layer is R_{Sh} = 70 Ω/□, both obtained from TLM measurements.

Fig. 4 shows transfer characteristics for another L_G = 70 nm device with $g_{m,peak}$ = 2.65 mS/µm at V_{DS} = 0.5 V. The average SS over one, two and three decades is 65, 69 and 73 mV/decade, respectively, all at V_{DS} = 0.5 V. This device shows I_{ON} = 535 µA/µm at I_{OFF} = 100 nA/µm and I_{ON} = 365 µA/µm at I_{OFF} = 10 nA/µm, V_{DD} = 0.5 V. This is the highest reported I_{ON} at I_{OFF} = 10 nA/µm. DIBL is 56 mV/V at I_{DS} = 1 µA/µm. The quality factor Q ≡ g_m/SS is 40 for this device, which is the highest reported Q-factor for a MOSFET. The difference in SS between these devices may in part be explained by the discrete nature of traps in the small channel area (2 × 10^{-3} µm^2).

The hysteresis (Fig. 5) is ΔV_T = 60 mV for V_{GS} = 0.2-1.0 V, indicating high-quality oxide and oxide interface. I_{OFF} versus I_{ON} for several devices with L_G = 70 nm and W_{NW}/H_{NW} = 25/7 nm is shown in Fig. 6, measured at a swing of V_{DD} = 0.5 V. Fig. 7 shows SS versus L_G. Error bars show the standard deviation. SS and DIBL versus nanowire width W_{NW} is shown in Fig. 8 (H_{NW} = 7 nm), with data points offset for clarity. Improved electrostatic control from use of smaller nanowires can clearly be observed. The trend indicates that SS can be further reduced by additionally scaling down W_{NW}. Fig. 9 and 10 show benchmarks of I_{ON} and Q for various planar and non-planar MOSFETs.

Conclusions

We have demonstrated highly scalable nanowire MOSFETs with record high performance in several key VLSI metrics. We have shown a device with g_m = 2.85 mS/µm, SS = 80 mV/decade and I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V. We have also shown a device with g_m = 2.65 mS/µm and SS = 65 mV/decade, which gives a quality factor Q = 40.

Acknowledgements

This work was supported in part by the Swedish Research Council, in part by the Knut and Alice Wallenberg Foundation, in part by the Swedish Foundation for Strategic Research, and in part by the European Union H2020 program INSIGHT (Grant Agreement No. 688784).

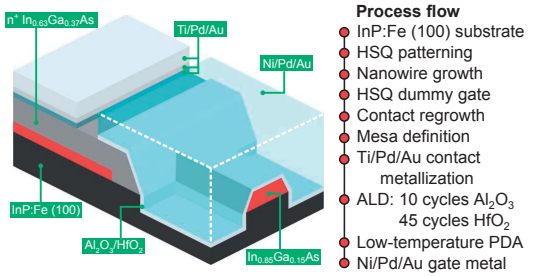

Fig. 1. Schematic of the final device, as well as the device fabrication process flow.

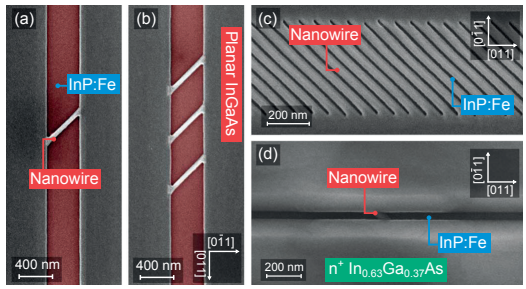

Fig. 2. (a-c) False-color SEM images showing the scalability of the NW fabrication process. (d) The device after contact regrowth.

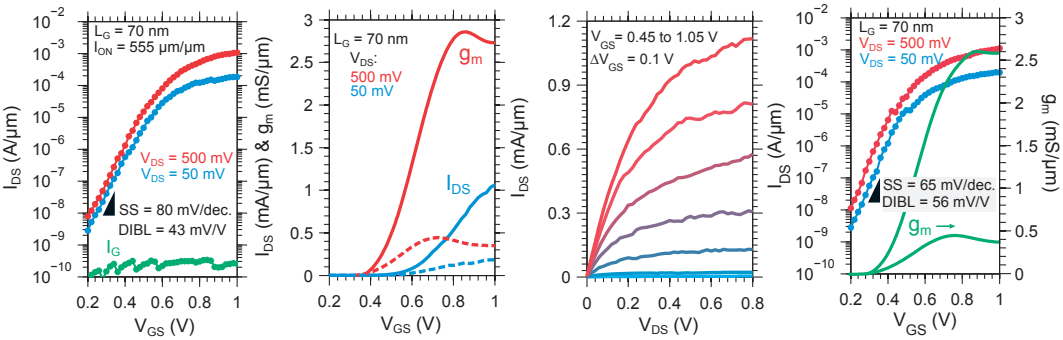

Fig. 3. (a) Subthreshold, (b) transfer and (c) output characteristics of the same L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device. I_{ON} = 555 μA/μm at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

Fig. 4. I_{DS}-V_{GS} for an L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device.

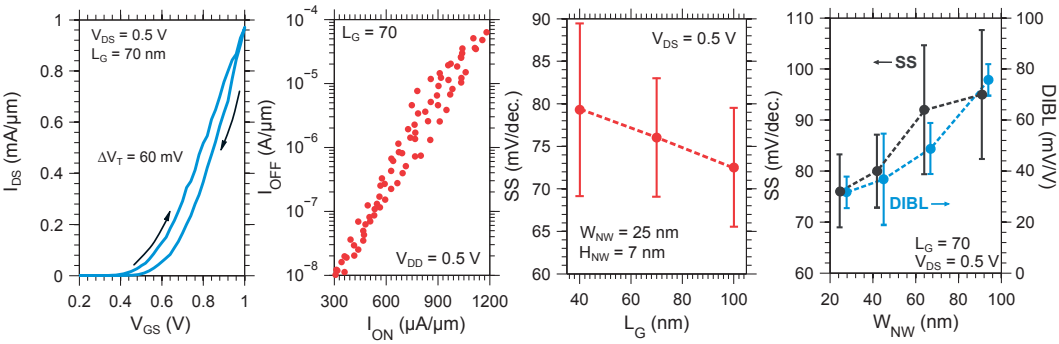

Fig. 5. Hysteresis measurement of an L_G = 70 nm device.

Fig. 6. I_{OFF} versus I_{OFF} for L_G = 70 nm devices.

Fig. 7. SS versus L_G for W_{NW} = 25 nm devices.

Fig. 8. SS and DIBL versus W_{NW} with L_G = 70 nm and H_{NW} = 7 nm.

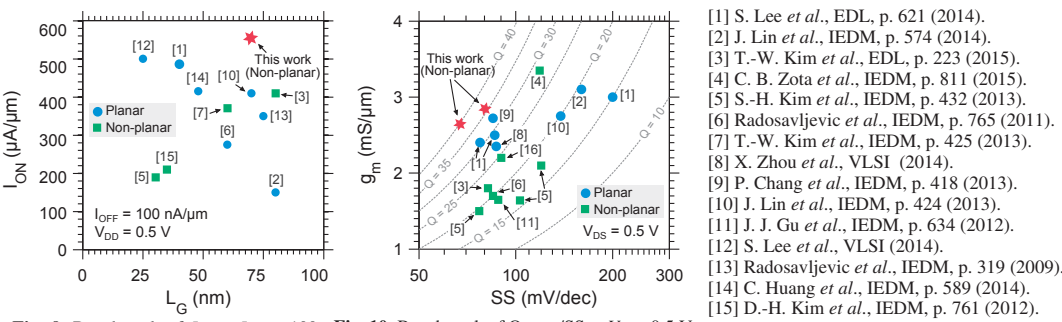

Fig. 9. Benchmark of I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

Fig. 10. Benchmark of Q = g_m/SS at V_{DS} = 0.5 V for various planar and non-planar III-V FETs.

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Paper VI

Paper VI

F. Lindelöw, M. Heurlin, G. Otnes, V Dagyte, D. Lindgren, O. Hultin, K. Storm, L. Samuelson, M. Borgström , ”Doping evaluation of InP nanowires for tandem junction solar cells”, *Nanotechnology,* 2016

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Doping evaluation of InP nanowires for tandem junction solar cells

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Abstract

In order to push the development of nanowire-based solar cells further using optimized nanowire diameter and pitch, a doping evaluation of the nanowire geometry is necessary. We report on a doping evaluation of n-type InP nanowires with diameters optimized for light absorption, grown by the use of metal–organic vapor phase epitaxy in particle-assisted growth mode using tetraethyltin (TESn) as the dopant precursor. The charge carrier concentration was evaluated using four-probe resistivity measurements and spatially resolved Hall measurements. In order to reach the highest possible nanowire doping level, we set the TESn molar fraction at a high constant value throughout growth and varied the trimethylindium (TMIn) molar fraction for different runs. Analysis shows that the charge carrier concentration in nanowires grown with the highest TMIn molar fraction (not leading to kinking nanowires) results in a low carrier concentration of approximately $10^{16}\,cm^{-3}$. By decreasing the molar fraction of TMIn, effectively increasing the IV/III ratio, the carrier concentration increases up to a level of about $10^{19}\,cm^{-3}$, where it seems to saturate. Axial carrier concentration gradients along the nanowires are found, which can be correlated to a combination of changes in the nanowire growth rate, measured *in situ* by optical reflectometry, and polytypism of the nanowires observed in transmission electron microscopy.

S Online supplementary data available from stacks.iop.org/NANO/27/065706/mmedia

Keywords: Hall effect, nanowires, resistivity, doping, carrier concentration, InP

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, nanowire-based solar cell technology has received increasing interest [1]. Progress has been made to lower production costs [2], and new advances in areas such as surface cleaning [3] and passivation [4], as well as the use of core–shell structures and perovskite nanowires [5] have been investigated to increase solar cell efficiency further. Due to the small diameter of the nanowire it is possible to combine normally incompatible lattice mismatched materials [6]. In addition, the antenna-like geometry of the nanowires leads to the resonant in-coupling of light [7–10]. These two effects carry the promise of highly efficient multi-junction nanowire solar cells with a fraction of the materials used in epitaxial thin-film multi-junction technology [11]. We have previously reported a 13.8% efficiency of InP nanowire solar cells, where the nanowires covered only 12% of the active surface [12]. In order to increase solar energy harvesting efficiency further, we have developed particle-assisted nanowire synthesis from metal particles, defined by nanoimprint lithography, with the theoretically determined optimal dimensions for an InP nanowire solar cell [13]. The use of nanoimprinting enables the formation of periodic nanowire arrays, suitable for solar cell applications on a large substrate area [14, 15]. Nanowire doping, which depends strongly on growth parameters and

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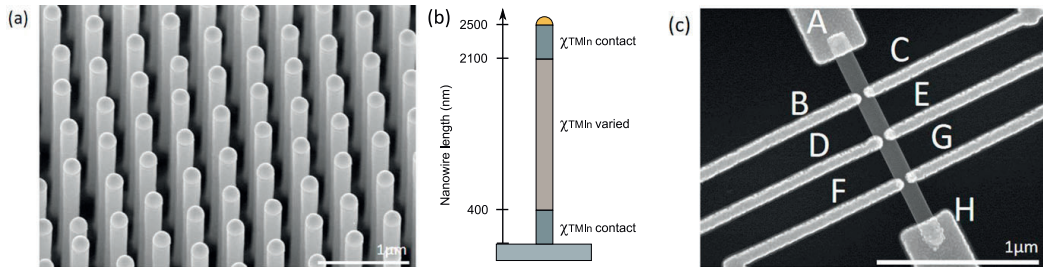

Figure 1. (a) SEM micrograph of an as-grown InP nanowire array using $\chi\text{TMIn} = 10.4 \times 10^{-5}$. The nanowires were grown from gold particles defined by nanoimprint, metal evaporation and lift-off with a diameter of 200 nm and a pitch of 500 nm. (b) Schematic image of a grown nanowire with the desired segment lengths. (c) SEM image of a nanowire contacted for Hall measurements and four-probe measurements with the different contacts marked as A-H.

the nanowire diameter and pitch, will set limits on performance and needs to be evaluated for patterns with predicted optimal dimensions [16]. Doping levels define the electric field across the p-i-n junction, which is used to separate photo-excited carriers. Additionally, the dopant precursors used should offer dopant incorporation which is high enough to enable electrically transparent contacts, and the formation of the Esaki tunnel junction connecting junctions of different band-gaps matching the solar spectrum in a multi-junction architecture. The preferred dopant precursor offers control from low to high doping levels, but does not severely affect nanowire growth dynamics. Tetraethyltin (TESn) has previously been used for this purpose with InP [17] as well as GaAs [18] nanowire doping.

In this paper, we report on the particle-assisted synthesis and doping evaluation of n-doped InP nanowires with dimensions optimized for light in coupling using TESn as a dopant precursor.

2. Experimental

The InP nanowires were grown on an InP (111)B:Zn substrate in metal particle-assisted growth mode using Au particles defined by nanoimprint lithography, reactive ion etching, metal evaporation and lift-off as catalysts. The growth was performed in a low-pressure (100 mbar) Aixtron 200/4 metal-organic vapor phase epitaxy (MOVPE) system with a total flow of 13 l min^{-1} using hydrogen as the carrier gas. Trimethylindium (TMIn), phosphine (PH_3) and TESn were used as precursor sources where the TMIn molar fraction was varied between $\chi\text{TMIn} = 3.0 \times 10^{-5}$–$10.4 \times 10^{-5}$, and the PH_3 and TESn molar fractions kept constant at $\chi\text{PH3} = 6.9 \times 10^{-3}$ and $\chi\text{TESn} = 6.4 \times 10^{-5}$. The growth temperature was 440 °C and hydrogen chloride (HCl) was supplied *in situ* to suppress radial growth at a molar fraction of $\chi\text{HCl} = 4.6 \times 10^{-5}$ [19]. For higher χTMIn than 10.4×10^{-5}, the nanowires were found to be kinked after growth. An example of the nanowires that were grown can be seen in figure 1. During nanowire array synthesis, a LayTec EpiR DA UV optical reflectometry system was used to measure the interference signal between the light reflected at the nanowire–substrate interface and the top of the nanowires. The interference signal was used to continuously monitor the average nanowire length *in situ* [20] and thus limit the number of experiments needed. The nanowire array had a pitch of 500 nm, and the nanowires had a diameter of 200 nm and were about 2.5 μm long. The growth time was adjusted to give approximately the same nanowire length, independent of χTMIn, except for the nanowires grown at $\chi\text{TMIn} = 3.0 \times 10^{-5}$, for which growth was stopped at 1.5 μm due to the slow growth rate of 0.2 nm s^{-1}. The nanowires were designed with 400 nm n-doped end segments at the top and bottom, grown using $\chi\text{TMIn} = 8.9 \times 10^{-5}$, to enable consistent contact properties of all nanowire types.

After growth, transmission electron microscopy (TEM) was performed on three samples with $\chi\text{TMIn} = 3.0 \times 10^{-5}$, 5.9×10^{-5} and 8.9×10^{-5} using a JEOL 3000F 300 kV microscope. Two nanowires were investigated from each sample by aligning them in the $[1\bar{1}0]$ zone axis and acquiring images along the nanowire length to probe any changes in atomic structure.

For electrical measurements the nanowires were mechanically transferred to insulated silicon measurement substrates with predefined bond pads. Electrical contacts at 30, 50 and 70% (base, center and top) of the nanowire length were defined by electron beam lithography followed by a 15 s native oxide etch in buffered oxide etch 10:1, after which metal evaporation of 10 nm titanium and 150 nm gold was carried out before lift-off. The electrical characterization methods have been described in the literature [21] and consisted of room temperature four-probe resistivity measurements [22] as well as Hall measurements [23, 24].

The four-probe resistivity measurements were performed in a probe station Cascade 1000B where a voltage sweep was applied between end contacts A and H, generating a current through the nanowire, see figure 1(c). The voltage drop between contacts B-D (base), B-F (center) and D-F (top) were plotted against the current measured in A-H in order to measure the resistance of the nanowire device at various positions. Resistivity was calculated from the resistance using segment lengths and the nanowire cross sectional area measured in scanning electron microscope (SEM) images. The use of four-probe resistivity measurements gives information

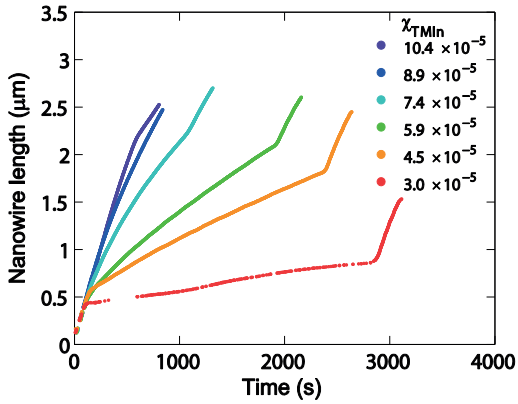

Figure 2. Average length of nanowire array as a function of time for the six different molar fractions of TMIn that yielded uniform nanowires. The different growth rates at the top and bottom of the nanowires occur due to the growth of contact segments with constant $\chi\text{TMIn} = 8.9 \times 10^{-5}$.

on the nanowire-related (intrinsic) transport properties, which in such a measurement can be separated from the extrinsic, contact-related properties.

The spatially resolved Hall measurements were performed in a Hall station setup where a current was sourced between A-H, a magnetic field of −0.2 to 0.2 T was applied perpendicular to the substrate and the corresponding Hall voltages were measured in pairs V_{BC} (base), V_{DE} (center) and V_{FG} (top). For the two lowest doped samples, the Hall voltage was also measured using a magnet with a maximum magnetic field of 2 T to increase the Hall voltage, effectively increasing the signal-to-noise ratio. Each measurement of the contacted nanowire, including nanowire diameter, length and contact position was modelled in COMSOL Multiphysics, where the current continuity equation was solved using a finite element method. The Hall voltage as a function of magnetic field was simulated for various doping levels and compared to the measured Hall voltage of each Hall pair to extract the charge carrier concentration at the three different positions along the wire. For more information regarding measurement technique and simulation see [23].

3. Results and discussion

In figure 2 the length of the nanowires grown with various χTMIn as a function of growth time can be seen as extracted from the *in situ* measurements. The growth rate of the contact segment using $\chi\text{TMIn} = 8.9 \times 10^{-5}$ is about 4 nm s^{-1} for the bottom segment and 2 nm s^{-1} for the top segment in all samples. This can be seen in figure 2 where the top and bottom contact segments have similar growth rates for all growth runs, but the growth rate in the middle segment is strongly affected by the change in χTMIn. Here, the growth rate varies from approximately 0.2 nm s^{-1} for $\chi\text{TMIn} = 3.0 \times 10^{-5}$ to 4 nm s^{-1} for $\chi\text{TMIn} = 10.4 \times 10^{-5}$. Interestingly, the nanowire growth rate increases with χTMIn to the power of 2.4. At this point we cannot determine the physical principle governing this behavior. Growth occurring in the kinetically limited temperature regime is complex, and a complete description requires further study. However, TMIn is known to strongly catalyze the pyrolysis of PH_3 at these low growth temperatures [25], which could explain why adding TMIn results in more In as well as P at the growth front. We note that there is also a trend of decreasing growth rate in the middle segment as the nanowires grow longer and that this is more significant for nanowires grown with higher χTMIn. The decreasing growth rate with increasing nanowire length can be attributed to the decrease in growth species arriving at the particle–semiconductor growth interface through surface diffusion for longer nanowires.

In figure 3(a) the results from the four-probe resistivity measurements at the top, center and base of the varied χTMIn nanowire segment are plotted as a function of the χTMIn. A decrease in χTMIn leads to a decrease in nanowire resistivity, indicating higher doping levels as an effect of the relatively higher group IV/III ratio. For sufficiently low amounts of χTMIn, a plateau level is reached with a small increase in resistivity at the top of the nanowires. This indicates saturation in the doping level for high IV/III ratios. From each nanowire array, at least three nanowires had successful four-probe measurements, see table S1 for further information.

To verify the trends observed in the resistivity measurements we extracted the carrier concentration from spatially resolved Hall measurements, see figure 3(b). The results show charge carrier concentrations in the nanowires spanning from as low as approximately 1×10^{16} cm^{-3} up to as high as 5×10^{19} cm^{-3} (InP becomes degenerately doped at 5.7×10^{17} cm^{-3} [26]). Thus, a large span with high control of the n-doping level is achieved by varying χTMIn only and keeping χTESn constant. The high carrier concentrations measured were also verified with photoluminescence measurements with methodology according to the literature [27], see supplementary information figures S1 and S2 available at stacks.iop.org/NANO/27/065706/mmedia.

The Hall measurement data agrees with the resistivity measurements: by decreasing χTMIn, higher carrier concentrations (lower resistivities) are observed until a plateau is reached, accompanied by a decrease in carrier concentration at the top of the NWs. A plot of the four-probe resistivity as a function of the carrier concentration from the Hall measurements can be seen in the online figure S3.

From the spatial doping gradient, we note that the top of the wires grown at higher χTMIn show a higher carrier concentration than the bottom. This could be explained by the observed trend of decreasing growth rate as the nanowires get longer for higher χTMIn, as seen in figure 2. The drop in growth rate indicates that less In reaches the growth front. For low χTMIn the trend in growth rate as well as carrier gradient is less pronounced, and for very low χTMIn the carrier gradient is observed to be inverted, indicating that the IV/III ratio decreases with the length of the nanowire. The effect could be explained by an increasing In-adatom surface

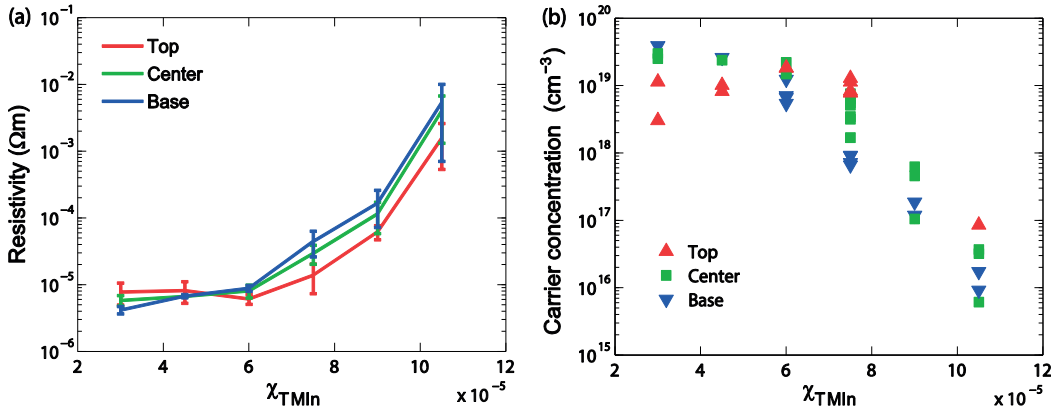

Figure 3. The measured four-probe resistivity (a) and carrier concentration from Hall measurements (b) measured in the base, center and top of the nanowire versus χTMIn. The error bars in (a) show the standard deviation of all the measurements for the specified TMIn molar fraction and nanowire part.

diffusion length with decreasing χTMIn, similar to results on GaAs nanowire growth when decreasing the trimethylgallium molar fraction [18]. However, our *in situ* measurements indicate no increase in the growth rate for nanowires with low χTMIn. Another possibility is that the use of relatively lower χTMIn accompanied by increased growth times due to a decreasing growth rate could lead to additional parasitic radial growth of highly doped layers at the bottom of the nanowires [28]. To test this theory we etched the nanowires in piranha etch solution (H_2SO_4:H_2O_2:H_2O, 1:1:20) for 1 min to decrease the nanowire diameter by 10–20 nm, and evaluated them electrically. The results indicate no change in the direction of the carrier gradient, thus ruling out the possibility of radial growth affecting the measurements (see the supplementary information figure S4).

A third possibility is that the well-known polytypic behavior of III-V nanowires affects the electrical measurements [29]. Previous doping evaluations have shown a correlation between the amount of stacking faults in the nanowires and the measured carrier concentration [30]. Nanometer-sized segments of wurtzite and zincblende crystal structure can act as quantum wells for carriers and effectively trap charges, leading to an apparent lower doping concentration [30]. We conducted a TEM study to evaluate the presence of stacking faults as a function of position in the nanowires in an attempt to establish any correlation to the observed carrier gradients. Figure 4(a) shows a TEM image of a nanowire grown with χTMIn $= 3.0 \times 10^{-5}$. The first part of the middle segment consists of a pure zincblende crystal structure while twin planes start to appear after approximately half the segment length. The twin density is increased further up into the middle segment and also causes a more uneven morphology. This is in line with the Hall measurements, where the carrier concentration at the top of the wire is lower than at the bottom, see figure 3(b). In figure 4(b), where a TEM image of a nanowire grown at χTMIn $= 8.9 \times 10^{-5}$ is shown, the twin density also increases towards the top of the wire. However, the stacking defect density is already substantial at the bottom of the measurement segment. Thus, the relative change in stacking fault density and its effect on electrical properties is less than for nanowires grown with low χTMIn, which show a transition from pure zincblende to a mixed crystal structure [29].

The formation of different carrier concentration gradients can thus be understood by a combination of two effects. For high χTMIn a decreasing growth rate for increasing nanowire length gives an effectively lower In concentration, and thus a higher IV/III ratio at the nanowire top rendering a higher doping level here. The change in crystal structure along the nanowire for high χTMIn is at the same time not enough to affect the electrical properties significantly. For low χTMIn the change in crystal structure along the nanowire is significant, transitioning from pure zincblende to zincblende with twin planes. These trap some of the carriers and thus reduce the carrier concentration. This causes an inversion of the carrier concentration gradient observed for high χTMIn.

4. Conclusions

Based on four-probe resistivity measurements and Hall measurements, we report on the ability to fine tune the doping levels of InP nanowires with carrier concentrations spanning between non-degenerate doping of 1×10^{16} cm^{-3} to degenerate at 5×10^{19} cm^{-3} by varying χTMIn during growth and keeping χTESn constant. We see a strong correlation between the resistivity measurements and the spatially resolved Hall measurements. A variation of measured charge carrier concentration at the top and bottom of the nanowires was observed, with the top having more carriers for high χTMIn and the opposite trend for relatively lower χTMIn. We explain the first phenomenon in terms of changes in the effective IV/III ratio at the growth front with an increasing length of the nanowire due to different diffusion lengths of In-based and Sn-

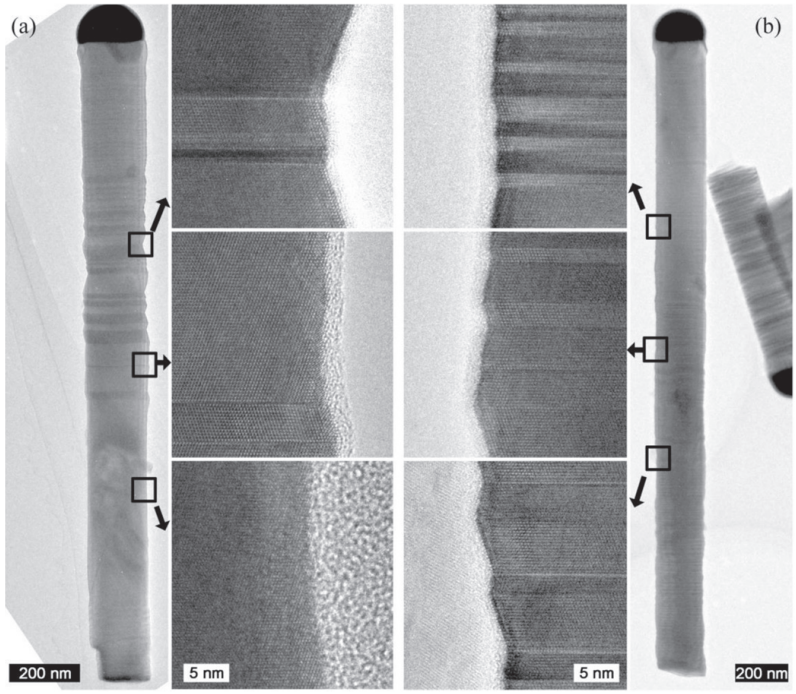

Figure 4. TEM images of a nanowire grown at χTMIn $= 3.0 \times 10^{-5}$ (a) and χTMIn $= 8.9 \times 10^{-5}$ (b). The nanowires are aligned in the [1$\bar{1}$0] zone axis.

based species supported by the nanowire growth rates measured in real time during growth. We argue that the inversion of the carrier concentration gradient moving to a lower χTMIn is due to the relative increase of stacking faults in the top compared to the bottom of the wires effectively trapping carriers, causing the measured carrier concentration to be lowered. In order to keep the doping constant along the nanowire, the data suggests that χTESn should be varied rather than χTMIn, since changes in χTESn do not affect the growth dynamics and crystal structure as much as χTMIn. The results open up for doping high enough to form a low-resistance contact between the nanowire and the transparent conducting oxide in nanowire solar cells, as well as Esaki tunnelling diode formation in tandem junction solar cells.

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