



# LUND UNIVERSITY

## Effects of traps in the gate stack on the small-signal RF response of III-V nanowire MOSFETs

Hellenbrand, Markus; Lind, Erik; Kilpi, Olli-Pekka; Wernersson, Lars-Erik

*Published in:*  
Solid-State Electronics

*DOI:*  
[10.1016/j.sse.2020.107840](https://doi.org/10.1016/j.sse.2020.107840)

2020

*Document Version:*  
Peer reviewed version (aka post-print)

[Link to publication](#)

*Citation for published version (APA):*  
Hellenbrand, M., Lind, E., Kilpi, O.-P., & Wernersson, L.-E. (2020). Effects of traps in the gate stack on the small-signal RF response of III-V nanowire MOSFETs. *Solid-State Electronics*, 171, Article 107840. <https://doi.org/10.1016/j.sse.2020.107840>

*Total number of authors:*  
4

### General rights

Unless other specific re-use rights are stated the following general rights apply:  
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: <https://creativecommons.org/licenses/>

### Take down policy

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117  
221 00 Lund  
+46 46-222 00 00



# Effects of traps in the gate stack on the small-signal RF response of III-V nanowire MOSFETs

Markus Hellenbrand\*, Erik Lind, Olli-Pekka Kilpi, Lars-Erik Wernersson

*Department of Electrical and Information Technology, Lund University, Ole Römers Väg 3, 223 63 Lund, Sweden*

---

## Abstract

We present a detailed study of the effect of gate-oxide-related defects (traps) on the small-signal radio frequency (RF) response of III-V nanowire MOSFETs and find that the effects are clearly identifiable in the measured admittance parameters and in important design parameters such as  $h_{21}$  (forward current gain) and MSG (maximum stable gain). We include the identified effects in a small-signal model alongside results from previous investigations of III-V RF MOSFETs and thus provide a comprehensive physical small-signal RF model for this type of transistor, which accurately describes the measured admittance parameters and gains. We verify the physical basis of the model assumptions by calculating the oxide defect density from the measured admittances.

**Keywords:** Border Traps, Gate Oxide Defects, Interface Defects, III-V, MOSFET, RF, Small-Signal Model

---

## 1. Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are essential components in high frequency electronics. III-V MOSFETs, due to their narrow band gap and high electron mobility, can achieve higher operation frequencies [1] than corresponding Si MOSFETs, which dominate the digital market. For digital applications, even after several years of investigations into the III-V/high- $\kappa$  material system, III-V MOSFETs are severely impaired by scalability and defects related to the gate oxide, so-called border and interface traps, which degrade reliability and lifetime of the transistors [2]. Two of the most common characterization techniques for traps are bias temperature instability (BTI) measurements in the time domain [3] and capacitance voltage (CV) measurements in the frequency domain [4]. Both techniques have greatly advanced our understanding of defects and led to significant improvement of transistor material qualities, which is reflected in nearly ideal inverse subthreshold slopes and high transconductances [5]. In both techniques, however, the direct observation of traps is typically limited to the megahertz regime and faster traps can only be accessed by decreasing the measurement temperature [6]. The effects of traps in the gate stack on the MOSFET radio frequency (RF) response have thus not yet been investigated in much detail. The few publications which take into account traps in RF investigations to a certain extent, usually focus on a single aspect only and simplify the small-signal model, in which the traps are studied, e.g. by disregarding non-quasi-static (NQS) effects [7–9]. A comprehensive description of the small-signal RF model, which takes into account all different

aspects of the contributions of gate-oxide-related traps to the admittance parameters ( $y$ -parameters), including both real and imaginary parts, and which does not disregard NQS effects, is yet to be developed.

Here, we demonstrate that despite the improvements in recent years, frequency dispersion in III-V MOSFETs at room temperature due to traps can be considerable even at gigahertz frequencies and we investigate the resulting effects on the small-signal  $y$ -parameters, the RF gains, and the stability factor. Based on our measurements, we provide a comprehensive small-signal model, which takes into account the observed dispersion and which accurately models the measurements. This model also takes into account previous results on small-signal analyses and can be applied at all bias points in the on-state of a transistor and in the off-state before the onset of minority carrier effects. We choose a small-signal approach for this analysis rather than a large-signal model to deconvolute the effect of traps on the RF response from their effect on the quiescent point. This simplifies the analysis and allows us to investigate the effects more clearly. As such, the presented model is not intended for circuit simulations, but it can be used e.g. for small-signal-based amplifier design.

The paper is structured as follows. First, in Section 2, we introduce the devices, which were used to develop and verify the small-signal model and explain the measurement setup and data processing. In Section 3, we briefly discuss the different kinds of defects, which can affect MOSFETs and point out assumptions, which enter into our analysis. In Section 4, we develop expressions for all small-signal model components and demonstrate the effects of traps with measured data in Sections 5 and 6. Lastly, in Section 7, we verify that the model assumptions, which take into account oxide traps, are physically meaningful by calculating the trap densities from the measured admittances.

---

\*Corresponding author

Email address: markus.hellenbrand@eit.lth.se (Markus Hellenbrand)

## 2. Devices and measurement

The development of the small-signal model presented here was based on measured data from a set of vertical III-V nanowire gate-all-around MOSFETs. The channels consisted of arrays of 180–300 parallel vertical nanowires of InAs graded to InGaAs on the drain side. The nanowire diameters varied between 25 and 30 nm. The high- $\kappa$  gate oxide consisted of a 1 nm/4 nm  $\text{Al}_2\text{O}_3/\text{HfO}_2$  bilayer and gate lengths varied between 100 nm and 220 nm. Details about processing can be found in [10]. For consistency, all measured data presented in this paper are from the same device.

For all investigated devices, scattering parameters ( $s$ -parameters) were measured with a vector network analyzer between 10 MHz and 67 GHz and for the subsequent analysis the  $s$ -parameters were converted to  $y$ -parameters. The measurement setup was calibrated off-chip by a load-reflect-reflect-match (LRRM) calibration procedure; on-chip open and short de-embedding structures were used to remove the effect of the pad parasitics. The parameters of the developed small-signal model were then determined by fitting the model to the measured  $y$ -parameters in Matlab.

The model was developed with a data set measured on the sample described above and verified by subsequent modeling of about thirty additional III-V devices on four different samples. Of the four samples, one was similar to the one described, one contained lateral nanowire MOSFETs, one contained MOSFETs with planar channels, and one contained steep-slope Tunnel FETs. Details about the samples can be found in [11–13]. While the measured parameters differed between samples due to their different geometries, their trends as a function of different bias points were consistent. Furthermore, the effects of traps on the gains, which will be described in Sections 5 and 6, can be discerned in examples from the literature as well [1, 14, 15]. Together with the different modeled samples, this demonstrates the general applicability of the model.

## 3. Traps in III-V MOSFET gate stacks

The application of high- $\kappa$  oxides on III-V semiconductors can cause many different material defects in the oxide or at the interface between oxide and semiconductor. Conventionally, these defects are often divided into so-called border traps and interface traps, where border traps are commonly associated for instance with oxygen vacancies in the ‘bulk’ of the oxygen layer, i.e. at least a few monolayers away from the oxide/channel interface [16, 17]. Interface traps are believed to be related to disorder, such as dangling bonds, dimers, antisites, or oxygen vacancies at the oxide/channel interface and possibly reaching a few monolayers into the oxide [18, 19]. Density functional theory calculations reveal that all of these defects can create electrically active states in the semiconductor band gap as well as in the conduction band [16–19] in a way that all of these defects can potentially affect MOSFET performance at different biases and time scales. Despite their different chemical natures, the capture and emission of charge carriers by both types of defect can be described by general

capture/emission time constants  $\tau_{c/e}$ , which depend on the tunneling distance and/or the activation energy associated with the charge exchange process [20, 21]:

$$\tau_{c/e} = \tau_0 \exp\left(\frac{x}{\lambda}\right) \exp\left(\frac{E_A}{k_B T}\right). \quad (1)$$

Here,  $x$  is the tunneling distance,  $\lambda$  the tunneling attenuation length according to the WKB approximation,  $E_A$  is the activation energy of a certain defect or defect population,  $k_B$  is the Boltzmann constant, and  $T$  the temperature. For the effective prefactor  $\tau_0$  it is usually assumed that  $\tau_0 = 1/(\sigma n v_{th})$  with the defect capture cross section  $\sigma$ , the carrier concentration  $n$ , and the thermal velocity  $v_{th}$  of the charge carriers [20]. In correspondence with a large variation of reported values for  $\sigma$ , literature values for  $\tau_0$  can be found to range from microseconds [22] all the way [6, 23] to below picoseconds [24]. Physically, and in accordance with (1),  $\tau_0$  is the time constant below which none of the defects can respond any longer. In our measurements here, we observe frequency dispersions, which we attribute to traps, even at gigahertz frequencies so that  $\tau_0 \approx 0.5$  ps (corresponding to an angular cutoff frequency  $\omega_0 = 1/\tau_0 = 2\pi \times 300$  GHz) is required to model these dispersions. This is well within the range of values for  $\tau_0$  reported in literature and with  $v_{th} = 5 \times 10^7$  cm/s and  $n = 5 \times 10^{18}$  cm $^{-3}$  [25] it results in  $\sigma = 8 \times 10^{-15}$  cm $^{-2}$ , which is a typical value for III-V materials [4, 26, 27]. As a convenient simplification, we typically treated  $\tau_0$  as a constant with respect to different bias points, but we point out that this is not a restriction, which is required to achieve agreement between measured values and our developed model.

Results from BTI measurements for example, have demonstrated that at relatively long time scales, the second exponential function in (1) usually dominates the overall time constant [28]. Eq. (1) then becomes  $\tau_{c/e} = \tau'_0 \times \exp(E_A/(k_B T))$  instead and the information about the location of the probed defects is hidden in the effective prefactor  $\tau'_0$  with typical values for  $\tau'_0$  in the nanosecond range [6, 29]. This, together with  $\lambda = 0.13$  nm (for an InAs/ $\text{Al}_2\text{O}_3$  interface), our assumption of  $\tau_0 \approx 0.5$  ps, and  $\tau'_0 = \tau_0 \times \exp(x/\lambda)$  indicates that the RF measurements here are probing defects at a depth of about 1 nm from the channel interface into the oxide. At the same time, with the measurement frequencies from 10 MHz to 67 GHz, the corresponding time constants  $\tau$  are already in the nanosecond range or below even without the exponential energy term. Thus, in the wide distribution of activation energies  $E_A$  that is assumed in BTI analyses [2, 6, 30], our measurements here seem to be probing the very smallest  $E_A$  so that the inelastic BTI models almost behave like an elastic model. In a purely elastic formulation (i.e.  $E_A = 0$ ), the given measurement frequencies would probe depths in the oxide between 1.3 nm and 0.2 nm, see (1). Based on these considerations, we expect to probe a blend of the aforementioned interface and border traps as well as a combination of elastically and inelastically responding traps.

In the following, we will demonstrate that at radio frequencies, this blend of electrically active traps can be successfully modeled by a simple distributed RC circuit. In CV analyses, sometimes, additional elements are added to this network to

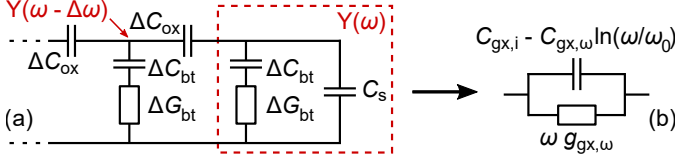


Figure 1: (a) Schematic of the distributed RC network, which models the effect of traps in a MOSFET.  $\Delta C_{ox}$  are the incremental parts of the gate oxide,  $\Delta C_t$  the trap capacitances,  $\Delta G_t$  the conductances, which set the corresponding time constants for the charge exchange, and  $C_s$  is the semiconductor capacitance.  $Y(\omega - \Delta\omega)$  and  $Y(\omega)$  are used for the derivation in Section 7. (b) Lumped representation of the circuit in (a) with corresponding frequency dependences.

separate interface defects as a distinct factor [22, 31, 32]. Since a distributed RC network simply models time constants without assumptions about the chemical nature or location of the defects in question, this addition proved to be unnecessary in our analysis. We do not consider this as a claim for or against either of the two kinds of defects, however, and just note that the transition between the two is probably fluent. This makes nomenclature ambiguous for the defects probed at radio frequencies so that for the remainder of the paper we will refer to the blend of probed defects simply as ‘traps’. The purpose of this paper is the inclusion of the effect of all kinds of traps in a small-signal model for the high frequency response of III-V MOSFETs.

#### 4. Small-signal model components

The wide distribution of traps with different time constants, which affect a MOSFET, can be modeled by a distributed network of RC elements as illustrated in Fig. 1(a), where the  $\Delta C_t$  model the capacitances associated with a certain trap population and the  $\Delta G_t$  in series determine the corresponding time constants. The different contributions are separated by incremental parts  $\Delta C_{ox}$  of the gate oxide and the RC branch next to the semiconductor capacitance  $C_s$  takes into account traps right at the interface. Carrier recombination far in the off-state is not taken into account in this model. Since the RC elements only model time constants, no assumptions are required at this point about the exact location, the chemical nature, or the exact capture mechanism of the corresponding defects.

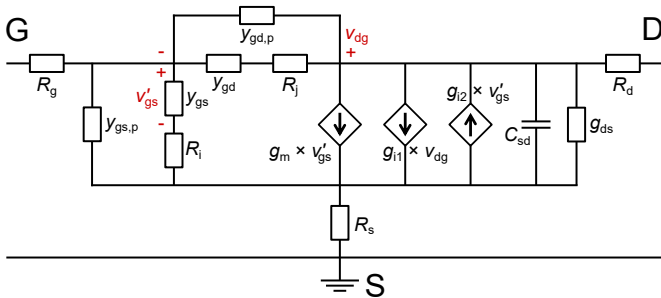


Figure 2: Complete small-signal model.  $y_{gs,p}$ ,  $y_{gd,p}$ ,  $y_{gs}$ , and  $y_{gd}$  each represent a lumped circuit as in Fig. 1(b). Detailed expressions for the different components are given by (1)–(6) and example values are listed in Table 1.

With a numerical solution of the voltage over  $C_s$  in the distributed network in Fig. 1(a) it can be shown that in the frequency range measured here, the distributed network can be approximated by a lumped admittance as depicted in Fig. 1(b), where the real part is linearly dependent on the angular frequency  $\omega$ , and the imaginary part is linearly dependent on  $-\ln(\omega/\omega_0)$  with  $\omega_0$  as discussed in Section 3. In a physical interpretation, the real part models losses due to a phase shift between the applied signal and the trap response, and the imaginary part models the capacitance due to traps capturing and emitting charges. The validity of this approximation is demonstrated by the measured data in Sections 5 and 6 and is illustrated in Fig. 4 and Fig. 6. Furthermore, similar RC networks have been successfully employed in BTI [33] and CV investigations [23] and the latter approach led to the same conclusion about the lumped frequency dependences that we use here.

In order to include the distributed RC network in the MOSFET small-signal model, equivalent lumped admittances like the one in Fig. 1(b) replace the otherwise constant intrinsic gate-to-source and gate-to-drain capacitances  $C_{gs,i}$  and  $C_{gd,i}$ , respectively. In Fig. 2, the equivalent admittances are denoted  $y_{gs}$  and  $y_{gd}$  and with the explanation above, for  $\omega < \omega_0$ , they can be expressed as

$$y_{gx} = \omega \times g_{gx,\omega} + j\omega (C_{gx,i} - C_{gx,\omega} \ln(\omega/\omega_0)), \quad (2)$$

where ‘x’ stands for either ‘s’ or ‘d’ (source or drain),  $g_{gx,\omega}$  and  $C_{gx,\omega}$  are the frequency-dependent components of the conductance and the capacitance, respectively, and the  $C_{gx,i}$  are the respective intrinsic capacitances without the effect of traps. While linearly frequency-dependent conductances were employed in small-signal models before [8, 9], none of those models included the trap contribution to the capacitances.

Furthermore, those previous models disregarded the NQS channel resistances  $R_i$  and  $R_j$  in Fig. 2 in series with  $y_{gs}$  and  $y_{gd}$ , respectively, which take into account the delay of charge carriers moving in the channel. This means that no distinction was made between intrinsic ( $y_{gs}$  and  $y_{gd}$  in Fig. 2) and parasitic

Table 1: Example parameters fitted to the small-signal model in Fig. 2 and used to calculate the modeled  $Y$ -parameters and gains in Fig. 5.

Parameter	Value	Parameter	Value
$V_{GS}, V_{DS}$	0.4 V, 0.5 V	$\tau_i$	500 ps
$V_T$	0.1 V	$g_{10}$	50 $\mu$ S
$R_g$	5 $\Omega$	$g_{20}$	0 <sup>†</sup>
$R_s$	4 $\Omega$	$\omega_0$	$2\pi \times 300$ GHz
$R_d$	16 $\Omega$	$R_i, R_j$	38 $\Omega$ , 229 $\Omega$
$g_{gs,i}$	10 $\mu$ S	$g_{gd,i}$	0.5 $\mu$ S
$g_{gs,\omega}$	2.5 fS/(rad/s)	$g_{gd,\omega}$	0.12 fF/(rad/s)
$C_{gs,p}$	20 fF	$C_{gd,p}$	6 fF
$C_{gs,i}$	6.0 fF	$C_{gd,i}$	1.0 fF
$C_{gs,\omega}$	0.35 fF	$C_{gd,\omega}$	0.2 fF
$C_{gsp,\omega}$	0.35 fF	$C_{gdp,\omega}$	0.2 fF
$g_{m,i}$	18.7 mS	$C_m$	1.0 fF
$\alpha$	0.03	$C_{m,\omega}$	0.2 fF
$\gamma_1$	$6 \times 10^{-3}$	$\gamma_2$	$80 \times 10^{-3}$
$g_{ds}$	1.55 mS	$C_{sd}$	10 fF

<sup>†</sup>  $g_{20}$  is zero at this bias point, but differs from zero at lower  $V_{GS}$ .

( $y_{gs,p}$  and  $y_{gd,p}$  in Fig. 2 – see next paragraph) components of those models. In order to keep the complexity of the equations for our model to a minimum, we derived analytical expressions for  $R_i$  and  $R_j$  based on an RC relaxation time model [34, 35]. The expressions

$$R_i = \frac{1}{1.4 g_{m,i}} \quad \text{and} \quad R_j = \frac{1}{1.4 g_{m,i} \times C_{gd,i}/C_{gs,i}}, \quad (3)$$

can be obtained by equating the time it takes charge carriers to move through half of the channel with the RC constant consisting of  $R_i(R_j)$  and  $C_{gs,i}(C_{gd,i})$ .  $g_{m,i}$  is the intrinsic transconductance, i.e. without the effect of traps.

For most MOSFETs even the intrinsic device, i.e. after de-embedding pad parasitics, is subject to some parasitic elements, which in Fig. 2 are denoted  $y_{gs,p}$  and  $y_{gd,p}$ . Typically, these parasitics consist of overlaps of the gate structure with the source and drain access regions and if they are dominated by structures, which contain oxides, they are expected to exhibit the same frequency dependence as (2). Furthermore, DC gate leakage can be considered as a parasitic effect and is included in  $y_{gs,p}$  and  $y_{gd,p}$  as well, so that for  $\omega < \omega_0$ ,

$$y_{gx,p} = \omega \times g_{gx,\omega} + j\omega (C_{gxp,0} - C_{gxp,\omega} \ln(\omega/\omega_0)) + g_{gx,l}. \quad (4)$$

Here again, ‘x’ stands for ‘s’ or ‘d’ (source or drain),  $g_{gx,l}$  takes into account the DC gate leakage,  $C_{gxp,0}$  is the parasitic capacitance without the effect of traps, and all other parameters are analogous to (2). While the constant parasitic  $C_{gxp,0}$  can be determined from the off-state of the transistor, the  $g_{gx,\omega}$  and  $C_{gxp,\omega}$  are energy- and thus voltage-dependent due to their dependence on the trap energy distribution so that they cannot be

subtracted as constant values. As a feasible approximation, we have assumed the same values for the intrinsic and the parasitic frequency dependences. This approach works well enough for modelling the  $y$ -parameters and gains and it only adds to the limitation of the quantitative analysis of the trap densities in Section 7.

Besides the admittances from (2) and (4), the transconductance  $g_m$  is also affected by traps. The numerical solution for the voltage over  $C_s$  in the distributed network in Fig. 1(a) reveals that the resulting dispersion affects both the real and the imaginary part. The complete expression for  $g_m$  below  $\omega_0$  is then

$$g_m = g_{m,i} [1 + \gamma_1 \ln(\omega/\omega_0) + j\alpha (1 + \gamma_2 \ln(\omega/\omega_0))] - j\omega (C_m - C_{m,\omega} \ln(\omega/\omega_0)), \quad (5)$$

where  $g_{m,i}$  is the intrinsic transconductance,  $\gamma_1$  and  $\gamma_2$  determine the strength of the frequency dispersions of the real and the imaginary part, respectively, and  $\alpha$  scales the imaginary part of this dispersion, since it is significantly smaller than the real part. A derivation of this transconductance-frequency ( $g_m$ - $f$ ) dispersion can be found in [7].  $C_m$  in the purely imaginary part of (5) is the mutual differential capacitance  $C_m = C_{dg} - C_{gd}$ , which balances the charge in the channel. Since in the presence of traps,  $C_{dg}$  and  $C_{gd}$  are both frequency-dependent according to (2),  $C_m$  in (5) exhibits the respective frequency dependence as well. In all our measurements, however, this frequency dependence of  $C_m$  was masked by the  $\gamma_2$  term in (5) so that we set  $C_{m,\omega} = C_{gd,\omega}$ .

Physically, equations like (2)–(5) should also apply to the source-drain elements  $C_{sd}$  and  $g_{ds}$ , since  $y_{22}$  is subject to the effect of traps as well. A corresponding resistance in series with  $C_{sd}$ , however, would always be masked by the large  $g_{ds}$  in par-

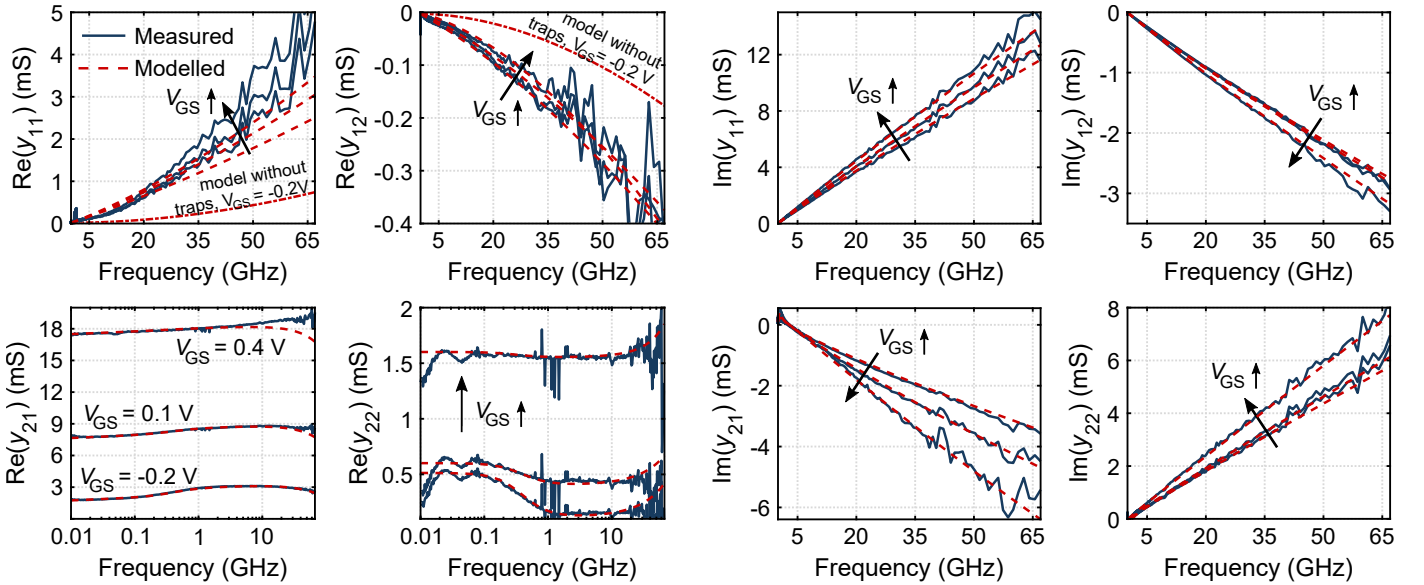


Figure 3: All  $y$ -parameters, measured (solid, blue lines) and modeled according to Fig. 2 (dashed, red lines), for three representative gate voltages  $V_{GS} = -0.2$  V, 0.1 V, and 0.4 V.  $V_T = 0.1$  V.  $\text{Re}(y_{21})$  and  $\text{Re}(y_{22})$  are plotted with logarithmic frequency axes to illustrate the frequency dispersion and the effects of impact ionization and band-to-band tunneling, respectively. In the subfigures for  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$ , example curves are provided for the model without traps at  $V_{GS} = -0.2$  V and the deviation is evident. All other modeled curves fit well with the measured data. For these figures,  $R_s$  and  $R_d$  have been subtracted, but not  $R_g$ . Complete expressions for the modeled  $y$ -parameters are provided in the Appendix.



allel with  $C_{sd}$  and a  $g_{ds}$ - $f$  dispersion corresponding to (5) was not observed. Instead, in virtually all our measurements we observed the onset of band-to-band tunneling (BTBT) or impact ionization (II) already at moderate electric fields between gate and drain. BTBT and II are well known effects in narrow band-gap MOSFETs even in DC measurements. They are not related to traps, but should be included in a comprehensive III-V MOSFET small-signal model. In Fig. 2, BTBT and II are modeled together by the current sources  $g_{i1}$  and  $g_{i2}$  with

$$g_{ik} = \frac{g_{k0}}{1 + j\omega\tau_i}. \quad (6)$$

Here,  $g_{k0}$  (with  $k = 1, 2$ ) determines the magnitude and  $\tau_i$  is the characteristic time constant. As an approximation, a common  $\tau_i$  was used for both effects. In fact, BTBT and II also affect  $\text{Re}(y_{21})$  (cf.  $y_{21}$  in the Appendix), but it requires higher gate-to-drain electric fields than in  $\text{Re}(y_{22})$  for these effects to emerge from the  $g_m$ - $f$  dispersion in  $\text{Re}(y_{21})$ . Since the time constant for BTBT and II is different from the dispersion time constant of the transconductance, the effects can be separated despite appearing in parallel in the model in Fig. 2. In Fig. 3, BTBT and II can be identified by the changing slope of  $\text{Re}(y_{21})$  for  $V_{GS} = -0.2$  V and  $V_{GS} = 0.1$  V at about 0.1 GHz and by the increase of the two lower curves of  $\text{Re}(y_{22})$  below about 1 GHz. Here it should be noted that a change in the RF output conductance  $\text{Re}(y_{22})$  can also be caused by self-heating. This would

result in a distinct stepwise increase in  $\text{Re}(y_{22})$  at about a few megahertz and the effect should increase with increasing  $V_{GS}$  [36]. We did not observe this in any of our measurements so that a convolution of our analysis with effects of self-heating is unlikely. Further details about BTBT and II in the small-signal model can be found in [37, 38].

The frequency-dependent expressions (2), (4), and (5) were provided with the constraint that  $\omega < \omega_0$ . Above  $\omega_0$ , none of the traps can respond anymore and the expressions become drastically simpler. The transconductance (5) becomes  $g_{m,i} - j\omega C_m$  and the intrinsic and parasitic conductances (2) and (4), respectively, become  $y_{gx} = j\omega C_{gx,i}$  and  $y_{gx,p} = j\omega C_{gx,p,0} + g_{gx,l}$ , respectively. For a physical model, this transition from the expressions below  $\omega_0$  to the ones above needs to be continuous. For the logarithmic parts, acceptable continuity is provided by the shape of the logarithm itself. For the real parts of the  $y_{gx}$  and  $y_{gx,p}$ , a transition function would be required, which describes the decrease of the modeled losses back to zero. Since the physical  $\omega_0$  seems to lie at higher frequencies than what we were able to measure, we could not investigate this transition of the real part. This does not affect the modeled  $y$ -parameters, however, since such a transition function would only affect the model close to  $\omega_0$  and thus outside of the measurement range.

The complete expressions for the  $y$ -parameters (below  $\omega_0$ ) are provided in the Appendix and an example of a complete set of small-signal parameters is provided in Table 1.

## 5. Linear components and their effect on the unilateral power gain and the stability factor

The importance of the linear contributions in (2) and (4) at high frequencies is demonstrated in Fig. 3 by the curves of  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$  at  $V_{GS} = -0.2$  V. Without it, the modeled  $\text{Re}(y_{11})$  is clearly lower and the modeled  $\text{Re}(y_{12})$  is clearly higher than the respective measured values. At first glance, on the linear scale of Fig. 3, better fits for  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$  could be achieved by increasing their quadratic contributions, for example by increasing the NQS resistances or the gate resistance  $R_g$ . On the logarithmic scale of Fig. 4(a), however, it becomes evident that such a purely quadratic function cannot describe the frequency dependence of  $\text{Re}(y_{11})$  or  $\text{Re}(y_{12})$  correctly. The inclusion of the linear trap contribution greatly alleviates the deviation between the measured values and the purely quadratic model, as demonstrated in Fig. 4(b), where the relative differences for the models with and without traps are compared. Furthermore, the linear contributions to  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$  are typically of different magnitudes, so that they cannot be corrected by a single common model parameter such as the gate resistance.

The linearly frequency-dependent contributions in  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$  also readily explain the change of the slope of the unilateral power gain  $U$ , which is evident in Fig. 5. This can be understood from the equation describing  $U$ , when traps are taken into account according to (2) and (4). Starting from the general definition of  $U$  [39], at low and intermediate frequencies ( $\leq 10$  GHz in Fig. 5), where second-order frequency terms

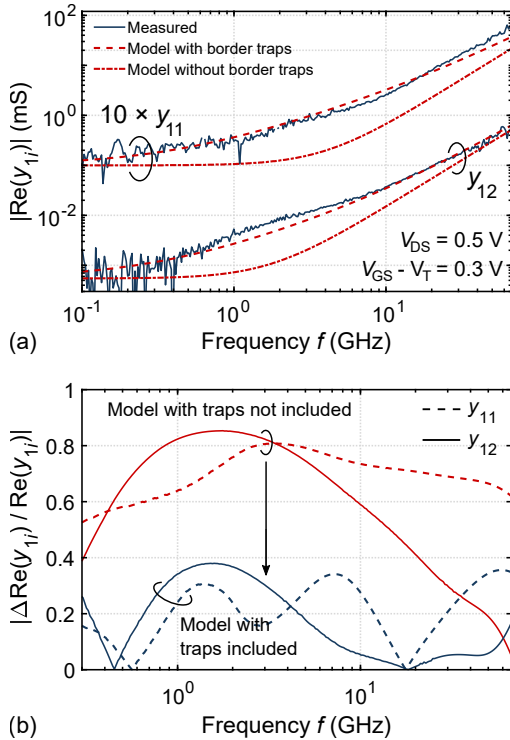


Figure 4: (a)  $10 \times \text{Re}(y_{11})$  (to avoid overlap) and  $\text{Re}(y_{12})$  on a logarithmic frequency axis. A purely quadratic model (i.e. without traps) cannot recreate the measured values properly. The model, which also includes the linear contribution from the traps, fits the data much better. (b) Relative deviation between measured and modeled  $\text{Re}(y_{11})$  and  $\text{Re}(y_{12})$  for the models with and without traps (same bias point as (a)). The inclusion of traps clearly reduces the deviations.

are small,  $U$  can be written as

$$U = \frac{|y_{21} - y_{12}|^2}{4 [\operatorname{Re}(y_{11}) \operatorname{Re}(y_{22}) - \operatorname{Re}(y_{12}) \operatorname{Re}(y_{21})]} \quad (7)$$

$$\approx \frac{|g_m|^2}{4 [\omega (g_{gs,\omega} + g_{gd,\omega}) g_{ds} + \omega g_{gd,\omega} \operatorname{Re}(g_m)]},$$

where the  $g_{gx,\omega}$  contain the frequency dependences of both the intrinsic and the parasitic elements, i.e. from (2) and (4). Since (7) aims to highlight the importance of the linear frequency dependence (and for better readability),  $g_{gs,l}$  and  $g_{gd,l}$  from (4) are omitted in this approximation. In (7), the linearly frequency-dependent contributions in  $\operatorname{Re}(y_{11})$  and  $\operatorname{Re}(y_{12})$  dominate over the usually squared frequency dependences, which would have resulted in the well-known expression  $U \propto g_m^2 / (4\omega^2 C_{gg}^2)$  with the total gate capacitance  $C_{gg}$ . The now predominantly linear frequency dependence in the denominator of (7) changes the roll-off of  $U$  from the typical -20 dB/decade to almost -10 dB/decade. This can be observed in examples from literature as well [14, 15]. When compared with the model without traps, in a certain frequency range this leads to a decrease of the unilateral power gain by almost 10 dB. For the design of unilateral amplifiers, which are limited by  $U$ , this is a severe penalty. The constant level of  $U$  at low frequencies is caused by the constant leakage contributions  $g_{gs,l}$  and  $g_{gd,l}$  in (4). Furthermore, it can be noted that  $U$  is affected by the logarithmic frequency dependence of  $g_m$ . However, the linear components in (7) largely dominate over this logarithmic contribution.

Besides the roll-off of  $U$ , the linear components in  $\operatorname{Re}(y_{11})$  and  $\operatorname{Re}(y_{12})$  affect the stability factor  $k$ , as illustrated in Fig. 5 as well. The modeled  $k$  without the inclusion of traps is always lower than the measured values. In the equation for  $k$ , the effect of the linear contributions can be seen clearest at frequencies, where  $k$  is almost constant, i.e. between 1 GHz and 10 GHz in Fig. 5. At these frequencies, starting from its general definition [39],  $k$  can be written as

$$k = \frac{2 \operatorname{Re}(y_{11}) \operatorname{Re}(y_{22}) - \operatorname{Re}(y_{12}) \operatorname{Re}(y_{21})}{|y_{12} y_{21}|} \quad (8)$$

$$\approx \frac{2\omega (g_{gs,\omega} + g_{gd,\omega}) g_{ds} + \omega g_{gd,\omega} \operatorname{Re}(g_m)}{\left| (-\omega g_{gd,\omega} - j\omega (C_{gd,i} + C_{gd,p})) g_m \right|},$$

where again, the  $g_{gx,\omega}$  contain the frequency dependences of both the intrinsic and the parasitic elements and  $g_{gs,l}$  and  $g_{gd,l}$  from (4) are omitted for increased readability. In this approximation it is obvious that without the effect of traps ( $g_{gx,\omega}$ ),  $k$  would become zero. Indeed, in Fig. 5, for the model without traps,  $k$  almost vanishes in the range between 1 GHz and 10 GHz, so that by the presence of traps,  $k$  is increased by a factor of up to five. Since the shift of  $k$  appears to be mostly constant in Fig. 5, the relative difference decreases towards higher frequencies, but can still amount to up to 30 % at 60 GHz. In Fig. 5, together with the effect of the traps on the gain, this lowers the  $k$ -point, i.e. the point, where MSG changes to the maximum available gain MAG, by 15 to 20 GHz. The remaining small difference of  $k$  from zero in the measured values stems from the constant leakage contributions  $g_{gs,l}$  and  $g_{gd,l}$  in  $y_{gs,p}$

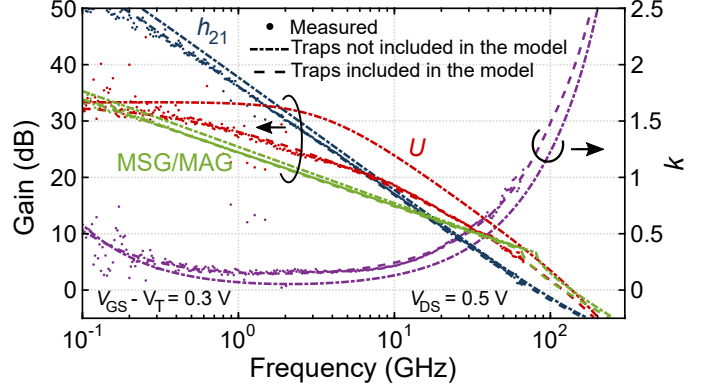


Figure 5: Gains and stability factor as a function of frequency. For each parameter, two different modeled curves are provided: The dashed lines (on top of the measured values) represent the complete model with traps, while the dash-dotted lines represent the model without the inclusion of traps.

and  $y_{gd,p}$ , which were omitted from (8). The lower  $k$ -point decreases the frequency range available for circuit design.

## 6. Logarithmic components and their effect on the forward current gain and the maximum stable gain

Logarithmic frequency dispersions due to traps are present in the transconductance, (5), and in the intrinsic and parasitic capacitances in (2) and (4), respectively. The frequency dispersion in the real part of the transconductance is visible in  $\operatorname{Re}(y_{21})$  in Fig. 3. The further increase of the measured  $\operatorname{Re}(y_{21})$  at the higher  $V_{GS}$  beyond approx. 20 GHz, as well as the further increase of  $\operatorname{Re}(y_{11})$  above approx. 35 GHz, is most likely due to the shortcomings of the open-short de-embedding at high frequencies.

Frequency dependences in capacitances due to traps have been resolved in CV measurements before [23], but not in transistor measurements. In Fig. 6(a), the measured  $\operatorname{Im}(y_{11})/\omega$  and  $\operatorname{Im}(y_{12})/\omega$ , which approximately correspond to the capacitances in (2) and (4), are compared with the models with and without the effect of traps. The model without traps results in horizontal lines, which corresponds to ordinary capacitances, whereas the measured values clearly deviate from this behavior. Upon inclusion of the logarithmic frequency dependences in (2) and (4), the deviation readily disappears. To quantify this, the relative differences of the measured and modelled  $\operatorname{Im}(y_{11})$  and  $\operatorname{Im}(y_{12})$  are plotted in Fig. 6(b). At high frequencies, less traps can respond, so that the capacitances of the model, which includes traps, are reduced to the intrinsic capacitances and the difference between the models with and without traps vanishes. Towards lower frequencies, the agreement between measured and modeled values is improved by up to 20 % by the inclusion of traps in the model.

The same logarithmic deviation between measured and modeled values, which is observed in  $\operatorname{Im}(y_{11})$  and  $\operatorname{Im}(y_{12})$ , can be identified in the forward current gain  $h_{21}$  and the maximum stable gain MSG in Fig. 5. Just as for the  $y$ -parameters, the deviation disappears upon inclusion of the frequency-dependent capacitances. Again, the difference between the two models can



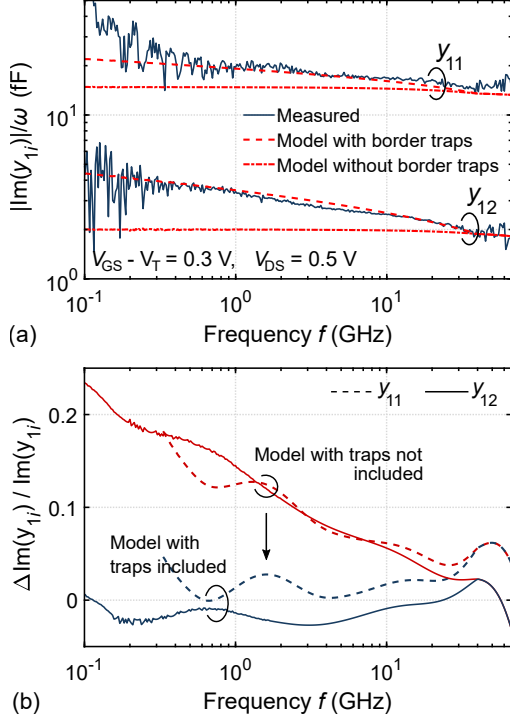


Figure 6: (a)  $\text{Im}(y_{11})$  and  $\text{Im}(y_{12})$  divided by  $\omega$  to illustrate the logarithmic contribution to the capacitances. Constant capacitances result in horizontal lines and cannot reproduce the measured results, whereas capacitances with logarithmic frequency dependences according to (2) and (4) fit well with the measured results. (b) Relative deviation between measured and modeled  $\text{Im}(y_{11})$  and  $\text{Im}(y_{12})$  for the models with and without traps (same bias point as (a)). The inclusion of traps in the model clearly reduces the deviations.

be explained by the equations of the two quantities. Starting with its general definition [39],  $h_{21}$  can be written as

$$h_{21} = \frac{|y_{21}|}{|y_{11}|} \approx \frac{|g_m|}{|j\omega(C_{gs} + C_{gs,p} + C_{gd} + C_{gd,p})|}, \quad (9)$$

where all four capacitances denote the total frequency-dependent capacitances from (2) and (4), e.g.  $C_{gd} = C_{gd,i} - C_{gd,\omega} \times \ln(\omega/\omega_0)$ . In the approximation in (9), typically, the real parts of  $y_{11}$ , which are important for e.g.  $U$  and  $k$ , are significantly smaller than the imaginary parts. Without the trap contribution, in a Bode plot, (9) would yield the typical -20 dB/decade roll-off. When the effects of traps are included, logarithmic frequency dependences are added to both the numerator (decrease towards lower frequencies) and to the denominator (increase towards lower frequencies), which causes the lower slope for  $h_{21}$  in Fig. 5. The same applies for MSG, which, again, starting from its general definition [39], can be written as

$$\text{MSG} = \frac{|y_{21}|}{|y_{12}|} \approx \frac{|g_m|}{|j\omega(C_{gd} + C_{gd,p})|}. \quad (10)$$

As in (9), both capacitances include the frequency dependences from (2) and (4) and as for  $U$ , the deviations of the slopes of  $h_{21}$  and MSG can be observed in examples in literature as well [1, 14]. MSG is an important metric for the design of small-signal amplifiers and the dispersion in the transistor MSG is

directly translated to the amplifier. Since the dispersion in MSG is much smaller than in  $U$ , the resulting penalty in the amplifier should be acceptable as long as the design is not dependent on single decibels of gain. In any case, it is important to be aware of the dispersion, so that the amplifier design will not be based on an idealized and thus incorrect transistor gain.

## 7. Physical origin of trap model parameters

In the following, the trap density  $N_t$  will be calculated from the measured admittances to verify that the small-signal parameters, which model the oxide traps, are physically meaningful. The approach to deriving an expression for  $N_t$  is indicated in Fig. 1. At a frequency  $\omega$ , the part of the distributed network, which responds at frequencies up to this  $\omega$ , can be seen as an admittance  $Y(\omega)$ . The change  $\Delta Y(\omega)$  for a change  $\Delta\omega$  can then be expressed as  $\Delta Y(\omega) = Y(\omega) - Y(\omega - \Delta\omega)$ , where  $Y(\omega - \Delta\omega)$  is the admittance corresponding to an incrementally lower  $\omega$ . The trap density  $N_t$ , as detailed in [23], is included in this model as  $\Delta C_t = q^2 N_t \Delta x$ , where  $q$  is the elemental charge, and the  $\Delta C_t$  are the incremental parts of the trap population within a thickness  $\Delta x$  in the gate oxide. The time constants  $\tau = \Delta C_t / \Delta G_t$  associated with each  $\Delta C_t$  are modeled by adding corresponding conductances  $\Delta G_t$  in series with the incremental capacitances. At this stage, the  $\Delta G_t$  and thus the different  $\tau$  can still be modeled independently of the position  $\Delta x$  in the oxide. To be able to calculate  $N_t$  from the measured admittances, the angular frequency  $\omega$ , and thus the time constants  $\tau$ , are related to  $\Delta x$  via elastic tunneling as  $\Delta x = -\lambda \Delta \ln(\omega)$ , where  $\lambda = 0.13$  nm is the tunneling attenuation length according to the WKB approximation as in Section 3. As discussed in Section 3 as well, elastic tunneling should be a viable approximation at gigahertz frequencies. With this, a change in the admittance  $Y(\omega)$  of the distributed RC network in Fig. 1 ( $y_{11}$  or  $y_{12}$  in the small-signal model) for a change in the angular frequency  $\omega$  can be expressed as

$$\frac{\Delta Y(\omega)}{\Delta \ln(\omega)} = \frac{1+j}{2} (\omega q^2 \lambda N_t L_G W_G), \quad (11)$$

where the term  $\lambda \Delta \ln(\omega) Y(\omega)$ , which appears during the derivation, is sufficiently small to be dropped from the expression. In (11),  $L_G$  and  $W_G$  are the gate length and width of the transistor, respectively. Examples for  $N_t$  as calculated from the measured  $y_{12}$  are presented in Fig. 7 alongside a calculation of  $N_t$  based on the  $g_m$ - $f$  dispersion as in [7]. The values for  $N_t$  calculated from  $y_{11}$  exhibited a similar behavior as the ones calculated from  $y_{12}$ .

For the calculations according to (11), first, the elements surrounding  $y_{11}$  and  $y_{12}$  in the small-signal model in Fig. 2 have to be subtracted until only the contribution of the  $y_{gd}$  or  $y_{gs}$  remains. The resulting uncertainties, indicated by the shaded areas in Fig. 7, reveal that an exact quantitative resolution of  $N_t$ , e.g. as a function of the gate voltage and thus of energy, is limited by the measurement accuracy of the  $s$  parameters and the subsequent deconvolution of the  $y$ -parameters. For the largest parts of the bias range, however, the average values for  $N_t$  calculated from the different components are within an order of magnitude of each other and they are in good agreement with results

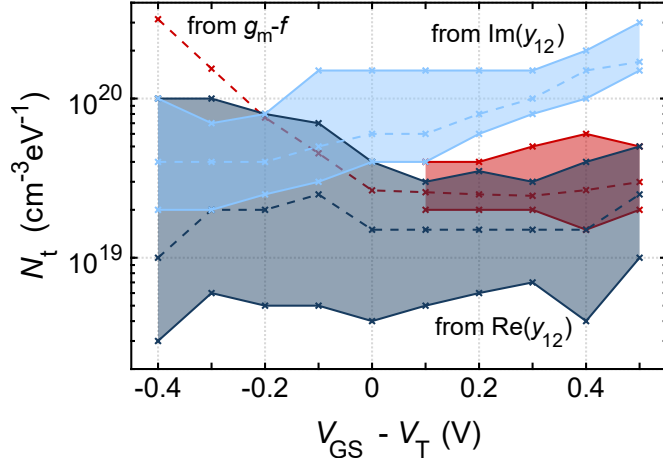


Figure 7:  $N_t$  as a function of  $V_{GS}$ . Dashed lines indicate the average values for  $N_t$  in approximately the first nanometer of the gate oxide from the channel. The shaded areas reflect the uncertainty due to the measurement accuracy.  $N_t$  from  $g_m$ - $f$  below  $V_{GS} - V_T = 0.1$  V was calculated from the modeled  $\gamma_1$  due to strong II and BTBT at these bias points.

that both we and others have observed with different characterization techniques [2, 40–43]. The results are thus sufficiently accurate to verify the physical origin of the model assumptions.

## 8. Conclusions

The effects of traps related to the gate oxide are clearly discernable in the RF  $y$ -parameters of III-V MOSFETs. The inclusion of traps in  $y_{11}$ ,  $y_{12}$ , and  $y_{21}$  is thus essential to accurately describe a small-signal model for these devices. Although the resulting effects on design parameters such as  $h_{21}$  and MSG are small, the effects have to be identified in the first place to be able to draw this conclusion with certainty. The calculation of the trap density  $N_t$  based on the presented model can be limited by the measurement accuracy, but it yields values for  $N_t$ , which are in agreement with values calculated by other techniques. This demonstrates that the model parameters reasonably reflect physical assumptions.

## Acknowledgements

We thank J. Svensson for growing the nanowires for the vertical nanowire MOSFETs, F. Lindelöw and J. Mo for providing us with samples of lateral nanowire MOSFETs and of planar MOSFETs, respectively, and S. Andrić for helpful discussions. This work was supported in part by the Swedish Foundation for Strategic Research and the Swedish Research Council, and in part by the European Union through the H2020 Program IN-SIGHT under Grant 688784.

## Appendix

Here we provide the complete expressions for the  $y$ -parameters for the model in Fig. 2. For convenience, we repeat the expressions for all parameters, which enter into the

$y$ -parameters:

$$\begin{aligned} y_{gx} &= \omega \times g_{gx,\omega} + j\omega \left( C_{gx,i} - C_{gx,\omega} \ln(\omega/\omega_0) \right), \\ y_{gx,p} &= \omega \times g_{gx,p,\omega} + j\omega \left( C_{gx,p,0} - C_{gx,p,\omega} \ln(\omega/\omega_0) \right) \\ &\quad + g_{gx,l}, \\ g_m &= g_{m,i} \left[ 1 + \gamma_1 \ln(\omega/\omega_0) + j\alpha (1 + \gamma_2 \ln(\omega/\omega_0)) \right] \\ &\quad - j\omega (C_m - C_{m,\omega} \ln(\omega/\omega_0)), \\ g_{ik} &= \frac{g_{k0}}{1 + j\omega\tau_i}, \\ R_i &= \frac{1}{1.4 g_{m,i}} \quad \text{and} \quad R_j = \frac{1}{1.4 g_{m,i} \times C_{gd,i}/C_{gs,i}}. \end{aligned}$$

With these, the intrinsic  $y$ -parameters (i.e. after subtracting the resistances  $R_s$ ,  $R_d$ , and  $R_g$ ) are

$$\begin{aligned} y_{11} &= \left. \frac{i_1}{v_1} \right|_{v_2=0} = y_{gs,p} + \frac{y_{gs}}{1 + y_{gs}R_i} - y_{12}, \\ y_{12} &= \left. \frac{i_1}{v_2} \right|_{v_1=0} = -y_{gd,p} - \frac{y_{gd}}{1 + y_{gd}R_j}, \\ y_{21} &= \left. \frac{i_2}{v_1} \right|_{v_2=0} = \frac{g_m}{1 + y_{gs}R_i} + y_{12} - g_{i1} - \frac{g_{i2}}{1 + y_{gs}R_i}, \\ y_{22} &= \left. \frac{i_2}{v_2} \right|_{v_1=0} = g_{ds} + j\omega C_{sd} - y_{12} + g_{i1}, \end{aligned}$$

## References

- [1] A. Tessmann, A. Leuther, F. Heinz, F. Bernhardt, L. John, H. Massler, L. Czornomaz, T. Merkle, 20-nm  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  MOSHEMT MMIC technology on silicon, *IEEE Journal of Solid-State Circuits* 54 (9) (2019) 2411–2418. doi:10.1109/JSSC.2019.2915161.
- [2] J. Franco, V. Putcha, A. Vais, S. Sioncke, N. Waldron, D. Zhou, G. Rzepa, P. J. Roussel, G. Groeseneken, M. Heyns, N. Collaert, D. Linten, T. Grassler, B. Kaczer, Characterization of oxide defects in InGaAs MOS gate stacks for high-mobility n-channel MOSFETs (invited), in: 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 751–754. doi:10.1109/IEDM.2017.8268347.
- [3] B. Kaczer, T. Grassler, J. Roussel, J. Martin-Martinez, R. O’Connor, B. J. O’Sullivan, G. Groeseneken, Ubiquitous relaxation in BTI stressing—new evaluation and insights, in: 2008 IEEE International Reliability Physics Symposium, 2008, pp. 20–27. doi:10.1109/RELPHY.2008.4558858.
- [4] R. Engel-Herbert, Y. Hwang, S. Stemmer, Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces, *Journal of Applied Physics* 108 (12) (2010) 124101. doi:10.1063/1.3520431.
- [5] H. Riel, L.-E. Wernersson, M. Hong, J. A. del Alamo, III-V compound semiconductor transistors—from planar to nanowire structures, *MRS Bulletin* 39 (8) (2014) 668–677. doi:10.1557/mrs.2014.137.
- [6] V. Putcha, J. Franco, A. Vais, S. Sioncke, B. Kaczer, D. Linten, G. Groeseneken, On the apparent non-arrhenius temperature dependence of charge trapping in III-V/high- $k$  MOS stack, *IEEE Transactions on Electron Devices* 65 (9) (2018) 3689–3696. doi:10.1109/TED.2018.2851189.
- [7] S. Johansson, M. Berg, K. Persson, E. Lind, A high-frequency transconductance method for characterization of high- $\kappa$  border traps in III-V MOSFETs, *IEEE Transactions on Electron Devices* 60 (2) (2013) 776–781. doi:10.1109/TED.2012.2231867.
- [8] M. Egard, L. Ohlsson, M. Årlelid, K. Persson, B. M. Borg, F. Lenrick, R. Wallenberg, E. Lind, L.-E. Wernersson, High-frequency performance of self-aligned gate-last surface channel  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSFET, *IEEE Electron Device Letters* 33 (3) (2012) 369–371. doi:10.1109/LED.2011.2181323.

- [9] C. B. Zota, G. Roll, L.-E. Wernersson, E. Lind, Radio-frequency characterization of selectively regrown InGaAs lateral nanowire MOSFETs, *IEEE Transactions on Electron Devices* 61 (12) (2014) 4078–4083. doi:10.1109/TED.2014.2363732.
- [10] O. Kilpi, J. Svensson, E. Lind, L. Wernersson, Electrical properties of vertical InAs/InGaAs heterostructure MOSFETs, *IEEE Journal of the Electron Devices Society* 7 (2018) 70–75. doi:10.1109/JEDS.2018.2878659.
- [11] C. B. Zota, F. Lindelöw, L.-E. Wernersson, E. Lind, High-frequency InGaAs tri-gate MOSFETs with  $f_{\max}$  of 400 GHz, *Electronics Letters* 52 (22) (2016) 1869–1871. doi:10.1049/el.2016.3108.
- [12] G. Roll, J. Mo, E. Lind, S. Johansson, L.-E. Wernersson, Defect evaluation in InGaAs field effect transistors with  $\text{HfO}_2$  or  $\text{Al}_2\text{O}_3$  dielectric, *Applied Physics Letters* 106 (20) (2015) 203503. doi:10.1063/1.4921483.
- [13] M. Hellenbrand, E. Memisevic, J. Svensson, A. Krishnaraja, E. Lind, L. Wernersson, Capacitance measurements in vertical III–V nanowire TFETs, *IEEE Electron Device Letters* 39 (7) (2018) 943–946. doi:10.1109/LED.2018.2833168.
- [14] J. Wu, Y. Fang, B. Markman, H. Y. Tseng, M. J. W. Rodwell,  $L_g = 30$  nm InAs channel MOSFETs exhibiting  $f_{\max} = 410$  GHz and  $f_t = 357$  GHz, *IEEE Electron Device Letters* 39 (4) (2018) 472–475. doi:10.1109/LED.2018.2803786.
- [15] C. B. Zota, C. Convertino, M. Sousa, D. Caimi, K. Moselund, L. Czornomaz, High-frequency quantum well InGaAs-on-Si MOSFETs with scaled gate lengths, *IEEE Electron Device Letters* 40 (4) (2019) 538–541. doi:10.1109/LED.2019.2902519.
- [16] K. Xiong, J. Robertson, M. C. Gibson, S. J. Clark, Defect energy levels in  $\text{HfO}_2$  high-dielectric-constant gate oxide, *Applied Physics Letters* 87 (18) (2005) 183505. doi:10.1063/1.2119425.
- [17] J. L. Gavartin, D. Muñoz Ramo, A. L. Shluger, G. Bersuker, B. H. Lee, Negative oxygen vacancies in  $\text{HfO}_2$  as charge traps in high- $\kappa$  stacks, *Applied Physics Letters* 89 (8) (2006) 082908. doi:10.1063/1.2236466.
- [18] J. Robertson, Y. Guo, L. Lin, Defect state passivation at III–V oxide interfaces for complementary metal–oxide–semiconductor devices, *Journal of Applied Physics* 117 (11) (2015) 112806. doi:10.1063/1.4913832.
- [19] G. Greene-Diniz, K. J. Kuhn, P. K. Hurley, J. C. Greer, First principles modeling of defects in the  $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  system, *Journal of Applied Physics* 121 (7) (2017) 075703. doi:10.1063/1.4975033.
- [20] F. P. Heiman, G. Warfield, The effects of oxide traps on the MOS capacitance, *IEEE Transactions on Electron Devices* 12 (4) (1965) 167–178. doi:10.1109/T-ED.1965.15475.
- [21] T. Grasser, The capture/emission time map approach to the bias temperature instability, in: T. Grasser (Ed.), *Bias Temperature Instability for Devices and Circuits*, Springer New York, New York, NY, 2014, pp. 447–481. doi:10.1007/978-1-4614-7909-3\_17.
- [22] H. Chen, Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, Y. Taur, Interface-state modeling of  $\text{Al}_2\text{O}_3$ –InGaAs mos from depletion to inversion, *IEEE Transactions on Electron Devices* 59 (9) (2012) 2383–2389. doi:10.1109/TED.2012.2205255.
- [23] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, Y. Taur, A distributed model for border traps in  $\text{Al}_2\text{O}_3$ –InGaAs MOS devices, *IEEE Electron Device Letters* 32 (4) (2011) 485–487. doi:10.1109/LED.2011.2105241.
- [24] I. Lundström, C. Svensson, Tunneling to traps in insulators 43 (12) (1972) 5045–5047. doi:10.1063/1.1661067.
- [25] K. Jansson, E. Lind, L.-E. Wernersson, Ballistic modeling of inas nanowire transistors, *Solid-State Electronics* 115 (2016) 47 – 53. doi:10.1016/j.sse.2015.10.009.
- [26] N. Khuchua, L. Khvedelidze, M. Tigishvili, N. Gorev, E. Privalov, I. Kodzheshirova, Deep-level effects in GaAs microelectronics: a review, *Russian Microelectronics* 32 (5) (2003) 257–274. doi:10.1023/A:1025528416032.
- [27] P. S. Whitney, W. Lee, C. G. Fonstad, Capacitance transient analysis of molecular-beam epitaxial n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and n- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ , *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena* 5 (3) (1987) 796–799. doi:10.1116/1.583753.
- [28] T. Grasser, Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities, *Microelectronics Reliability* 52 (1) (2011) 39 – 70. doi:https://doi.org/10.1016/j.microrel.2011.09.002.
- [29] G. Rzepa, J. Franco, A. Subirats, M. Jech, A. Chasin, A. Grill, M. Waltl, T. Knobloch, B. Stampfer, T. Chiarella, N. Horiguchi, L. Ragnarsson, D. Linten, B. Kaczer, T. Grasser, Efficient physical defect model applied to PBTI in high- $\kappa$  stacks, in: 2017 IEEE International Reliability Physics Symposium (IRPS), 2017, pp. XT–11.1–XT–11.6. doi:10.1109/IRPS.2017.7936425.
- [30] T. Grasser, P. Wagner, H. Reisinger, T. Aichinger, G. Poben, M. Nelhiebel, B. Kaczer, Analytic modeling of the bias temperature instability using capture/emission time maps, in: 2011 International Electron Devices Meeting, 2011, pp. 27.4.1–27.4.4. doi:10.1109/IEDM.2011.6131624.
- [31] A. S. Babadi, E. Lind, L. E. Wernersson, Modeling of n-InAs metal oxide semiconductor capacitors with high- $\kappa$  gate dielectric 116 (21) (2014) 214508–1–214508–6. doi:10.1063/1.4903520.
- [32] G. Brammertz, A. Alian, D. H. Lin, M. Meuris, M. Caymax, W. Wang, A combined interface and border trap model for high-mobility substrate metal–oxide–semiconductor devices applied to  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and InP capacitors, *IEEE Transactions on Electron Devices* 58 (11) (2011) 3890–3897. doi:10.1109/TED.2011.2165725.
- [33] H. Reisinger, T. Grasser, W. Gustin, C. Schlünder, The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress, in: 2010 IEEE International Reliability Physics Symposium, 2010, pp. 7–15. doi:10.1109/IRPS.2010.5488858.
- [34] W. Liu, *FET High-Frequency Properties*, Wiley Interscience, 1999, Ch. 6, pp. 371–446.
- [35] H. R. P. Roblin, Small- and large-signal AC models for the short-channel MODFET, Cambridge University Press, 2002, Ch. 12, pp. 384–411.
- [36] S. Makovejev, S. Olsen, J. Raskin, RF extraction of self-heating effects in FinFETs, *IEEE Transactions on Electron Devices* 58 (10) (2011) 3335–3341. doi:10.1109/TED.2011.2162333.
- [37] M. Isler, K. Schünemann, Impact-ionization effects on the high-frequency behavior of HFETs 52 (3) (2004) 858–863. doi:10.1109/TMTT.2004.823553.
- [38] S. Johansson, M. Egard, S. G. Ghalamestani, B. M. Borg, M. Berg, L.-E. Wernersson, E. Lind, RF characterization of vertical InAs nanowire wrap-gate transistors integrated on Si substrates, *IEEE Transactions on Microwave Theory and Techniques* 59 (10) (2011) 2733–2738. doi:10.1109/TMTT.2011.2163076.
- [39] H. R. P. Roblin, MODFET high-frequency performance, Cambridge University Press, 2002, Ch. 17, pp. 567–612.
- [40] M. Hellenbrand, O.-P. Kilpi, J. Svensson, E. Lind, L.-E. Wernersson, Low-frequency noise in nanowire and planar III–V MOSFETs, *Microelectronic Engineering* 215 (2019) 110986. doi:https://doi.org/10.1016/j.mee.2019.110986.
- [41] B. Kaczer, J. Franco, P. Weckx, P. Roussel, V. Putcha, E. Bury, M. Simicic, A. Chasin, D. Linten, B. Parvais, F. Catthoor, G. Rzepa, M. Waltl, T. Grasser, A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability, *Microelectronics Reliability* 81 (2018) 186 – 194. doi:https://doi.org/10.1016/j.microrel.2017.11.022.
- [42] E. Caruso, J. Lin, K. F. Burke, K. Cherkaoui, D. Esseni, F. Gity, S. Monaghan, P. Palestri, P. Hurley, L. Selmi, Profiling border-traps by TCAD analysis of multifrequency CV-curves in  $\text{Al}_2\text{O}_3/\text{InGaAs}$  stacks, in: 2018 Joint International EUROSOL Workshop and International Conference on Ultimate Integration on Silicon (EUROSOL-ULIS), 2018, pp. 1–4. doi:10.1109/ULIS.2018.8354757.
- [43] G. Roll, E. Lind, M. Egard, S. Johansson, L. Ohlsson, L. E. Wernersson, RF and DC analysis of stressed InGaAs mosfets, *IEEE Electron Device Letters* 35 (2) (2014) 181–183. doi:10.1109/LED.2013.2295526.