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Kilpi, Olli-Pekka; Hellenbrand, Markus; Svensson, Johannes; Lind, Erik; Wernersson, Lars-Erik

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PO Box 117
221 00 Lund
+46 46-222 00 00

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Vertical nanowire III–V MOSFETs with improved high-frequency gain

O.-P. Kilpi✉, M. Hellenbrand, J. Svensson, E. Lind and L.-E. Wernersson

High-frequency performance of vertical InAs/InGaAs heterostructure nanowire MOSFETs on Si is demonstrated for the first time for a gate-last configuration. The device architecture allows highly asymmetric capacitances, which increases the power gain. A device with $L_g = 120$ nm demonstrates $f_T = 120$ GHz, $f_{max} = 130$ GHz and maximum stable gain (MSG) = 14.4 dB at 20 GHz. These metrics demonstrate the state-of-the-art performance of vertical nanowire MOSFETs.

Introduction: Moore's law has been the driving force for the development of electrical devices for the last few decades. Si-based MOSFETs have shown excellent scalability in digital applications and especially III–V MOSFETs have surpassed other transistor architectures in the transconductance g_m [1] and the on-current I_{on} [2, 3]. For high-frequency transistors, the inability to scale high electron mobility transistor (HEMTs) further due to the insufficient gate-barrier has stagnated the development of f_T at 700 GHz [4, 5]. Better scaling III–V MOSFETs could, therefore, surpass HEMTs also in high-frequency applications. Recently, several high-frequency planar MOSFETs have been presented with f_T and f_{max} about 400 GHz [6, 7]. In this Letter, the prospect of vertical III–V nanowires for high-frequency devices is evaluated.

III–V vertical vapour–liquid–solid (VLS) grown nanowires offer an interesting option as they are less limited by the lattice mismatch; therefore, they can be easily integrated on Si. The VLS growth further allows band-gap engineering along the electron transport direction, which enables improved intrinsic voltage gain (g_m/g_d) and higher breakdown voltage without substantially deteriorating other performance metrics [8, 9]. This kind of transistor architecture has a large potential for scaling due to the excellent electrostatics provided by the gate-all-around structure. Recently, DC operation of well scalable vertical nanowire MOSFETs has been presented [8]. In this Letter, the high-frequency performance of a similar structure is presented.

Device structure and fabrication: Schematics and SEM images of the finished device are shown in Fig. 1. The vertical nanowire MOSFET processes can generally be divided into gate-last and gate-first processes. The difference between the two processes is highlighted in Fig. 1*a*. Gate-first devices generate thin nanowire contacts and leave ungated regions at the top, which will increase the access resistance. Gate-last devices have addressed this problem by forming a recessed gate and adding metal on the nanowire sidewalls to reduce the access resistance, therefore decoupling the relation between the contact resistance and channel diameter. In this Letter, the RF performance of the gate-last MOSFETs is evaluated.

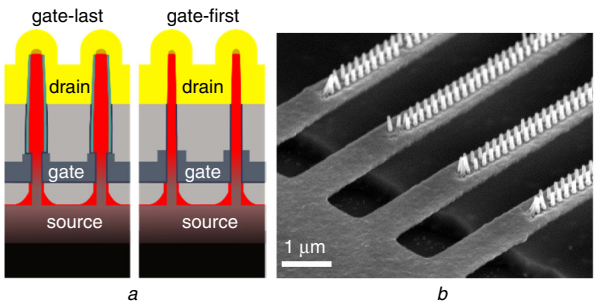

Fig. 1 *Illustrations of the vertical nanowire MOSFETs structure*

a Schematic illustration of finalised device
b SEM picture after gate-finger fabrication. Isolation mesa and air bridge allow reduction in the parasitic capacitance

The fabricated gate-last MOSFETs are based on InAs/$In_{0.4}Ga_{0.6}As$ heterostructure nanowires fabricated on a highly resistive Si{111} substrate. The nanowire consists of three parts: (i) a 100-nm-long highly doped InAs bottom segment; (ii) a 100-nm-long segment with unintentionally doped grading from InAs to InGaAs; and (iii) a 300-nm-long highly doped InGaAs top segment. The gate is connected to the InAs and the graded segment. A detailed DC evaluation of similar nanowire structures including gate-length scaling has been shown earlier [9]. The fabrication closely follows the process flow previously used up to the gate-metal deposition; here the process is adjusted by reducing the gate-drain and gate-source capacitance. After the 60-nm-thick W gate-metal is deposited, finger gate structures are patterned using deep ultraviolet and electron-beam lithography patterning. The finger gate process was presented in [10]. The patterned fingers are dry-etched and the isolation mesa is wet-etched, forming a structure as shown in Fig. 1*b*. In the figure, the gate pad is separated from the source by an air bridge between the source and gate pad. The device is finalised by depositing a second spacer, contact vias, and contact pads.

Results: In Fig. 2, transfer and output characteristics of a device with 180 nanowires are shown. The channel diameter is 30 nm and $L_g = 120$ nm. The device saturates well, which leads to a good intrinsic voltage gain $g_m/g_d = 12$. The device $R_{on} = 780$ Ωµm and $g_m = 1.1$ mS/µm correlate well with the state-of-the-art vertical III–V MOSFETs with the corresponding L_g, although here, the doped source causes a degraded subthreshold performance (subthreshold swing = 380 mV/dec) due to a dopant memory effect during growth.

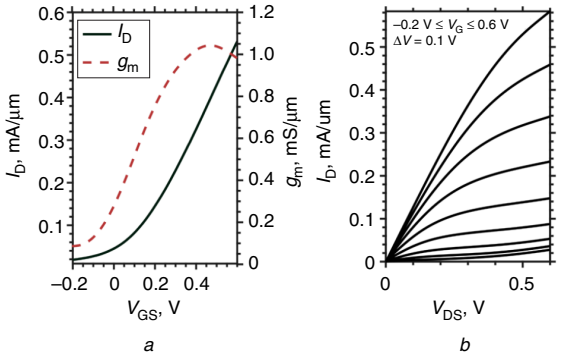

Fig. 2 *DC characterisation of the vertical nanowire MOSFET with 180 nanowires, average diameter 30 nm and $L_g = 120$ nm*

a Transfer characteristic measured at $V_{DD} = 0.5$ V
b Output characteristic

In Fig. 3, the high-frequency performance of the MOSFET and the corresponding small-signal model are presented. *S*-parameters were measured from 10 MHz to 67 GHz using an Agilent E8361A vector network analyser. Calibration was performed by using off-chip two-port line reflect reflect match calibration and on-chip open/short de-embedding. The implemented small-signal model results in a good fit to the experimental data, as shown in Fig. 3*a*, where measured and modelled forward current gain h_{21}, the unilateral power gain U, and the maximum stable/available gain MSG/MAG are presented. Based on the model, $f_t = 122$ GHz and $f_{max} = 131$ GHz can be extrapolated. The device achieves a high gain of MSG = 14.5 dB at 20 GHz, which is comparable to planar RF nanowire MOSFETs with $f_{max} = 400$ GHz [11]. The lower f_{max} in the vertical MOSFET is attributed mainly to the larger gate resistance R_g. This conclusion can be drawn from the approximate equations, which relate the small-signal parameters from Fig. 3*a* to the cut-off frequency f_T, the maximum oscillation frequency f_{max}, and the maximum stable gain (MSG)

$$f_{max} \simeq \sqrt{f_T/(8\pi R_g C_{gd})}, \quad (1)$$

$$f_T \simeq g_{m,i}/[2\pi(C_{gd} + C_{gs,i} + C_{gs,p})], \quad (2)$$

$$|\mathrm{MSG}| \simeq g_{m,i}/(\omega C_{gd}). \quad (3)$$

In the on-state of the transistor, the parasitic gate-drain capacitance dominates over the intrinsic one, so that the model in Fig. 3*b* does not differentiate between the two and C_{gd} mainly consists of the parasitic contribution. Owing to the asymmetric gate-last process of the vertical MOSFETs, a reduction of this parasitic C_{gd} to about 8 fF was possible without deteriorating other parameters. It is likely that the main restriction for $f_{max}$is the gate resistance R_g. Reduction of R_g would require further process development.

For the gate-source capacitance, both the parasitic $C_{gs,p}$ and the intrinsic $C_{gs,i}$ can be determined from the small-signal model. Equation (2)

indicates that $C_{gs,p} = 15$ fF is a major limiting factor for f_T. $C_{gs,p}$ mainly originates from the plate-capacitor-like structure and fringing capacitance of the gate fingers, compare Fig. 1*b*. Owing to the highly doped shell around the bottom of the nanowires (cf. Fig. 1*a*) it is possible to reduce $C_{gs,p}$ by increasing the distance of the gate fingers from the substrate without largely increasing the access resistance. The intrinsic $C_{gs,i}$ can be scaled by reducing the gate length. Gate-length down to 25 nm has already been demonstrated for vertical nanowire MOSFETs with a 100-nm-thick bottom spacer [8]. Thus, by straightforward dimension scaling, f_T and f_{max} can be drastically increased in further transistor generations.

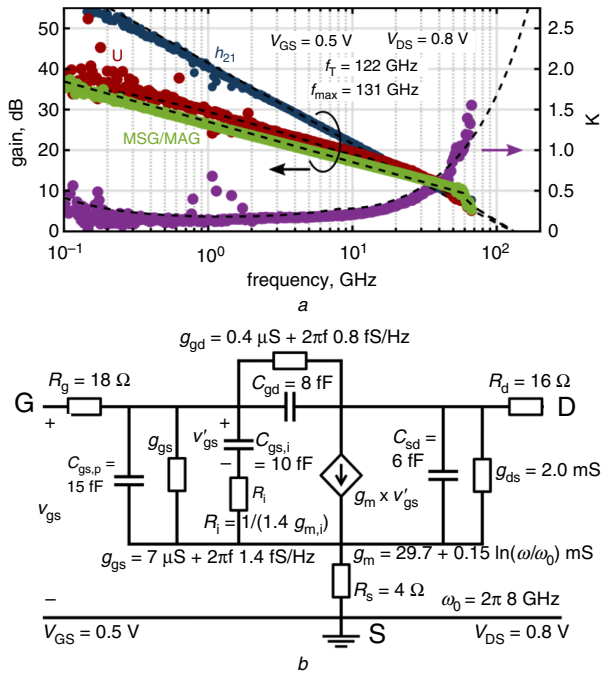

Fig. 3 *RF characterisation of the vertical nanowire MOSFET with 180 nanowires, average diameter 30 nm and $L_g = 120$*

a Measured current gain h_{21}, maximum stable/available gain MSG/MAG, and stability factor *K*. Dashed line describe fitted small-signal model
b Small-signal model with the fitted values for the measurement presented in (a)

Table 1 benchmarks the performance of this work versus other III–V RF MOSFETs on Si [6] and versus 28 nm silicon on insulator (SOI) RF MOSFETs [7] with comparable gate-lengths. Although the device structure of the asymmetric MOSFETs presented here is not fully optimised yet, its RF performance is comparable to that of the other technologies. As discussed, further improvement is mostly a matter of scaling the structure to reduce the capacitances.

Table 1: Comparison of RF MOSFETs on Si with similar gate-lengths

	L_g, nm	g_m, mS/µm	f_T, GHz	f_{max}, GHz
this work	120	1.1	125	130
SOI 28 nm [7]	90	0.9	110	103
SOI 28 nm [7]	150	0.75	70	80
III–V on Si [6]	100	1.3	140	170
III–V on Si [6]	150	1	100	120

In Fig. 4*a*, C_{gs} and C_{gd} are shown as a function of V_{GS} at different drive voltages ($V_{dd} = 0.2$, 0.5 and 0.8 V). For C_{gd}, it is straightforward to extract the parasitic capacitance from the off-state, $C_{gd,p} \simeq 8$ fF. Furthermore, the figure confirms that for high V_{dd}, C_{gd} is barely affected by an intrinsic contribution. C_{gs} does not saturate for the lowest V_{GS} measured, which is likely because of the high channel doping due to the memory effect as mentioned previously. However, based on the trend in Fig. 4*a*, $C_{gs,p} \simeq 15$ fF and $C_{gs,i} \simeq 10$ fF can be estimated for the small-signal model in Fig. 3*b*. Fig. 4*b* presents g_m derived from *S*-parameter measurements at 50 MHz for the same bias points as the capacitances in Fig. 4*a*. The extracted g_m corresponds well with the DC measurements in Fig. 2 and only minor improvement in g_m is observed when increasing V_{dd} over 0.5 V.

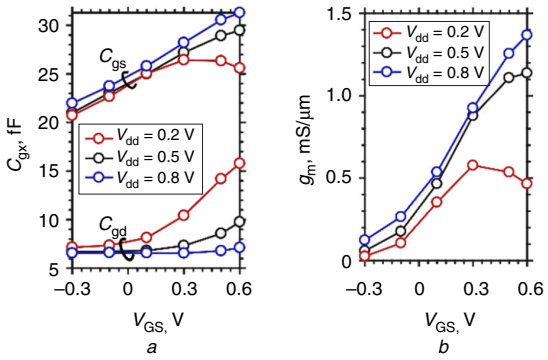

Fig. 4 *C_{gs} and C_{gd} bias dependence*

a Transistor with 180 nanowires, average diameter 30 nm and $L_g = 120$ nm. g_m bias dependence
b Measured at 50 MHz. g_m corresponds well with the earlier presented DC measurements

In the small-signal model in Fig. 3, the intrinsic transconductance ($g_{m,i}$) is the constant part of the total g_m. At frequencies below a certain ω_0, g_m is reduced due to the presence of border traps in the gate oxide [12], which gives rise to the logarithmic term in the expression for g_m. ω_0 is the frequency at which border traps cannot respond to the AC signal anymore. The intrinsic resistance $R_i = 1/(1.4\ g_{m,i})$ in series with $C_{gs,i}$ takes into account the delay, which charge carriers experience when moving inside the channel. Physically, a corresponding intrinsic resistance should be placed in series with the intrinsic gate-drain capacitance, but since C_{gd} is dominated by the parasitic component, as described earlier, the resistance is disregarded.

Besides the g_m-*f* dispersion, border traps also give rise to the frequency dependence of the conductances g_{gd} and g_{gs} in the small-signal model, which is based on modelling the border traps by distributed RC networks as elaborated in [13]. The constant part of g_{gd} and g_{gs} models DC gate leakage. All components in the model can be determined from the real and imaginary part of the admittance parameters at different frequencies and all are necessary for accurate modelling of the RF response of the transistors. Fig. 3*a* demonstrates excellent agreement between measured and modelled values.

Conclusion: Vertical nanowire gate-last high-frequency MOSFETs on Si have been demonstrated. The devices show performance comparable to or higher than other Si and III–V MOSFETs on Si with similar gate-length. The devices are fabricated by using a scalable gate-last process, which has been shown to be scalable down to 25 nm.

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One or more of the Figures in this Letter are available in colour online.

O.-P. Kilpi, M. Hellenbrand, J. Svensson, E. Lind and L.-E. Wernersson (*Department of Electrical and Information Technology, Lund University, Box 118 S-22100, Lund, Sweden*)

✉ E-mail: olli-pekka.kilpi@eit.lth.se

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