



LUND UNIVERSITY

Test Scheduling and Test Access Optimization for Core-Based 3D Stacked ICs with Through-Silicon Vias: poster

Sengupta, Breeta; Ingelsson, Urban; Larsson, Erik

Published in:

European Test Symposium (ETS11), Trondheim, Norway, May 23-27, 2011., 2011

2011

Document Version:

Publisher's PDF, also known as Version of record

[Link to publication](#)

Citation for published version (APA):

Sengupta, B., Ingelsson, U., & Larsson, E. (2011). Test Scheduling and Test Access Optimization for Core-Based 3D Stacked ICs with Through-Silicon Vias: poster. In *European Test Symposium (ETS11), Trondheim, Norway, May 23-27, 2011., 2011*

Total number of authors:

3

General rights

Unless other specific re-use rights are stated the following general rights apply:

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: <https://creativecommons.org/licenses/>

Take down policy

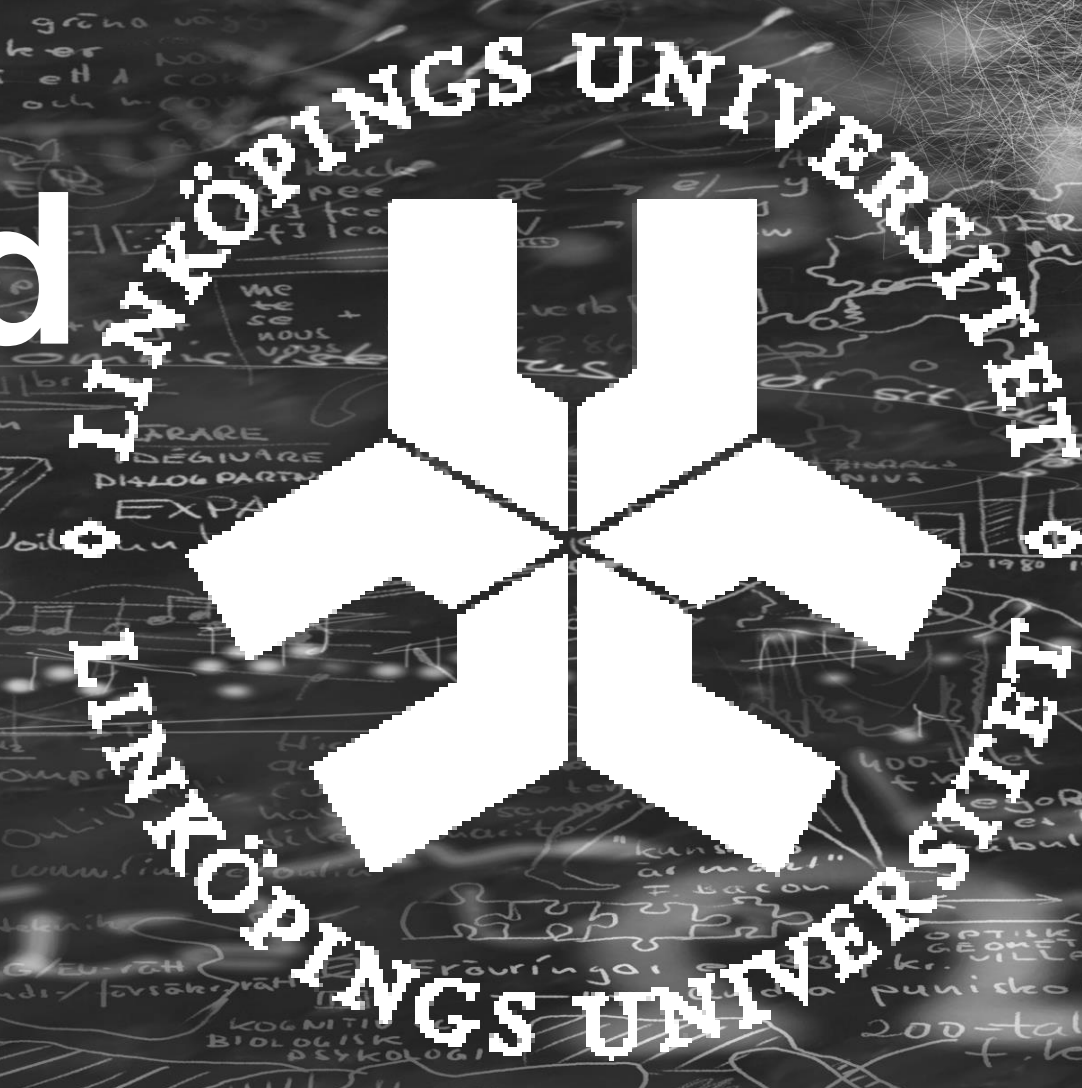
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Test Scheduling and Test Access Optimization for Core-Based 3D Stacked ICs with Through-Silicon Vias

Breeta SenGupta Urban Ingelsson Erik Larsson
 {breeta.sengupta, urban.ingelsson, erik.larsson}@liu.se
 Linköping University, Sweden



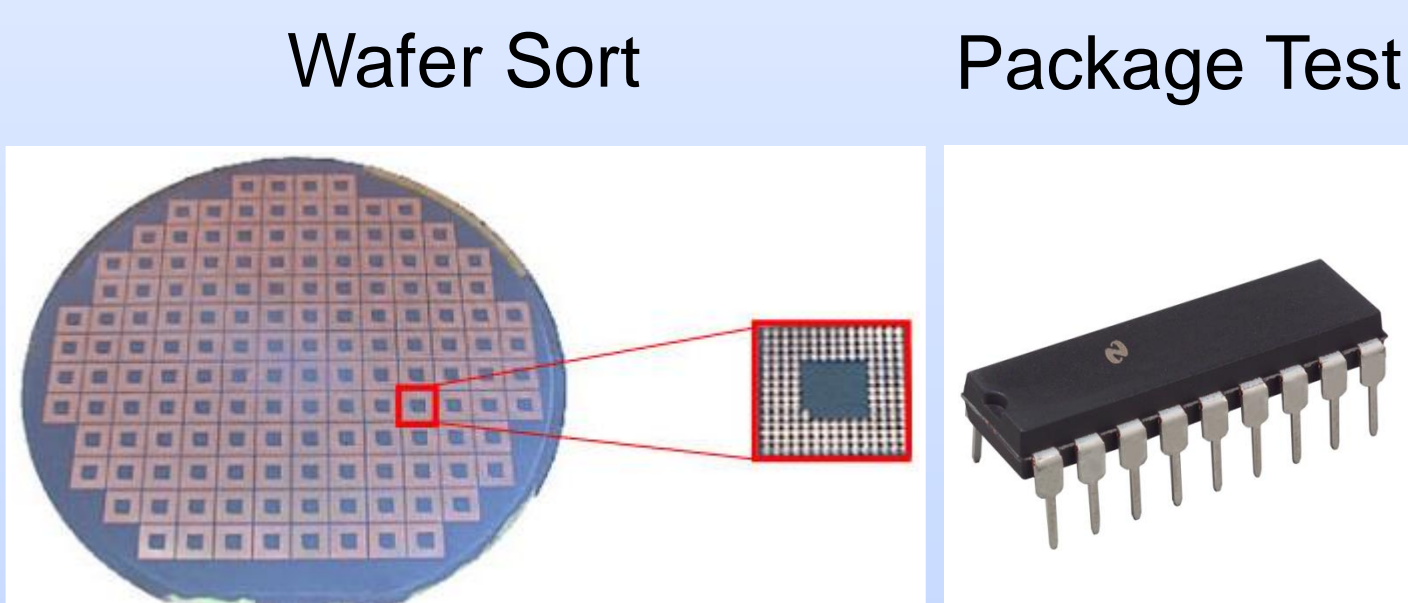
Purpose

- ❖ Schedule core tests for 3D stacked ICs (SICs) with Through-Silicon Vias (TSVs)
- ❖ Reduction of overall test time (wafer sort + package test)
- ❖ Consider hardware cost of test data registers (TDRs)

1 Manufacturing Test

Testing of non stacked chips

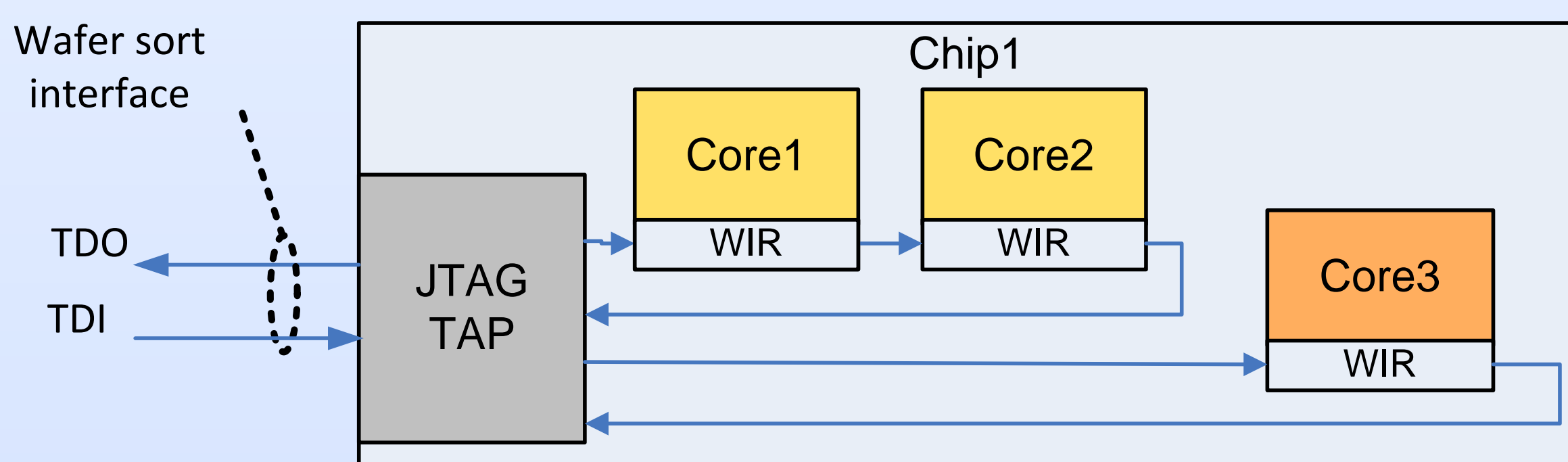
- Two stages
 - Wafer sort
 - Package test
- Same schedule in both stages



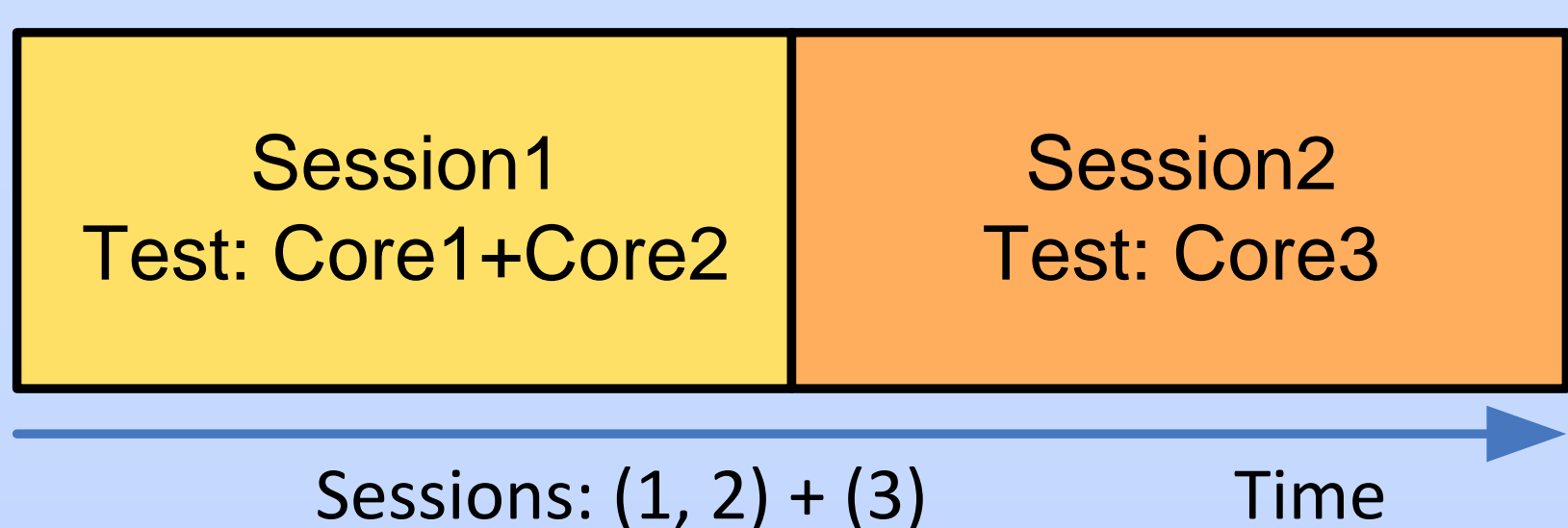
Testing of 3D Stacked chips

- Two stages
 - Wafer sort (individual chips)
 - Package test (all chips combined)
- Creating the schedule for package test by applying wafer sort test schedules serially may lead to sub optimal test time
- Test scheduling is therefore different from non stacked chip testing

2 Wafer Sort



- Above: Test access mechanism for a single chip during wafer sort
- Cores in the chips are accessed by JTAG
- On each chip, only one TDR can be accessed at a time
- Cores on the same TDR are in the same session
- Core1 and Core2 share the same TDR, therefore must be tested in the same session (Session1)
- Core3 has an independent TDR, therefore Core3 must have a separate session (Session2)
- Therefore, additional sessions \Rightarrow Additional TDR hardware cost



Trade off between test time and number of TDRs among various alternatives

When Core1 and Core2 are in the same session

- TDRs required: 1
- Test time required:

$$T_{(1,2)} = \max(P_1, P_2) \cdot (L_1 + L_2 + 1) + (L_1 + L_2) = 1700$$

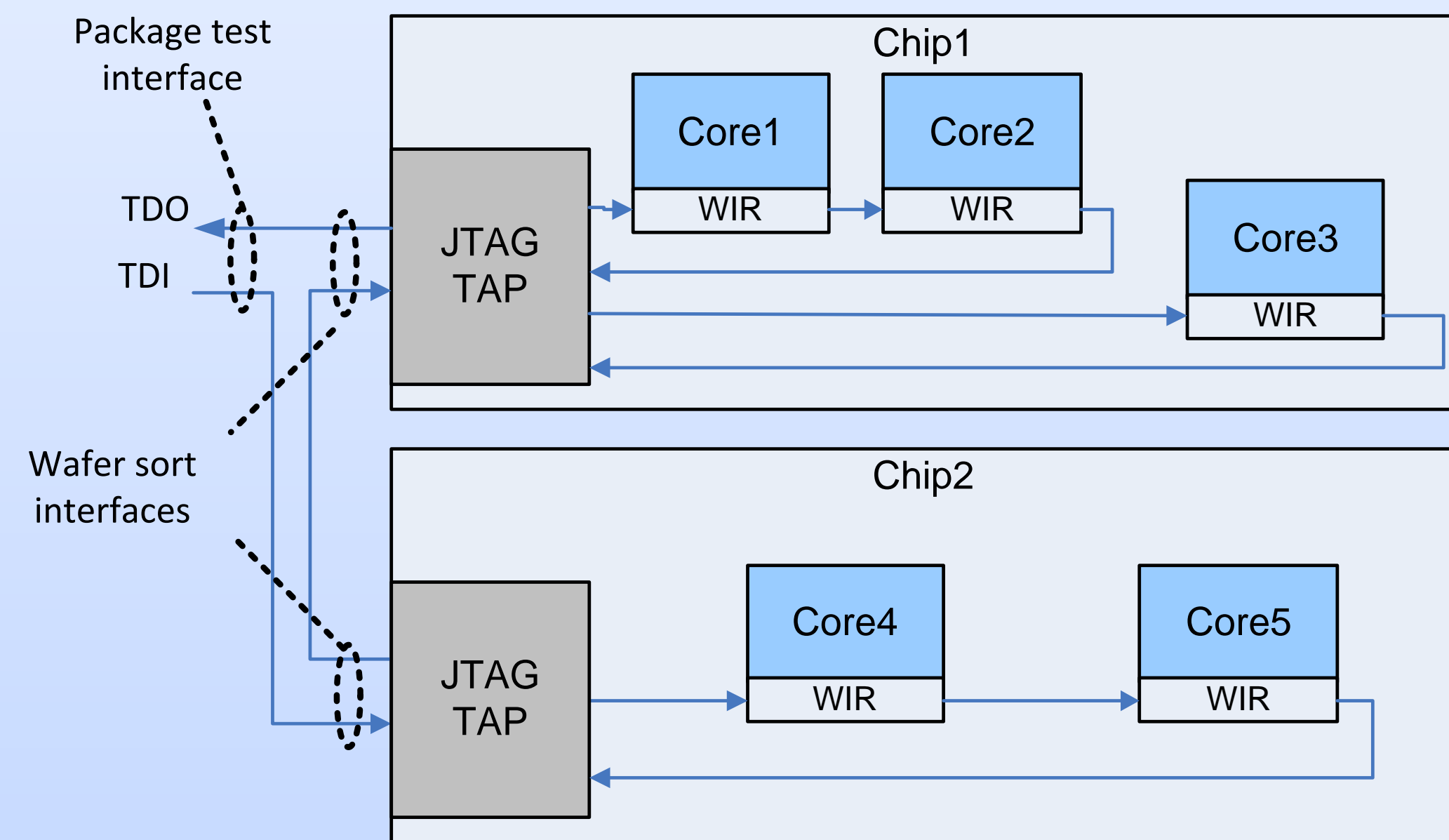
When Core1 and Core2 are in different sessions

- TDRs required: 2
- Test time required:

$$T_{(1)+(2)} = (L_1 + 1) \cdot P_1 + L_1 + (L_2 + 1) \cdot P_2 + L_2 = 1210$$

- Number of TDRs required increases
- Required test time decreases
- To obtain the lowest overall cost (test time and hardware), there is a trade-off between test time and the number of TDRs

3 Package Test



Above: Test access mechanism for a stack during package test

When Core3, Core4 and Core5 are in the same session

- TDRs required: 2
- Test time required: $T_{(3)+(4,5)} = 340 + 3600 = 3940$

When Core3 is in a different session with Core4 and Core5

- TDRs required: 2
- Test time required: $T_{(3,4,5)} = \max(340, 3600) = 3600$
- Number of TDRs required remains same
- Required test time decreases
- To obtain the lowest overall cost (test time and hardware), cores of different chips should be tested concurrently

4 Objective

Co-optimization of overall test time (wafer sort + package test) along with the TDR (hardware) cost

5 Experimental Results

The L and P values for each core is provided in the table below, for the 3D TSV-SIC design considered

	Chip1		Chip2		
	Core 1	Core 2	Core 3	Core 4	Core 5
Length of scan chain (L)	50	30	10	40	20
Number of patterns (P)	10	20	30	40	50

The test time variations with the number of sessions is shown

Cases	Wafer Sort				Package Test		Total Time	Number of TDRs
	Chip 1		Chip 2		Core Test in Session			
	Core Test in Session	Time	Core Test in Session	Time	Time	Time		
1	(1) + (2) + (3)	1400	(4) + (5)	2600	(1) + (2) + (3) + (4) + (5)	4000	8000	5
2	(1, 2) + (3)	2000	(4, 5)	3600	(1, 2) + (3) + (4, 5)	5600	11200	3
3	(1, 2) + (3)	2000	(4, 5)	3600	(1, 2) + (3, 4, 5)	4700	10300	3
4	(1, 2, 3)	3000	(4, 5)	3600	(1, 2, 3) + (4, 5)	6600	13200	2
5	(1, 2, 3)	3000	(4, 5)	3600	(1, 2, 3, 4, 5)	7500	14100	2

- It is seen that Case 3 has lower test time as well as number of sessions when compared to Case 6
- Compared to Case 4, Case 3 has lower test time but more TDRs
- The lowest total time is achieved at the highest TDR cost
- The lowest number of TDRs is achieved at a high cost in terms of test time

Conclusions

- ❖ Testing of stacked 3D chips is different from non-stacked chip testing, since, in the case of 3D TSV-SICs, the package test requires all chips in the stack to be tested together
- ❖ Increase in number of sessions \Rightarrow Increase in number of TDRs \Rightarrow Increased Cost
- ❖ Core tests of different chips performed simultaneously during package test may lead to reduction in the total test time
- ❖ This also leads to lower TDR cost