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Power Constrained Test Scheduling for 3D Stacked Chips: poster

Sengupta, Breeta; Ingelsson, Urban; Larsson, Erik

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# Power Constrained Test Scheduling for 3D Stacked Chips

Breeta SenGupta   Urban Ingelsson   Erik Larsson

{breeta.sengupta, urban.ingelsson, erik.larsson}@liu.se

Linkopings University, Sweden

Purpose :-

- ❖ Schedule core tests for stacked 3D chips
- ❖ Minimize the Test Application Time (TAT)
- ❖ A maximum power limitation
- ❖ The cost of control lines is considered

Test Scheduling Modes :-
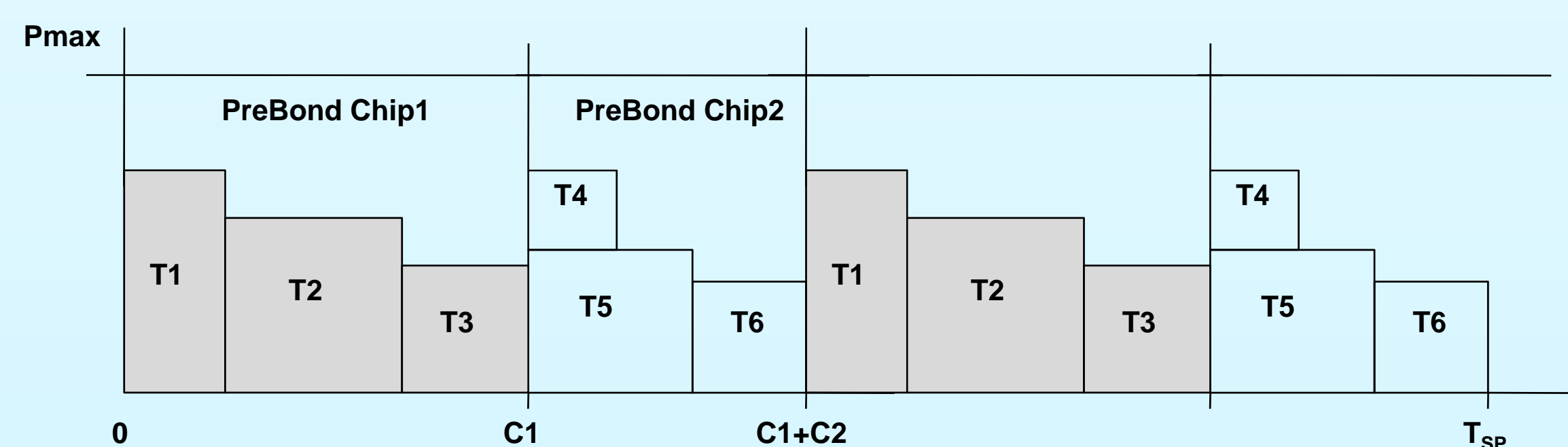
Serial Processing (SP)

- ➤ Pre-bond test schedules of each chip are performed serially in post-bond
- ➤ Minimizing pre-bond requirement for control lines for each chip, the overall number of control lines remain at a minimum
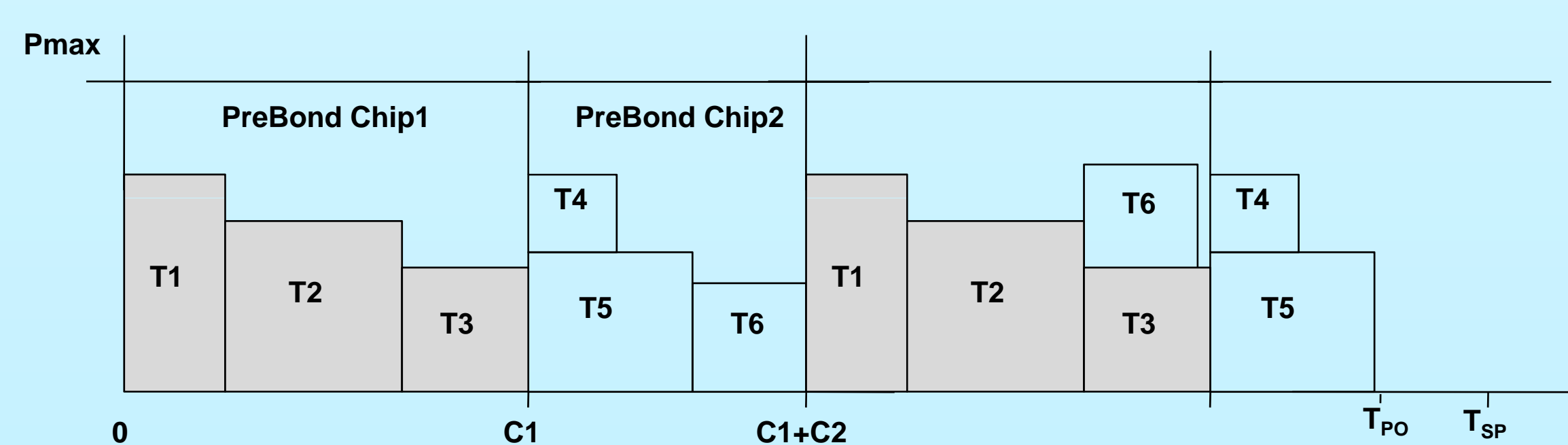
Partial Overlap (PO)

- ➤ In post-bond, power compatible sessions of pre-bond are performed concurrently
- ➤ The number of sessions for each chip still remains the same, hence the number of control lines required also remain at a minimum, the same as SP
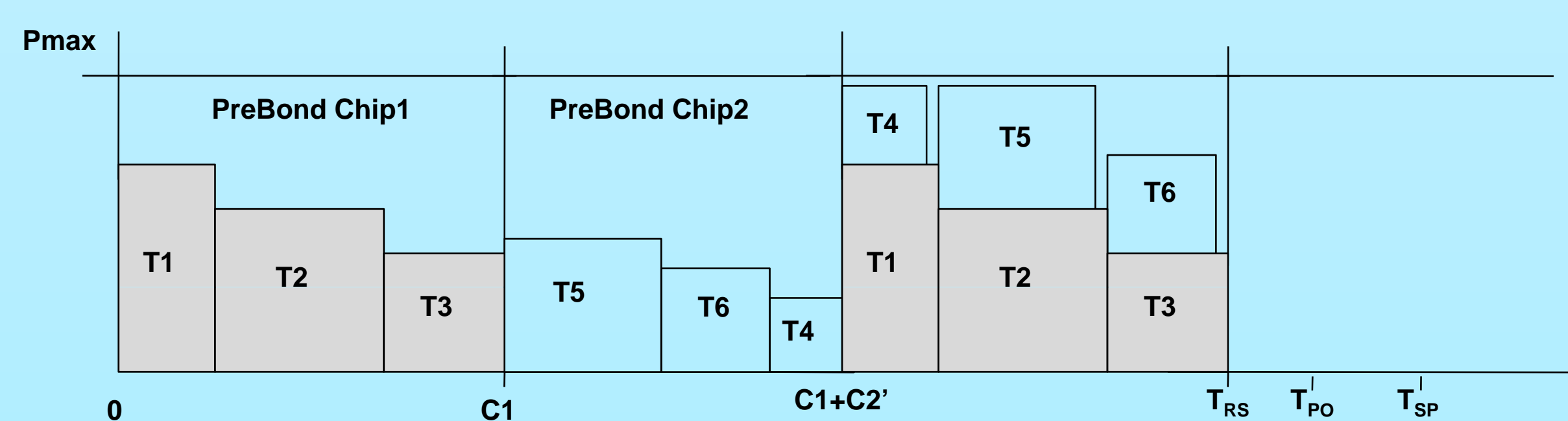
ReScheduling (RS)

- ➤ Sessions are split in pre-bond, such that they can be performed concurrently with sessions of other chips in post-bond, thus reducing the overall test time
- ➤ Each split of session requires an additional control line

Pre-bond tests in SP are scheduled as per: V. Muresan *et al*. Greedy Tree Growing Heuristics on Block-Test Scheduling Under Power Constraints, *JETTA*, 2004.

Introduction :-

Non Stacked Chip Testing

- ➤ Two stages
  - ➤ Wafer sort
  - ➤ Final test
- ➤ Single schedule

Pre-bond and post-bond test schedule

3D Stacked Chip Testing

- ➤ Two stages
  - ➤ Pre-bond (individual chips)
  - ➤ Post-bond (all chips combined)
- ➤ Multiple schedules

Principle :-

The main objective of the algorithm implemented for ReScheduling are:

- ➤ Minimum number of splitting of sessions (wrt SP test schedules)

  This helps in keeping the number of control lines to a minimum.
- ➤ The minimum TAT is accepted which has an acceptable number of control lines

The objective is attained by:

- ➤ Considering two pre-bond sessions at a time, which belong to two different chips

  This preserves the sessions defined by SP to the maximum possible extent, since all tests in the stack are not considered individually
- ➤ Reductions in test time for all possible session pairs is calculated and tabulated, TAT_{RS} is obtained by maximizing the sum of the time reductions by mutually exclusive session pairs, from the table.

The problem has a large solution space, hence a greedy heuristic was applied, which has a overall complexity of $O(N \log N)$ for N sessions

Experimental Results :-

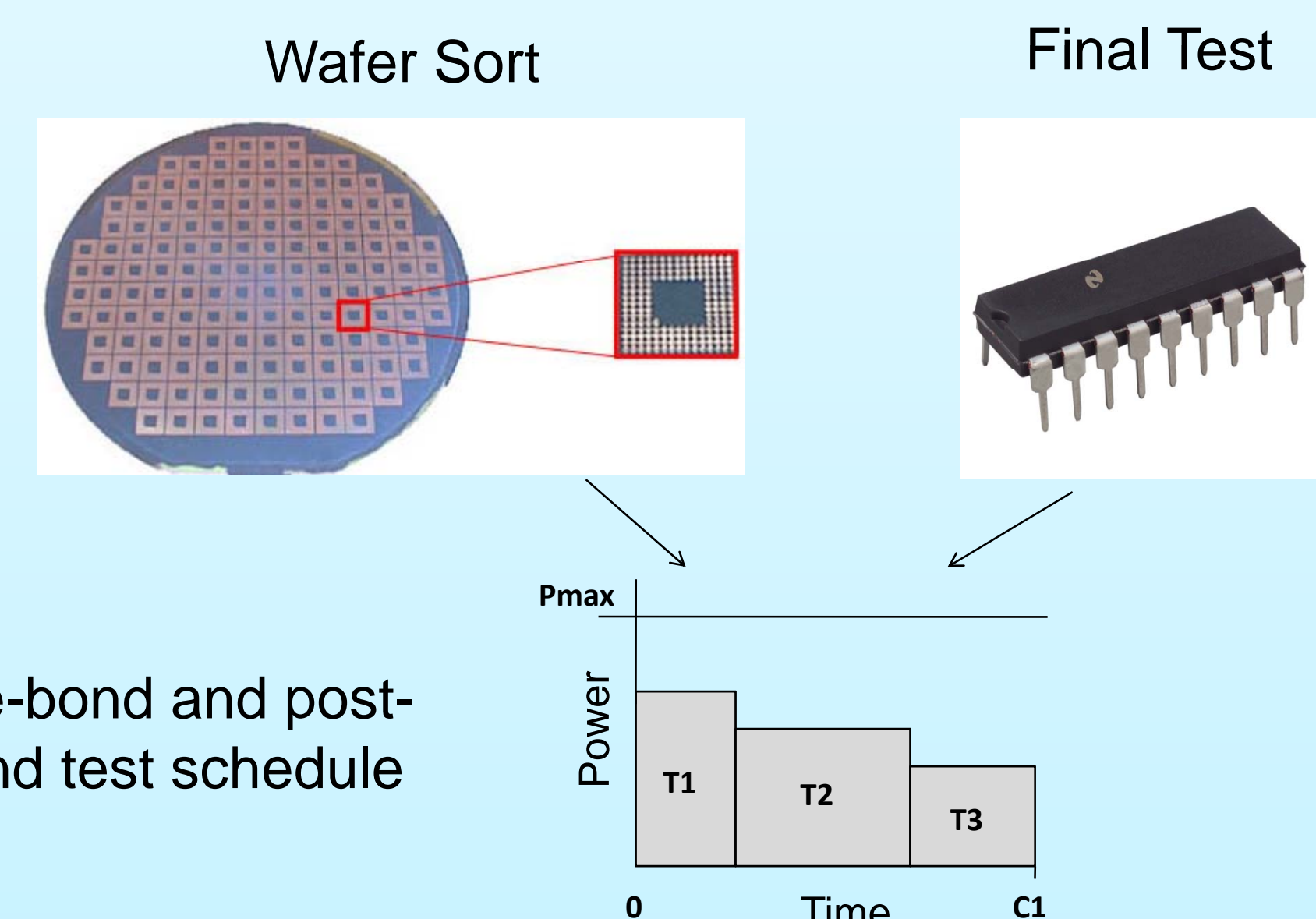| | Chip1 | | | | Chip2 | | | | Chip1 & Chip2 | | | | TAT | | | | Incr. in control lines |
| | Pre-bond Test | | | | Pre-bond Test | | | | Post-Bond Test | | | | Pre-bond + Post-bond | | | | %(orig) |
	T_{SP}	T_{PO}	T_{RS}	R (%)		T_{SP}	T_{PO}	T_{RS}	R (%)	T_{SP}	T_{PO}	T_{RS}	R (%)	T_{SP}	T_{PO}	T_{RS}	R (%)	
Z	300	300	300	0	Z	300	300	300	0	600	560	560	6.7	1200	1160	1160	3.3	0 (6)
L	1374	1374	1374	0	L	1374	1374	1592	-15.9	2748	2107	1592	42.1	5496	4855	4558	17.1	3 (36)
M	26	26	27	-3.8	M	26	26	27	-3.8	52	52	48	7.7	104	104	102	1.9	20 (10)
Z	300	300	300	0	L	1374	1374	1374	0	1674	1374	1374	17.9	3348	3048	3048	9.0	0 (16)
Z	300	300	300	0	M*	520	520	520	0	820	780	780	4.9	1640	1600	1600	2.4	0 (8)
L	1374	1374	1374	0	M**	1040	1040	1040	0	2414	1824	1824	24.4	4828	4238	4238	12.2	0 (18)

Z: ASIC Z, L: System L, M:Muresans' Design ; SP: Serial Processing, PO: Partial Overlap, RS: ReScheduling, R: Reduction (test time)

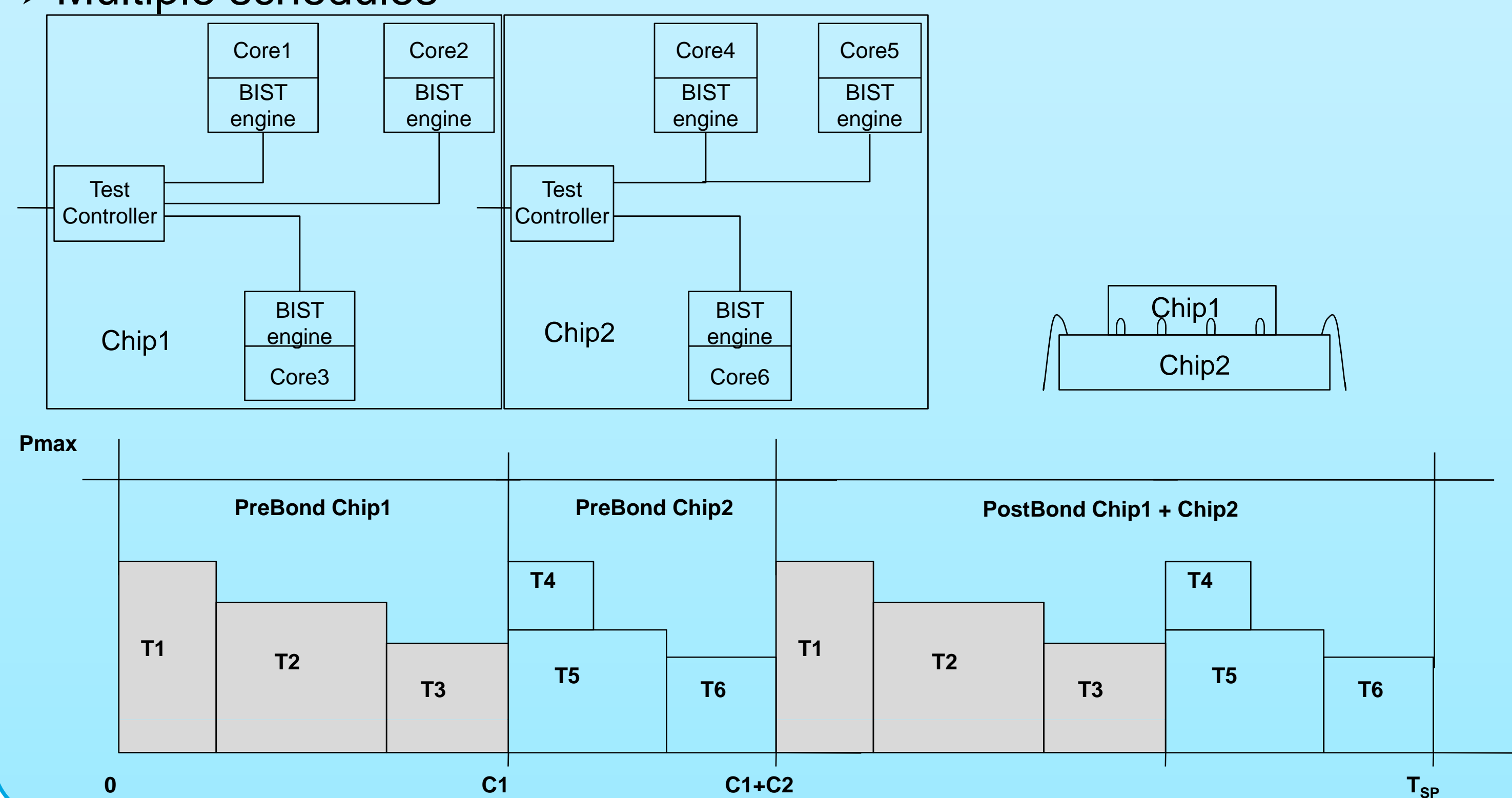RS shows significant test time reductions wrt SP and PO

Conclusions :-

- ❖ Testing of stacked 3D chips is different from non-stacked chip testing, as the same test schedule does not hold good in pre-bond and post-bond stages
- ❖ Splitting of sessions ⇒ Increase in Number of Control Lines ⇒ Increased Cost
- ❖ ReScheduling focuses on minimal splitting of pre-bond sessions
- ❖ Experimental results depict up to 42% reduction in post-bond test time and 17% in overall test time