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Low-Power Resistive Memory Integrated on III-V Vertical Nanowire MOSFETs on Silicon

Mamidala Saketh Ram, Karl-Magnus Persson, Mattias Borg and Lars-Erik Wernersson

***Abstract*— III-V vertical nanowire MOSFETs (VNW-FETs) have the potential to extend Moore's law owing to their excellent material properties. To integrate highly scaled memory cells coupled with high performance selectors at minimal memory cell area, it is attractive to integrate low-power resistive random access memory (RRAM) cells directly on to III-V VNW-FETs. In this work, we report the experimental demonstration of successful RRAM integration with III-V VNW-FETs. The combined use of VNW-FET drain metal electrode and the RRAM bottom electrode reduces the process complexity and maintains material compatibility. The vertical nanowire geometry allows the RRAM cell area to be aggressively scaled down to 0.01 μm^2 enabling realization of dense memory (1T1R) cross-point arrays on silicon.**

***Index Terms*— Resistive random access memory (RRAM), 1T1R, ITO, Vertical nanowire, InAs, InGaAs, Gate-All-Around MOSFET**

I. Introduction

Neuromorphic and In-memory computing have gained a rapid increase in interest [1-3]. These systems are being developed to speed up handling of large data sets within information heavy applications [4]. The major roadblock to increase energy efficiency and to reach faster computing speed using conventional von-Neumann architecture is the separation of the memory and processing unit. In-memory boolean computing using Resistive Random Access Memories (RRAMs) show promise and is expected to emerge as a potential technology to break the von-Neumann bottleneck [8]. The 1T1R (1-transistor-1-resistor) configuration has also been used in memristive neural networks and to demonstrate logic operations [5-8]. It makes use of a transistor as the selector coupled with a memory cell. The main advantages of using a transistor selector in memristive crossbar arrays are: (1) it inhibits current sneak paths, which would otherwise limit the array size, and (2) it provides a robust and adjustable compliance current level protecting the memory cell from a hard breakdown and switching instabilities, and (3) unlike a diode selector, it does not substantially increase the required operational voltage.

The IRDS 2020 has recently identified Vertical Gate-All-Around (GAA) Metal-Oxide-Semiconductor Field-Effect-transistors (MOSFETs) as the selector in need for dense RRAM cross-point arrays [9]. Although selector-less RRAMs and RRAMs on vertical silicon (Si) MOSFETs have been demonstrated to be promising, using a III-V selector would allow to scale the supply voltage for a constant programming and read-out current while simultaneously suppressing leakage currents [10-12]. An optimized III-V VNWFET reported in Kilpi et. al. [13] shows an OFF-state leakage current of below 1 nA/μm and the ON-state current saturates at a low supply voltage of only 0.5 V. This allows efficient suppression of sneak-path leakage currents while delivering high operation currents [13]. A record high g_m > 3 mS/μm and low R_{ON} = 190 Ωμm at V_{DS} = 0.5 V have been reported on a scaled III-V VNW-FET with L_G = 25 nm and a channel diameter of 17 nm with a similar process used for the selector in this work [14].

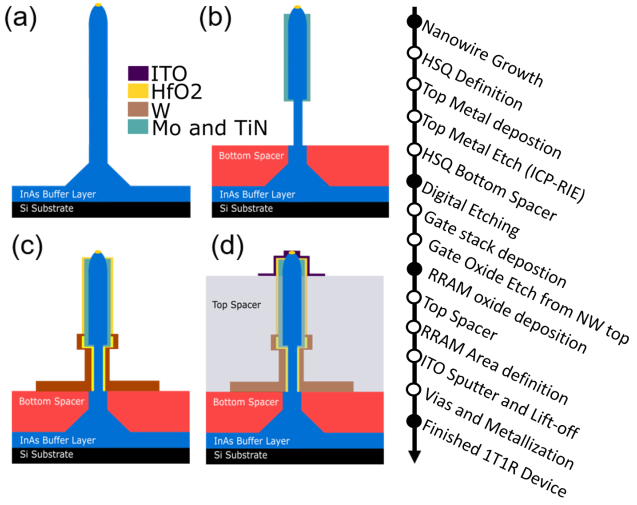

Fig. 1. Cross-sectional process schematic of the VNW 1T1R after (a) Nanowire growth (b) RRAM BE/MOSFET drain metal patterning (c) selector gate stack deposition (d) RRAM area definition and process completion

A planar MOSFET selector significantly increases the minimal area footprint. The favourable III-V material properties combined with the vertical NW geometry allow decoupling the gate and contact lengths from the area footprint leading to higher integration densities. [12-16]. Recently, HfO_2 has gained attention as a switching oxide for RRAMs and metal electrodes for RRAMs such as platinum (Pt), titanium nitride (TiN) and indium-tin-oxide (ITO) have been explored [17-21]. ITO is an attractive option for the top electrode (TE) as it prevents the RRAM from a hard-breakdown due to its self-

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compliance properties and accomplishes low voltage (sub-0.6 V) switching, enabling low-power RRAM operation [22, 23]. The ITO/HfO_2 RRAM compatibility with vertical III-V nanowires was previously demonstrated and operated with an external VNW selector in series to achieve an endurance of 10^6 cycles and a retention of 10^4 seconds measured at 125°C [23]. In this work, we report the successful monolithic co-integration of ITO/HfO_2 based RRAM with III-V vertical transistors (VNW-FETs) on the same nanowire and demonstrate that the gate can be used to program the current level within the resistive element. The compact integration as demonstrated here, not only provides efficient switching elements, it also provides a path to reduce parasitic capacitances and resistances to improve power consumption and speed.

II. Device Fabrication

The process flow for an integrated III-V VNW-1T1R device is shown in Fig. 1. First, Metalorganic Vapor Phase Epitaxy (MOVPE) is used to grow a 300-nm-thick InAs buffer layer on a p-type Si substrate. Next Au seed particles were patterned using electron beam lithography (EBL), which are then used to grow vertical nanowires by the Vapor-Liquid-Solid growth in MOVPE [24]. The top segment of the nanowire is highly doped InGaAs. A similar growth sequence with more details has been reported in [15]. The III-V VNW-FET drain contact that in our process also acts as the RRAM bottom electrode (BE) is fabricated next. This is done by first spin coating a 400-nm-thick hydrogen silsesquioxane (HSQ) film and thickness definition using EBL. 20-nm-thick Mo is sputtered followed by 15-nm-thick TiN deposited using ALD for the VNW-FET drain contact and the RRAM BE. Reactive ion etching (RIE) is used to anisotropically etch the horizontal metal layer on the HSQ so that it remains only on the vertical nanowire sidewalls. The HSQ is then removed by a buffered oxide etch (BOE). A SEM image of the III-V VNW-1T1R after top metal definition is shown in Fig. 2(a).

The gate length (L_G) of the selector III-V VNW-FET is then defined by EBL as done in the gate-last process for vertical MOSFETs [25]. In these devices, L_G was defined to be 170 nm. The highly doped shell is etched away using a digital etch process reducing the NW diameter from 32 nm to 28 nm under the gate. The gate dielectric deposited using thermal ALD is an Al_2O_3/HfO_2 bilayer. The thickness of the oxide (t_{ox}) is 4 nm that results in an EOT of 1.5 nm. For the gate metal, first, 2-nm-thick TiN is deposited using ALD after which 60-nm-thick W is deposited using sputtering. A SEM image of the device after gate stack completion is shown in Fig.2 (b). The gate dielectric that was deposited during thermal ALD is selectively removed from the top of the wire where the RRAM will be fabricated.

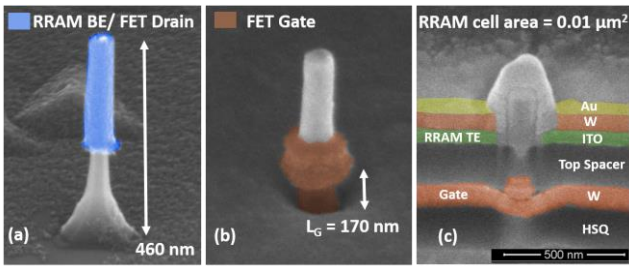

Fig. 2. SEM images of III-V VNW-1T1R after (a) drain electrode/bottom electrode deposition (b) selector gate stack deposition and (c) device completion

For the RRAM, 2.8 nm HfO_2 is deposited using plasma enhanced ALD (PEALD). The film was grown at an optimized temperature of 200°C using a tetrakis-ethylmethylaminohafnium (TEMA-Hf) precursor [26]. To isolate the VNW-MOSFET gate from the RRAM, S1813 resist spacer is applied and baked at 200°C. The RRAM cell area is defined by thinning the resist spacer using oxygen plasma until ~50 nm from the top of the nanowire is exposed. The RRAM top electrode is finally formed by sputtering 30-nm-thick ITO and definition using a lift-off process. A cross-sectional SEM image of the complete integrated device is shown in Fig.2 (c).

III. Electrical Characterization

The electrical characterization was performed using a Keithley 4200A-SCS. The integrated RRAM forming was carried out by applying a positive bias (V_{DS}) to the RRAM top electrode (TE). The bias at the selector gate (V_{GS}) was set to 1.0 V to ensure the selector is in its ON-state and delivers an ON-state current, I_{ON} = 15 μA. As the RRAM at first is in its high resistive state (HRS), most of the applied voltage falls across the RRAM before the conductive filament is formed. We observe that the forming voltage (V_{FORM}) for the integrated RRAM is ~3.1 V. The InGaAs segment at the drain segment having a wider bandgap as compared to the InAs source segment helps to protect the selector against a breakdown during the forming process [15, 23]. Once the oxygen vacancy induced filament was formed, sub-0.5 V RRAM switching was measured that is

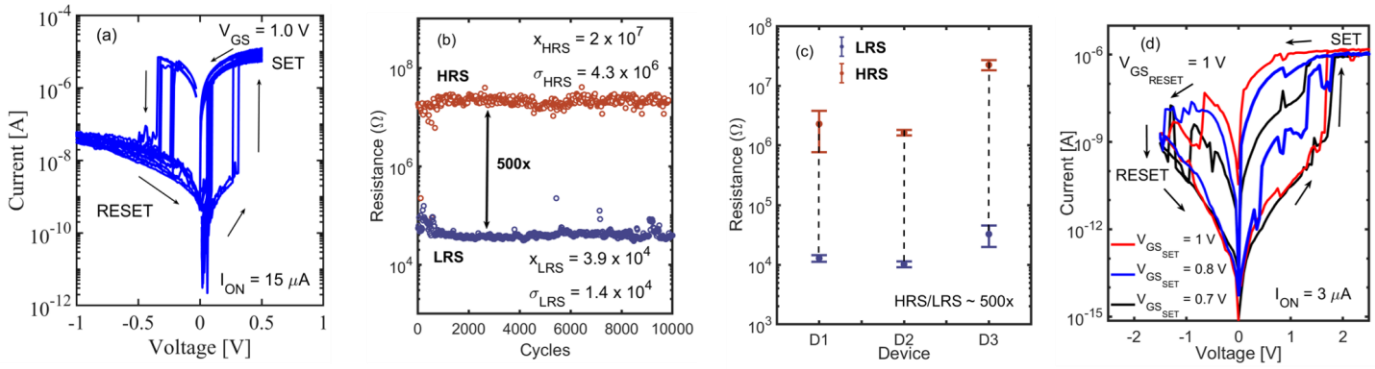

Fig. 3. (a) I-V Switching characteristics with selector I_{ON} = 15 μA (b) Endurance measurement up to 10^4 cycles with V_{READ} = -100 mV (c) Device-to-device variability of HRS and LRS between three different devices with V_{READ} = -100 mV (d) I-V switching characteristics at different V_{GS} of a III-V VNW-FET selector during the SET operation with I_{ON} = 3 μA

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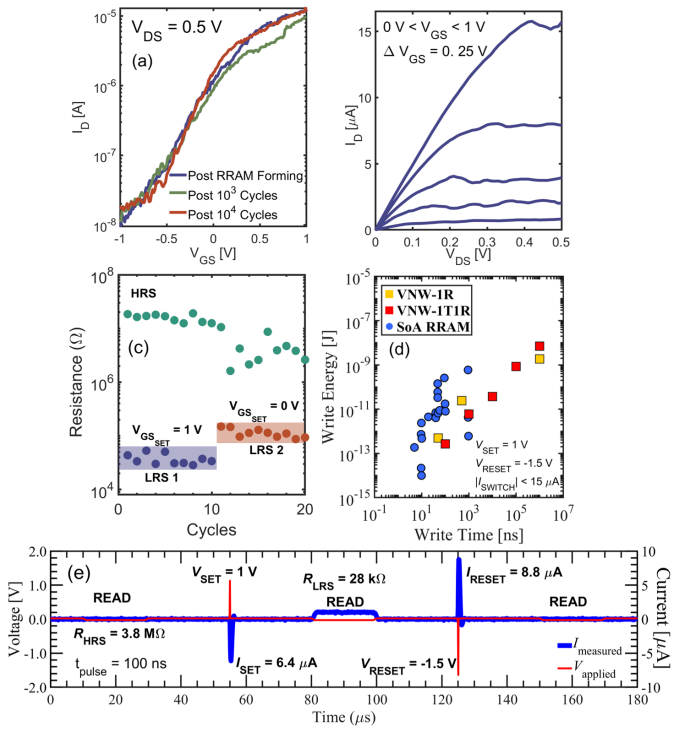

Fig. 4. (a) Transfer and (b) output characteristics of integrated III-V VNW-FET selector (c) Distinct LRS of RRAM measured at V_{READ} = -100 mV controlled by V_{GS} of selector with I_{ON} = 15 µA , V_{SET} = 300 mV and V_{RESET} = --400 mV (d) Benchmarking our results with state-of-the-art (SoA) RRAMs [27] and RRAMs integrated on III-V VNWs without an integrated selector (VNW-1R) [23] (e) Pulsed programming of integrated RRAM with pulse width, t_{pulse} = 100 ns

shown in Fig. 3(a). The endurance, shown in Fig. 3(b), was measured up to 10^4 cycles with a resistance window of 500×. The RRAM device-to-device variation in resistance states for 3 devices measured on the same sample is shown in Fig. 3(c). The data indicates that the RRAM elements operate with low cycle-to-cycle and device-to-device variability after VNW selector integration. It is to be noted from Fig. 3(d), that when the selector delivers a lower I_{ON} = 3 µA, the SET voltage (V_{SET}) is higher and the RESET current (I_{RESET}) is lower compared to the switching observed in Fig. 3(a) with a higher I_{ON}. This indicates that there is a barrier at the contact that is electrically annealed at higher currents allowing low-voltage RRAM operation. The difference in selector I_{ON} is most likely induced by variations over the sample during the VNW-FET fabrication and shows that a sufficient drive current is essential for optimal RRAM operation.

To investigate the III-V VNW-FET selector functionality, the transfer and output characteristics were measured. The integrated RRAM was first set to its low resistance state (LRS) so that a conductive path was formed between the RRAM top electrode and the drain contact of the III-V VNW-FET. The applied bias under these conditions is divided between the transistor and the RRAM in its LRS. From Fig. 4(a) and (b) it can be seen that the gate potential of the integrated III-V VNW-FET selector has good control over the selector channel. Also, there is no visible degradation in selector performance after the integrated RRAM forming and switching, which is clearly seen in Fig.4 (a). Notably, the VNW-FET gate-modulation both offers an effective way to control the compliance current in its ON-state and would block sneak currents through unselected devices in an array in its OFF-state.

The possibility to control the magnitude of the LRS by modulating the current reaching the integrated RRAM using the integrated selector gate bias is demonstrated in Fig. 3(d) and Fig.4 (c). With I_{ON} = 3 µA as shown in Fig.3 (d), the RRAM characteristics show a higher variability but multi-level LRS functionality can still be observed, which with material optimization could potentially be improved. Whereas, with a higher I_{ON} = 15 µA as shown in Fig. 4(c), two LRS levels for 10 cycles each with V_{GS} = 0 V and V_{GS} = 1 V are distinctly observable. The demonstration of distinct resistive levels combined with low-voltage operation is attractive for the prospective use in energy efficient in-memory computing systems and in neuromorphic applications. It has been shown on planar RRAMs that by introducing an Al_2O_3 barrier between the ITO and HfO_2 interface, the RESET is more gradual rather than abrupt allowing for better LRS tuning [27].

To establish fast pulsed switching capability, a series of five different SET and RESET pulse widths down to 100 ns were performed. The higher of the two calculated programming energies (SET and RESET) for each pulse width are benchmarked in Fig.4 (d) together with other state-of-the-art (SoA) resistive memories [28] as well as RRAMs integrated on III-V VNWs without an integrated selector (VNW-1R) [23]. The 100 ns pulse train is shown in Fig.4 (e). In our prior reported data of pulsed programming on VNW-1R RRAMs, the calculated power for the SET operation corresponded to P = 10 µW, which is significantly higher due to a current overshoot that in our current work is reduced by the integrated selector down to P = 2.7 µW.

It has been shown in other studies that as the area of the RRAM is scaled down, the probability of having defects that effectively reduce the required applied field for filament formation also reduces, thereby increasing the forming voltage with scaling [29]. Importantly, the 3D vertical nanowire geometry provides freedom to increase the RRAM area without increasing the total footprint, when desired. As a consequence, we can separately (1) tailor the performance of the selector by controlling L_G and (2) scale V_{FORM} of the RRAM by controlling the RRAM area without compromising the minimal footprint of the memory cell. The presented results encourage further experimental exploration of III-V vertical nanowire selectors with co-integrated resistive memory cells.

IV. Conclusions

In this letter, we have successfully demonstrated a III-V VNW-1T1R where the VNW-FET measured with the RRAM in LRS saturates at sub-0.5 V V_{DS}. The RRAM switching voltages are sub ±0.5 V at DC with a programming energy of 0.27 pJ for t_{pulse} = 100 ns. The RRAM cell area of 0.01 µm^2 and the selector L_G of 170 nm, can be varied independent of the total footprint. With the potential of a low R_{ON} and I_{OFF}, multibit capability along with the possibility to achieve highly dense cross-point arrays due to its vertical geometry, the III-V VNW-1T1R stands as a strong candidate to be used in non-volatile and energy-efficient memory applications.

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