High-Speed Analog-to-Digital Converters in CMOS

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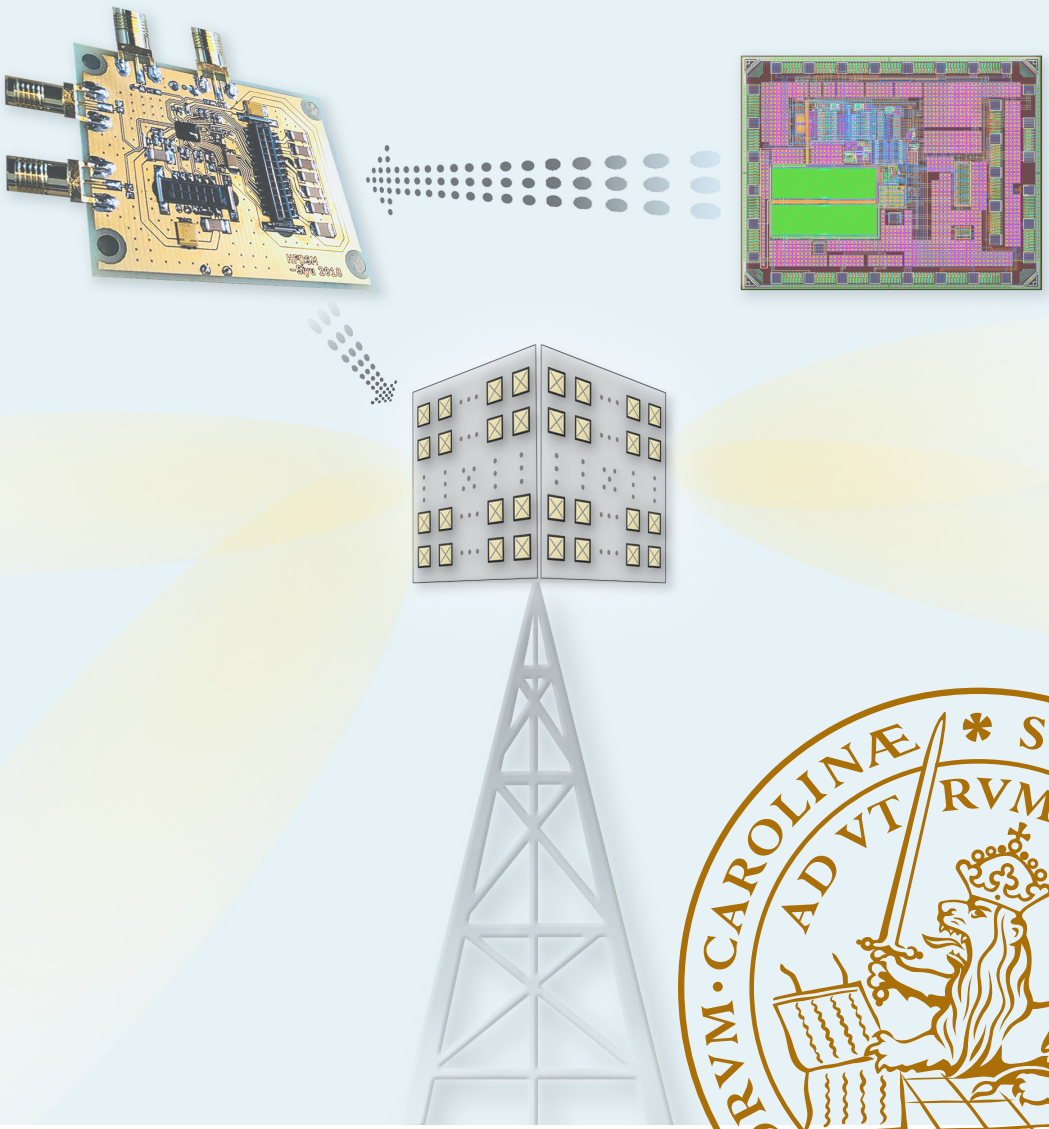

High-Speed Analog-to-Digital Converters in CMOS

by Siyu Tan

LUND
UNIVERSITY

Doctoral Dissertation

A doctoral thesis at a university in Sweden takes either the form of a single, cohesive research study (monograph) or a summary of research papers (compilation thesis), which the doctoral student has written alone or together with one or several other author(s).

In the latter case the thesis consists of two parts. An introductory text puts the research work into context and summarizes the main points of the papers. Then, the research publications themselves are reproduced, together with a description of the individual contributions of the authors. The research papers may either have been already published or are manuscripts at various stages (in press, submitted, or in draft).

Cover illustration front: an ADC CMOS chip layout and its circuit board photo, to be integrated into high-performance communication devices in the future.

Cover illustration back: a prototype ADC CMOS chip bonded on a circuit board.

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Popular Summary

Technology advancements in the 21^{st} century create a vast amount of possibilities, allowing us to make strides that our ancestors could only dream of. Communication systems improved greatly in the past several decades. The development of these systems closely follows the evolution of cellular mobile network standards to the latest commercialized 5G: the fifth generation that starts deploying globally. The emerging 5G communication systems enable reliable connections with significantly reduced latency at an increased transmission rate. Communication among people is not limited to voice-only anymore but extended to more versatile formats such as video chat and multimedia message. It is already an essential part of our daily lives: communication among us is through smart devices besides face-to-face.

Nowadays, the rapid development of high-performance handheld devices facilitates fast and secure access to the Internet: a global system that connects people worldwide. We share lives, acquire new knowledge, learn history, and explore the world without leaving home by merely surfing the Internet. The ever increased demands of smooth surfing experiences increase current communication systems' pressure and bring up the stringent requirements for technology advancement of next-generation communication devices. They prefer low latency, stable and fast upload/download transmission speed, and broad coverage with low energy dissipation.

The advance of communication systems will not be successful without the high-performance Analog to Digital Converter (ADC), an essential component in a modern high-performance radio transceiver device. The ADC acts as a bridge connecting the analog and the digital domain. Usually, the analog domain signals are real-world analog measurable physical quantities, such as voltage or current. However, the high-performance processors are entirely digital and only capable of processing signals in the digital format.

High-performance ADCs are capable of immediately digitalizing the analog sig-

nal at high-speed. A high-speed ADC coping with a high-speed digital processor can digitalize the input analog signals. It allows very flexible, reliable, and highly power-efficient digital signal processing, filtering and calibrating the digital signal in real-time. All the great features are possible thanks to the maturity of Complementary Metal Oxide Semiconductor (CMOS) technology nodes in integrated circuits.

The main focus of this research is designing high-performance ADCs on integrated circuits. This research analyzes various ADC architectures and their component-level implementations in advanced CMOS technologies. This research aims to find optimized designs for high-speed analog-to-digital conversion, understand their benefits and limitations, and evaluate the possibilities of integrating them inside the advanced base station devices in the future.

The author performed extensive literature studies to examine the state-of-the-art designs from the research field and industry before the actual circuit designs. The ADC specifications and requirements are carefully drawn up. This dissertation explains the experimented ADC designs in detail and includes the relevant research papers at the end.

Abstract

The Analog to Digital (A/D) Converters (ADC) are vital components in high-performance radio devices. In the receiver end, the signal received by the analog front-end can not be directly analyzed by the digital core, thus requiring high-performance ADC circuits acting as bridges connecting the analog and digital domain. These circuits are integrated into Complementary Metal-Oxide-Semiconductor (CMOS) chips, which achieve high performance and consume low power at the same time.

In this research, various types of ADCs are analyzed both in architectural designs and component-level implementations. The goal is to find out optimized circuit designs to be used in high-speed communication devices in the future.

Two Successive-Approximation-Register (SAR) ADCs are studied. One of the SAR ADCs is a previously designed synchronous SAR ADC CMOS chip, implemented in the 22 nm Fully Depleted Silicon On Insulator (FD-SOI) CMOS, whose measurement results are shown. An estimation and calibration technique for linearizing its Digital to Analog Converter (DAC) imbalance is presented. Another SAR ADC is improved from the synchronous version, which has asynchronously clocked internal components, designed and implemented in 22 nm FD-SOI.

Two Continuous-Time (CT) $\Delta\Sigma$ ADCs were designed and analyzed. One of the $\Delta\Sigma$ ADCs is a high-speed converter implemented in 28 nm FD-SOI CMOS, running at 5 GHz sampling frequency and targeting at 250 MHz signal bandwidth. Another $\Delta\Sigma$ ADC is implemented in 65 nm CMOS and fabricated. It evaluates the effectiveness of digital calibration techniques in linearizing a critical outer-most DAC in the feedback.

All the ADC designs showing in this work are closely related to the state-of-the-art research works. The design specifications from the industry field are

also carefully considered during the design phase. The introductions and the design details are explained in the first part of this dissertation, and the relevant research papers are attached in the second part.

Contents

List of Publications

This dissertation is based on the following publications, referred to by their Roman numerals:

I **Digital Background Calibration in Continuous-time $\Delta\Sigma$ Analog to Digital Converters**
Siyu Tan, Yun Miao, Mattias Palm, Joachim Rodrigues and Pietro Andreani
2015 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

II **A continuous-time delta-sigma ADC with integrated digital background calibration**
Siyu Tan, Yun Miao, Mattias Palm, Joachim Neves Rodrigues and Pietro Andreani
Analog Integrated Circuits and Signal Processing volume 89, pages 273–282 (2016)

III **A 5 GHz CT $\Delta\Sigma$ ADC with 250MHz Signal Bandwidth in 28 nm-FDSOI CMOS**
Siyu Tan, Lars Sundström, Mattias Palm, Sven Mattisson and Pietro Andreani
2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

IV **A 10-bit Split-Capacitor SAR ADC with DAC Imbalance Estimation and Calibration**
Siyu Tan, Daniele Mastantuono, Roland Strandberg, Lars Sundström, Pietro Andreani and Mattias Palm
2020 IEEE International Symposium on Circuits and Systems (ISCAS 2020)

V **Asynchronous vs. Synchronous CMOS SAR ADCs - A Comparison**

Siyu Tan, Mattias Palm, Daniele Mastantuono, Roland Strandberg, Lars Sundström and Pietro Andreani

Submitted to: IEEE Access

VI **A Design Method to Minimize the Impact of Bit Conversion Errors in SAR ADCs**

Siyu Tan, Mattias Palm, Daniele Mastantuono, Roland Strandberg, Lars Sundström, Sven Mattisson and Pietro Andreani

2020 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

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List of Acronyms

AAF	Anti-Aliasing Filter
ACL	Asynchronous Control Logic
ADC	Analog to Digital Converter
ASAR	Asynchronous SAR
BS	Base Station
CDAC	Capacitive Digital to Analog Converter
CIFB	Cascade of Integrators with Distributed Feedback
CIFF	Cascade of Integrators with Feed-Forward Summation
CMFB	Common-Mode Feedback
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous-Time
CRFB	Cascade of Resonators with Feedback
CRFF	Cascade of Resonators with Feed-Forward Summation
DAC	Digital to Analog Converter
DC	Direct Current
DFF	D-Flip-Flop
DT	Discrete-Time

DSM $\Delta\Sigma$ Modulator

DSP Digital Signal Processor

DUT Design Under Test

ELD Excess Loop Delay

ENOB Effective Number of Bits

ETF Error Transfer Function

FD-SOI Fully Depleted Silicon On Insulator

FinFET Fin Field-Effect Transistor

FOM$_s$ Schreier Figure of Merit

FOM$_w$ Walden Figure of Merit

FPGA Field-Programmable Gate Array

GBW Gain-Bandwidth Product

GSM Global System for Mobile Communications

IC Integrated Circuit

IoT Internet of Things

LDO Low-Dropout Regulator

LF Loop Filter

LPF Low-Pass Filter

LSB Least Significant Bit

LTE Long Term Evolution

LTI Linear Time-Invariant

MIMO Multiple-Input Multiple-Output

MCS Merged Capacitor Switching

NMOS N-Channel Metal-Oxide-Semiconductor

MOM Metal-Oxide-Metal

MSB Most Significant Bit

NTF Noise Transfer Function

NRZ Non-Return-to-Zero

OBG Out-of-Band Gain

OFDM Orthogonal Frequency-Division Multiplexing

OSR Oversampling Ratio

PCB Printed Circuit Board

PGA Programmable-Gain Amplifier

PMOS P-Channel Metal-Oxide-Semiconductor

PRBS Pseudo-Random Bit Sequence

PVT Process-Voltage-Temperature

RAM Random Access Memory

RF Radio Frequency

RA Residue Amplifier

ROM Read-Only Memory

RZ Return-to-Zero

SA Successive Approximation

SAR Successive Approximation Register

SCL Synchronous Control Logic

SNDR Signal to Noise and Distortion Ratio

SL Switch Logic

S/H Sample and Hold

SFDR Spurious-Free Dynamic Range

SNR Signal to Noise Ratio

SPI Serial Peripheral Interface

SQNR Signal to Quantization Noise Ratio

SSAR Synchronous SAR

STF Signal Transfer Function

TI Time-Interleaved

TTF Test Transfer Function

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Chapter 1

Introduction

1.1 Overview of Radio Communication

The rapid development of communication technologies has already shown huge potential in the business world and our colorful daily lives. The transmission data rate increases enormously from the Global System for Mobile Communications (GSM) systems, to the latest fifth-generation (5G) of the communication system.

The earlier generations of communication systems were only capable of voice traffic. Around 2000, the third-generation (3G) was launched worldwide, supporting more multimedia formats to be transmitted and providing access to the Internet through mobile phone networks. The Internet is one of the greatest inventions connecting individuals and the world, whose origin and development have been explained in [1]. It provides an opportunity for us to explore the world in real-time and without geometric limitations. The fourth-generation (4G) technology, based on Orthogonal Frequency-Division Multiplexing (OFDM) technology, utilizes multiple-antenna transmission for spatial multiplexing. It has the potential to reach 100 Mbps, a data transfer rate much higher than 3G.

The 4G communication system has already allowed us to enjoy our lives full of adventure without leaving our homes. Online virtual meetings have become an alternative to face-to-face conferences. Online courses provide students an excellent opportunity for seamless experience as in a physical lecture room. E-Commerce becomes more popular than physical retail stores, with many advantages such as low costs, no geographical limitations, and easy to locate a

product.

The significantly increased data transmissions impose pressure on the existing communication system. In the current communication scenario, mobile devices are serviced in the cellular network by base stations. The network traffic can be crowded when multiple users simultaneously connect to the same base station. In some particular locations where the user number is large, denser base stations are deployed, and the cell size is shrunk to avoid dense traffic. However, the same frequency resources are dynamically shared between the users, which vastly impacts the bandwidth per user when the user number increases, commonly happened in a stadium or a large shopping center where user density is high.

The increased network traffic demands the development of the 5G network. The 5G network employs a much higher frequency than the current 4G Long Term Evolution (LTE) standard, benefiting from millimeter-wave technology, an attractive technique to boost transmission rate. It is very suitable to be deployed in dense urban cities and areas where potentially a large crowd of people is gathered. The 5G network enables a significantly higher system capacity, allowing low latency. The 5G network introduces various opportunities, benefiting both the consumer market and the business field, creating a fully connected society.

Fig. 1.1 briefly demonstrates the future 5G radio scenario, in which a Base Station (BS) communicates with typical user devices. These devices include Internet of Things (IoT) devices, autonomous cars, robotics, high-resolution streaming, and many more. The yellow side lobes represent the beam-forming technique, which is a technique concentrating the transmission power to narrow directions, providing spatial filtering, and improving the transmission efficiency [2][3]. Conventionally, the BS communicates with each of the receiving devices in a separate time/frequency domain, which increases the occupation of frequency spectrum resources [4] [5]. The high-performance components in a BS consume a large amount of power to effectively distribute its transmission energy, mainly due to its internal ultra-linear high-performance power amplifier. Using beam-forming technology, the BS can communicate with multiple users at the same time/frequency domain and efficiently deliver the power to the receiving devices [6]. Thus, the total transmission power is decreased since the emitted Radio Frequency (RF) power is reduced [7].

A key enabler of 5G radio communication is the Massive Multiple-Input Multiple-Output (MIMO) technique, which has already attracted many research interests for years. By incorporating the Massive MIMO technique, the BS is equipped with several hundreds of antennas in a single device [8]. At the receiver end, the

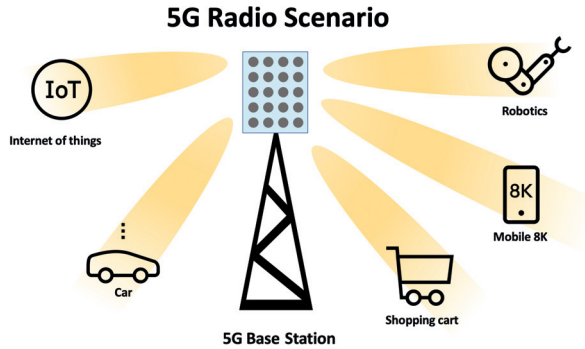

Figure 1.1: Conceptual illustration of 5G radio scenario.

analog signal is received by multiple antennas and passed through the RF chain. Instead of a single amplifier, hundreds of low-power, low-cost amplifiers work simultaneously to improve the BS transmission efficiency at the transmission side. For example, the world's first real-time Massive MIMO testbed (LuMaMi) has been presented at Lund University in Lund, Sweden, utilizing up to 100 base station antennas to serve up to 12 user equipment at the same time/frequency domain [9]. The antennas are small in size and low cost in hardware.

Fig. 1.2 shows a conceptual block diagram of a single receiver core in a high-performance BS. In the receiver chain, analog signals are firstly converted to digital signals using the Analog to Digital Converter (ADC). Then, the digital signals are processed by the Digital Signal Processor (DSP) for analyzing the transmitted information in real-time in the digital domain.

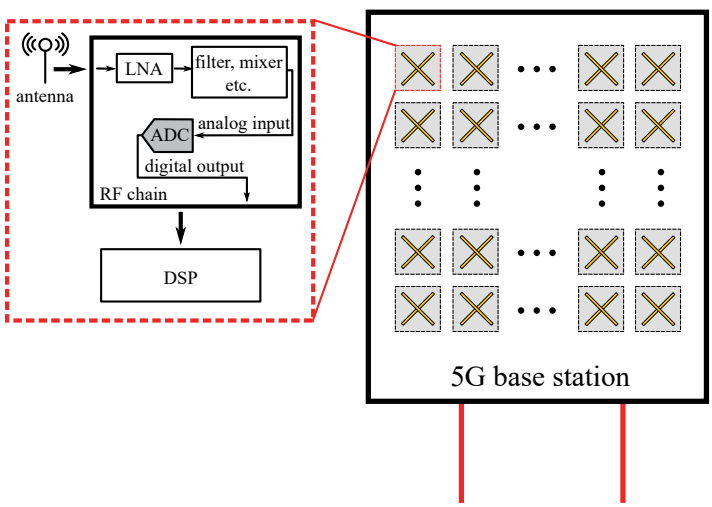

Figure 1.2: System-level block diagram of a single receiver core in 5G base station.

All in all, a wide variety of user devices in the future are possibly connected to the 5G network, benefiting from the system's wide signal bandwidth, high energy power efficiency, and broad signal coverage. All the above features require essential components: high-performance ADC cores. Their operations and circuit implementations are the main topics in this research work.

1.2 Analog to Digital Data Conversion

The ADCs are widely used in communications devices and almost all daily life appliances. They act as bridges between the analog and the digital domain, convert a real-world analog signal to an equivalent digital counterpart for further processing by the high-performance digital processors. In our lives, ADCs are very common: high-resolution ADC converts sounds picked up by the microphone into the digital signal for further processing; high-speed ADC converts light detected by a high-resolution digital camera sensor into digital pixels as an image storing in the memory card.

In communication devices, ADCs are vital. The ADCs should impose minimum noise to the system and accurately convert high-speed continuous varying analog signals to digital codes in almost real-time. The ADCs should be fast and efficient, without occupying too much power budget of the whole system.

1.2.1 Analog to Digital Data Conversion Principle

In this section, the analog to digital data conversion principle is overviewed. A fundamental principle that governs the design of mixed-mode systems is the Nyquist theorem [10]. It states that "an analog signal waveform may be uniquely and precisely reconstructed from samples taken of the waveform at equal time intervals, provided the sampling rate is equal to, or greater than, twice the highest significant frequency in the analog signal." The Nyquist theorem is a fundamental consideration in the ADC designs to determine how fast a signal to be sampled and correctly reconstructed.

There are two main data converter categories, the Nyquist-rate converter and the oversampled converter [11]. The signal bandwidth in Nyquist-rate converters is close to half of the sampling frequency. While in contrast, the oversampled converters have a signal bandwidth of a fraction of the sampling frequency, which is able to achieve a high resolution. However, this type of architecture usually involves sophisticated noise-shaping feedback loops.

A basic ADC block diagram is shown in Fig. 1.3, which consists of an Anti-Aliasing Filter (AAF), a Sample and Hold (S/H) circuit, and a quantizer.

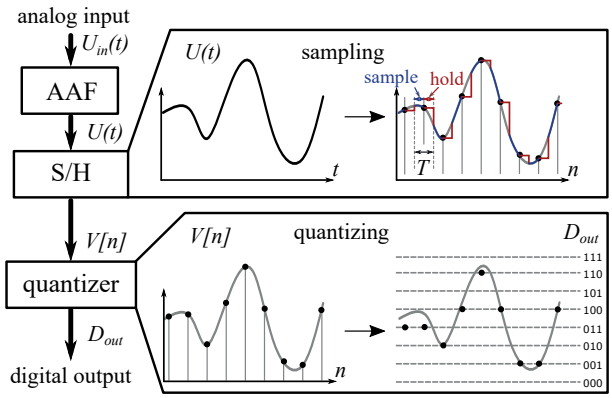

Figure 1.3: An analog to digital conversion example.

The AAF is located in front of the S/H circuit. It can be an analog low pass filter removing unwanted interference higher than Nyquist frequency so that they are no longer folded back into the signal bandwidth that deteriorates the original signal.

A continuously varying analog input $U(t)$ is sampled into an equivalent voltage in each discrete time step in the sampling process. The sampled voltage is held for a duration usually equal to half of the sampling signal period T. The sampled analog voltage $V[n]$ is updated in the interval of T, which is:

$$V[n] = U(t) \cdot \delta(t - n \cdot T) \tag{1.1}$$

where the delta function $\delta(t)$ is the unit impulse.

In the quantizing process, the sampled signal $V[n]$ is quantized to a corresponding digital code D_{out} by a quantizer. This step rounds the analog input voltage into discrete voltage steps, introducing quantization errors due to the finite digital word length. The finer the quantization step, the lower the quantization error.

1.3 ADC Specifications

The ADC specifications are essential considerations before the actual design phase. A set of specifications describe the ADC performance, for example, input bandwidth, ADC resolution, power consumption, and ADC noise [12].

The ADC performance survey in [13], analyzed by Prof. Boris Murmann, summarizes the state-of-the-art ADC designs from 1997 to 2020 from ISSCC and VLSI Symposium. Both the Schreier Figure of Merit (FOM_s) and the Walden Figure of Merit (FOM_w) are important performance metrics in benchmarking the ADC performance. The FOM_w relates the ADC power to its performance and sampling rate [14], is:

$$FOM_w = \frac{P}{2 \cdot f_b \cdot 2^{ENOB}} [\frac{Joule}{Conversion - Step}] \tag{1.2}$$

where P is the ADC power consumption, and f_b is signal bandwidth. The Effective Number of Bits (ENOB), representing the effective accuracy in the ADC [15], is :

$$ENOB = \frac{SNDR–1.76}{6.02} \tag{1.3}$$

where the Signal to Noise and Distortion Ratio (SNDR) represents the performance of the ADC, which will be explained in Section 1.3.2.

The FOM_s is:

$$FOM_s = SNDR + 10log_{10}(\frac{f_b}{P})[dB] \tag{1.4}$$

From the above equations, we could metric the ADC performance by evaluating the three key variables: f_b, ENOB, and P, which will be explained next.

1.3.1 ADC Input Bandwidth

In the communication systems, the input signal bandwidth (f_b) could be in the GHz range, requiring the high-performance ADCs that are capable of handling a large f_b [16] [17] [18]. The multi-GHz sampling frequency is thus a must for correctly sampling the high-speed input signal without losing information.

As already mentioned, before being converted to the digital domain, the analog input signal passes through an AAF to limit its maximum signal frequency component to Nyquist frequency. It avoids any aliasing issue that high-frequency signals folded back to f_b that contaminates the original signal. For a Nyquist-rate ADC, the relation between the f_b and the sampling frequency (f_s) is graphically illustrated in Fig. 1.4 (a). It can be directly seen that the sampled input signal spectrum is replicated at the multiple of f_s, which has to be at least twice the f_b to satisfy the Nyquist theorem.

In an oversampled ADC, the requirement of an AAF design is more relaxed than in the Nyquist-rate ADC. The spectrum in Fig. 1.4 (b) shows that the f_b

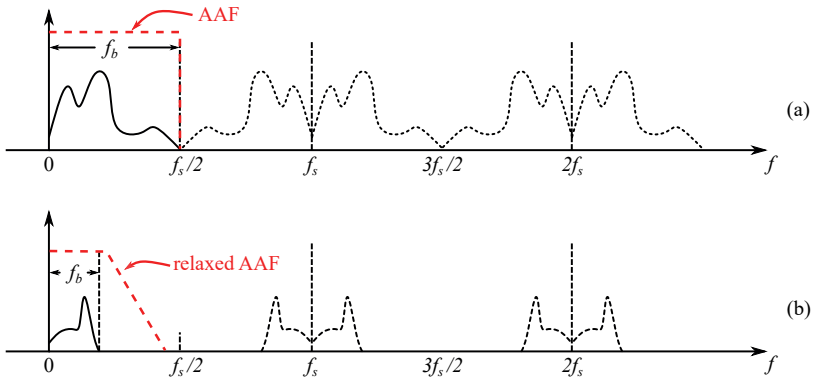

Figure 1.4: Graphical illustration of the input signal bandwidth versus the ADC sampling frequency in the frequency domain, of (a) Nyquist-rate ADC and (b) oversampled ADC.

is only a fraction of the Nyquist frequency ($f_s/2$). From another point of view, to achieve an equivalent f_b to the Nyquist-rate ADC, the oversampled ADC requires much higher f_s.

1.3.2 ADC Resolution

The primary consideration in designing an ADC is choosing an appropriate ADC resolution depending on the application. The higher the resolution, the finer the quantization steps become, usually results in a higher ADC power consumption and a larger chip area. Signal to Noise Ratio (SNR) is an important criterion to evaluate the ADC performance, which is the ratio of the signal power (P_{sig}) to the noise power (P_{noise}). When a full-scale sine wave input is applied to an N-bit ADC, and only the quantization noise is taken into account, the SNR [or Signal to Quantization Noise Ratio (SQNR)] becomes [12]:

$$SNR = SQNR = 6.02 \cdot N + 1.76\,[dB] \tag{1.5}$$

and including all the circuit noise and any possible distortions (P_{dist}), the SNDR is:

$$SNDR = \frac{P_{sig}}{P_{noise} + P_{dist}}\,[dB] \tag{1.6}$$

1.3.3 ADC Power Consumption

There is always a trade-off between ADC performance and ADC power consumption. For devices used in BSs, slightly larger power consumption may not be the main problem since the BS is powered from the grid. However, regarding

the battery-powered handheld devices, they are more favorable to utilize low power components.

Technology advance in the semiconductor field followed quite well with Moore's law, which predicted that the number of transistors in a dense Integrated Circuit (IC) doubles about every two years [19]. Thanks to Complementary Metal-Oxide-Semiconductor (CMOS) technology developments, the transistor has a smaller feature size. It benefits in a vast improvement to the circuit speed and a tremendous decrease in power consumption than the older technologies.

In recent years, 28 nm and 22 nm Fully Depleted Silicon On Insulator (FD-SOI) CMOS technologies reveal good potentials in the high-performance designs. In the future, the transistor size is predicted to be even smaller. The ADC designs in this research work have been implemented in 65 nm CMOS and in 28 nm and 22 nm FD-SOI CMOS, trying to reach high performance and low power at the same time. Besides, these designs utilize power-efficient architectures, trying to further decrease the total ADC power consumption.

1.3.4 ADC Noise

In a real circuit, noise degrades the ADC performance, causes a deviation to the expected ADC resolution. There are two main types of ADC noise. The first type is the quantization noise, which is generated during the quantization process. The second type is the thermal noise related to component value, temperature, and bandwidth.

The quantization errors represent the differences between the sampled analog input and its converted digital output, which appears to be non-linear and signal-dependent noise. These errors are generated during the quantization process, in which the sampled version of analog input is quantized and converted to a series of digital codes with a finite resolution. The quantization errors, referred to as quantization noise, are usually modeled as uniform noise [20].

The amount of the quantization noise is directly related to the chosen ADC resolution. Theoretically, in an N-bit ADC with the number of quantization levels equal to 2^N, the Δ represents the minimum quantization step, is:

$$\Delta = \frac{V_{FS}}{2^N} \tag{1.7}$$

where V_{FS} is the full-scale voltage of the input signal. A high-resolution ADC with a large N results in a smaller quantization step Δ. Assuming an input signal

has an amplitude much larger than Δ, and the quantization noise follows uniform distribution from $-\Delta/2$ to $\Delta/2$, the quantization noise power P_Q becomes [12]:

$$P_Q = \frac{\Delta^2}{12} \tag{1.8}$$

Obviously, P_Q decreases four times when the Δ is reduced by two for every 1-bit increase in the ADC resolution.

Besides the quantization noise limiting the theoretical limit of ADC resolution, the thermal noise is another critical design consideration in actual component-level implementation. Thermal noise in a circuit is mainly generated from the random thermal motion of charge carriers in electrical components. The component value affects the thermal noise, such as the mean square voltage variance per hertz of bandwidth ($\bar{v_n^2}$) of a resistor is proportional to the resistance R:

$$\bar{v_n^2} = 4k_B \cdot T \cdot R \tag{1.9}$$

where k_B is Boltzmann constant, and T is the temperature. When an input is sampled on the capacitor through a non-ideal switch in the sample and hold system, the sampling noise is directly related to the sampling capacitance C_s. The $\bar{v}_n^2$ is [21]:

$$\bar{v_n^2} = \frac{k_B \cdot T}{C_s} \tag{1.10}$$

Thus a sufficiently large C_s is necessary for low noise, especially in high-resolution ADCs.

There is a balance between the quantization noise and the thermal noise, such that too much thermal noise causes the resulting ADC resolution much lower than expected, while in the other case, the ADC efficiency is reduced. In a practical design, the thermal noise in an ADC could be selected comparable to the quantization noise, which may cause a slight degradation in SNDR but benefit in a reduced chip area occupation and power consumption.

1.4 Overview of Nyquist-Rate ADCs

Nyquist-rate ADCs are attractive due to their fast speed and straightforward architectures. Some of the popular Nyquist-rate ADC architectures such as Flash ADC, Successive Approximation Register (SAR) ADC, and Pipeline ADC, are shown in Fig. 1.5. These ADCs are sampled at a sampling frequency f_s twice the input signal bandwidth to satisfy the Nyquist theorem.

The Nyquist-rate data converters usually have a deterministic digital output corresponding to each of the sampled analog inputs or the so-called one-to-one correspondence between an analog input signal and its digitized output. This category of data converters usually does not require a sophisticated digital post-processing circuit, such as a decimation filter commonly used in oversampled ADCs that will be explained in the next section.

The Flash ADC architecture, illustrated in Fig. 1.5 (a), is a fast technique that converts the analog input signal to a digital output. The Flash ADC usually complete conversions within one clock cycle, which is a candidate architecture in building a widely used quantizer in this research work.

Despite its speed benefits, Flash ADC's parallel conversions cause the circuit complexity to grow exponentially with increased resolution. Thus, achieving a high-resolution Flash ADC is difficult. Generally, to resolve N bits, $2^N - 1$ reference voltages and a similar number of comparators are required [12]. The comparator outputs are thermometer code, which is hard to be directly used except decoded to binary code first. An additional thermometer to binary code decoder is required, inevitably consumes power, and occupies the chip area.

The SAR ADC is exceedingly power-efficient. It trades time for resolution, whose architecture is shown in Fig. 1.5 (b). In a typical SAR ADC, the N-bit ADC resolution requires at least N+1 clock cycles to be resolved. Internally, a single comparator is used N times to compare the voltage presented at the comparator's input with a reference voltage. The comparator's input voltage varies from bit to bit, which is the voltage presented on an internal capacitor array achieved by charge redistribution.

However, the SAR ADC suffers from limited resolution due to matching between the capacitors in the physical layout and imperfections introduced by parasitic capacitance in the capacitor array in Capacitive Digital to Analog Converter (CDAC). The non-idealities can be minimized by careful layout and further estimated and calibrated by digital circuits.

The third attractive ADC architecture is pipeline ADC, which converts the bits sequentially. Unlike the SAR ADCs that takes several clock cycles to convert each sample, the pipeline ADC only introduces latency between the digital output and the analog input signal. A typical pipeline ADC consists of several cascaded stages, as shown in Fig. 1.5 (c). A digital logic combines all the stage outputs to form the final digital output. For example, in stage i, digital bit b_i is resolved by a fast ADC (usually a Flash ADC), then converted back to the analog domain by a Digital to Analog Converter (DAC) and subtracted from the input. The residue voltage is amplified by a Residue Amplifier (RA), and

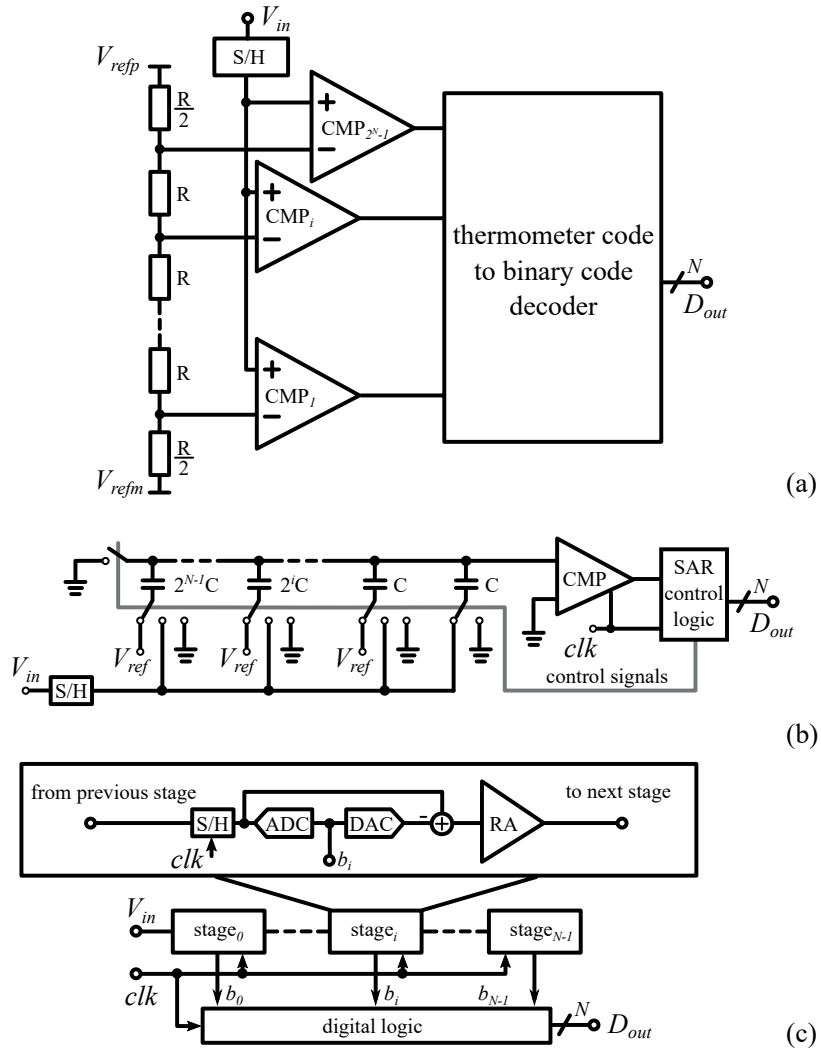

Figure 1.5: The Nyquist-rate ADC architectures, including (a) Flash ADC, (b) SAR ADC, and (c) Pipeline ADC.

propagates to the next stage.

The limitation of a pipeline ADC is its RA, which usually has a critical accuracy requirement. These amplifiers are sensitive to process variations that cause non-linearities in gain and offset and consume modest levels of power dissipation that could exceed the system's power budget.

1.5 Overview of Oversampled ADCs

Another ADC category is the oversampled data converter, which includes the popular $\Delta\Sigma$ ADC that employing the principle of $\Delta\Sigma$ Modulator (DSM). Compared to the Nyquist-rate ADCs, as the name implies, a noticeable difference is that the oversampled ADC is sampled at a much higher f_s for a similar f_b. These architectures typically reach a high performance using moderate-resolution analog components, reducing in-band noise due to oversampling and noise shaping techniques.

A simplified $\Delta\Sigma$ ADC linear model is shown in Fig. 1.6. The subtraction residue (Δ) of the input signal $U(t)$ and the feedback DAC output is fed to a chain of integrators (whose transfer function is L) for quantization noise shaping (Σ). In its linear model, a quantizer converts the Loop Filter (LF) output $Y(t)$ to the digital output $V[n]$, with a quantization noise $E(t)$ added in the model.

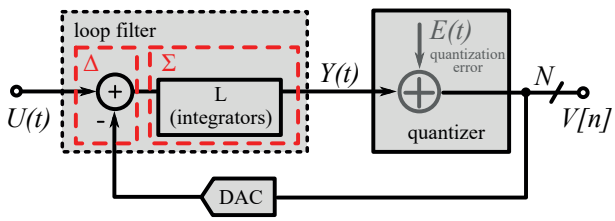

Figure 1.6: The $\Delta\Sigma$ ADC architecture.

The ADC transfer function in z-domain [11] is:

$$V(z) = Y(z) + E(z) = STF \cdot U(z) + NTF \cdot E(z) \tag{1.11}$$

where the Noise Transfer Function (NTF) applies to the quantization noise and the Signal Transfer Function (STF) applies to the signal, are:

$$NTF(z) = \frac{1}{1 + L(z)} \tag{1.12}$$

$$STF(z) = \frac{L(z)}{1 + L(z)} \tag{1.13}$$

Eq. 1.11, Eq. 1.12 and Eq. 1.13 indicate that the NTF is an inverse function of the LF's transfer function $L(z)$. By selecting a low-pass filter in the LF, such as a chain of integrators, the NTF is a high-pass filter that filters $E(t)$. When the open-loop gain of $L(z)$ is large, the STF is flat. Note that the STF can be

unity when an additional feed-forward path bypassing the loop filter, from U to Y, is implemented.

The combination of the NTF and the STF determines the transfer function of the DSM. The desired transfer function is realized by selecting an appropriate architecture based on component-level considerations such as power consumption and chip area requirement.

Fig. 1.7 shows an examplar simulated ADC output spectrum of a 4^{th} order DSM sampled at 5 GHz, achieves 250 MHz input signal bandwidth. The SNR is 80 dB, and noise shaping behavior is clearly visible. Note that a notch is presented at approximately 200 MHz, which is achieved by optimizing zeros in the NTF for the maximum ADC resolution.

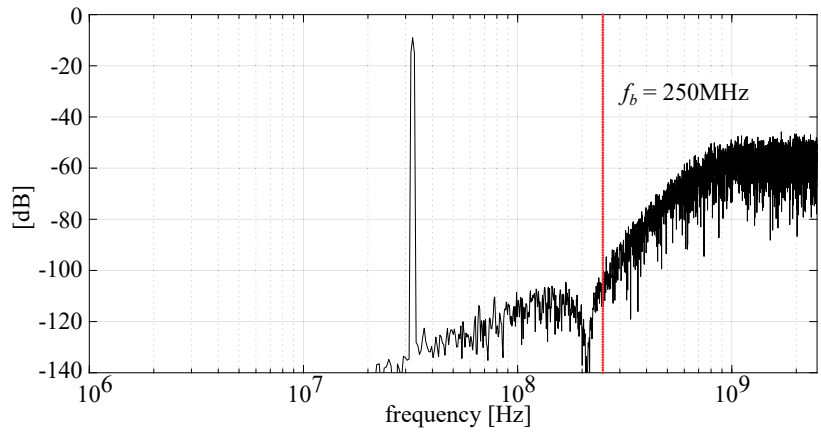

Figure 1.7: A examplar simulated ADC output spectrum with 250 MHz signal bandwidth and sampled at 5 GHz.

At the ADC output, the bitstream is produced at the sampling rate, which contains high-frequency noise. These high-frequency noises should be filtered by a digital decimation filter to filter the out-of-band high-frequency noise and down-sample the digital output data to Nyquist-rate [22].

1.6 Relate to State-of-the-Art ADC Designs

The state-of-the-art ADC designs are briefly discussed and compared. In the research area, there are two main tracks of ADC designs, namely high-speed designs and ultra low power designs. This research work mostly focuses on ADCs that will be implemented in future high-performance base stations thus it is more favorable to high-speed ADC designs.

Considering the Nyquist-rate ADCs, Time-Interleaved (TI) architecture is an attractive technique that parallels multiple identical ADC cores at a much higher sampling frequency than an individual one. Thanks to the CMOS technology node advance which provides high-speed transistors, multi-GHz sampling frequency becomes possible, resulting in a signal bandwidth above 1 GHz.

In ISSCC 2018, Kull et al. presented a high-speed TI ADC implemented in 14 nm CMOS Fin Field-Effect Transistor (FinFET) technology [23]. The ADC was sampled at 72 GS/s and optimized for best SNDR at the Nyquist frequency of up to 36 GHz. The proposed ADC achieved 39.3 dB at low input frequencies and 30.4 dB at Nyquist frequency. In ISSCC 2019, Pisati et al. presented a complete transceiver design implemented in TSMC 7 nm FinFET CMOS [24]. The design incorporates a 7-bit 40-way time-interleaved ADC, divided into eight front-end track and hold circuits running at 3.75 GS/s. Each consists of five 750 MS/s non-binary charge-redistribution DAC-based asynchronous SAR ADCs. The overall power consumption of the complete design is 244 mW. Both ADC designs show that TI architecture is a viable solution for achieving a large input signal bandwidth, which is also the selected technique used in SAR ADC designs presented in this dissertation.

The oversampled ADCs already achieved a signal bandwidth exceeding 100 MHz. A $\Delta\Sigma$ ADC sampled at 4 GHz that achieves 125 MHz signal bandwidth was presented by Bolatkale et al. in ISSCC 2011 [25], and later published in JSSC [26]. A 3^{rd} order ADC was implemented in 45 nm CMOS, consumed 256 mW energy from dual-supply voltages 1.1 V, and 1.8 V and achieved 70 dB dynamic range (DR). This work shows a good reference to my ADC design: a high-speed $\Delta\Sigma$ ADC tries to push circuit limits for achieving a much higher signal bandwidth using an advanced technology node.

Besides the SAR ADCs and $\Delta\Sigma$ ADCs, pipeline ADCs are attractive in recent years. It is also possible to interleave multiple Pipeline ADCs. Devarajan et al. presented a 12-bit interleaved Pipeline ADC in ISSCC 2017 [27], which is capable of being sampled at 10 GS/s, achieved an SNDR of 55 dB and an Spurious-Free Dynamic Range (SFDR) of 64 dB with a 4 GHz input signal. The design was implemented in 28 nm CMOS, dissipating 2.9 W power.

Even smartly, SAR ADCs and Pipeline ADCs can be integrated into a so-called pipelined-SAR hybrid ADC. Ramkaj et al. presented a TI ADC with eight 625 MS/s channels, at a sampling rate of 5 GS/s [18]. Inside each ADC channel, three dynamic SAR stages with 4-4-6 bits per stage are pipelined. The prototype ADC, fabricated in 28 nm bulk CMOS, achieved an SNDR of 61.3 dB at 600 MHz and 58.5 dB at 2.4 GHz and consumed 158.6 mW energy. The pipeline ADCs

show promising results, which will be chosen as a candidate architecture for future designs.

In the industry, high-performance chips for high-performance applications have been released. In 2019, the industry's widest bandwidth, fastest sampling rate, and lowest power consumption ADC was introduced by Texas Instruments (www.ti.com): a 12-bit ADC *ADC12DJ5200RF*, which is a dual- and single-channel ultra-high-speed ADC, capable to run at a sampling frequency up to 5.2 GHz, suitable for devices such as oscilloscopes, wide-band digitizers, and communications testers. The specifications of this chip are very attractive, which sets a target for future ADC designs in research.

1.7 Summaries of Experimented ADCs

In this research work, a high-speed Nyquist-rate Asynchronous SAR (ASAR) ADC has been designed. A self-generated internal clock triggers its internal comparator sequentially. Comparing with a similar Synchronous SAR (SSAR) ADC, which was previously designed by Ericsson Research, the asynchronous version shows a graceful SNDR degradation at the increased sampling frequency, with a small penalty in design complexity. The SSAR ADC was measured, with their non-idealities in the capacitor bank estimated using the post-processor in MATLAB (www.mathworks.com) and calibrated.

The oversampled ADC's behavior and performance are evaluated by designing and implementing a high-speed $\Delta\Sigma$ ADC in 28 nm FD-SOI CMOS. This design targets the application in high-performance 5G base stations. The sampling frequency is in the GHz range with a low Oversampling Ratio (OSR) and aggressive noise shaping. Inverter-based integrators are used to boost the ADC speed, and Current Mode Logic (CML) digital cells are used to improve the speed of the digital feedback loop, with a trade-off in higher power consumption than a conventional digital circuit design using CMOS digital cells.

The last presented ADC design is a $\Delta\Sigma$ ADC implemented in 65 nm CMOS, which integrates a digital calibration core. This design aims to examine the possibility of using an on-chip calibration core to perform background calibration to linearize the outer-most DAC in the feedback loop.

Chapter 2

SAR ADC

2.1 Introduction

The rapid growth of the transmission rate in the communication systems requires advanced high-performance hand-held mobile devices. High-speed, medium-to-high resolution, and power-efficient ADCs are essential. The A/D converters accurately convert the fast varying analog signal presented at their input to a digital counterpart, achieving a high resolution and a low power dissipation at the same time.

SAR ADC is an attractive architecture in recent years according to [13], which is very suitable for various modern wired and wireless communication applications. The SAR ADCs incorporate power-efficient and digital-friendly architecture. The term *digital-friendly* means that the ADC is partially built with many digital blocks and scales well into deep-submicrometer CMOS technology nodes.

The first commercial data converter, the vacuum-tube based "DATRAC" in 1954, uses shift-programmable successive approximation architecture, achieves an 11-bit resolution in 50KS/s, and consumes a power of 500 W [28]. Nowadays, state-of-the-art SAR ADCs accomplish a 13-bit resolution in 40 MS/s while only consuming a power less than 1 mW [29]. It is a significant leap in almost a half-century.

The SAR ADC is categorized in the type of Nyquist-rate ADC. Comparing with other Nyquist-rate ADCs, the SAR ADC shows significant benefits in terms of power-efficiency, minimized design complexity, low chip area occupation, and high-speed operation.

Comparing with a Flash ADC, the SAR ADC consumes significantly lower power. In the Flash ADC architecture, N-bit resolution typically requires 2^N-1 comparators for a full parallel comparison with the entire quantization levels in one clock cycle. It means that the number of highly accurate comparators will be doubled at each increased bit. On the contrary, in the SAR ADC, the increased resolution only requires an increased number of accurate and well-matched components, e.g., twice the number of capacitors for an extra bit. Even including the additional switches necessary to control those added capacitors, the whole design complexity does not increase exponentially.

Comparing with the Pipeline ADC, the SAR ADC does not show large latency as the Pipeline ADC usually does. Latency means a time delay between the sampled voltage and its corresponding digital output value. It is the nature of a Pipeline architecture since it has inherent parallelism to utilize each stage simultaneously. Furthermore, the SAR ADC does not require the high-performance inter-stage amplifiers as needed in the Pipeline ADCs. The high linearity and low noise amplifiers between the stages contribute to increased power consumption and increased circuit complexity, limiting the maximum circuit speed.

In short, the SAR ADC divides the bit conversions into several conversion stages by using a single comparator approximately N times for N-bit resolution.

This chapter focuses on the theory and the circuit implementations of two practical SAR ADC designs: an SSAR ADC and an ASAR ADC. Their architectures are explained, and the differences in clocking schemes are shown. In Section 2.2, a basic SAR ADC architecture is shown, and the Successive Approximation (SA) algorithm is briefly explained. Section 2.3 shows a TI SAR ADC architecture, which has great potential in increasing the ADC signal bandwidth. Then, Section 2.4 discusses the synchronous and asynchronous clocking scheme. Section 2.5 explains the component-level implementations of the ASAR ADC designs, with the comparator, CDAC, and SAR control logic explained in detail. Lastly, in Section 2.6, the SAR ADC non-idealities, introduced by Process-Voltage-Temperature (PVT) variations, will be addressed. Techniques to improve the SAR ADC robustness are presented, including redundancy technique, CDAC array imbalance estimation and calibration, ASAR ADC internal clock pulse width tuning, and a proposed design method to reduce SSAR ADC random noise when incorrect bit conversions occur.

2.2 SAR ADC Architecture

The SAR operation, as the name implies, converts the analog input signal to an equivalent digital output based on the SA algorithm. The SA algorithm is an implementation of binary searching, realizing N-bit resolution by N comparisons. Many of the SAR ADCs nowadays incorporate the operation principle similar to the charge redistribution technique described in [30], using a binary-weighted capacitor array to perform high-speed conversion.

The SSAR and ASAR ADC architectures share numerous similar internal components but differ in the control logic design. Fig. 2.1 shows a conceptual 6-bit SAR ADC architecture using a synchronous clocking scheme. In this particular SAR ADC architecture, four main components are shown: a S/H circuit, a CDAC, a comparator (CMP), and a SAR control logic. An external clock *clk* controls the comparator and the SAR control logic. The comparator makes comparisons at the *clk* falling edge, and the SAR control logic sequentially generates digital outputs b_5 to b_0 at the *clk* rising edge.

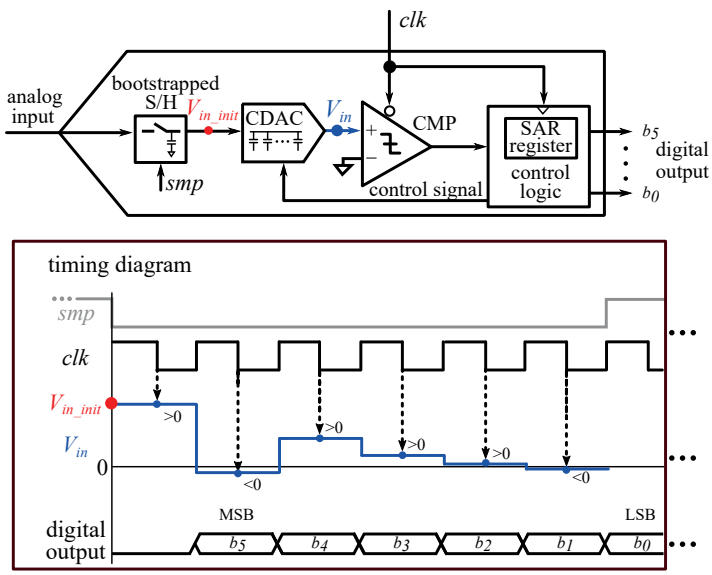

Figure 2.1: A 6-bit SAR ADC conversion example, with the timing diagram illustration of the ADC input and output signals.

To facilitate understanding the SA algorithm, the timing diagram of external clock signal *clk*, sampling signal *smp*, comparator input voltage (also the CDAC output voltage) V_{in}, and six digital output bits b_5 to b_0 are shown in the bottom part of Fig. 2.1. The algorithm finds a unique digital code representing the

sampled input voltage V_{in_init}, marked in the red dot in the timing diagram. In the sampling mode, the analog input voltage is sampled on the binary-weighted capacitors in the CDAC. In the hold mode, the sampling signal *smp* is released, and the $V_{in} = V_{in\_init}$ is proportional to the sampled input voltage. Next, bit conversions start.

At a first *clk* falling edge, V_{in} is compared with a reference voltage (0 in this example). When $V_{in} > 0$, the comparator output is a logic one, and vise versa. Next, the comparator output is latched by the SAR register at the *clk* rising edge, which determines the Most Significant Bit (MSB) (b_5) in the digital output. In the meantime, the control logic sets a set of control signals based on the comparison result to redistribute the charge in the CDAC, causing the V_{in} increases or decreases to a new value accordingly, in a step half of the previous step. The same procedure continues until the Least Significant Bit (LSB) conversion is completed. The bits determined during each conversion step are combined as the ADC digital output.

The S/H, placed at the front of the ADC, samples the analog input voltage to generate a series of sampled voltage (V_{in_init}). The linearity of the S/H block is essential since any non-linearity introduced by the S/H directly propagates to the ADC output. Typically, the S/H component-level design is based on the bootstrapped architecture, an architecture initially proposed in [31]. The bootstrap technique allows a constant voltage applied to the sampling transistor's gate-to-source terminals, allowing a low and constant conducting resistance independent of the input signal voltage. Therefore, the sampling switch introduces minimum distortion to maintain the overall SAR ADC linearity.

The CDAC follows the S/H, constructed by an internal capacitor array of capacitors with binary-weighted capacitance. The controlling scheme and charge redistribution details will be explained in Section 2.5.1.

The comparator is a crucial component in a SAR ADC. Noise, offset, and comparison speed of the selected comparator design dominant the SAR ADC performance, thus requires a trade-off between its performance and power consumption.

Lastly, the SAR control logic latches the comparator outputs. Its primary function is to generate a series of control signals for the switches in the CDAC in each clock cycle, connecting the corresponding capacitor to one of the reference voltages to redistribute charge stored on the capacitors. In the meantime, the comparison results are saved in the registers in the SAR control logic, becoming the SAR ADC digital output.

2.3 TI SAR ADC Architecture

The high-speed, high-resolution ADCs commonly incorporate TI architecture. It is a practical method that interleaves multiple SAR ADCs for increased performance, satisfying a broad signal bandwidth requirement and a fast sampling rate. In the TI ADC architecture, each of the single SAR ADC is called a sub-ADC core. The sub-ADC core specification is chosen such that an optimum point is reached between the total ADC power consumption versus the sampling rate.

Fig. 2.2 shows a 7-channel TI SAR ADC architecture. A timing diagram is explicitly shown at the lower-left corner to illustrate the sampling signal timing differences between the common S/H and the sub-ADC cores. The common S/H is clocked by a sampling signal *smp*, which samples the buffered analog input signal to be V_{smp}, then distributes to all the sub-ADC cores. The sub-samplers in the sub-ADCs are clocked in turn, sample the V_{smp} to be V_{in_init} by non-overlapped sampling signals smp_0 to smp_6, each with a pulse width equal to one *smp* period. Thus, at a time, only one of the sub-ADCs is in the sampling state while the rest are in bit conversions. The seven sub-ADC core outputs are sequentially selected by a digital multiplexer. The TI-ADC digital output is generated at a rate of f_s for further signal processing in the digital domain.

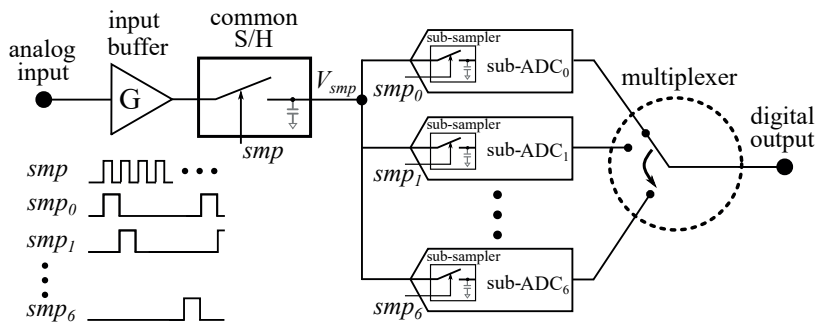

Figure 2.2: Time-Interleaved ADC architecture, with sampling signals timing diagram shown at the lower-left corner.

There could be a trade-off in selecting the sub-ADC core bandwidth and the number of sub-ADC cores. In many of the TI ADC designs, the single sub-ADC core has a minimum 10-bit resolution and a sampling frequency of 200–300 MS/s. For example, in [32], a 10-bit non-interleaving SAR ADC design is presented, which achieves an SNDR at Nyquist frequency of 57.7 dB at 160 MS/s and 57.1 dB at 320 MS/s.

Interleaving a small number of high-performance sub-ADCs becomes a sensible choice in wide-bandwidth designs. The total number of sub-ADC cores is re-

duced, but each sub-ADC core's sampling rate is increased. It is beneficial in terms of matching between sub-ADC cores and a simplified calibration module. The work in [33] presents a high-speed single SAR ADC running at a sampling rate of 1.25 GS/s, which still maintains an SNDR of 36.4 dB up to 5 GHz input frequency, allowing smooth integration into a future interleaved system. However, a single ADC core only achieves a resolution of 7-bit, it is not very suitable for a TI-ADC requiring a higher resolution. The TI SAR ADC could also have a large number of sub-ADCs interleaved for an even higher sampling rate. For example, in [34], a 16-channel TI SAR ADC has been presented with a 10-bit resolution and a sampling rate of 2.6 GS/s, which achieves an SNDR of 50.6 dB at Nyquist frequency; in [35], a 12-bit 8-way time-interleaved SAR ADC has been designed, achieving an SNDR above 65.3 dB at 1 GHz input frequency under a sampling rate of 1.6 GS/s.

2.4 SAR ADC Clocking Schemes

One of the key differences between the two types of SAR ADCs is their clocking schemes. Specifically, the term *synchronous* or *asynchronous* is used to describe whether or not the SAR ADC internal blocks are synchronized to an external clock. If the SAR ADC internal states are updated synchronously with the clock cycles, it is an SSAR ADC. On the other hand, if the internal states are changed depending on the status of the internal comparator decision and an internal clock generated upon the completion of the previous comparison, it is an ASAR ADC.

Both architectures have benefits and drawbacks, with trade-offs among the performance, power consumption, and design complexities. In the following Sections, the SSAR ADC is described first, followed by the detailed explanations of ASAR ADC.

2.4.1 Synchronous SAR ADC Clocking Scheme

The SSAR ADC is clocked by a high-speed external clock signal *clk* possibly running at the GHz frequency range. Such a high-speed clock is distributed to all the internal blocks, provides synchronization of the internal blocks. Thus, digital-friendly SAR control logic can be designed, attracting interests both in commercial applications and research [23].

However, a potential risk for the SSAR ADC is an insufficient decision time

for the comparator to complete a comparison. If the clock is fast and an error appears on deciding a high-weight bit, the resulting performance may degrade abruptly. Thus, the external clock frequency has to be slow enough to fulfill the worst-case scenario, which significantly limits the maximum speed of the SSAR ADC.

Fig. 2.3 shows a simplified SSAR ADC architecture. The illustration is single-ended, but the real implementation has a differential architecture. The timing diagram of the sampling signal *smp*, the digital output b_{N-1} to b_0, and the external clock *clk*, are shown. It can be seen from Fig. 2.3, that at least $N+1$ clock cycles are required for a complete N-bit conversion, where one clock cycle is used for sampling, and the rest N clock cycles are occupied for bit conversions. Note that there is one clock cycle latency due to the comparator output been latched by the SAR register at the upcoming clock rising edge.

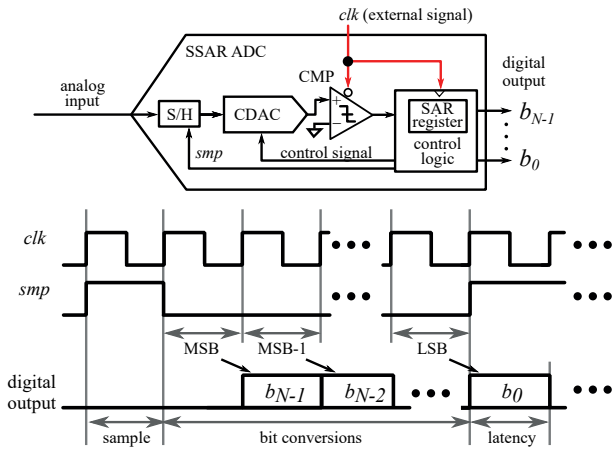

Figure 2.3: N-bit SSAR ADC architecture and critical nodes timing diagram.

The SSAR benefits from a structural digital-cell-based SAR control logic design but also has a few drawbacks.

- The SSAR ADC could consume high power and require a complicated layout to distribute a high-speed external clock (*clk*). At an increased ADC resolution, multiple clock cycles are needed to complete a single sample conversion. The *clk* frequency could be up to a few GHz, while the sampling frequency f_s is only in a few hundred MHz range. It shows that buffering such a high-frequency clock signal requires a large amount of power to be dispensed, which is higher than only buffering f_s in an ASAR ADC counterpart. Besides, such a high-speed external clock signal

distribution in the chip layout requires design experiences. Any clock delay between the comparator and the control logic may affect the circuit functionality, which must be well controlled. Thus, a general rule is to draw the layout routes as short as possible and match the critical clock routes length.

- The SSAR suffers an inefficient clock cycle utilization. Since the external clock signal to the SSAR ADC has a fixed clock cycle, it becomes less efficient in clocking the ADC since the comparator decision time is input voltage dependent. Previous works pointed out that the comparator decision time versus comparator input voltage follows a logarithm function as described in [36]. The maximum *clk* frequency has to satisfy the worst-case scenario, i.e., a very long comparator decision time when the comparator experiences a minimum input voltage. Thus, the maximum SSAR ADC sampling frequency is limited since it is usually proportional to the external clock frequency.

2.4.2 Asynchronous SAR ADC Clocking Scheme

Alternatively, to utilize the clocking more efficiently, a similar ASAR ADC is designed. The scenario becomes different when an asynchronous clocking scheme is used. The ASAR ADC architecture, shown in Fig. 2.4, is similar to the SSAR ADC architecture in Fig. 2.3, but differs in clocking scheme. A low duty cycle external sampling signal *smp*, with a frequency of a few hundred MHz, controls the start time of each sample conversion. Internally in the ASAR ADC, the bit conversions are converted by the quantizer clocked by a self-generated high-speed clock *cmp_clk* from the ASAR control logic. The ASAR ADC robustness is significantly improved compared to the SSAR ADC since the dynamic clock guarantees each bit conversion finished before the start of the subsequent bit conversion. Any bit conversion error caused by insufficient timing will only appear to the low-weighted bits in a sample that causes marginal performance degradation. Furthermore, it avoids the necessity of directly injecting a high-speed external clock into the ADC, which saves power and avoids any potential timing issues.

In summary, the ASAR ADC only requires an external low frequency sampling signal clocking the ADC, which consumes less power in buffering it, therefore, showing a better power efficiency. It is a preferable choice as a high-performance sub-ADC core to be further used in a time-interleaved way.

The benefits of selecting an ASAR ADC over an SSAR ADC counterpart are

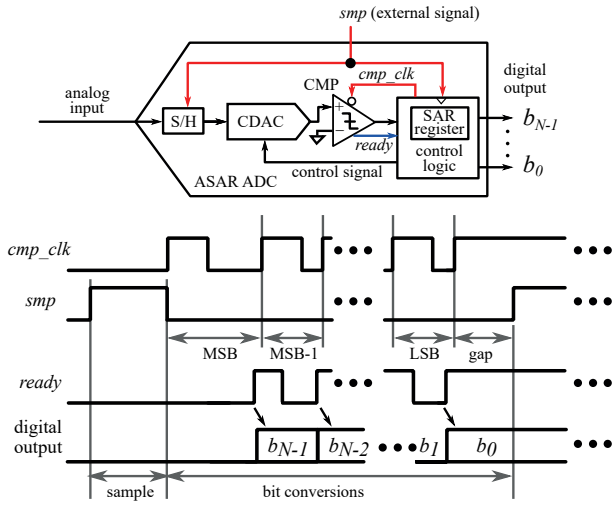

Figure 2.4: N-bit ASAR ADC architecture and critical nodes timing diagram.

two-fold:

- Buffering and distributing the external high-speed clock signal as in the SSAR is alleviated. Instead, a much slower sampling signal *smp* is distributed to both the S/H block and the ASAR ADC control logic. Distributing and buffing the *smp* to the ASAR ADC consumes much less power than the high-frequency *clk* to the SSAR ADC. In the meantime, reduce the layout complexity as well as the chip size.
- The ASAR ADC is generally faster than the SSAR ADC. The prior work [36] claims that the asynchronous conversion takes advantage of the faster comparison cycles since there is only one critical bit conversion with a worst-case comparator decision time. It proves mathematically that the total conversion time in the ASAR ADC is shorter than the SSAR ADC counterpart. The difference becomes more pronounced when the ADC resolution is high, which means more bits need to be converted.

Above all, the ASAR ADC dynamically utilizes the bit conversion time slot as the timing diagram example illustrated in Fig. 2.4. Because the comparator decision time depends on its input voltage, the clock pulse widths can be dynamically adjusted in the ASAR ADC to match the conversion time of each bit for maximum efficiency. Therefore, an important task is to understand the comparator behavior. The comparator will be studied in Section 2.5.3 where the input voltage versus the comparator decision time is studied in detail supported

by the results from component-level simulations. In the next section, the timing differences between the two architectures are analyzed first.

2.4.3 SSAR and ASAR ADC Timing Differences

The timing differences of the SSAR and the ASAR ADC have been briefly explained in the previous Sections, where the N-bit SSAR and ASAR ADC architectures and their timing diagrams were illustrated in Fig. 2.3 and Fig. 2.4. In this section, the timing differences between the two ADC architectures are analyzed mathematically.

Fig. 2.5 (a) and (b) show the detailed timing diagram of the SSAR and the ASAR ADC, respectively. The key controlling signals i.e., *clk*, *smp*, *cmp_clk*, and *ready*, are marked in bold. The sampled analog input voltage V_{in_init} that applied onto the CDAC is assumed to be equal in the two timing diagrams. In Fig. 2.5, τ_k denotes the comparator decision time for k^{th} conversion (where k ranges from N-1 down to 0), and T is the clock period of the external clock signal *clk* to the SSAR ADC. The t_{dac} is the time allocated for CDAC charge redistribution, and the t_{smp} is the sampling signal width, lasting one clock cycle T and are aligned between the two designs. The comparator differential input voltage is denoted as V_{in} (=$V_{inp} - V_{inm}$), and its differential outputs are $dout_p$ and $dout_m$.

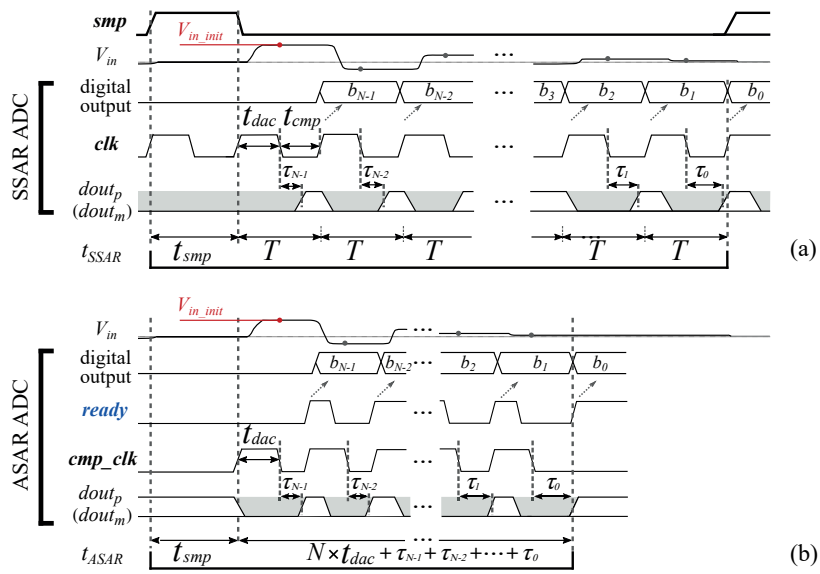

Figure 2.5: The timing diagram of (a) an SSAR ADC and (b) an ASAR ADC.

The bit conversions start after sampling. The V_{in_init} is the first voltage to be compared, and the comparison result determines the MSB bit b_{N-1} value. The rest bit (b_{N-2} to b_0) are converted following the direction from MSB to LSB, described below:

- A new V_{in} is loaded onto the CDAC, in response to the previous $(k+1)^{th}$ bit conversion. At the same time, comparator outputs $dout_p$ and $dout_m$ are reset to 0. In the SSAR ADC, the length t_{dac} of this phase is half the period T of the clock clk, which is $t_{dac} \approx 120\,\text{ps}$ under nominal working conditions based on simulation results.
- The value of the k^{th} bit is decided: $dout_p$ and $dout_m$ are resolved at the falling edge of cmp_clk after a signal-dependent decision time τ_k.

In the SSAR ADC, the decision time is typically fixed to t_{cmp}, which is equal to one half of T, independent of k. To cope with the metastability errors, t_{cmp} should be long enough to cover all but the most extended decision times. The conversion time t_{SSAR} of the N-bit SSAR ADC is then:

$$t_{SSAR} = N \cdot (t_{dac} + t_{cmp}) + t_{smp} = N \cdot T + t_{smp} \tag{2.1}$$

where t_{smp} is the time allocated for sampling analog input into the ADC.

In the ASAR ADC, the conversion time t_{ASAR} is instead:

$$t_{ASAR} = N \cdot t_{dac} + t_{tot} + t_{smp} \tag{2.2}$$

with t_{tot} in each sample:

$$t_{tot} = \sum_{k=0}^{N-1} \tau_k \tag{2.3}$$

The ASAR ADC is faster than the SSAR ADC if the t_{tot} is smaller than the $N \cdot t_{cmp}$, which is valid in most situations.

2.5 Component-Level Implementations

Both the SSAR and ASAR ADCs have been implemented in 22 nm FD-SOI CMOS and tested. The architectures of both SAR ADC designs are shown in Fig. 2.6. Note that the designs implement differential architectures to reduce even-order distortions. One of the CDAC architecture is drawn explicitly

to show the controlling switches and their corresponding control signals generated by the Asynchronous Control Logic (ACL). The two designs share similar hardware blocks, e.g., similar CDAC and comparator, but different in the SAR control designs. In the SSAR ADC architecture shown in Fig. 2.6 (a), the external clock signal *clk_ext* is buffered before clocking the comparator and the Synchronous Control Logic (SCL). On the contrary, in the ASAR ADC architecture shown in Fig. 2.6 (b), a low duty cycle external sampling signal *smp_ext* is buffered and then sent to the ACL. As mentioned earlier, a series of dynamic clock pulses *cmp_clk* are generated to trigger the comparator for making decisions.

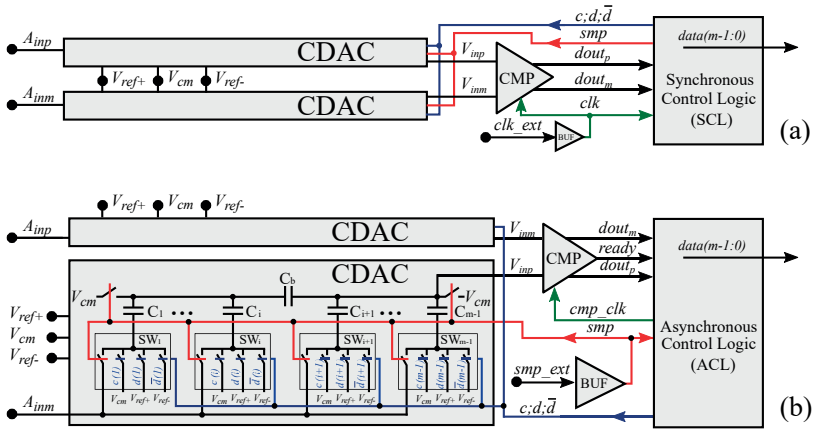

Figure 2.6: Component-level implementation of (a) m-bit SSAR ADC and (b) m-bit ASAR ADC, with one of the CDAC explicitly drawn.

In the following sections, the power-efficient CDAC design with split-capacitor array architecture and Merged Capacitor Switching (MCS) switching scheme will be described, and the bridge capacitor value (C_b) will be mathematically calculated. The comparator design will be described, and both the SCL and the ACL designs will be presented in detail.

2.5.1 CDAC Design

The CDAC is a vital component dominating the SAR ADC performance. The CDAC has to be well-matched without creating linearity issues to the ADC performance. In this section, the binary-weighted CDAC is firstly explained for illustrating the CDAC operation principles. A split-capacitor CDAC design is then shown, which uses a reduced total capacitance for the same ADC resolution.

Fig. 2.7 (a) shows a single-ended binary-weighted N-bit CDAC with bottom-

plate sampling. The capacitor array consists of switchable binary-weighted capacitors. It is implemented by an integer number of unit capacitance C_u, which is beneficial in terms of the device matching. There is an extra C_u connected to the ground, resulting in a total capacitance in the CDAC equal to exactly $2^{N-1} \cdot C_u$.

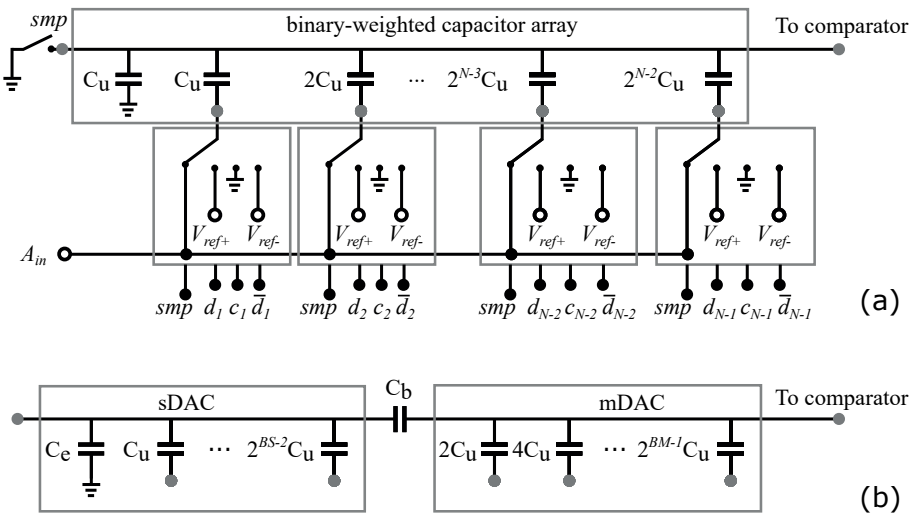

Figure 2.7: The CDAC architecture of (a) a bottom plate sampling binary-weighted CDAC and its controlling switches, and (b) a split capacitor array with a bridge capacitor C_b between the mDAC and the sDAC.

The switches for controlling the capacitors array are drawn explicitly in Fig. 2.7 (a), with connections to either the input A_{in} ($=A_{inp} - A_{inm}$) during sampling or to the reference voltages during bit conversions. The reference voltages are ground, plus (V_{ref+}), and minus (V_{ref-}) reference voltage. The i^{th} capacitor's connection for the i^{th} bit conversion is depended on the control signals $c(i)$, $d(i)$, and $d(\overline{i})$. The CDAC utilizes bottom plate sampling, which provides good signal isolation between the input and the comparator.

In the binary-weighted CDAC design, the total capacitance grows exponentially with the increased ADC resolution. An efficient way of reducing the total capacitance is implementing a split-capacitor array [12], as shown in Fig. 2.7 (b). In the architecture, a small bridge capacitor C_b is placed between the main-DAC (mDAC) and the sub-DAC (sDAC) as an attenuation capacitance. It reduces the total capacitance by approximately half compared to the binary-weighted CDAC array while agreeing with the SA algorithm. Since the total capacitance is reduced, the split-capacitor CDAC architecture shows a decreased ADC power consumption and reduced chip area than the binary-weighted CDAC.

During sampling, the sampling switches controlled by sampling signal *smp* are

closed. The input signal is applied to the capacitor bottom plates. The bit conversions start after sampling when the sampling switches are opened, causing an initial voltage V_{in_init} appears at the CDAC output. The charge stored on the CDAC capacitors are redistributed in the following bit conversions, governed by the control signals c, d, and $\bar{d}$ from the SAR control logic, resulting in a change to the CDAC output voltage.

There are multiple switching schemes to efficiently redistribute CDAC charges in response to the c, d, and $\bar{d}$. In the conventional switching method presented in [37], there are a series of *up* and *down* transitions for the CDAC to redistribute the charge. The prior work [38] claimed that the *down* transitions consume almost five times higher the power than the *up* transitions, which makes the conventional algorithm insufficient. It presented a method to split an MSB capacitor into binary scaled sub-capacitors, which achieves an average switching energy reduction of 37% compared with the conventional switching algorithm. However, it is still less efficient than the MCS scheme presented in [39] and [40], which is 93.4% more power-efficient than the conventional switching scheme. Briefly, in the MCS switching scheme, the capacitor bottom plates are first connected to the input A_{in} in the sampling phase, then to the common-mode voltage in a differential architecture. The reversed polarity A_{in} now appears at the CDAC output for the MSB to be converted. Afterward, each capacitor bottom plate is connected to either V_{ref+} or V_{ref-} depending on the previous bit conversion, until the LSB capacitor is switched. Using three reference levels in the MCS scheme instead of two in the conventional method, the average CDAC switching power is significantly reduced.

To further analyze the split-capacitor CDAC, a complete 10-bit split-capacitor array is drawn in Fig. 2.8 (a). The C_S in sDAC and the C_M in mDAC are chosen to be equal weight for the Pseudo-Random Bit Sequence (PRBS) signal injection for calibration purposes, which will be explained in Section 2.5.2. Fig. 2.8 (b) shows a simplified capacitor array, where the capacitors except C_S and C_M are combined into C_{Se} in sDAC and C_{Me} in mDAC.

Each capacitance is preferably chosen as an integer number of unit capacitance C_u to improve the matching between components in an actual design. In the proposed split-capacitor architecture, C_b is an integer number of C_u, while the C_e is set accordingly. It was shown that to set $C_b = 2\,C_u$ [41], or even simply $C_b = C_u$ [42] is possible for a linear transfer function.

To derive a relation between C_b and the other capacitances, the inverse polarity voltage $-V$ and $+V$ act on the C_S and C_M, respectively. A Norton equivalent circuit is used, which is shown in Fig. 2.8 (b).

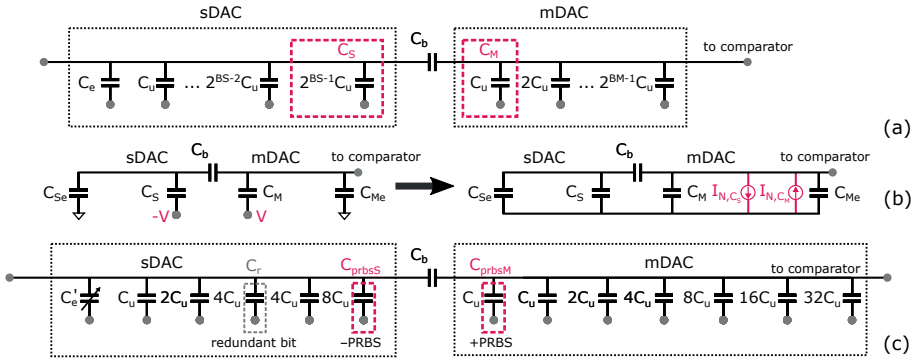

Figure 2.8: 10-bit capacitor array with PRBS calibration bits and redundancy bit, where (a) shows a complete capacitor array, (b) shows a simplified capacitor array, and (c) shows the actual implementation in the presented work.

The Norton current I_{N,C_S} injected by C_S across the mDAC is:

$$I_{N,C_S} = V \frac{C_b C_S s}{C_b + C_S + C_{Se}} \tag{2.4}$$

and the Norton current I_{N,C_M} injected by C_M across the mDAC, is:

$$I_{N,C_M} = V C_M s \tag{2.5}$$

The bridge attenuation r is defined by the ratio of the two Norton currents, which is:

$$r = \frac{I_{N,C_S}}{I_{N,C_M}} = \frac{C_b C_S}{C_M(C_b + C_S + C_{Se})} \tag{2.6}$$

Clearly, the r is only affected by C_{Se} in the sDAC.

The C_e, which is an extra capacitor next to the binary-weighted capacitor array in sDAC, is set by:

$$C_e = \left(\frac{2^{BS-1}}{r} - 1\right) C_b - \left(2^{BS} - 1\right) C_u \tag{2.7}$$

From the above equations, it can be concluded that for a predefined r, the number of bits in sDAC (BS) and the capacitance C_b determine the required value of C_e.

Fig. 2.9 graphically shows the relationship between C_e and C_b normalized to C_u, with different BS when $r = 1$. Since the C_e has to be a positive value, the C_b has to be larger than $2C_u$. In the chosen architecture, BS=4 and C_b=4C_u, which results in a C_e=13C_u that is marked as a red dot.

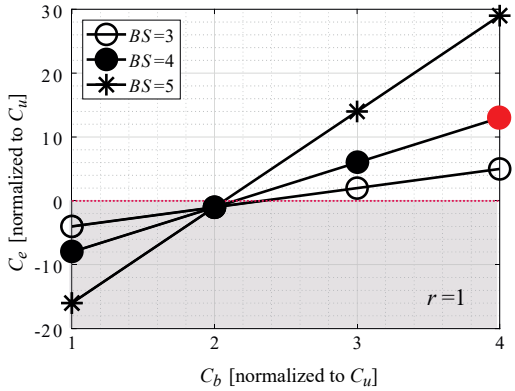

Figure 2.9: The relationship between C_e and C_b in different BS in the proposed 10-bit capacitor array, normalized to C_u.

In the proposed CDAC architecture, parts of the capacitors are used for adding an extra bit for redundancy. The redundancy scheme that will be explained in Section 2.6.5 is a practical way to reduce the errors introduced by slow CDAC settling time in particular bits. Therefore, 4 out of 13 C_u from C_e are occupied for capacitors implementing redundant bit. As a result, the actual extra capacitance C'_e is $9C_u$, and the actual CDAC implementation is shown in Fig. 2.8(c).

2.5.2 Estimation and Calibration of CDAC Imbalance

This part explains the estimation and calibration of the split CDAC array imbalance. The capacitor matching can be ensured by layout matching in sDAC and mDAC, respectively. However, the parasitic capacitance introduces a weight imbalance between the two CDAC arrays, leading to performance degradation.

A practical way to balance the two capacitor arrays is by injecting PRBS to the same weighted capacitor in both sides of the capacitor bank and examine their outputs. Still consider the CDAC array shown in Fig. 2.8, where the C_{prbsS} and C_{prbsM} on each side of the DAC array are two equal weights capacitors, when $r = 1$. Ideally, without parasitic capacitance, the test sequence will not be visible at the output since the Norton equivalent current I_{N,C_S}, and I_{N,C_M} are canceled out. However, influenced by DAC imbalance due to parasitic capacitance in the sDAC, the test sequence residue may appear at the SAR ADC digital output. The characteristic of the DAC arrays is determined by post-processing, namely, using correlation to detect the residue value and estimate the weight difference between sDAC and mDAC.

The post-processor finds the correlation between the known PRBS signal (S_{PRBS})

and the ADC output (S_o). Its output is proportional to the deviation Δr from the ideal value of r. The estimated $\hat{r}$ of the bridge attenuation is:

$$\hat{r} = 1 + \Delta r = 1 + \frac{1}{w\,M} \sum_{k=1}^{M} S_o[k] S_{PRBS}[k] \tag{2.8}$$

where M is the number of samples and w is the PRBS bit weight.

To calibrate the CDAC, it is preferable to use $\hat{r}$ directly switching on or off a fraction of C_e' on-chip, which is made tunable by digital control signals; alternatively, the SDAC bit weights can be corrected in the digital domain through multiplication by $\hat{r}$, then combined with the MDAC bits.

Fig. 2.10 plots $\hat{r}$ vs. C_e' between 3 and 15 C_u, where its nominal value is 9 C_u. In the first scenario shown in blue curve, the $\hat{r}$ is implicitly given by Eq.2.7. In the second scenario shown in green curve, the $\hat{r}$ is estimated using Eq.2.8. Lastly, $\hat{r}$ is swept and found when maximum SNDR is reached, shown in purple curve. From the simulation, the three methods generate nearly identical results.

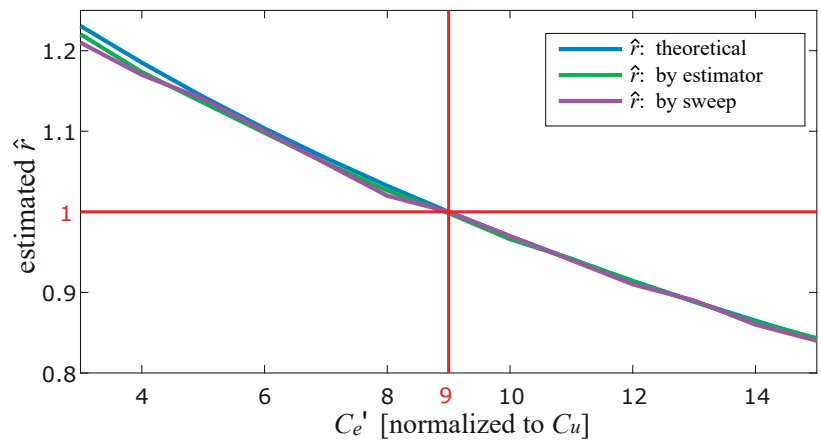

Figure 2.10: Theoretical $\hat{r}$ values, estimated value by the correlation-based estimator, and estimated value by SNDR maximization sweep, as a function of C_e'. Capacitor values are normalized to C_u.

2.5.3 Comparator Design

In a SAR ADC, another core component is a comparator. The comparator compares its input voltage V_{in} with a reference voltage (zero in the single-ended illustration) to generate a digital logic value based on the comparison result. Specifically, the V_{in}, which is also the CDAC output voltage, varies in each conversion step in response to a previous bit decision. In the following examples,

assume logic one is generated when the V_{in} is positive, and a logic zero is generated when the V_{in} is negative or zero.

2.5.3.1 Comparator Component-Level Implementation

In the component-level implementation, a simplified differential dynamic comparator schematic is shown in Fig. 2.11. The circuit is similar to the design presented in [43], which consists of a clocked pre-amplifier, a regenerative latch, and an output stage. Note that there are two choices of the output stages: either an SR latch or simply two buffers.

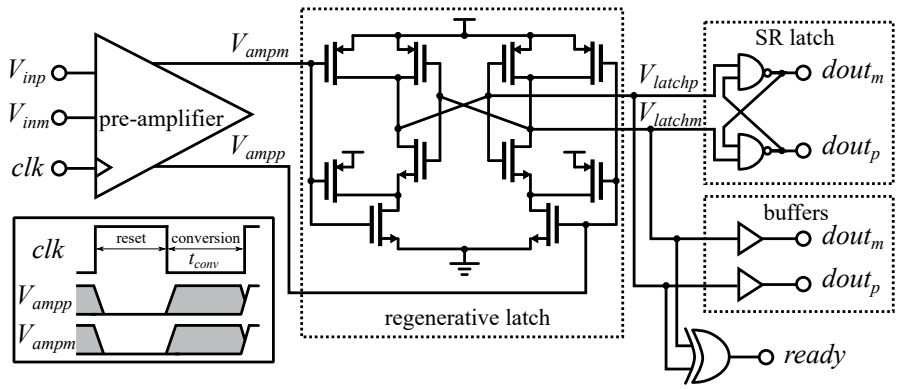

Figure 2.11: Comparator schematic with either an SR latch or two buffers in its output stage.

The timing diagram of the *clk* and the pre-amplifier output signal V_{amp} is drawn at the lower-left corner in Fig. 2.11. At the *clk* high pulse, the pre-amplifier is in reset. Both of the pre-amplifier outputs V_{ampp} and V_{ampm} are reset to ground, which resets the regenerative latch internal nodes and removes any memory effect from the previous bit conversion. At the *clk* low pulse, the comparator's differential input voltage V_{in} is amplified to toggle the regenerative latch.

The pre-amplifier schematic is drawn in Fig. 2.12, including a clocked amplify stage and an inverter second stage to increase gain. There are an optional input pair of P-Channel Metal-Oxide-Semiconductor (PMOS) transistors drawn in the blue dashed box, behaving as a push-pull architecture together with the N-Channel Metal-Oxide-Semiconductor (NMOS) transistor pair, to reduce the comparator noise. However, the input capacitance is increased, which slightly affects the V_{in} transition speed.

There are two options at the comparator output stage: either an SR latch or merely a pair of buffers. By implementing an SR latch, the comparator

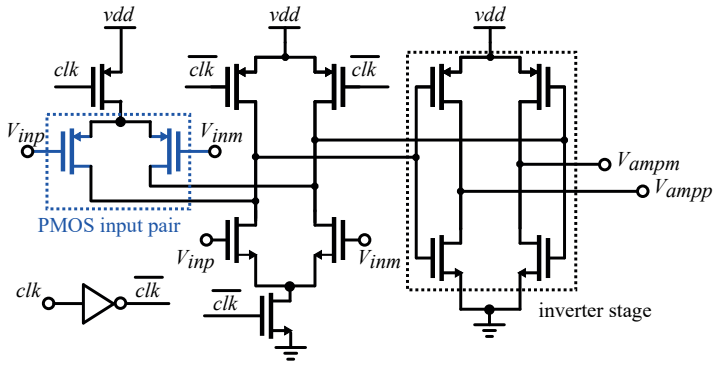

Figure 2.12: Pre-amplifier schematic, used in the comparator.

outputs $dout_p$, and $dout_m$ are stable for a whole clock period [44], which eases the following control logic design. However, it may experience bit conversion errors due to a remained previous bit conversion: the previous comparator decision is not updated in time due to a short clock cycle period before latched by the following SAR control logic. By replacing the SR latch with two buffers for the differential output terminals, the $dout_p$ and $dout_m$ switch exactly as the regenerative latch's outputs V_{latchp} and V_{latchm}. In other words, the comparator outputs $dout_p$ and $dout_m$ exercise a reset pulse before becoming valid.

A benefit of replacing the SR latch with buffers is that reset values are always used instead of the remaining previous decisions whenever comparator decisions are not ready. It will no longer randomize the bit decisions but instead set them to a default value. Equivalently, the default decisions create a high ADC offset voltage, showing an increased Direct Current (DC) offset to the ADC output spectrum and a reduced ADC dynamic range. More importantly, the ADC will not suffer a significant performance drop. Another benefit of removing the SR latch is that the comparator becomes faster, since the SR latch's cross-coupled architecture inevitably introduces a small propagation delay to the output signals.

2.5.3.2 Comparator Decision Time

The comparison speed is one of the dominant factors limiting the maximum SAR ADC conversion speed, which is studied in detail in this section.

In an actual circuit, the comparator decision time τ is not a constant value. It is signal-dependent and is directly related to the V_{in}. Fig. 2.13 shows a conceptual timing diagram of the regenerative latch, in which differential input V_{in} and two

outputs V_{latchp} and V_{latchm} are shown. For illustration purposes, the regenerative latch generates V_{latchp} and V_{latchm} within a finite decision time $\tau_A = 36\,ps$ for a large V_{in} (100 mV) and $\tau_B = 74\,ps$ for a small (100 uV) V_{in}, where both decision times are derived from component-level simulations.

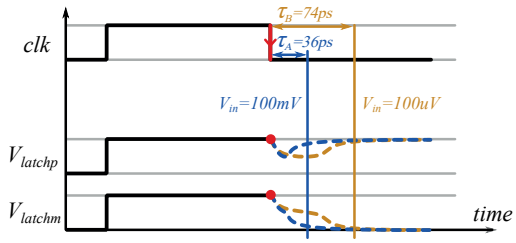

Figure 2.13: Regenerative latch timing diagram for a 100 mV and a 100 uV differential latch input voltage V_{in}.

Based on the discussions presented in [45], the dependence of τ on V_{in} is expressed by a logarithm equation, which is:

$$\tau = f(V_{in}) = \alpha \ln(V_{in}) + \beta \tag{2.9}$$

where α and β are constants, determined by the selected components and comparator architecture.

The component-level comparator, whose schematic was already shown in Fig. 2.11, is simulated in 22 nm FD-SOI CMOS. A τ versus V_{in} plot is drawn in the red curve in Fig. 2.14. Besides, the ideal calculation using Eq. 2.9, with $\alpha = -3.5\,ps$ and $\beta = 70\,ps$, is plotted in the blue dashed curve. A trend is clearly visible: at a very small V_{in}, the τ is very large. With the V_{in} continuously increasing, the τ reduces.

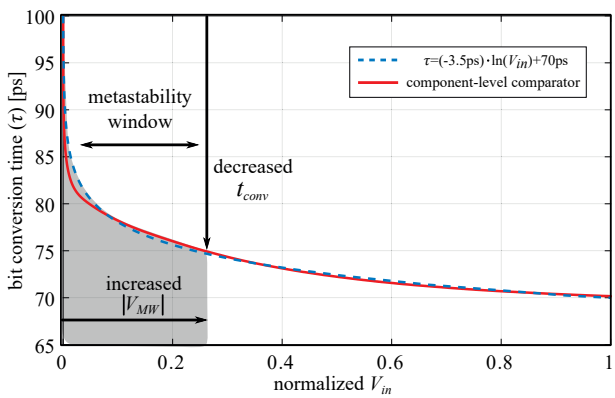

Figure 2.14: τ vs. input voltage V_{in}, in a component-level comparator and an ideal comparator model.

The fully-differential comparator architecture has symmetrical plus and minus signal paths. Ideally, with a small input voltage $V_{in} \approx 0$, the clocked pre-amplifier outputs are very close to each other. The slight voltage difference is not sufficient to drive the regenerative latch, causing a long decision time for a full separation of V_{latchp} and V_{latchm}.

Due to such input signal dependent variation of τ, the limitation of an SSAR ADC architecture emerges. Still, seeing from the timing diagram shown in Fig. 2.5, the clock negative pulse width t_{conv} is the allocated time for a comparator to complete a decision in time. Therefore, the t_{conv} is selected so that most of the τ is guaranteed to be lower than this threshold. However, it is inefficient since the external clock clk to the SSAR is selected with a minimum period of T (usually chosen to be twice the t_{conv}). As a result, the maximum clock frequency, directly related to the ADC sampling frequency, is reduced.

Alternatively, an asynchronous architecture dynamically generates the comparator clock to satisfy the signal-dependent variation of τ. Fig. 2.15 shows a simulated histogram of τ for each bit in an exemplar 10-bit SAR ADC design, where the ADC is fed with a full-scale amplitude sinusoidal input signal. In the figure, the average τ for each bit conversion is marked as vertical dashed lines. It can be seen that there is as large as a 20 ps difference between the MSB decision (τ_9) and the LSB decision (τ_0). Fig. 2.16 shows the total conversion time, which is the summation of the τ in those as mentioned above, ten individual bits. It appears a much narrow distribution than τ distributions in the individual bits, e.g., very a few points beyond 750 ps compared with a few τ beyond 100 ps in bit 0 in Fig. 2.15.

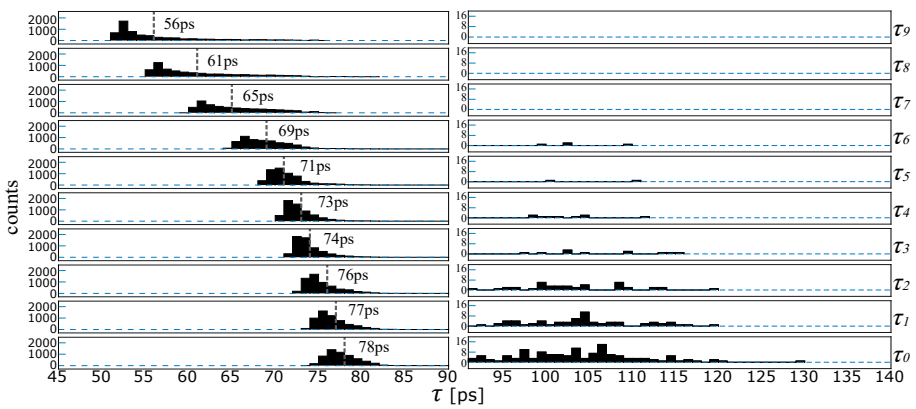

Figure 2.15: τ in ten individual ADC bit conversions, when the ADC input is a full-scale amplitude sinusoidal signal.

These circuit-level simulations show that the t_{tot} in the ASAR ADC is smaller than $N \cdot t_{cmp}$ in the SSAR as explained earlier in Section 2.4.3. It results in a

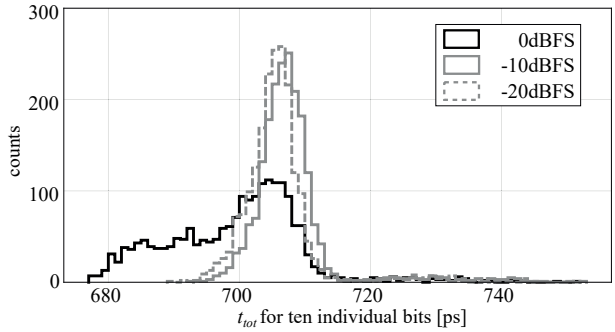

Figure 2.16: Total conversion time distribution, with input amplitudes of 0 dBFS, -10 dBFS and -20 dBFS.

reduced t_{ASAR}, which in turn, increases the maximum sampling rate.

2.5.3.3 Decision Time Limiter

The comparator used in the ASAR ADC requires an indication signal *ready* for signaling a comparison completion. The *ready* signal generator is implemented by adding an XOR gate to the outputs in the comparator. It detects the difference between the two terminals and releases a high pulse whenever the difference is large. Upon the *ready* is set, the next *cmp_clk* pulse is released from the control logic preparing for the following comparison. The *ready* signal is an enabler for the control logic to correctly generate the next clock pulse for the comparator, which is crucial for uninterrupted bit conversions.

The *ready* and the *cmp_clk* are closely related to each other, which means the *cmp_clk* will not release until the previous comparator decision has been completed. It could interrupt ADC bit conversions: for a very long comparator decision time, a bit conversion may take too much time, leaving the remaining bits unable to be decided within the allocated time.

A precautionary method is implemented to avoid the ASAR ADC entering such a situation. Suppose the clock generation is suspended at a particular bit. In that case, a limiter forces the generation of a decision and releases *ready* after a preset time whenever a bit decision takes a too long time. Fig. 2.17(a) shows the limiter circuit schematic. Its timing diagram is shown in Fig. 2.17(b). The adjustable capacitance C is controlled digitally to select a preset time threshold. Two possibilities are shown for illustration purposes: tight timing and relaxed timing. By tuning the C to compensate for any possible long decision time that may suspend the current and the following bit conversions, the ASAR ADC runs under different PVT corners.

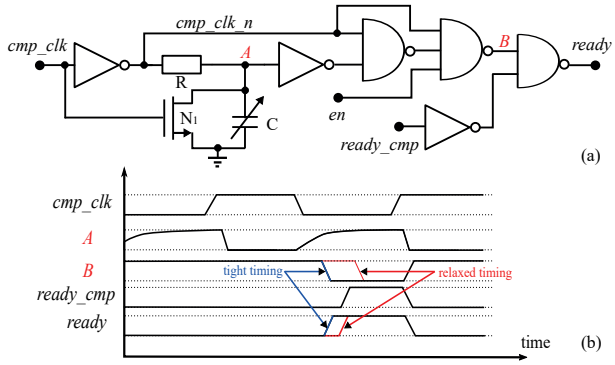

Figure 2.17: A limiter to force a decision within a preset time, digitally tuned by an adjustable capacitance C, with (a) schematic and (b) timing diagram.

2.5.4 SAR Contol Logic Design

The SAR control logic is a circuit that latches the comparator outputs to generate a set of feedback control signals correspondingly to toggle the CDAC switches. In the meantime, it creates the ADC output bitstream. The detailed design of SCL and ACL will be explained separately.

The control logic circuits have not been widely analyzed in the published works. Most of the articles mainly focus on the architecture and algorithm level, such as [36]. Especially an ACL, which is an essential block that dynamically generates a variable pulse width clock signal, benefiting from a customized design.

2.5.4.1 The SCL Design

The SSAR ADC design architecture was shown in Fig. 2.6(a). Recall that in this particular architecture, all the internal blocks are synchronized to a clock signal *clk* that is buffered from an external clock *clk_ext*. Since the SCL is a digital circuit, presenting a state machine is necessary to demonstrate the state propagation and the control signals c, d, and $\bar{d}$ generation. The SCL design is usually implemented using digital standard cells, which can be easily migrated to other CMOS technologies in the future.

The state-machine for the SCL is shown in Fig. 2.18. During the first sampling state (S_{smp}), the *smp* is a logic one, and all the control signals c, d, and $\bar{d}$ are zero. Next, in the S_N state, all the c are one, which connects all the capacitor bottom plates to a common-mode voltage V_{cm} in differential architecture. The sampled input differential voltage now appears on the CDAC output, compared

by the comparator, and becomes MSB $[data(N-1)]$ at the next state. This MSB determines the generation of a next set of control signals, i.e., c_{N-1}, d_{N-1}, and $\bar{d}_{N-1}$ in the S_{N-1} state, that toggles the following CDAC charge redistribution. The rest bits are converted in sequence in the following states until reaching the S_1 state, where the last set of control signals c_1, d_1, and $\bar{d}_1$ is determined. N bit conversions are completed, and the LSB $[data(0)]$ is determined.

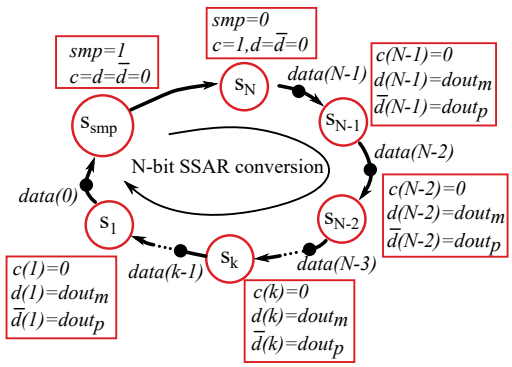

Figure 2.18: N-bit SCL state machine, including a sampling state S_{smp} and bit conversion states S_N to S_1.

Fig. 2.19 shows the SCL schematic. It consists of two main parts: a ring counter and a control & data generator. The ring counter converts the *cmp_clk* to a series of non-overlapping pulses for controlling the multiplexers c_MUX and d_MUX in the control & data generator. The *smp* is originated from the ring counter for sampling the input voltage onto the CDAC. At *cmp_clk* rising edge, the control & data generator has N pairs of D-Flip-Flop (DFF) to either latch a new pair of CMP outputs $dout_p$ and $dout_m$, or to store the previous decision, depending on the combination of controlling pulses (p) from the ring counter. The SCL output $data(N:1)$ is a combination of $\bar{d}(N-1:1)$ and the LSB bit, which will be either directly read out by a DSP device or temporarily stored into an on-chip memory device.

2.5.4.2 The ACL Design

Comparing with the SCL design, the ACL design is more sophisticated. The previous article presented by Harpe et al. [46] proposed a detailed ACL design, where a set of control signals control the logic to switch the CDAC properly. Besides, capacitors are used as memory elements to store the states, and a dynamic logic implements state transitions.

In this research work, the ACL is built mainly based on the digital logic cells.

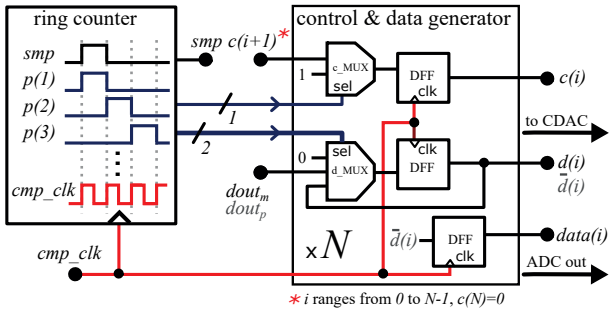

Figure 2.19: The SCL schematic, including a ring counter to generate sampling signal and a control & data generator to generate control signals.

The proposed ACL schematic is shown in Fig. 2.20. Like the SCL design, it has two main parts: a clock generator and a control & data generator.

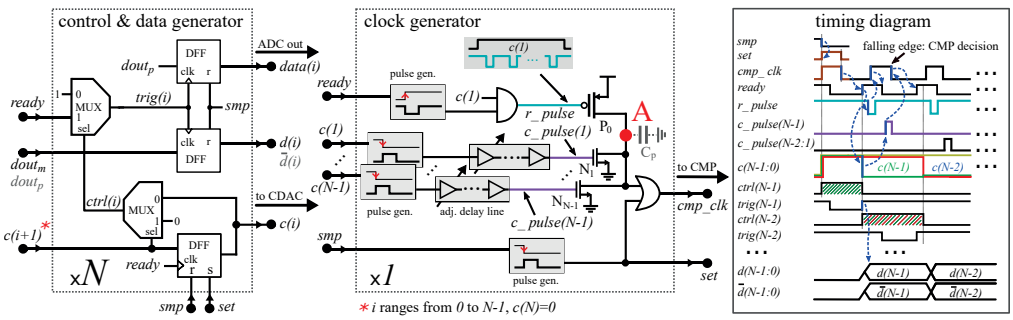

Figure 2.20: The ACL schematic, including a control & data generator for control signals generation and a clock generator for comparator clock cmp_clk generation.

As seen from the ACL schematic, instead of having a high-frequency clock signal *cmp_clk* that directly clocks the SCL, there is a low duty cycle sampling signal *smp* controls the ACL. The *smp* starts each sample conversion, for the internal comparator clock *cmp_clk* generation. The control & data generator schematic is similar to the SCL schematic but clocked by a completion indicator *ready* from the comparator instead of the clock. The *ready* is gated by multiplexers (MUX) first and delivered to the DFFs.

The clock generator is the core for generating the *cmp_clk* pulses in sequence, with most of its components chosen from the digital standard cell library. Since understanding such a complicated circuit is not easy and straightforward, in the following paragraphs, the details of this circuit are studied by using the timing diagram shown on the right side of Fig. 2.20.

To begin with, the *smp* pulse initially resets all the DFFs in the control & data generator. Afterward, a pulse *set* pulls up c but remains d and $\bar{d}$ low. Then,

the rising edge of *ready* (issued by the comparator) triggers the shift registers to shift $c(i+1)$ to $c(i)$ [similar to the SCL, $c(N) = 0$]; $c(i+1)$ and $c(i)$ act as a window-like $ctrl(i)$, which passes only one *ready* pulse to $trig(i)$ in each of the unit cells. The $d(i)$, $\bar{d}(i)$, and $data(i)$ are then generated from *dout* at the rising edge of $trig(i)$.

Pulse generators are used extensively to convert the falling edge of each $c(i)$ into a short pulse $c\_pulse(i)$. The corresponding NMOS transistor N_i is then turned on to pull node A down. Similarly, each of the rising edges of *ready* generates a negative pulse *r_pulse* to pull node A up. The absence of overlap between *r_pulse* and *c_pulse* is enforced by adjustable delay lines placed after the pulse generators, and the desired *cmp_clk* is generated.

2.6 SAR ADC Non-Idealities

In SAR ADCs, circuit non-idealities impair the ADC performance. The capacitor mismatches in CDAC limit the ADC resolution, which can be minimized during layout using the common-centroid technique. Non-negligible parasitic capacitances in circuit layout increase the capacitance on the CDAC array, causing an imbalance between sDAC and mDAC in split-capacitor DAC, requiring estimation and calibration by a calibration engine. Furthermore, PVT variations cause the circuit's operation points to deviate from their designed values. It results in a slow CDAC settling, which requires redundancy technique to be implemented. The uncertainties to the internally generated clock pulse widths in the ASAR ADC are introduced, which need tunings to counter.

2.6.1 Bit Conversion Errors in SSAR ADC

A potential problem in SSAR ADC arises when performing extensive simulations: the SCL latches a pair of incorrect comparator output signals in a differential architecture and releases a set of invalid control signals, suspending charge redistribution in the CDAC. It causes bit conversion error and may affect the subsequent decisions' correctness thus imposing large errors to the ADC output.

The comparator schematic was shown in Fig. 2.11. The timing diagram of the comparator outputs $dout_p$ and $dout_m$ is illustrated in Fig. 2.21. Fig. 2.21 (a) shows the output signal transitions when an SR latch is used. Clearly, the comparator's previous decisions remain until updated. Fig. 2.21 (b) shows the result when two buffers are used. In this case, the $dout_p$ and $dout_m$ are firstly

reset to logic one at clk high phase, then updated after clk falling edge. The delay between the clk falling edge and the time when output values are settled is denoted as τ.

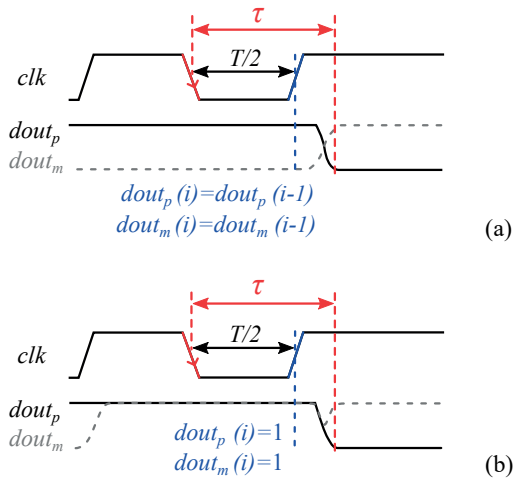

Figure 2.21: Comparator differential outputs vs. clk, when (a) an SR latch is used, and (b) two buffers are used in the comparator output stage.

Recall that τ vs. V_{in} follows the equation shown in Eq. 2.9, which was plotted in Fig. 2.14, showing that a small V_{in} leads to a large τ which could be larger than the allocated t_{conv}, usually equal to half clock period ($t_{conv} = T/2$). The insufficient t_{conv} leads to an increase of $|V_{MW}|$. The $|V_{MW}|$ means a metastability window, which is an uncertain region that a comparator takes a long time to resolve a decision. Thus, under a high sampling frequency where $T/2$ is small, comparator decisions are not settled in time, causing a wrong value been read by the SCL, either the previous decisions [Fig. 2.21 (a)], or the reset values [Fig. 2.21 (b)].

There are also two uncertainties when the SCL processing the $dout_p$ and $dout_m$. Fig. 2.22 (a) shows a fully differential SCL architecture, where the $dout_p$ and $dout_m$ are processed in parallel. The CDAC control signals $d(i)$ and $\bar{d}(i)$ are generated separately, which could become invalid when $dout_p$ and $dout_m$ are equal, i.e. the comparator outputs are still in reset and SR latch is not used. On the other hand, Fig. 2.22 (b) is the proposed modified architecture, that single-ended comparator output signal $dout_p$ is used for generating $d(i)$, and its inverse $\bar{d}(i)$ is created by adding an inversion circuit in the SCL. The timing diagram is shown on the right side of each architecture.

The effectiveness of the proposed method can be graphically illustrated in time domain in Fig. 2.23. Fig. 2.23 (a) is an ideal condition that t_{conv} is sufficient,

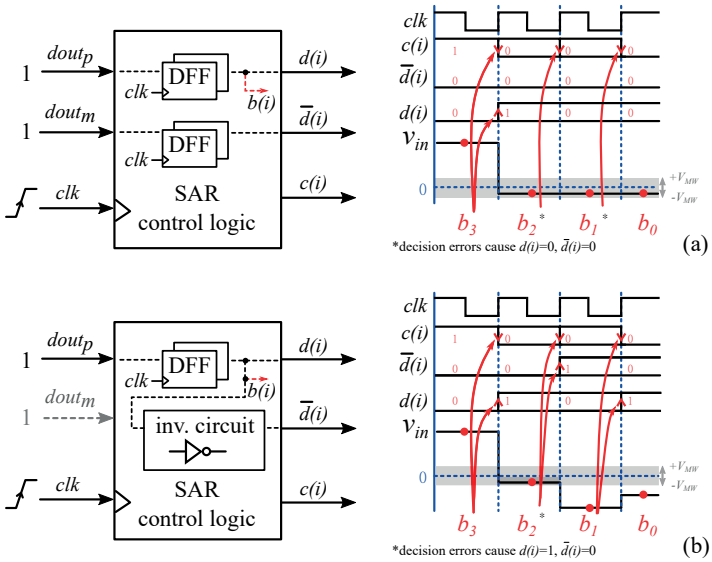

Figure 2.22: Conceptual illustration of SCL decision errors when latching comparator differential outputs, where (a) shows an SCL design with parallel signal paths, and (b) shows a modified SCL design by processing single-ended comparator output for generating non-overlapping control signals.

all the comparisons are completed in time and V_{in} continuously approaching 0 reference voltage, no error occurs. Fig. 2.23 (b) is the case when t_{conv} is short causing a large $|V_{MW}|$ appears. By implementing the proposed method, the reset value of the comparator outputs is selected. Whenever $|V_{in}| < |V_{MW}|$, a set of default control signals is generated to control a default charge redistribution in CDAC. The V_{in} gradually finds its way to $-V_{MW}$ instead of 0. For two exemplar voltages to be converted: $V_{in} = V_1$ and $V_{in} = V_2$, the proposed method shows a constant +11 increase to the digital output *data*.

In short, to avoid generating invalid control codes, the proposed method replaces the SR latch that is commonly found in the comparator with two buffers. An inversion circuit is included in the SCL that using single-ended output from the comparator for control signal generation. A reduced t_{conv} causing V_{in} pursuing a new reference voltage of approximately $-V_{MW}$ (or $+V_{MW}$ depending on the predefined default values of the control signals) other than 0, effectively causing an increased DC offset to the SSAR ADC other than an increased random noise when the standard method is used. In the frequency domain, this is illustrated in Fig. 2.24. When using the standard method, as the red spectrum shows, the noise floor is much higher than the ideal error-free spectrum shown in black. By using the proposed method, seen from the spectrum shown in blue, a high DC bin is visible when the $|V_{MW}|$ is large. It shows a very slight increase to the noise floor compared to the ideal scenario. However, the proposed method

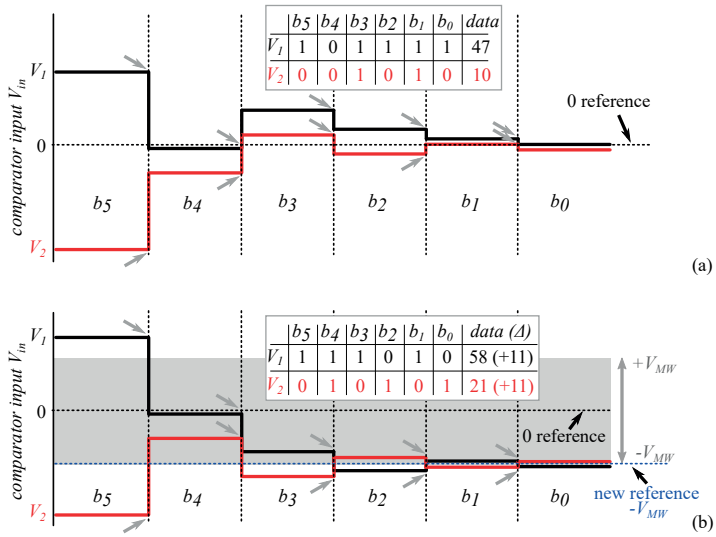

Figure 2.23: Graphical illustration of V_{in} after each bit conversion in a 6-bit SAR ADC example. (a) $|V_{MW}|$ is very small, V_{in} approaches 0 reference. (b) The t_{conv} is insufficient, causing a relatively large $|V_{MW}|$, V_{in} converges to a new reference voltage $-V_{MW}$ using the proposed method, where the default control signals are $d(i) = 1$ and $\bar{d}(i) = 0$.

causes a reduction to the ADC's dynamic range, requiring a reduced input signal amplitude to avoid over-ranging the ADC.

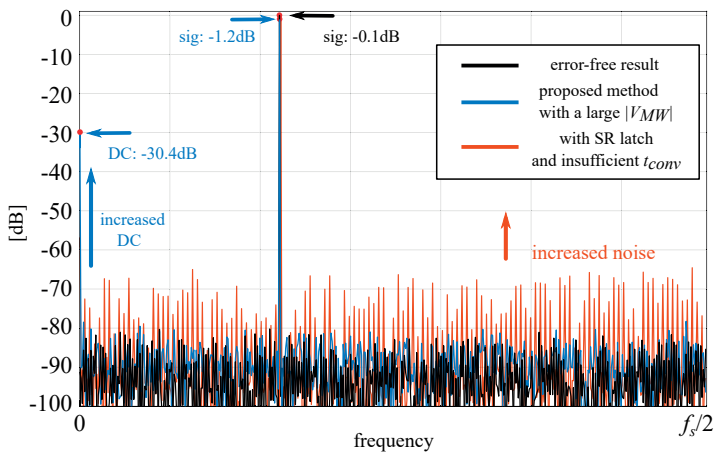

Figure 2.24: Simulated ADC output spectra, with an ideal error-free result shown in black; with large $|V_{MW}|$ and buffers in the comparator, shown in blue; with the SR latch in the comparator, shown in red.

By continuously decreasing the t_{conv}, the proposed method shows a more graceful degradation to the SNDR than the standard design. In the standard design, an SR latch is used in its comparator, and the SCL may latch the comparator's

previous decision. The maximum SNDR vs. t_{conv} for the proposed design (using buffers in the comparator) and the standard design (using SR latch in the comparator) is shown in Fig. 2.25, with identical SAR control logic in the two ADC designs which readout a single comparator output. The SNDR starts degrading rapidly at approximately t_{conv}=95 ps for the standard design, but degrades slower and holds a reasonable value up to t_{conv}=78 ps by using the proposed design method.

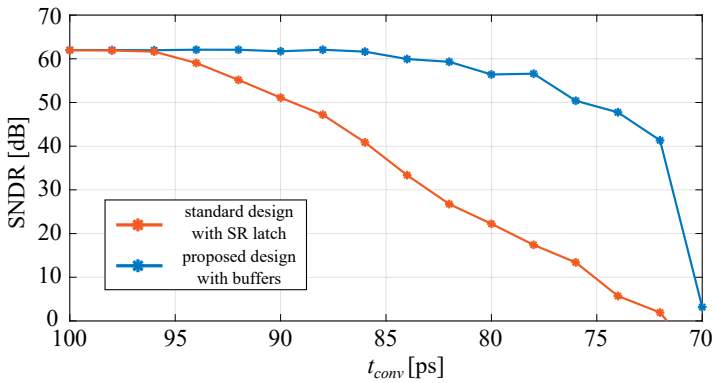

Figure 2.25: SNDR vs. t_{conv} plots, using proposed and standard design.

2.6.2 SNDR Degradation at Increased Sampling Rate

With a decreased t_{conv} from an increased f_s, the incomplete comparisons cause bit conversion errors. If the errors happen frequently, the SNDR may degrade abruptly. The SSAR ADCs are easier to generate such errors since identical time is allocated for all the bit conversions. In contrast, an ASAR ADC uses an internally generated dynamic clock, allocating variable time for each bit conversion. Thus, it experiences a graceful SNDR degradation at an increased f_s, causing a significant improvement to the design robustness.

Recall that Fig. 2.16 showed the total conversion time simulated in an ASAR ADC, which is a key consideration for error-free conversions. In contrast, the maximum bit-wise decision time is a limiting factor to the SSAR ADC performance. Assume sampling frequency is sufficiently low (f_{smp} <350 MHz), both of SSAR ADC and ASAR ADC can complete the conversions in time, shown as red and black curves in Fig. 2.26. With the f_s continuously increased beyond 350 MHz, the two plots deviate. The SNDR in the SSAR degrades rapidly when f_s increases to 10% larger than an edge frequency $f_{e,SSAR}$=390 MHz. It is because the errors may appear at the high-weight bits that significantly impact

the SSAR ADC performance. Thus for a robust SSAR ADC across the process corners, the f_s has to be selected as a lower value.

On the other hand, the ASAR ADC is more robust. The incomplete comparator decisions mainly appear at low-weight bits, while the high-weight bits are not influenced. Seen from Fig. 2.26, at a continuously increased f_s beyond an edge frequency $f_{e,ASAR}$=410 MHz, the effect ADC resolution reduces by 1 bit, then 2 bits, etc, and shows graceful SNDR degradation. Therefore, the ASAR ADC can tolerate larger PVT variations and still functioning at a high f_s. Abrupt performance degradation will not occur.

The similar behaviors can be observed when noise are presented in the circuits. The ASAR ADC still shows an extended operational sampling frequencies, while the SSAR ADC shows an abrupt SNDR degradation at a much lower frequency.

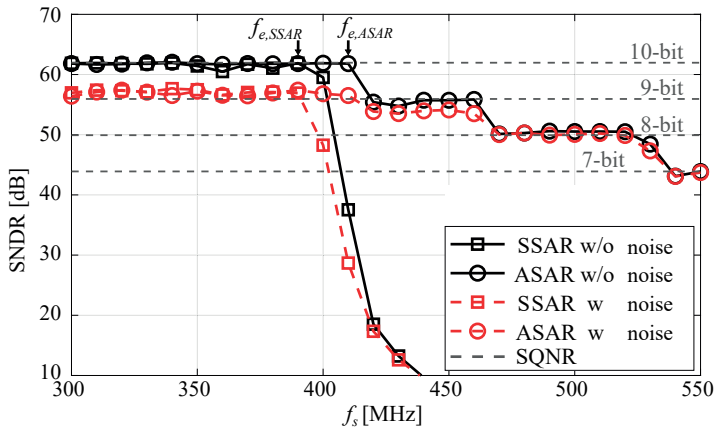

Figure 2.26: SNDR vs. sampling frequency sweep.

2.6.3 Internal Clock Pulse Width Variations in ASAR ADC

Another uncertainty due to PVT variations is the pulse width of the internally generated clock in ASAR. A very short clock pulse may reset the comparator incorrectly. Therefore, it is wise to add tunability for generating the internal clock to satisfy the timing requirements.

In the ACL schematic shown in Fig. 2.20, adjustable delay lines in the clock generators control the pulse width of the *cmp_clk*, which are configured by using external digital control bits to select one of the internal outputs from a chain

of inverters. The delay lines slow down the signals to internal NOMS/PMOS transistors for an optimized clock pulse width to counter PVT variations.

2.6.4 Extra Capacitance Tuning

A challenge in high-performance SAR ADC design is constructing a well-matched capacitor array. It is beneficial to have a unit cell-based design from the device matching perspective, meaning that a single component is designed and used multiple times. The CDAC in the SSAR ADC has a C_u of 2 fF constructed by a 10 V Metal-Oxide-Metal (MOM) capacitor. In the ASAR ADC, instead, a 2.5 V MOM capacitor is used with a capacitance of 6 fF, without increasing the parasitic capacitance and the physical size.

As mentioned previously, the split-capacitor array is implemented in both the SSAR ADC and the proposed ASAR ADC, with the architecture shown in Fig. 2.7 (b). All the capacitances are chosen as an integer number of C_u. It was already shown by Eq. 2.6, that the r is not changed if there is any parasitic capacitance appears in the mDAC array (an increased C_{Me}).

In contrast, the parasitic capacitance at the sDAC array causes the r deviates from its original value. Without proper compensation, large distortions appear at the SAR ADC output. Therefore, efforts are taken to reduce the impact from the SAR ADC non-idealities: either by digital tuning or by post-processing.

In the CDAC circuit, four digital tuning bits are placed to shift in or out parts of the capacitors in C'_e, coarsely compensating for the r variations due to the increased parasitic capacitance during the layout. Further, the DAC imbalance is calibrated by applying gains to the sDAC bit weights in the post-processor to estimate an exact value of r and calibrate it, which has been explained in Section 2.5.2.

2.6.5 Redundancy Technique in SAR ADCs

In a SAR ADC, the capacitor switching speed is finite. It causes a problem: the CDAC output voltage has not entirely settled but was already compared with a reference voltage. It leads to bit conversion errors that impair the SAR ADC resolution. It becomes critical if such errors appear at high-weight bits decisions. For example, a large high-weight bit capacitor is switched at a slow speed that causing an error, is more pronounced than an error from a smaller capacitor at a low-weight bit. A solution to improve the switching speed is using larger

switches in the CDAC and add large buffers to drive long inter-connection wires between the SAR control logic and their large loads. However, this method inevitably increases the SAR ADC physical area and its power consumption.

Another attractive method to minimize the influence of a finite capacitor settling time is adding redundancy bits to the SAR ADC. In short, the redundant architecture creates a small overlap region for the bit conversions, where any analog input is guaranteed to be converted to one equivalent digital representation. The previous works already analyzed the effectiveness of redundancy in the SAR ADCs. In the article presented by Prof. Murmann [47], various redundancy methods used in state-of-the-art SAR ADC designs are reviewed. The paper claims that "the errors are neither measured nor corrected but simply tolerated and rejected by the conversion algorithm." In [48], the redundant architecture uses three redundancy bits to improve the SAR ADC performance. It addresses that the impact from the CDAC settling issues reduces from cycle to cycle. Three redundancy bits are placed in the CDAC, and digital error correction logic is used to convert 13-bit redundant codes to 10-bit binary codes. Three extra clock cycles are required to tolerate the non-linearities appear in the ADC, partially caused by the missing analog input range.

In the following analysis, a redundancy method is explained. A 5-bit SAR ADC example is shown for illustration purposes, as shown in Fig. 2.27, which is based on a binary searching algorithm. Three analog input voltages are shown: the initial analog voltage equal to the plus and minus reference voltages (1 V and -1 V, respectively), and an arbitrary voltage (-0.42 V). The corresponding digital outputs are calculated and marked on the vertical axis shown on the right.

According to binary searching algorithm, in the conversion step i where i=4 to 0, the analog voltage V_i is compared with the reference voltage 0 for i^{th} bit conversion to be b_i. Then, depending on b_i, the CDAC output voltage is decreased or increased from V_i by half of the previous step to be V_{i-1}. Eventually, the LSB code (b_0) is determined, and b_4 to b_0 is the final ADC digital output.

The ADC digital output D_{out} is a combination of the digital output bit with their weights, which are binary scaled in a binary searching SAR ADC. Therefore in the proposed exemplar 5-bit SAR ADC, Eq. 2.10 shows the D_{out} reconstruction:

$$D_{out} = \sum_{i=0}^{4} b_i \cdot 2^i \tag{2.10}$$

For a digital code b_4:b_0=00000, the D_{out} is 0 while the D_{out} is 31 with b_4:b_0=11111.

Next, one redundancy bit is added with an equal weight of b_3, called b_{3r}. With

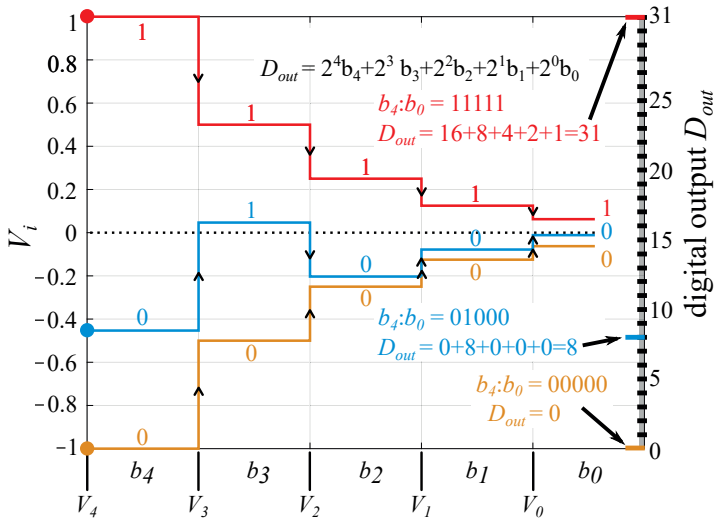

Figure 2.27: A 5-bit binary searching algorithm shows the internal voltage V_i changes in each bit conversion step, including the converted bits and ADC output.

this extra bit, more digital codes are created to cover the same input voltage range meaning that a certain degree of redundancy is added. The architecture has one or a few extra bits beside the regular binary-weighted capacitors to create an overlapping region for the input voltage decision, meaning that the clock cycles required for each sample conversions are larger than the SAR ADC actual resolution.

Fig. 2.28 shows an example of the conversion steps with the aforementioned extra redundancy bit b_{3r}. Similar to Fig. 2.27, two input voltages close-to reference voltages are selected, and an exemplar input voltage of -0.42 V is chosen. However, the output digital code range is still 0 to 31 to cover the input voltage range from -1 V to 1 V even though six conversion steps are used for a 5-bit conversion.

The new digital output range is not increased with an extra bit. Fig. 2.28 (a) is an example with a redundancy bit but without conversion errors. The ADC digital output D_{out} is calculated using Eq. 2.11:

$$D_{out} = 2^4 \cdot b_4 + 2^3 \cdot b_3 + 2^3 \cdot (b_{3r} - 0.5) + 2^2 \cdot b_2 + 2^1 \cdot b_1 + 2^0 \cdot b_0 \qquad (2.11)$$

Notice that there is a -0.5 subtracted from b_{3r}, which is included to compensate for the offset introduced by the redundancy bit. Comparing the b_2 and b_{3r} in Fig. 2.28(a), clearly, these two bits are always contradictory to each other if errors does not exist. This is due to the combination of these two bits are

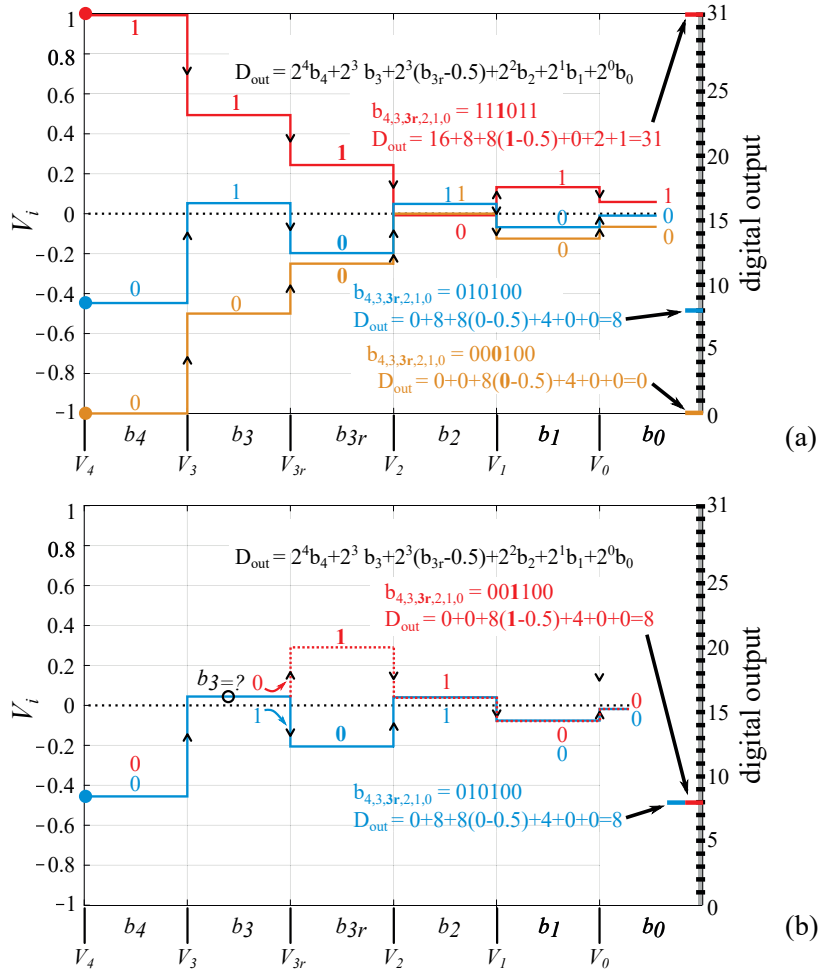

Figure 2.28: (5+1)-bit binary searching algorithm with 1-bit redundancy. (a) shows the ideal scenario without conversion errors, and (b) shows a -0.42 V is converted regardless of error presented in b_3 conversion, resulting in the same ADC digital output.

treated as a single weight of 4. $b_{3r}, b_2 = 01$ representing a digital value of 0, and $b_{3r}, b_2 = 10$ representing a digital value of 4.

If b_3 is not converted correctly, e.g. due to insufficient CDAC settling, the red dashed branch is selected in Fig. 2.28(b). $b_3 = 0$ (error) and $b_{3r} = 1$, still leads to an analog voltage equal to the one from the blue branch when the rest bits are assumed to be error free. Apply Eq. 2.11, $D_{out} = 2^4 \cdot 0 + 2^3 \cdot 1 + 2^3 \cdot (\mathbf{0} - 0.5) + 2^2 \cdot 1 + 2^1 \cdot 0 + 2^0 \cdot 0 = 8$ for the error free blue branch and $D_{out} = 2^4 \cdot 0 + 2^3 \cdot 0 + 2^3 \cdot (\mathbf{1} - 0.5) + 2^2 \cdot 1 + 2^1 \cdot 0 + 2^0 \cdot 0 = 8$ for the red-dashed branch with one conversion error in b_3. $b_{3r} = b_2$ counters a range of errors prior

to the redundancy bit. The resulting D_{out} are the same.

In terms of circuit-level implementation, the redundancy is accomplished by placing a capacitor C_r in the sDAC. Seeing from the actual implementation shown in Fig. 2.8 (c), 4 out of $13C_u$ from the C_e are used as C_r. The ADC digital output (D_{out}) of the proposed (10+1)-bit SAR ADC is:

$$D_{out} = D_{mDAC} + D_{sDAC} \tag{2.12}$$

where:

$$D_{mDAC} = 2^9 \cdot b_{10} + 2^8 \cdot b_9 + 2^7 \cdot b_8 + 2^6 \cdot b_7 + 2^5 \cdot b_6 + 2^4 \cdot b_5 \tag{2.13}$$

and

$$D_{sDAC} = 2^3 \cdot b_4 + 2^3 \cdot (b_3 - 0.5) + 2^2 \cdot b_2 + 2^1 \cdot b_1 + b_0 \tag{2.14}$$

where b_3 is the redundant bit.

Chapter 3

SSAR and ASAR ADC Chip Photos, Layouts, Simulation and Measurement Results

This chapter presents chip-level implementations of a 7-channel TI SSAR ADC and an improved 7-channel TI ASAR ADC, using the design techniques described in Chapter 2. The ASAR ADC simulation results and the SSAR ADC chip measurement results will be shown. The extensive simulations before chip tape-out provide the designer an insight into how well the chip will perform, and the chip prototype measurements further verify the design concept.

3.1 SSAR and ASAR ADC Chip-Level Implementations

Fig. 3.1 shows the chip photo of the 7-channel TI SSAR ADC that was implemented in 22 nm FD-SOI CMOS. A single SSAR sub-ADC core occupies a chip area of 280 um×60 um, whose layout is drawn beside the chip photo. In the design layout, crucial components, i.e., comparator, SCL, and differential CDAC are marked. The layout of the differential CDAC incorporates the so-called common-centroid technique for fabricating an array of matched capacitors [49].

Like the SSAR ADC, seven ASAR sub-ADC cores are time-interleaved into a 7-channel TI ASAR ADC. Fig. 3.2 illustrates the complete 7-channel TI ASAR

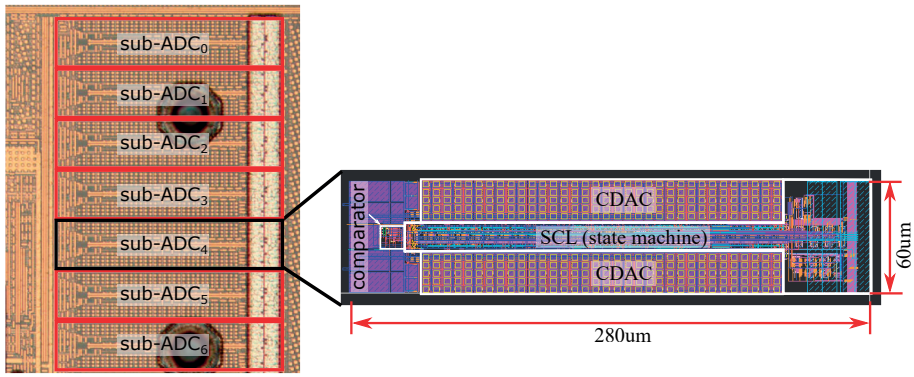

Figure 3.1: Chip photo of the 7-channel TI SSAR ADC fabricated in 22 nm FD-SOI CMOS, and its SSAR sub-ADC core layout.

ADC chip layout in 22 nm FD-SOI CMOS, which occupies a total chip area of 495 um×448 um. The chip layout includes the surrounding circuits: two Low-Dropout Regulator (LDO) regulate the external supply voltage and provide analog (*vdda*) and digital (*vddd*) supply voltages to the ASAR sub-ADC cores; a V_{ref} generator provides plus, minus, and common-mode reference voltages for capacitors in CDAC; an input buffer to buffer the analog input signal; and lastly, a common S/H samples the buffered analog input signal and distributes it to each of the ASAR sub-ADC cores in a time-interleaved fashion.

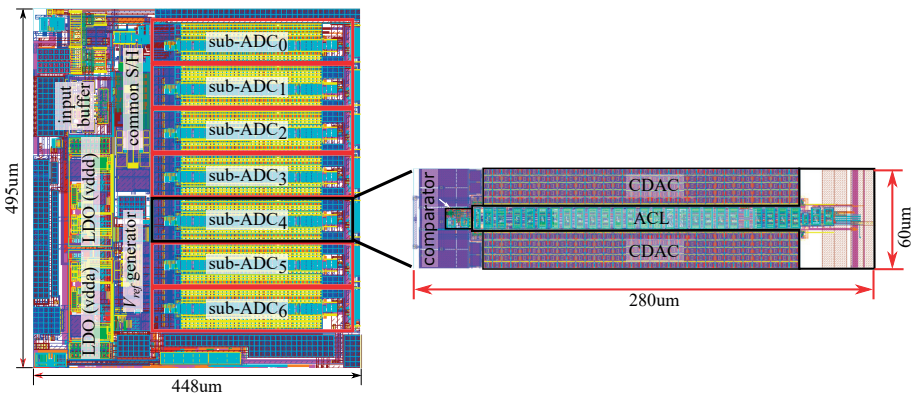

Figure 3.2: A 7-channel TI ASAR ADC layout, designed in 22 nm FD-SOI CMOS.

Regarding the ASAR sub-ADC core, it has a layout similar to the SSAR sub-ADC core shown in Fig. 3.1, which also occupies a similar chip area. Internally, the ACL has similar pin placements as the SCL, which dramatically reduces the layout efforts when connecting it to the comparator and the differential CDAC, which was previously designed and used in the SSAR sub-ADC core.

All the individual building blocks were extensively simulated and tuned for reaching a satisfying ADC performance. Moreover, the PVT variations during chip manufacturing are also considered.

3.2 SSAR ADC Measurement Procedures and Results

In this research, the SSAR ADC chip (designed by Ericsson Research) is measured. The measurement procedure and the measurement results are presented.

The measurement test-bench is illustrated in Fig. 3.3, where a SAR ADC chip [Design Under Test (DUT)] is placed in the middle and tested by lab equipment. Among the lab equipment, two signal generators are used. One is for high-speed clock signal generation, and the other one is for input signal generation. Multiple power sources provide various DC voltages to the ADC internal components, namely, an on-chip Programmable-Gain Amplifier (PGA) and two LDOs (not shown in the chip photo in Fig. 3.1). The analog input signal to be measured passes through a Low-Pass Filter (LPF) then fed to the ADC chip. The LPF limits the input signal bandwidth and avoids any high-frequency interference originating from the signal source.

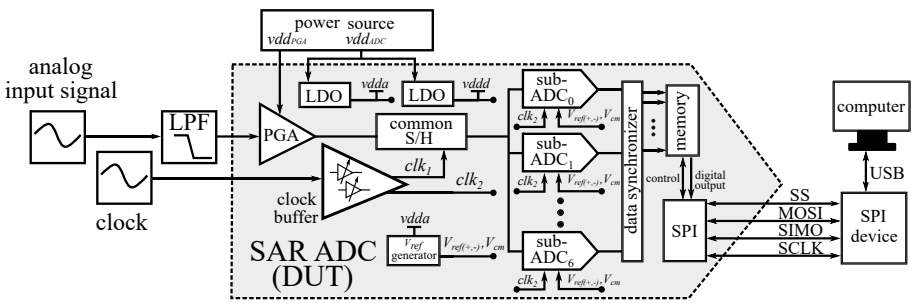

Figure 3.3: The SSAR ADC (DUT) chip measurement test-bench.

Inside the chip, the bandwidth-limited analog input signal is amplified by the PGA and sampled by the common S/H at clk_1, then distributed to the seven SSAR sub-ADC cores clocked by clk_2. Thus, the time delay between clk_1 and clk_2 is critical. Without carefully aligning the two clocks, a slewing signal can be sampled by the SSAR sub-ADC cores, in consequence, degrades the ADC performance. Therefore, the first step in measurement procedures is to sweep the relative delay between clk_1 and clk_2 by changing adjustable delay lines in the clock buffer until reaching a maximum ADC performance.

At the chip output side, a data synchronizer is used to receive and reassemble each of the ADC digital outputs into a long word length at slow speed and then store them in on-chip memory. An external Serial Peripheral Interface (SPI) device communicates with the on-chip SPI module to sequentially read out the ADC digital values that have been stored in the on-chip memory. The collected ADC digital output is further post-processed by an appropriate computer software, such as MATLAB.

A single SSAR sub-ADC core performance is evaluated by examining its 11 output bits, in which one redundant bit is added. The measured ADC output spectrum, with a 95.7 MHz input sine signal sampled at f_s=200 MHz, is plotted in Fig. 3.4. The resulting maximum SNDR is 48.7 dB, by tuning the on-chip calibration capacitors and using the aforementioned off-chip DAC imbalance estimation and calibration methods. Still, third and fifth-order harmonic tones are visible.

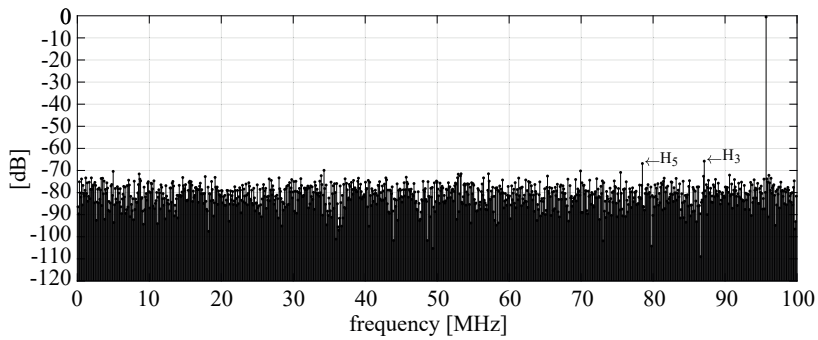

Figure 3.4: Measured ADC output spectrum of a single sub-ADC core running at f_s=200 MHz , with 95.7 MHz input frequency.

Fig. 3.5 (a) shows the SNDR and SFDR of a single SSAR sub-ADC core, with input signal frequency swept up to 191.4 MHz and f_s=200 MHz. It shows that the SNDR is almost constant at approximately 48 dB, and the SFDR is above 60 dB.

The seven sub-ADC core output results are combined, post-processed and analyzed, reflecting the 7-channel TI SSAR ADC performance. The measurement results are shown in Fig. 3.5 (b), where the input signal frequency is swept from a low frequency to Nyquist frequency (735 MHz), with an external sampling frequency for 7-channel TI SSAR ADC of 1.47 GHz. Thus, each sub-ADC core is sampled at 210 MHz.

It could be observed that the SNDR and SFDR in the TI SSAR ADC shown in Fig. 3.5 (b) is slightly lower than its single SSAR sub-ADC core performance

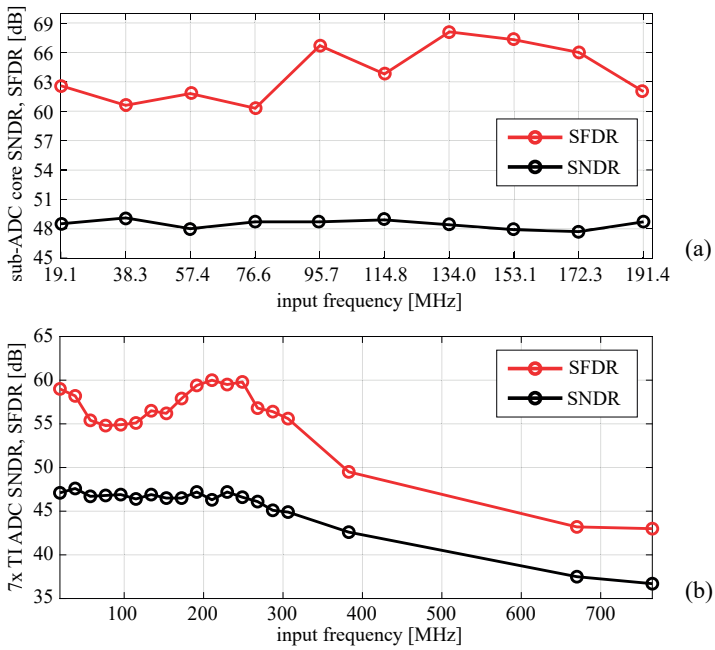

Figure 3.5: Measured SNDR and SFDR versus input signal frequency sweep, where (a) shows a single SSAR sub-ADC core performance, with f_{in} up to 191.4 MHz; (b) shows the 7-channel TI SSAR ADC performance, with f_{in} up to Nyquist frequency of 735 MHz.

shown in Fig. 3.5 (a) within the same f_{in} range. In a fabricated chip, the sub-ADC cores are not identical, which introduces gain mismatches. It introduces harmonic distortion tones to the ADC output spectrum, which are hard to be entirely removed by the post-processor and result in performance degradation.

Fig. 3.5 (b) also indicates that the SNDR degrades to below 45 dB with an input frequency beyond 300 MHz, a frequency much lower than the Nyquist frequency. One reason for such a narrow input signal bandwidth is the weak amplifier used in the common S/H, whose linearity is degraded at a high input frequency. In the modified design (TI ASAR ADC), the S/H is driven by a separate supply voltage that can be individually optimized. The input bandwidth in S/H can be further extended by slightly increase its supply voltage.

3.3 SSAR ADC Power Consumption

The simulated and measured SSAR sub-ADC core power consumption is listed in Table 3.1. The second column in the table shows the power consumption from the simulation. It includes the average power consumption of global blocks such

Table 3.1: Single SSAR sub-ADC core power consumption from the simulation and measurement, and the simulation-adjusted power consumption in the last column.

component	simulation		measurement	simulation-adj.
	power (uW)	% of total	power (uW)	power (uW)
clock buffer	642	18%	3189	**798**
common S/H	845	24%		**1050**
control logic	1006	29%		**1250**
V_{ref} generator	234	7%	543	**291**
comparator	584	17%		**725**
CDAC	0.002	0%	-	-
other	184	5%	611	**229**
total	3495	100%	4343	**4343**

as the common S/H shared by seven sub-ADC cores, and the power consumption of SSAR sub-ADC core internal blocks such as clock buffer, SSAR control logic, V_{ref} generator, comparator, CDAC, and other un-categorized blocks. The third column shows the percentage of the total sub-ADC core power consumption regarding each component.

The fourth column shows the measured ADC power consumption. Notice that the power consumption of each group of components is combined. These components operate closely related to each other and can not be fully separated. In other words, it is not possible to directly measure the current and voltage of chip internal components. The power consumption is estimated indirectly by toggling the SSAR sub-ADC core individual blocks' enable signals and keep track of the differences in current drawn from the external power source. The differences represent how much power is consumed when a set of blocks become active. For example, the clock buffer, the common S/H, and the control logic are all started when enabled, drawing 3189 uW power compared with the case when disabled.

The last column, called *simulation-adjusted power*, is an adjusted power consumption by multiplying the total measured power consumption (4343 uW) with the percentage showing in column three. It reveals an estimation of component-wise power consumption. It can be seen that the common S/H and the SSAR control logic occupy almost half of the total power consumption of a sub-ADC core. The CDAC consumes almost no average power benefitting from the MCS CDAC switching scheme, and it is not feasible to measure such tiny power differences accurately.

3.4 ASAR ADC Simulation Results

In this section, the ASAR ADC simulation results are shown. Specifically, the sub-ADC core post-layout simulations compared to the schematic-level simulations are presented. A non-ideality effect introduced by layout is the increased parasitic capacitance in the capacitor array, which causes the bridge attenuation r deviating from a designed value thus impairs the ADC performance.

Recall that an extra capacitance C'_e=9C_u is required for maintaining a predefined r between the sDAC and the mDAC, as explained in Section 2.5.1. However, due to increased sDAC parasitic capacitance, the C'_e may not be accurate anymore. The C'_e can be coarsely tuned on-chip by switching in or out several unit capacitances. For achieving a maximum SNDR, a post-processor, which is currently implemented in the MATLAB, further applies a gain to the sDAC bit weights and swept. An optimized r of sDAC and mDAC bit weights is achieved when the SNDR is maximum.

Fig. 3.6 shows the SNDR and SFDR of the schematic-level and post-layout simulation results, with r swept from 0.6 to 1.4. The post-layout simulation result shows a maximum SNDR of 53.5 dB at $r = 0.95$. It is slightly smaller than $r = 1$ in the schematic-level simulation, at which a maximum SNDR of 53.2 dB is achieved. The unit gain means no adjustment to the sDAC bit weights is required in the post-processing.

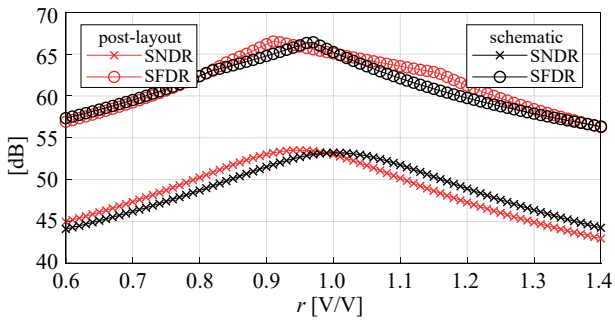

Figure 3.6: Single ASAR sub-ADC core post-layout vs. schematic-level simulations, with gain swept between sDAC and mDAC bit weights, for a maximum SNDR.

The ADC output spectra from the previous simulations are plotted in Fig. 3.7, with an optimized r applied in the post-processor. Note that the two spectra are similar in terms of their noise floor and signal peak but differ in the DC bin. The ADC post-layout output spectrum shows a higher DC offset than from the schematic-level simulation. Such DC offset is usually not included in the SNDR

calculation, resulting in similar SDNRs from the two simulations.

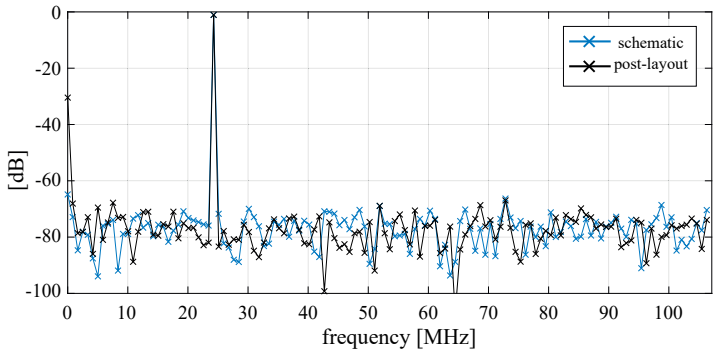

Figure 3.7: ADC output spectra for schematic and post-layout simulation results at the maximum SNDR.

Before sending the chip for fabrication, the post-layout simulation of the full chip design is usually performed, providing the designer an opportunity to estimate the fabricated chip's performance and paving the way to success. However, it is not possible without extensive simulation time and computing resources, especially in large designs. In this work, the complete 10-bit 7-channel TI ASAR ADC design is simulated at schematic-level in five process corners, with thermal noise enabled in the simulator, and these simulation results are plotted in Fig. 3.8. The process corner models are described by two letters, referring to the corner model of NMOS transistors and PMOS transistors. For example, tt means typical PMOS transistors and typical NMOS transistors, which is a normal operational condition; ss means all the NMOS and the PMOS transistors are slow, and ff means all the NMOS and the PMOS transistors are fast.

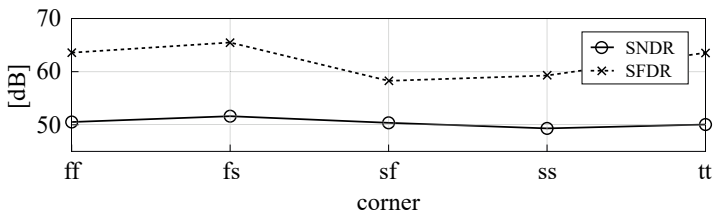

Figure 3.8: SNDR and SFDR of the 10-bit 7-channel TI ASAR ADC, simulated in five process corners.

In all these simulations, the input amplitude is full-scale voltage, and the input frequency is 211 MHz. The TI ASAR ADC is sampled at 2 GHz, and the tunable parameters are carefully selected, i.e., the clock delay between the common S/H and the sub-ADC cores is properly chosen, and the pulse width of the comparator clock generated from ACL is optimized. It can be seen in Fig. 3.8,

Table 3.2: Simulated power consumption in 10-bit ASAR and SSAR sub-ADC cores.

	10-bit ASAR ADC power (uW)			10-bit SSAR ADC power (uW)	
f_s	300MHz	390MHz	500MHz	300MHz	390MHz
comparator	897	1010	1078	877	974
digital	945	1181	1352	915	1143
-unit cells	536	664	751	609	763
-clock gen.	410	517	601	-	-
-ring count.	-	-	-	306	380
clock buffer	78	96	117	606	780
total	**1920**	**2287**	**2547**	**2398**	**2897**

that the SNDR is approximately 50 dB in all the corners, and the SFDR is approximately 60 dB.

The SNDR of TI ASAR ADC (shown in Fig. 3.8) is lower than the single ASAR sub-ADC core (shown in Fig. 3.6). Further analysis reveals that the degraded performance is caused by increased thermal noise in the global blocks such as the common S/H and the input buffer. These two blocks will be optimized in future designs.

3.5 ASAR ADC Power Consumption

Since the ASAR and SSAR sub-ADC core has similar building blocks and architectures, their key component power consumptions are very similar when running at the same f_s. Table 3.2 lists the power consumption breakdown of main components in the 10-bit ASAR and SSAR sub-ADC core, sampled at f_s of 300 MHz and 390 MHz. Besides, the ASAR sub-ADC core is sampled at an additional sampling frequency f_s=500 MHz, and its power consumption is included as well. However, this frequency becomes too high for the SSAR ADC to function correctly.

As seen from Table 3.2, the clock buffer in the SSAR sub-ADC core consumes almost eight times higher power than the same clock buffer in the ASAR sub-ADC core. It is because a multi-GHz external clock needs to be buffered in the SSAR sub-ADC core, while a low duty cycle external sampling signal with a frequency in hundreds of MHz is buffered in the ASAR sub-ADC core.

3.6 Conclusion

In this chapter, the SAR ADC chip implementation, simulation, and measurement results are shown. Both the SSAR and ASAR ADC have 7-channel time-interleaved architecture and were implemented in 22 nm FD-SOI CMOS.

A single SSAR sub-ADC core was measured, showing an SNDR of 48 dB with an input frequency up to the sampling frequency of 200 MHz. Seven identical SSAR sub-ADC cores are time-interleaved to a 7-channel TI SSAR ADC, consuming a total power of 30.1 mW. This total power includes the seven SSAR sub-ADC cores, their surrounding biasing blocks, and a common S/H. On average, each sub-ADC core, together with the necessary surrounding blocks, consumes 4.3 mW power and results in a FoM_s of 152 dB.

The ASAR ADC was simulated using the circuit simulator Spectre in Cadence (www.cadence.com), and the results are analyzed. The post-processor implemented in MATLAB allows a maximum ADC performance to be achieved by adjusting the bridge attenuation r of sDAC and mDAC in fine steps. The ASAR sub-ADC core is simulated both in schematic-level and post-layout, resulting in an SNDR of 53.2 dB, and 53.5 dB respectively. In a higher hierarchy level, the 7-channel TI ASAR ADC was simulated across five process corners, resulting in an SNDR of approximately 50 dB. Compared with a single ASAR sub-ADC core, the 7-channel TI ASAR ADC exhibits a decreased performance, partially due to thermal noise introduced by the input buffer and the common S/H.

Regarding the circuit design, the control logic in the SSAR ADC is based on pure-digital standard-cell architecture, which scales well with the future sub-micrometer CMOS technology node. However, the SSAR ADC is less power-efficient since the control logic and the comparator are clocked by a high-speed external clock signal, which needs to be adequately buffered by a power-hungry clock buffer in a practical ADC chip design. In this particular design, such a clock buffer consumes approximately 25% of the total power.

It shows that an ASAR ADC is more power-efficient than a similar SSAR ADC. The ASAR ADC is clocked by an external sampling signal with short pulse-widths and a much-reduced frequency, compared with the high-speed external clock in the SSAR ADC. These sampling pulses synchronize the start of each sample conversion and trigger the sampling of the analog input signal. The simulation results show that a clock buffer in the ASAR ADC consumes up to eight times less power than an identical clock buffer in the SSAR ADC.

Chapter 4

High-Speed $\Delta\Sigma$ ADC

4.1 Introduction

The $\Delta\Sigma$ ADC is categorized as an oversampled ADC, which incorporates DSM to convert an analog input signal to a fast varying digital representation. For achieving a similar input bandwidth compared with the Nyquist-rate ADC, the $\Delta\Sigma$ ADC typically uses a significantly higher sampling rate. An important term: OSR defines the ratio between the Nyquist rate and the signal bandwidth. The $\Delta\Sigma$ ADC has the potential to achieve a high resolution by sampling the comparator at a very high rate to distribute the noise power injected into the sampled signal to a wider bandwidth, resulting in an in-band noise becomes a fraction of the total noise.

A simple DSM may only incorporate one bit to represent the analog signal but can still reach an ADC resolution up to 16-bit. The single-bit DSM was studied date back to 1996 by Aziz et al. [50]. The single-bit DSM is intrinsic linear since the quantizer in DSM can be designed merely using a 2-level comparator. The feedback circuit is also linear since the multi-bit DAC is avoided. The feedback DAC output is either a plus or a minus reference voltage, which will not deteriorate the overall system resolution. One drawback of the single bit architecture is that it usually necessitates much higher OSR than the multi-bit equivalent for achieving a similar SQNR.

The DSM usually incorporates an LF, which provides some noise filtering to further reduce in-band noise. The LF can be constructed by a chain of integrators, whose number determines the order of LF. Its purpose is to suppress the in-band noise but leave the signal unchanged. It "pushes" the in-band noise to

high frequencies, effectively increases in-band ADC resolution.

The signal injected into the LF is the difference between the input and the quantized output. By using a multi-bit quantizer and DAC, the input voltages to integrators are reduced. The linearity of the feedback DAC affects the DSM accuracy as the non-linearities of the outer-most DAC can be modeled as an additional input to the ADC without being shaped by the LF. Therefore, estimation and calibration methods are important to improve the DAC linearity and the ADC resolution.

Above all, a high-performance DSM usually incorporates a high-order multi-bit architecture. A high-order DSM efficiently shapes the quantization noise, which shows a higher suppression on the in-band noise and a higher amplification on the out-of-band noise. However, high-order DSM may also experience stability issues.

Furthermore, Continuous-Time (CT) DSM architecture is implemented in the high-speed design. The CT DSM generally benefits from two aspects compared with its Discrete-Time (DT) counterpart. First, CT DSM has an inherent anti-aliasing function. It does not require a dedicated anti-aliasing filter that is usually required in a discrete-time DSM. Second, the CT DSM is, in general, faster than the DT DSM. The components in the LF are continuous-time integrators such as a *gm*-C integrator or an active-RC integrator, whose design details will be explained in the following sections.

For achieving a large input bandwidth, the CT DSM could be sampled at a high sampling rate. A $\Delta\Sigma$ ADC design previously presented by Bolatkale et al. in [26] presented that as large as 125 MHz input bandwidth can be achieved when sampled at 4 GHz. For reaching such a large input bandwidth, inevitably, the OSR becomes low compared with conventional DSMs, which incorporates a large OSR, requiring aggressive noise shaping.

In this chapter, a high-speed $\Delta\Sigma$ ADC design is proposed. The target applications are in high-performance communication systems, such as base station devices. The following sections focus on a high-speed single-loop $\Delta\Sigma$ ADC design, study the ADC operation principles and present component-level implementations.

The behavior model construction will be presented in Section 4.2.1. Various $\Delta\Sigma$ ADC architectures will be explained, and the synthesize of DT DSM coefficients will be addressed. Then, in Section 4.3, the synthesized DT DSM model is transformed into a CT DSM equivalent, with a set of CT coefficients calculated using time-invariant transformation from the DT coefficients. The Excess Loop

Delay (ELD) will be addressed, which is an important consideration during the transformation of the coefficients from DT to CT. Furthermore, an additional fast feedback path is added. A new set of coefficients are calculated so that an ELD larger than one clock cycle between the quantizer and feedback DACs can be compensated.

In the last section, the CT DSM model will be mapped into a component-level design. The $\Delta\Sigma$ ADC design, implemented in 28 nm FD-SOI CMOS, will be explained. The ADC is sampled at a target sampling frequency of 5 GHz, achieves a maximum signal bandwidth of 250 MHz. The component-level design incorporates inverter-based integrators in its loop filter and CML in the digital blocks to increase the digital signal speed.

4.2 Model Construction in MATLAB

4.2.1 $\Delta\Sigma$ ADC Model

The first step in constructing a $\Delta\Sigma$ ADC is selecting an appropriate discrete-time architecture. Four types of basic architectures can be chosen for a high-order modulator, as discussed extensively in [11]. There are two feedback architectures: Cascade of Integrators with Distributed Feedback (CIFB) and Cascade of Resonators with Feedback (CRFB). Each has an LF containing a cascade of N delaying or delaying-free integrators (where N is the order of the LF). Similarly, two feed-forward architectures contain the chain of integrators: Cascade of Integrators with Feed-Forward Summation (CIFF) and Cascade of Resonators with Feed-Forward Summation (CRFF). Each has a summation node that sums and amplifies the feed-forward signals from the integrator outputs and the input signal.

The aforementioned four $\Delta\Sigma$ ADC architectures have been illustrated in Fig. 4.1, with a 4^{th} order LF shown for illustration purposes. Fig. 4.1(a) illustrates the CIFB and CRFB architectures, and Fig. 4.1(b) illustrates the CIFF and CRFF architectures.

The quantizer is a 4-bit flash ADC, with 2^4-1 comparators converting the analog signal to digital codes at a fast pace, then drive the feedback DACs. For the component matching perspective, the feedback DAC is implemented with unit cell design, which means identical DAC unit cells are used several times. Again, any mismatch in the outer-most DAC will inject into the system in parallel with the input. These mismatches result in distortions, which requires a calibration

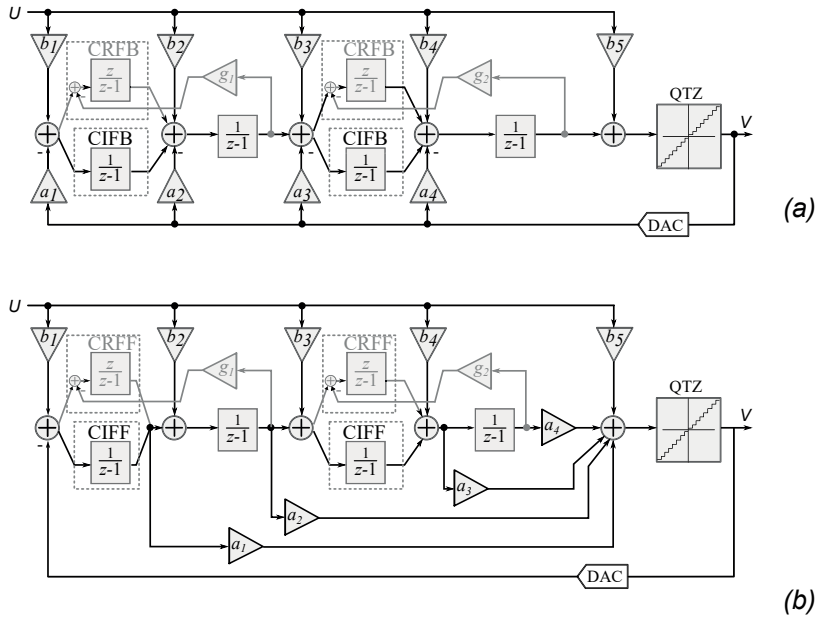

Figure 4.1: $\Delta\Sigma$ ADC implemented with (a) CIFB and CRFB architectures and (b) CIFF and CRFF architecture.

module whose details will be presented in Section 4.5.

In the CIFB architecture, a chain of delaying integrators ($\frac{1}{z-1}$) is the core. The CRFB architecture is similar to the CIFB architecture but has delaying-free integrators $\frac{z}{z-1}$ as its first and third integrators. A pair of delaying and delaying-free integrators, together with local feedback path (g_1 and g_2) across two integrators, form a resonator. The potentially unstable resonators are placed inside a stable feedback system, which avoids local oscillation and optimizes zeros of the noise transfer function $H(z)$.

The feed-forward architecture reduces the feedback paths to one, only requiring a summation node that handles all the feed-forward paths. Compared with CIFB and CRFB architectures, the outer-most feedback path is kept, but the rest of the feedback paths are removed. In the CIFF architecture, all the integrator outputs are scaled by a_1 to a_4 and feed-forward to a summation node. In the CRFF architecture, local resonators are formed by every two integrators in LF.

For high-speed operation and low internal signal swings, the feed-forward architectures are preferable. The presented $\Delta\Sigma$ ADC uses CRFF architecture and incorporates a resonator across the second and third integrators.

4.2.2 DT Coefficients

A method of synthesizing a DT architecture can be performed in MATLAB using the Delta-Sigma toolbox [51]. It is a tool for synthesizing the DT coefficients a, b, and g and an NTF from given parameters such as LF order, Out-of-Band Gain (OBG), OSR, and whether the NTF zeros are optimized. There are trade-offs between these parameters: a higher-order LF provides aggressive noise shaping, requiring a long chain of integrators which increases delay and harms loop stability; a higher OSR results in a lower in-band noise, but in need of a proportionally higher sampling frequency; the OBG determines the maximum out-of-band gain for noise shaping, but still, a too high OBG may lead to stability issues.

The low OSR $\Delta\Sigma$ ADC requires an aggressive noise shaping to reach a certain ADC resolution. The chosen parameters are 4^{th} order, OSR of 10, OBG of 3.5, and optimized for at least one zero at band-center. The pole-zero plot is graphically illustrated in Fig. 4.2, where the zeros are separated due to zero optimization, and poles are within the unit-circle. The NTF is:

$$\text{NTF}= \frac{(z-1)^2(z^2-1.93z+1)}{(z^2-0.7923z+0.176)(z^2-0.8354z+0.4464)} \tag{4.1}$$

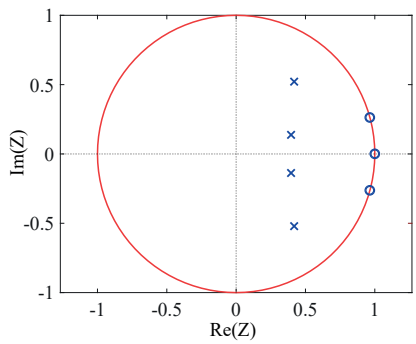

Figure 4.2: Pole and zero plot of an NTF with parameters: 4^{th} order LF, OSR=10, and OBG=3.5.

This NTF is mapped into the DT CRFF architecture, where a set of DT coefficients is generated. During the mapping from the transfer function to real implementation, a high-resolution internal quantizer will potentially result in a high-accuracy ADC since each 1-bit increase in resolution results in a 6 dB accuracy improvement. A drawback of the multi-bit DAC is their linearity issues, which require sufficient linearity in the component design in components.

A DT CRFF DSM is constructed in the Simulink model in MATLAB using the synthesized coefficients. The simulation results of the Simulink model and

the calculations from a mathematical model show marginal differences. In the next section, DT to CT transformation will be explained. The CT architecture is transformed from a DT equivalent, but with considerations of ELD. The calculations of ELD compensation will be covered in Section 4.3.3.

4.3 DT to CT Transformation

4.3.1 Impulse-Invariant Transformation

Conventionally, the architecture is synthesized in DT. It means that a S/H circuit is placed before the circuit to provide sampled input to the loop filter. The internal components are discrete-time circuits, such as switched capacitor integrator. One step further, CT architecture is another alternative. It has an inherent anti-aliasing feature and handles the continuous varying signal. As a result, circuit speed is improved since the slow-slewing switch-capacitor circuits are avoided.

Prior researches addressed constructing an equivalent CT model transformed from a DT counterpart, such as [52] and [53]. Moreover, in [54], an intuitive way of calculating equivalent CT coefficients from DT was proposed.

The CT model is transformed from an equivalent DT model to be used in the high-speed $\Delta\Sigma$ ADC. It has been implemented at component-level and fabricated in a chip. The DT to CT conversion is calculated based on impulse-invariant transformation. At the quantizer sampling instant, the impulse response seen at the quantizer input is identical between CT and DT models.

In the CT model, feedback DAC pulse shapes determine the integration values within one clock period. Appendix A presents the detailed calculations of DT to CT transformation. In short, the goal is to match the LF output voltages in CT DSM with the DT DSM at the sampling instant, when a DAC pulse feedback either a Return-to-Zero (RZ) or a Non-Return-to-Zero (NRZ) pulse to the Linear Time-Invariant (LTI) system. Thus, in the feedback loop, the signal settles within one clock cycle, and the transformed CT architecture behaves identically to the DT counterpart.

Besides, when the NTF zeros are optimized, the original DT model has resonators across the first two and the last two integrators. It is also possible to form the resonator across the middle two integrators to reduce the load to the last integrator by re-calculating the coefficients.

4.3.2 DAC Output Pulse Shape

In the DT to CT transformation, the DAC feedback pulse shape is another consideration. NRZ DAC feedback pulses are commonly used, but its performance is limited by the inter-symbol-interference (ISI) from the switching events. Another alternative is to use RZ DAC feedback pulses, which benefits from reducing ISI commonly seen from an NRZ DAC. However, using RZ pulse will increase clock jitter sensitivity [55], although the unequal DAC edge rise and fall times are avoided by implementing differential architecture [56].

The NRZ and RZ DAC feedback pulses are illustrated in Fig. 4.3. The parameters α and β represent the start and stop time of the DAC pulse, respectively, related to T. For example, in an NRZ feedback pulse, α=0 and β=1 when ELD=0 and α=0.5 and β=1.5 when ELD=0.5T.

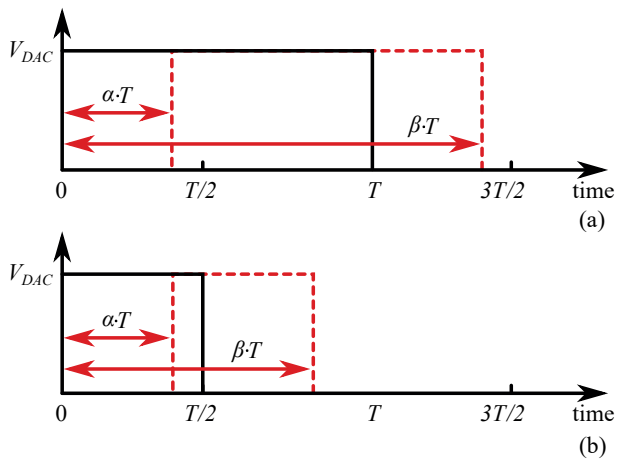

Figure 4.3: The DAC output pulses vs. T, where (a) shows an NRZ DAC and (b) shows an RZ DAC pulse.

4.3.3 ELD Compensation

The ELD measures the time difference between the quantizer output instant and the next LF output becoming available, which is an important consideration in calculating coefficients in the CT DSM. Usually, an ELD should not be larger than one clock cycle for correct transformation between DT to CT model. However, under a high clocking rate, the feedback signal may not settle in time. In such a scenario, the longest ELD from the sampling instant to the next analog voltage appearing at the quantizer input can be larger than one clock cycle.

The larger than one clock cycle ELD is partially due to the relatively slow quant-

izer. The propagation delay from the sampling instant to a settled feedback DAC output could be large. In the previous work presented by Balagopal and Saxena, a 1.5 T ELD can be successfully compensated by creating a fast-loop around the last integrator using a sample-and-hold [57]. Without this additional fast feedback loop, the DT to CT transformation becomes incorrect due to an unmatched sample in the CT impulse response.

The ELD compensation is studied by examining the proposed high-speed $\Delta\Sigma$ ADC architecture in Fig. 4.4. It is based on the CRFF architecture, where two additional feedback paths a_{fb} and a_{dly} are introduced for ELD compensation. Based on the calculations in Section A.2.2 in Appendix A, it is clear that a different direct feedback path is required for the CT transfer function matching to the original DT counterpart.

Instead of adding an analog fast-feedback path around the last integrator, in the presented $\Delta\Sigma$ ADC, a fast DAC is scaled by a_{fb}, to directly inject the quantized signal back to the summation node. This DAC is not clocked, which outputs an analog voltage immediately when the quantizer completes a conversion. The other DACs are delayed by T, where a typical value $0.5T$ is not sufficient.

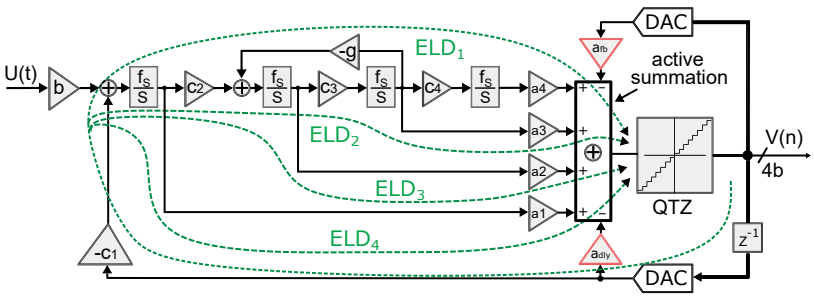

Figure 4.4: Proposed DSM architecture in the Simulink model, with ELD paths shown.

The detailed calculations of DT to CT transformation are presented in the Appendix A, which is based on time-invariant transformation. In Table. 4.1, the converted CT coefficients are listed, and the original DT coefficients are presented. The estimated ELD values are based on each component delay simulated at the component-level. In total, four ELD paths need to be considered, where each ELD path is marked with a number. The longest ELD is ELD_1, which has a nominal value of $1.6T$ estimated from the simulation.

Table 4.1: The DT model coefficients from a 4^{th} order LF, 4-bit quantizer and DAC, OSR=10 CRFF architecture, and its equivalent CT model coefficients.

coefficient	DT architecture	CT architecture
a_1	0.9214	2.2162
a_2	1.3808	3.3136
a_3	0.6513	3.9187
a_4	0.2345	4.4927
a_{dly}	-	1.6885
a_{fb}	-	2.3022
b	1	2
c_1	1	2
c_2	1	0.4
c_3	1	0.3
c_4	1	0.3
g	0.0701	0.2336

4.3.4 Dynamic Range Scaling

The CT coefficients calculated in Appendix A using Eq. A.15 and Eq. A.16 are dynamic range scaled to limit the LF internal nodes signal swings. In Table 4.1, the equivalent CT coefficients are scaled by applying coefficients c. The output nodes voltages are simulated under different input signal frequencies to guarantee no over-ranging problem occurs. The scaled CT coefficients are then implemented at component-level, which will be explained in the next section.

4.4 Component-Level Implementation

The synthesized model is further realized at the component-level. A $\Delta\Sigma$ ADC was designed in 28 nm FD-SOI CMOS and fabricated. The ADC input bandwidth is up to 250 MHz, sampled at 5 GHz. The output is first stored in the memory and then read out sequentially at a slower pace for further signal processing.

Designing the high-speed $\Delta\Sigma$ ADC becomes challenging, which requires selecting high-performance components and laying out the circuit carefully. Especially in feed-forward architecture, a high-speed summation node needs to be designed. From the simulation, the designed $\Delta\Sigma$ ADC achieves approximately 80 dB SNDR in 250 MHz signal bandwidth.

4.4.1 LF Design

A complete component-level LF design is shown in Fig. 4.5. The LF is built with a chain of integrators, where the first integrator is an active-RC integrator, and the rest are gm-C integrators. Each of the feedback current-steering DACs generates a current proportional to a 15-bit thermometer code from the quantizer. Note that the DAC_1 and the DAC_{dly} are clocked by a high-speed external clock clk. It is also the sampling signal to the quantizer. Equivalently, one clock cycle delay is added in the feedback loop.

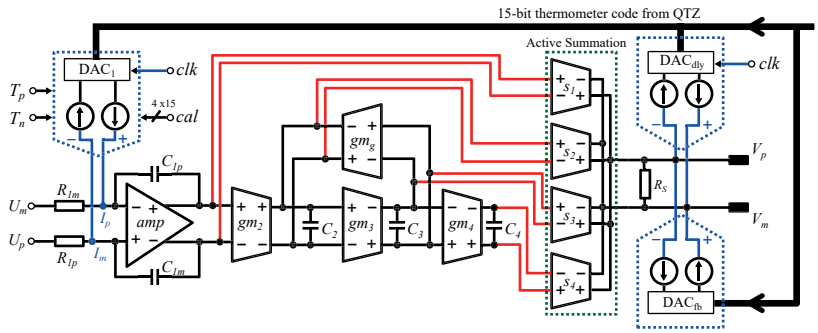

Figure 4.5: LF component-level design, including integrators, an active summation block, and feedback DACs.

4.4.1.1 Integrator Design

Inside the LF shown in Fig. 4.5, active-RC and gm-C integrators are used. The first integrator is an active-RC integrator, which has better linearity and can handle a large input and output signal swing. The amplifier schematic is shown in Fig. 4.6(a), which is based on a single-stage integrator with a local cross-coupled negative load connected to the drains of the NMOS transistor input pair (N_1 and N_2). A large Gain-Bandwidth Product (GBW) is needed for high-speed applications, therefore, it was designed with a DC gain of 53 dB and a GBW of 7.8 GHz. The common-mode voltage of outputs V_p and V_m is detected using two resistors R_1 and R_2.

The following integrators are built based on well-known CMOS inverters [58], which uses inverters as transconductor (gm_1, gm_2 and gm_3) and uses capacitive load for integration. Instead of being used in pure digital circuits, the inverters are biased at a common-mode voltage (V_{cm}) for extended usage in an analog way.

Inverter-based integrator schematic is shown in Fig. 4.6(b). In total, six inverters

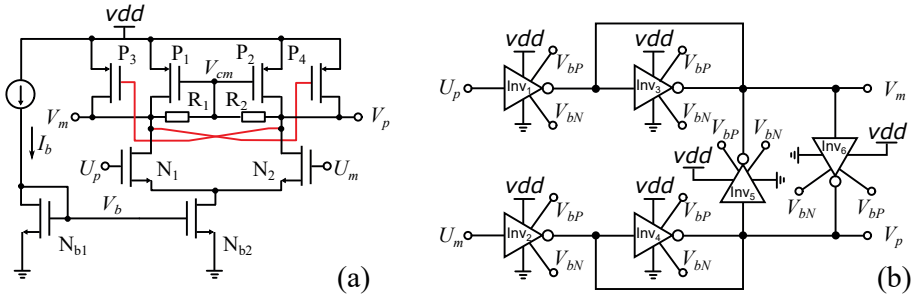

Figure 4.6: Schematic of (a) the amplifier used in the active-RC integrator and (b) the transconductor in the inverter-based integrator.

in three pairs are used, which can be categorized into three functions: Inv_1 and Inv_2 define the transconductance gm of the cell; short connected Inv_3 and Inv_4 set the output common-mode voltage; cross-coupled Inv_5 and Inv_6 are the negative resistance as a load to the gm stage for boosting the gain. Based on the calculations presented in [58], transconductor differential output nodes V_p and V_m behave a high differential resistance and low common-mode resistance. The differential and common-mode resistance are listed in Table 4.2, where the gm_i represents the transconductance of inverter i whose input and output voltages are biased at V_{cm}.

Thanks to the 28 nm FD-SOI CMOS, a biasing voltage directly controls the transistor body biasing voltage. The body biasing in a transistor behaves as an extra gate controlling the threshold voltage V_{th} of transistors. Typically, an NMOS transistor is biased by a positive body-biasing voltage from 0 to 1 V, and a PMOS transistor is biased by a negative body-biasing voltage from 0 to -1 V.

For maximum tunability, the body biasing voltage of NMOS and PMOS transistors are individually tuned. However, in a practical design, the number of tunable points is limited. Currently, for simplicity, all the PMOS transistors share the same body-biasing voltage V_{bP}, and all the NMOS transistors are tuned by V_{bN}.

Fig. 4.7 shows an example where the gm=1 mS and the load capacitance C=1 pF. The integrator crossover frequency, at which the gain is 0 dB, varies at different body-biasing voltage combinations. The body-biasing voltages $V_{bN} = -V_{bP} = 0$ result in a crossover frequency of 110.48 MHz, and $V_{bN} = -V_{bP} = 1V$ results in a crossover frequency of 208.38 MHz. The transistors are properly sized so that at the middle of the body-biasing range $V_{bN} = -V_{bP} = 0.5\,V$, the crossover frequency is close to the nominal calculation value of 159.16 MHz.

Table 4.2: Differential and common-mode load resistance in inverter-based gm cell.

Output node	Differential mode resistance	Common mode resistance
V_p	$\frac{1}{gm_4 - gm_6}$	$\frac{1}{gm_4 + gm_6}$
V_m	$\frac{1}{gm_3 - gm_5}$	$\frac{1}{gm_3 + gm_5}$

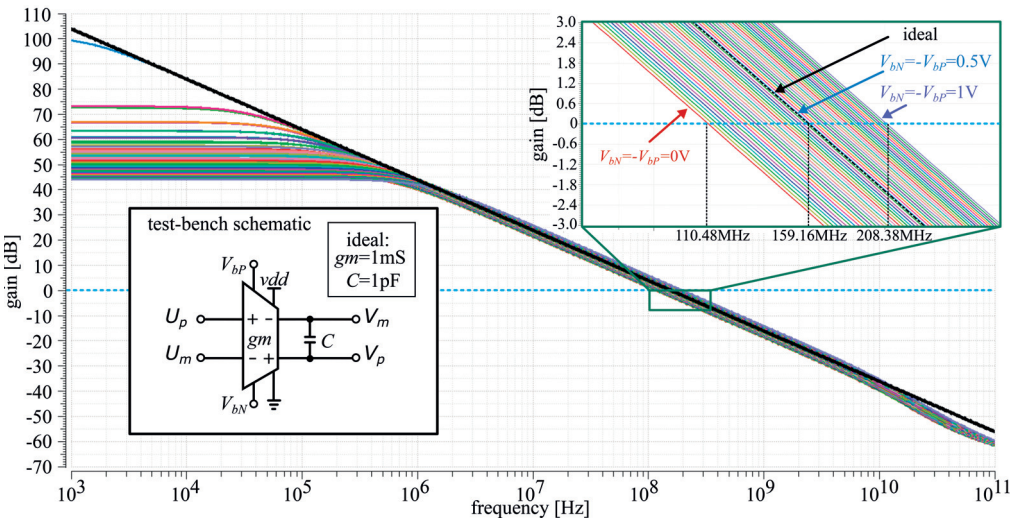

Figure 4.7: Tuning the gm-C integrator using body-biasing, where nominally gm=1 mS and C=1 pF.

4.4.2 Active Summation

In feed-forward architecture, the summation node is one of the critical nodes that need to be appropriately designed. It can be realized by a passive summation method, as explained in [26], where the capacitors are connected between the integrator output nodes and the passive summation nodes at the quantizer input. The parasitic capacitance at the quantizer input, together with the integration capacitance in the last gm-C integrator, can be used to sum the voltage from all the integrator outputs. The passive summation architecture constructed by capacitors is faster but can only achieve less than unity feed-forward coefficients a_1 to a_4 as shown in Fig. 4.1(b), defined by:

$$a_i = \frac{C_{ai}}{C_{total}} \tag{4.2}$$

where C_{ai} is the capacitor for i^{th} feed-forward path, and C_{total} is the total capacitance appear at the summation node. The a_i never exceeds one, which

results in a signal attenuation after the summation.

Another alternative is using active summation, which uses an active summing amplifier in the LF to sum feed-forward voltages. A gain of one or larger can be realized using the active summation, requiring a high-bandwidth amplifier to accomplish it. This is attractive since it could amplify rather than attenuate the feed-forward signals.

Revisit the coefficients shown in Table 4.1, in which the feed-forward paths require coefficients larger than one. These large coefficients are partially due to the limited input and output swing in the integrators. The active summation block implemented in this work is based on *gm-R* architecture, as shown in Fig. 4.5. The cores in s_1 to s_4 are the inverter-based transconductors, similar to those used in the aforementioned integrators.

4.4.3 Quantizer Design

The quantizer is the main decision block in a $\Delta\Sigma$ ADC. The quantizer has a speed requirement since any delay introduced will directly influence the feedback loop delays. A large delay impairs the loop stability if it is beyond the coefficients tuning range.

Flash ADC is fast to convert an analog input signal to a digital output. The architecture of a Flash-based quantizer is similar to Fig. 1.5 (a).

The Flash quantizer output is a thermometer code, similar to a thermometer measuring temperature: a bar rises with increased temperature and falls at a decreased temperature. The digital representation of an analog input voltage is the number of logic ones of the low-weight bits counting from b_0. For example, in a 4-bit quantizer, all zeros in the 15 output bits represent an ADC digital output of 0, and all ones mean a digital output of 15, in decimal representation. The thermometer code is then encoded into binary code by an encoder built with readily available digital standard cells.

4.4.4 Current-Steering Feedback DACs

The feedback DAC is a crucial component that converts the quantized digital outputs back to the analog domain. In the feedback system, negative coefficients are accomplished by subtracting the DAC analog outputs from the desired signals, either current or voltage.

In high-speed operations, current-steering DAC is preferable. The digital codes are converted to an analog current proportional to the digital value, and such feedback current is injected into a selected node in the LF integrator chains.

All the DACs have similar architectures, where each DAC consists of multiple unit cells, and their output currents are superpositioned at the DAC output node, becoming the DAC output current. In the specific architecture presented in this research, the outer-most DAC (DAC1 in Fig. 4.5) is connected to the virtual ground nodes I_p and I_m of the amplifier in the first active-RC integrator. The DAC differential current is subtracted from the differential input current, which is the current flowing through the input resistors R_{1p} and R_{1m} when an input signal is applied. The schematic of the outer-most DAC is shown in Fig. 4.8, which incorporates a 4-bit tuning functionality to each of their internal unit cell for improved linearity.

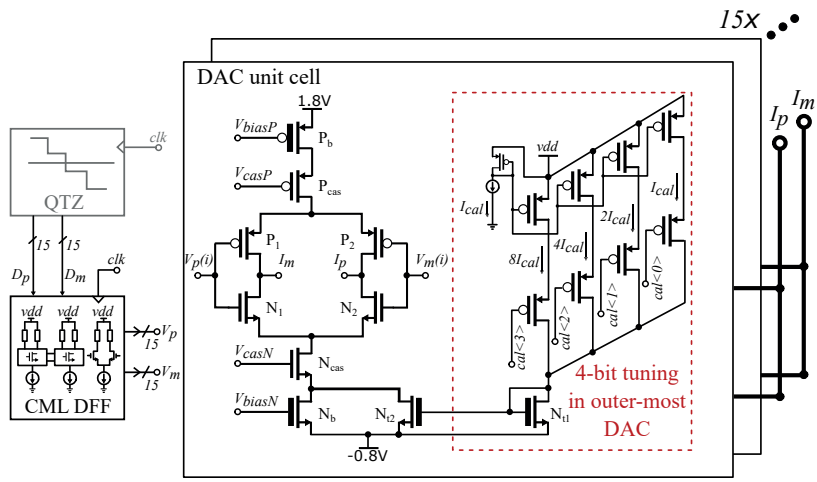

Figure 4.8: Outer-most DAC architecture with 4-bit biasing current tuning.

Note that the supply voltage to the DAC unit cells is much higher than the standard 1 V supply voltage. The technique is similar to [26], where the high supply voltage is 1.8 V, and the low supply voltage is -0.8 V to provide enough headroom for the current source devices to reduce DAC noise [59]. There are cascode transistors P_{cas} and N_{cas} to the current source transistors P_b and N_b, respectively, which improve the biasing current accuracy and reduce the voltage appears on top of the middle four switching transistors. The current source transistors P_b and N_b are thick oxide gate devices to operate at high voltage.

The DAC_{dly} and DAC_1 are clocked at the same clock edge as the quantizer, equivalent to creating one clock cycle delay between the quantizer and DACs. The DAC_{fb}, is the one directly controlled by the quantizer, i.e., whenever a com-

parison is completed, the DAC immediately process the digital output without waiting for a clocking pulse. From Fig. 4.5, it can be seen that the latter two DACs inject currents onto the summation resistor R_s. In such a way, the DAC currents are subtracted from the current from the active summation block. The net current is applied to the summation resistor R_s and becomes LF output voltage ready to be compared by the quantizer.

4.4.5 CML in Quantizer and DAC

The CML circuit is beneficial in high-speed digital circuit designs. In the presented work, the CML circuits have been extensively used in the quantizer and the DAC. Compared with a typical CMOS digital logic that incorporates several NMOS transistors and PMOS transistors, the CML circuits mainly use NMOS transistors with constant bias current. The CML inverters are better than CMOS inverters since it can operate with higher operating frequency at lower supply voltage. It has been studied in [60] based on model simulation results and experiments.

A CML inverter and a CML buffer schematic are shown in Fig. 4.9 (a), where only the NMOS transistor is used as current switching components. The connection between output nodes (V_p and V_m) and drains of input transistors (N_2 and N_1) determines whether the circuit is an inverter or a buffer (shown in gray). The PMOS transistor, which is typically used in the conventional CMOS inverters, are replaced with resistors. The constant bias current flowing in the CML inverter is determined by the tail current source transistor N_3, and the output common-mode voltage is determined by this current and the load resistors R_1 and R_2, with a nominal value of 750 mV under 1 V supply voltage *vdd*.

Fig. 4.9 (b) shows the CML latch schematic. There is a pair of current switching transistors N_5 and N_6 clocked by *clk*, switching the CML latch between the input tracking mode and the latching mode. In the input tracking mode, the circuit is similar to a CML buffer, and the differential outputs V_p and V_m track the differential input value V_p and V_m. Next, the latch mode is activated when the *clk* is high. The V_p and V_m will hold for a duration until the *clk* becomes low again, which controls the current flowing to one of the cross-coupled transistors N_3 and N_4. Furthermore, a small PMOS transistor (P_{rst}) is used to facilitate the reset of the value stored in the CML latch, which conducts during the input tracking mode when the *clk* is low.

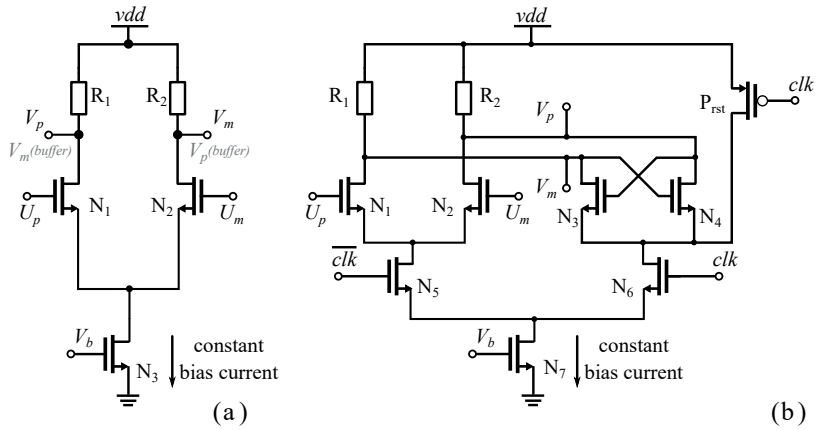

Figure 4.9: Schematic of (a) a CML inverter or a CML buffer, and (b) a CML latch with a PMOS transistor reset switch.

4.5 DAC Unit Cell Mismatches and Tuning

Due to the design complexity and the PVT variations, extensive tunings are required for an optimized DSM performance. There are two main types of tuning methods used in this work: 1) analog bias voltage and current tuning, and 2) digital calibration.

4.5.1 Bias Voltage and Current Tuning

The analog tuning of part of the design was already addressed in the previous sections. For example, the integrators are tuned by altering their body-biasing voltages, which have dedicated pins on the chip connected to different voltage sources externally. Based on the simulation, altering the transistor body-biasing voltages lead to changes to the integrator crossover frequency, resulting in a tuning range of approximately $\pm 30\%$.

The bias current of the CML cells is tuned for reaching a desirable common-mode output voltage to compensate for the resistance variations. Therefore, the current sources in the CML cells can be tuned in a small range to compensate for resistance variation.

Furthermore, bias currents to the feedback DACs are individually tuned. The simulations show that the required output current from the DAC_{dly} is sensitive to the ELD variations, which needs a tuning range of approximately $\pm 30\%$.

4.5.2 Digital Tuning

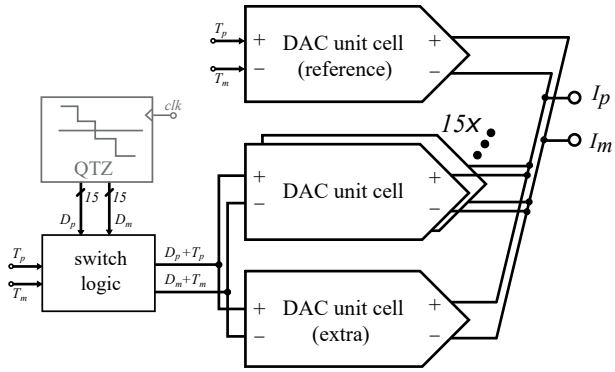

Figure 4.10: DAC conceptual architecture, including 15 DAC unit cells, an extra unit cell, and a reference unit cell.

In addition to the analog tuning, digital tuning is implemented in the outer-most DAC for further DAC linearity adjustments. An extra unit and a reference DAC unit cell are integrated into the outer-most DAC for injecting the test sequence, as shown in 4.10. The reference cell is controlled by a pair of test bits T_p and T_m, while the switching logic recombines the input code to each DAC unit cell. The test bits are routed to one of the DAC unit cells at a time, and the extra cell is switched in to replace the function of the cell under test. As can be seen, the reference cell has its outputs reversely connected to the rest of the unit cells.

Ideally, with all the cells matched, the reference cell output current is entirely canceled out with the DAC unit cell under test. However, if the unit cells are not matched, the current differences between the reference cell and the cell under test are proportional to the mismatches between cells. By using this method, the static DAC unit cell matching can be estimated by cycling the external test bits through all the 15 unit cells. Finally, the optimized compensation currents in each unit cell are found by observing the ADC performance.

4.6 Layout, Simulation, and Measurement Results

The high-speed $\Delta\Sigma$ ADC has been implemented in 28 nm FD-SOI CMOS and fabricated into a chip. The chip layout is presented in Fig. 4.11, occupying a silicon size of 1.5 mm×1.2 mm, including a $\Delta\Sigma$ ADC core of 573 um×340 um. The simulated power consumption breakdown pie chart is shown in the top-right corner in Fig. 4.11, with a total power consumption of 216.1 mW when clocked at 5 GHz.

Besides the ADC core, there is a synthesized SPI module placed in the center of the chip. It has two functions. First, it provides tuning signals to internal analog blocks. Second, it controls the on-chip Random Access Memory (RAM) cells, RAM_1 and RAM_2, for temporarily storing the ADC outputs and sequentially reads out for further post-processing.

Fig. 4.12 plots the 2048-point ADC output spectrum of the component-level simulations in Spectre with and without transient noise. The simulation results using a DT and a CT model with $1.5T$ ELD are overlaid for comparison purposes. The signal frequency is selected close to f_b. It shows that an analog signal up to 250 MHz input frequency can be successfully converted to digital codes, with an SNDR up to 73.1 dB. The transformed CT model almost matches with the original DT model with small SNDR differences. Notice that the thermal noise is included in the simulation, causing the SNDR degrades from 81.4 dB in the DT model and 82.8 dB in the CT model. The thermal noise is comparable to the ADC quantization noise for a balance between performance and power consumption.

The chip microscope view, its bonding diagram, and the Printed Circuit Board (PCB) photo are shown in Fig. 4.13. Note that two internal pads that bonded to the bottom PCB traces are additional supply pads for extra power delivery. The five internal pads on the right sides are used for outputting four ADC digital outputs and one clock signal. The purpose of these pads is to provide an alternative way to directly measure the ADC digital output, possibly by a

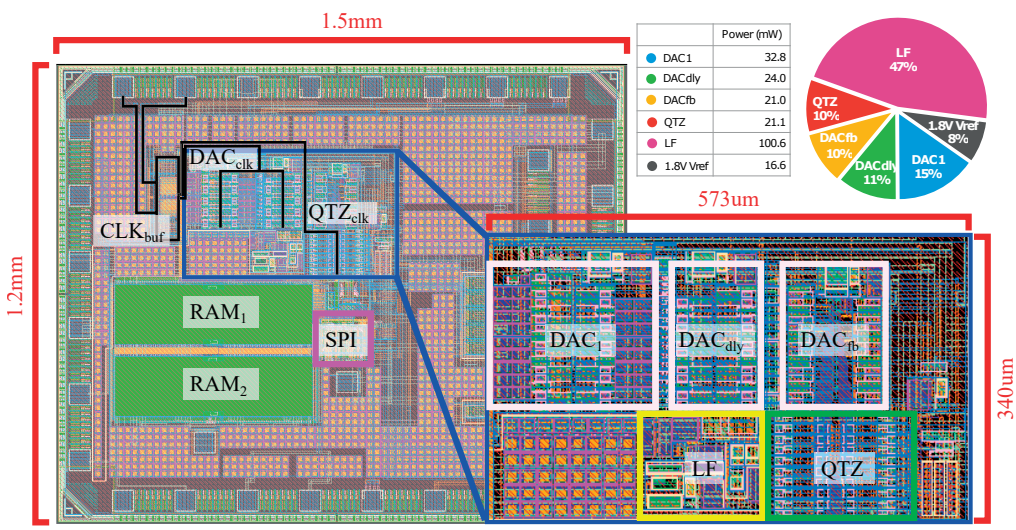

Figure 4.11: Chip layout and simulated power consumption breakdown.

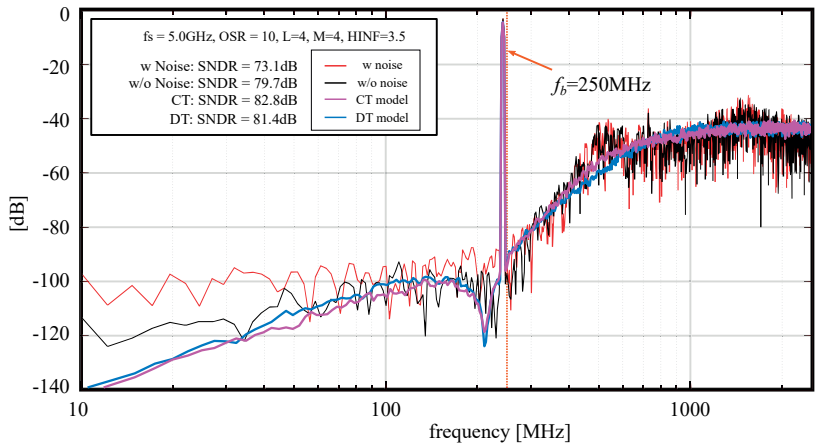

Figure 4.12: The $\Delta\Sigma$ ADC output spectra, including the CT and DT DSM MATLAB model simulations, and with or without transient noise results in component-level simulations.

high-speed logic analyzer without using the SPI module.

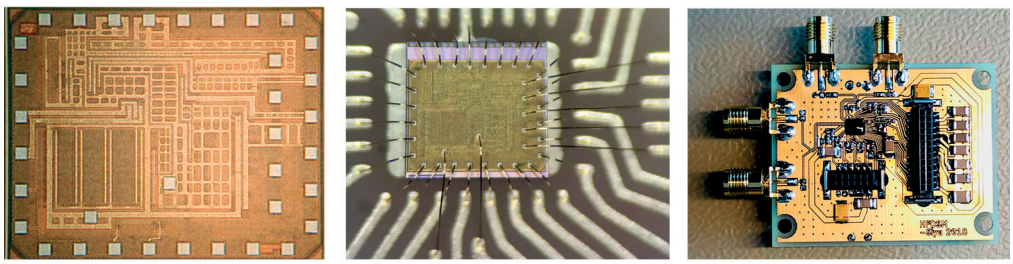

Figure 4.13: Photo of (a) chip, (b) bonded chip, and (c) PCB.

Fig. 4.14 shows a customized PCB for this $\Delta\Sigma$ ADC chip. Its purpose is to provide stable and tunable bias voltages for optimizing the operation points of various on-chip components, such as tuning the aforementioned body bias voltages for the inverter-based integrators and changing reference currents in the feedback DACs.

The $\Delta\Sigma$ ADC chip was measured, showing an unsatisfying SNDR even after extensive tuning, does not fully agree with the simulation results. A potential error is in a MUX that selecting the data from one of the on-chip memories was failed. To overcome the issue, one memory is initially filled with zeros. Then the ADC outputs are able to be extracted from the other memory with a minimum amount of error.

However, the $\Delta\Sigma$ ADC is still difficult to reach a satisfying performance at 5 GHz

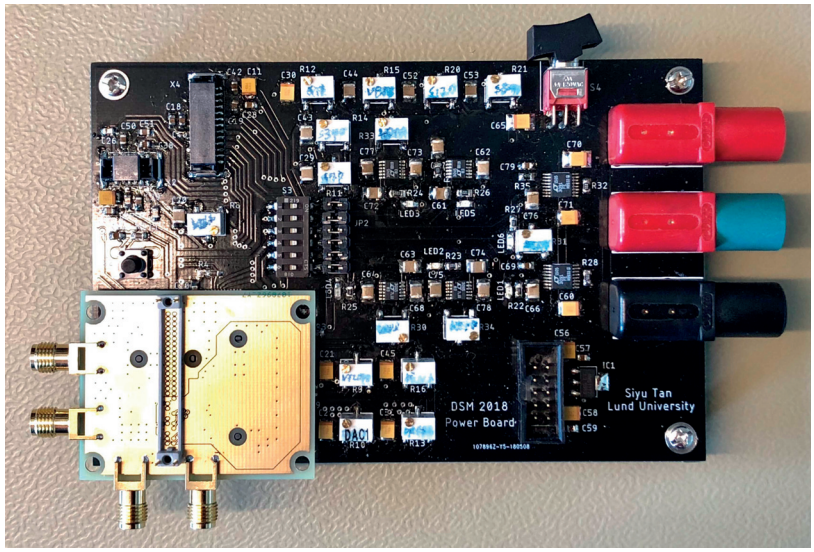

Figure 4.14: A base PCB, providing bias voltages to the ΔΣ ADC chip that is stacked on.

sampling frequency. Thus, the sampling frequency was decreased to 3.3 GHz for stability consideration, and coefficients are carefully tuned. Fig. 4.15 shows the time-domain measured ADC output, with a result of (a) an 11 MHz input signal and (b) a 60 MHz input signal. Notice that there are already random errors causing a significant decrease in the ADC performance.

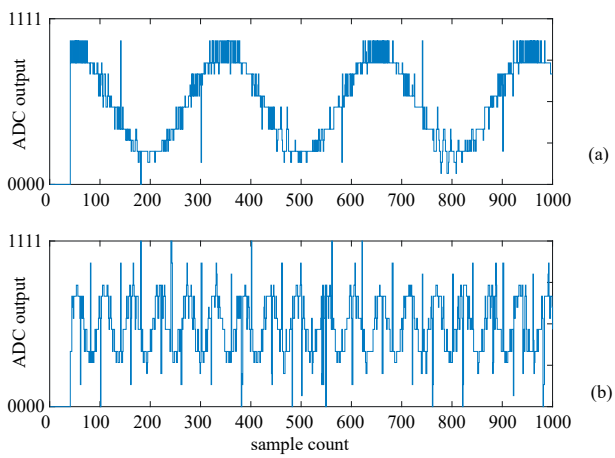

Figure 4.15: Measured time-domain ADC digital output, with the ΔΣ ADC fed with (a) an input of 11 MHz and (b) an input of 60 MHz, sampled at 3.3 GHz.

4.7 Conclusion

In this chapter, a complete design of a high-speed $\Delta\Sigma$ ADC is presented. A DT DSM has been synthesized in high-level using the Delta-Sigma toolbox in MATLAB and transformed into an equivalent CT DSM using time-invariant transformation. During DT to CT transformation, ELD in the feedback loops is considered. Larger than one clock cycle ELD can be successfully compensated by introducing a fast feedback loop around the quantizer. Therefore, the impulse responses between DT and CT DSMs are matched at the sampling instant in front of the quantizer.

The component-level design incorporates several high-speed circuits, such as inverter-based integrators and CML digital cells. Biasing voltages and currents can be tuned to achieve an optimized ADC performance. Thanks to the body-biasing technique in 28 nm FD-SOI CMOS, the transconductance of the inverter-based transconductor can be tuned. Moreover, bias currents to the CML digital cells can be adjusted to compensate for the resistance variations that cause changes to the output common-mode voltages.

In the simulation, the $\Delta\Sigma$ ADC has an input bandwidth up to 250 MHz when sampled at 5 GHz. The design becomes challenging when running at such a high sampling frequency and a low OSR, requiring aggressive noise shaping to reach a desired ADC resolution, which could cause stability issues. Therefore, expertise in the circuit designs and extensive layout works are required.

The proposed design has been implemented in 28 nm FD-SOI CMOS, fabricated, and tested. Due to the design complexity, the measured performance is not satisfying, compared with the simulation results both in schematic-level and post-layout. An unexpected error was found in a MUX, which is crucial in selecting the internal memory data, causing random read-out errors. The $\Delta\Sigma$ ADC also exhibits stability issues, which can be partially resolved by tuning the analog voltages to its internal components during the measurement. This design is an excellent opportunity for studying the $\Delta\Sigma$ ADC design in detail, providing a vital lesson to be learned to facilitate future designs.

Chapter 5

$\Delta\Sigma$ ADC with Digital Background Calibration

5.1 Introduction

In the previous chapter, a $\Delta\Sigma$ ADC has been extensively studied. In this chapter, the ADC performance degradation caused by DAC non-idealities is addressed.

Recall that in a $\Delta\Sigma$ ADC, a feedback loop exists. The digital signal from the quantizer output is fed back into the LF using DACs. Among all the feedback DACs, the linearity of the outer-most DAC is essential since it behaves as an additional input to the DSM. Any non-linearity issue can not be shaped by the high loop gain, which increases signal distortions seen from the output. In a simple single-bit DSM, the DAC is perfectly linear since the feedback signal is either a plus or a minus reference voltage. While in a $\Delta\Sigma$ ADC architecture where multi-bit DACs are used, linearizing the DACs becomes a challenge that may require a large chip area and high power consumption.

In a multi-bit DAC, unit cell matching is one of the dominant factors for good linearity. Seen from a higher-level perspective, the DAC requires its linearity better than the overall modulator, even though it only has a limited number of bits [61]. There are many methods to linearize the DAC. The static DAC calibration can be performed in the analog domain, that the current source currents are fine-tuned as presented in Section 4.5 in Chapter 4.

Another commonly used method is the dynamic element matching (DEM) tech-

nique, which is beneficial to eliminate distortion tones at the expense of additional noise [12]. The Data Weighted Averaging (DWA) and Individual Level Averaging (ILA) are algorithms to randomize the selection of the unit cells, so that mismatch error is first-order shaped. However, the DEM is less effective when the OSR is low [62], which may require a second-order DEM and a modified NTF for better performance [63].

For low OSR designs, the DAC calibration is an alternative method that uses a low-cost digital core to estimate and calibrate the individual DAC unit cells, as proposed in [64]. The digital approach is attractive since it avoids the linearization block such as DEM in-the-loop, and all the estimation and calibration are performed in the digital domain. The DAC can be implemented using small-sized devices, which further reduces power consumption.

This chapter presents a $\Delta\Sigma$ ADC design, using a digital calibration method similar to [64]. A single chip is designed by integrating a $\Delta\Sigma$ ADC core and the digital calibration core on the same chip in 65 nm CMOS. The digital circuits are synthesized in Synopsys Design Compiler (www.synopsys.com) and placed-and-routed using Cadence SoC Encounter.

5.2 $\Delta\Sigma$ ADC Architecture

The proposed $\Delta\Sigma$ ADC is built using CIFB architecture, which means the feedback signals are injected into the inputs of each of the integrators in the LF. The synthesized NTF is:

$$NTF = \frac{(z-1)(z^2-1.908z+1)}{(z-0.1808)(z^2-0.02173z+0.08153)} \tag{5.1}$$

which is further mapped to an equivalent CT architecture using time-invariant transformation similar to the approach presented in Section A.2.1 in Appendix A.

The proposed CT $\Delta\Sigma$ ADC architecture is shown in Fig. 5.1. Comparing with the DT CIFB architecture illustrated earlier in Fig. 4.1(a), the second DAC is omitted, replaced by a direct feed-forward path K_2 from the first integrator output to a summation node to sum the second integrator and the DAC_3 outputs. This feed-forward path yields a lower signal swing at the first integrator output due to the lack of subtraction with the feedback signal and reduces the total ADC power consumption. Still, mathematically, all the coefficients in the standard CIFB architecture in Fig. 4.1(a) can be accurately mapped.

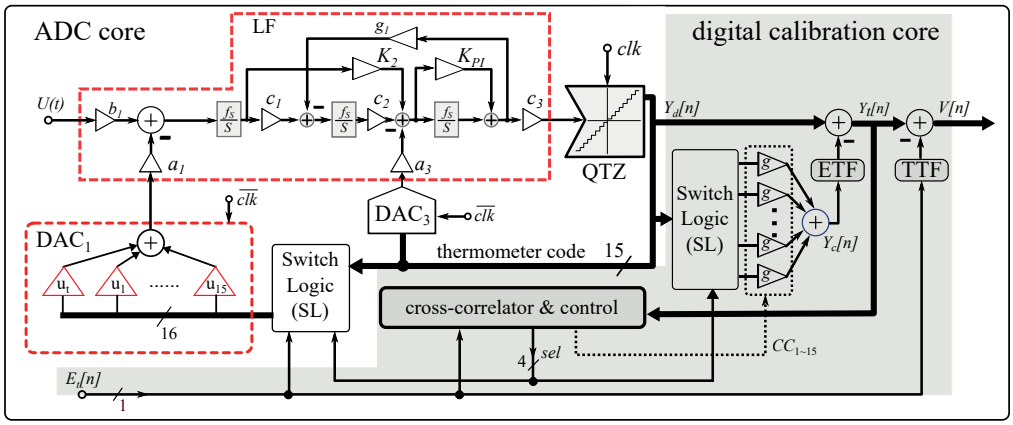

Figure 5.1: 3^{rd} order, 4-bit feedback CIFB $\Delta\Sigma$ ADC architecture, including a built-in digital calibration core.

The LF is a mix of feedback and feed-forward architecture. A feed-forward proportional path K_{PI} bypassing the last integrator, to feed-forward the DAC_3 output directly into the summation node before the quantizer. The additional DAC, usually required for a correct transformation from DT to CT DSM model, is avoided.

5.3 Digital Calibration Algorithm

At the DSM output, the cross-correlation between the digital code and the known test signal E_t is calculated. The cross-correlator could be implemented in a Field-Programmable Gate Array (FPGA), as presented in the previous work shown in [64]. For better performance, the cross-correlator is integrated with the $\Delta\Sigma$ ADC in this work. Each DAC unit cell mismatch characteristic is estimated and compensated using the built-in calibration module in the digital domain. The calibration can be performed in the background, with a trade-off in -0.5 dB reduction of the ADC dynamic range due to the additional test signal injection.

In the outer-most 4-bit current-steering DAC, the digital code is translated to a current and then subtracted by the input signal. An external test bit E_t is injected into a selected DAC unit cell in the analog domain to calibrate each DAC unit cell weights, controlled by a Switch Logic (SL).

Recall that in the CIFB architecture, contrary to the NTF, the STF is almost flat, as previously explained in Eq. 1.12. The STF can be approximated to unity if the loop gain is large. Thus, the residue of the known sequence E_t will be

visible in the quantizer output: Y_d. Therefore, the DAC unit cell characteristics are estimated by calculating the cross-correlation between the Y_d and the E_t.

The calibration relies on cross-correlation, as presented in [65]. The cross-correlator & control module shown in Fig. 5.1, which calculates the cross-correlation between E_t and Y_t and generates a set of calibration coefficient CC_i. The block diagram of the cross-correlator & control module is shown in Fig. 5.2.

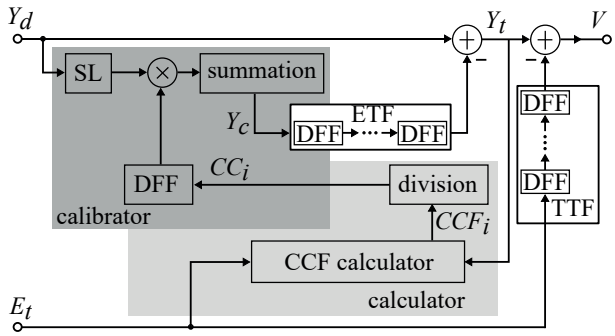

Figure 5.2: Block diagram of the cross-correlator & control module.

During estimation, first, the cross-correlation factor CCF_i for i^{th} unit cell in DAC_1 is calculated, which is:

$$CCF_i = \sum_{n=1}^{L} E_t[n] \cdot Y_t[n] \approx k_i \cdot s_{E_t}^2, \quad i = t, 1, 2, ..., 15 \tag{5.2}$$

where, k_i is the individual gain of the unit element under test, and $s_{E_t}^2$ is the variance of the known test signal E_t. The L is the number of samples for calculating cross-correlation, which is 2^{18} that proved to be sufficient for properly characterizing the DAC linearity.

The next step is to calculate the calibration coefficient of CC_i for each of the DAC unit cells. Note that there is one additional feedback DAC unit U_t in the DAC_1, which provides a calibration reference for the rest unit cells, and replaces a specific unit cell under test that avoids disturbing the DAC_1 operation during calibration.

The CC_i is calculated based on the division between the CCF_i and the reference CCF_t, which is:

$$CC_i = k(\frac{CCF_i}{CCF_t} - 1), \quad i = 1, 2, ..., 15 \tag{5.3}$$

During calibration, the 15-bit thermometer code Y_d from the quantizer output

is multiplied by the CC in bit-wise, which is:

$$Y_c = \sum_{i=1}^{15} Y_d[i] \cdot CC_i \tag{5.4}$$

The Y_c passes through an Error Transfer Function (ETF), then subtracted by the Y_d, and becomes the calibrated ADC digital output Y_t. The Y_t is fed-back to the cross-correlator for iteratively refining its value. Finally, the test signal E_t passed through a Test Transfer Function (TTF) and subtracted by Y_t. The ETF and TTF are pure delays in this design, since the STF is flat, and the error and test signal are injected into the system with the same path as the input signal U.

The calibrated ADC output V becomes:

$$V[n] = Y_d[n] - Y_c[n] \cdot ETF - E_t[n] \cdot TTF \tag{5.5}$$

5.4 Component-Level Implementation

A design has been implemented in 65 nm CMOS to verify the concept of digital calibration. The DSM core is built with 3^{rd} order, 4-bit output CIFB architecture, shown earlier in Fig. 5.1. The synthesized digital core, using cross-correlator to process the ADC output Y_d and the known pseudo-random test sequence E_t, is placed on the same chip. The CCF for each of the ADC output bits is calculated and stored in the internal memory. The digital calibration module is synthesized and laid out in the same chip as the DSM core, with manually drawn connection wires between them.

5.4.1 DAC Unit Cell Design

The chosen DAC unit cells are based on resistive current-mode DAC. The resistor is used to generate a current into the LF summation node, which is the virtual ground node of the integrator, in response to the digital codes presented on their input bit lines. Compared to the widely used current-steering DAC, the resistive DAC shows less noise [54].

The unit cell schematic is shown in Fig. 5.3. The DFF drives an inverter consisting of P_8 and N_8, and then convert the reference voltages to current by the resistor R. The DFF is built by two latches which are connected in series, updating the signal Q from the digital input D at the *clk* rising edge. The inverter

is connected to either V_{ref+} or V_{ref-} controlled by Q. Lastly, the DAC unit cell's output current I_{out} is the current flowing through the resistor R [66]. The direction I_{out} is controlled by the inverter, which either from V_{ref+} to A or the other way.

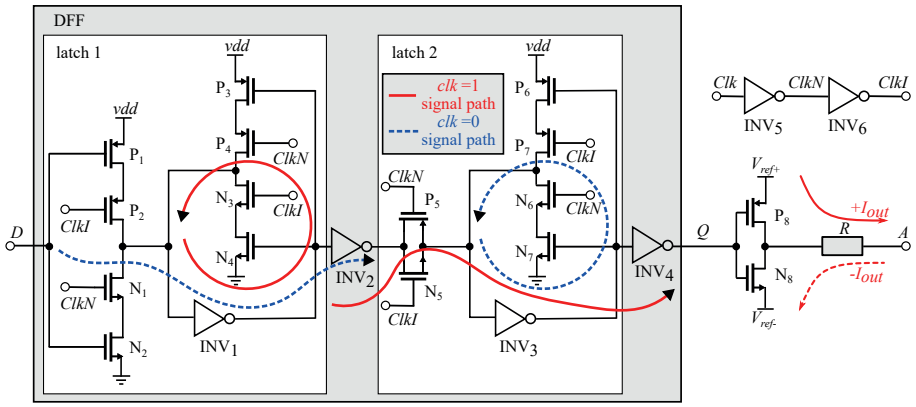

Figure 5.3: The resistive DAC unit cell schematic.

The differential DAC_1 and DAC_3 share an identical layout, but different in the purpose of each unit cell, which is shown in Fig. 5.4. In the DAC layout, the DAC unit cells are placed next to each other. In DAC_1, two of the unit cells at the edges are used for pseudo-random test sequence injection for calibration purposes. In DAC_3, dummy unit cells are added to both sides of the DAC unit cell array to mitigate the difference of diffusion under the resistors between the outer and inner unit cells [49]. Thus, the DAC unit cell matching is preserved if the mismatches between the resistors are minimized.

5.4.2 Switch Logic Design

For calibration purposes, the digital code to the outer-most DAC_1 is re-routed by an array of switches: a SL, which re-routes the thermometer codes from the quantizer to the outer-most DAC. Fig. 5.5(a) shows the schematic of the switches, which is controlled by a Read-Only Memory (ROM): *switch ROM* that generates a 30-bit predefined control signals c_0 to c_{29} to the switches. The layout of the switch ROM is shown in Fig. 5.5(b), and the layout of switches is shown in Fig. 5.5(c).

By selecting a predefined c from the switch ROM using the external digital control bits, the test bit D_{inT} is injected into one of the selected DAC_1 unit cells. In the meantime, the last unit cell is selected to maintain the $\Delta\Sigma$ ADC operation.

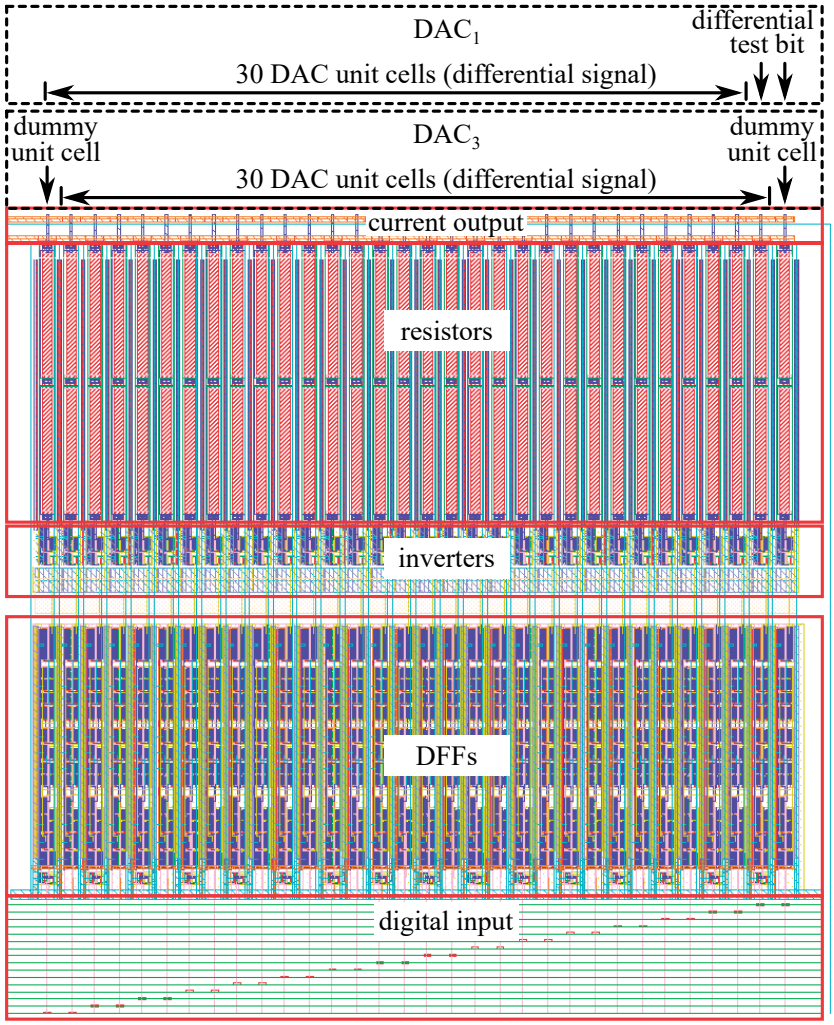

Figure 5.4: 4-bit differential DAC layout.

For example, by default, the D_{inT} is injected into the bit line D_{outT} to the test unit cell. The 15 input bit line D_{in0-14} are connected to the $D_{out0-14}$, respectively. For testing the DAC unit cell 0, c_0 reconnects the D_{in0} to D_{outT}, and D_{inT} is connected to the D_{out0}. The rest bits remain unchanged. By cycling the D_{inT} through all the 15 DAC unit cells, the correlation-based estimator implemented in the digital domain can effectively estimate the mismatches between the DAC unit cells in the outer-most DAC.

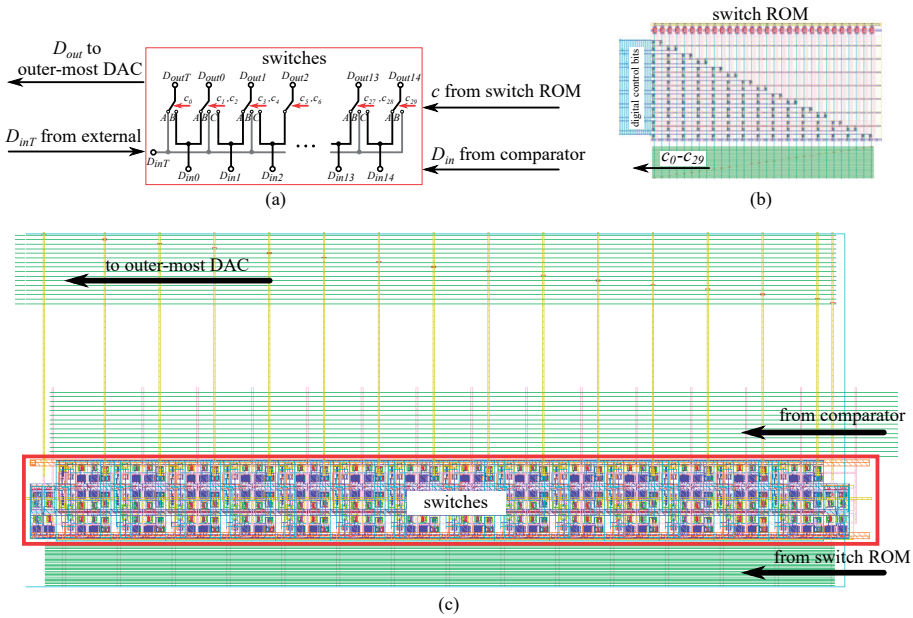

Figure 5.5: The SL design, (a) shows the schematic of switches, (b) shows the layout of switch ROM, and (c) shows the layout of switches.

5.4.3 Quantizer Design

The quantizer is a core block for converting the signal from the analog domain to the digital domain. The delay between the clocking edge and the stable digital output codes is critical since the quantizer is placed inside the feedback loop. The Flash ADC is one type of ADC that is fast in performing A/D conversion, which is suitable to be the core in a quantizer architecture.

The four-bit flash quantizer schematic is presented in Fig. 5.6, which consists of 15 comparators. Each comparator receives its reference voltage from a resistor ladder. The resistor ladder divides a high reference voltage and the ground into 15 pairs of reference voltages, of which the high reference voltage is buffered from an external reference voltage V_{ref}. In contrast, the low reference voltage is the voltage that appears on the bottom resistance R_{foot}. The differential input signal V_{inp} and V_{inm} are connected to the plus and the minus terminals, respectively, in all the 15 comparators.

The comparator schematic is shown in Fig. 5.7. In the pre-amplifier,the difference between the differential input signal, V_{inp} and V_{inm}, and differential reference voltages, V_{refp} and V_{refm}, is amplified. The pre-amplifier outputs V_{ampp} and V_{ampm} are latched by a dynamic cross-coupled inverter latch [67]. During

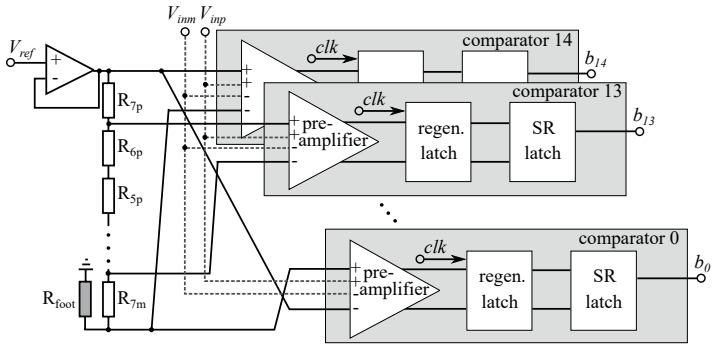

Figure 5.6: 4-bit quantizer schematic.

the *clk* low pulse, the regenerative latch is in reset mode so that the S_{int} and R_{int} are reset to the supply voltage *vdd*. During the *clk* high pulse, the regenerative latch is in latch mode that the pre-amplifier's outputs are latched and stored in the SR latch. The SR latch acts as a memory device that maintains the comparison results for one clock period.

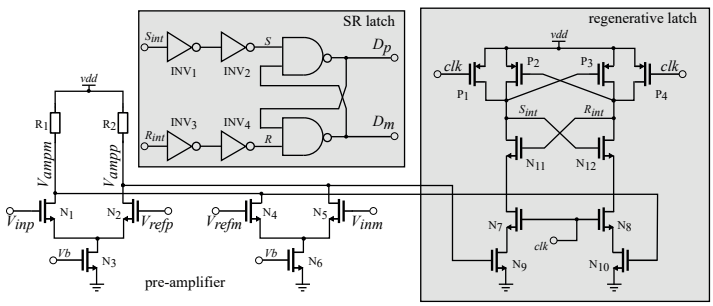

Figure 5.7: Comparator schematic.

5.4.4 Amplifier Design

The amplifiers are critical components in an active-RC integrator, used throughout this design. The first integrator in the LF requires high linearity as any non-linearity in this stage directly degrades the $\Delta\Sigma$ ADC accuracy. The amplifier used in the last integrator requires a high driving capability due to a large input capacitance in the multi-bit quantizer.

In this $\Delta\Sigma$ ADC design, the amplifiers share the same two-stage, Miller-compensated, class-AB output architecture [14]. The bias current in each amplifier is unique for balancing the speed, area, and power consumption.

Fig. 5.8 shows the amplifier schematic. An external bias current I_{ref} is injected into the bias circuit and mirrored into the tail current sources N_{b1} and N_{b2}, which are cascoded to provide a stable bias current. The common-mode voltage of the outputs V_{outp} and V_{outm} are sensed by a Common-Mode Feedback (CMFB) circuit, which controls a part of the PMOS transistors in the input differential stage active load.

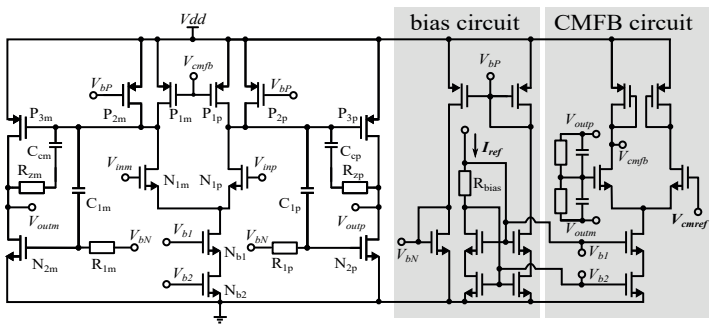

Figure 5.8: OP-amplifier schematic, includes a bias circuit and a CMFB circuit.

The first amplifier has the highest linearity requirements, and the last amplifier handles the K_{PI} path that needs to be fast, while the second integrator has the lowest GBW requirement. The optimized simulated GBW of the three amplifiers are 600, 350, and 600 MHz, respectively.

5.5 Simulation and Measurement Results

The design was implemented in 65 nm CMOS and has been simulated in the Spectre simulator in Cadence. The effectiveness of the proposed digital calibration method is evaluated by introducing mismatches in DAC, based on Monte-Carlo simulation results, and then estimated and calibrated. Fig. 5.9 shows the ADC output spectra with an input sine wave at 2 MHz. Assume 2% unit element mismatch appear in the outer-most DAC, without calibration, the SNDR is 55.7 dB, and large distortion tones are visible. By injecting a pseudo-random test sequence E_t into the system and cycle through all the unit cells, the calibrated system shows a much improved SNDR of 69.2 dB, close to the well-matched system that has a simulated SNDR of 70.0 dB.

Fig. 5.10 shows the microscopic photo of the fabricated chip. The $\Delta\Sigma$ ADC core and the digital calibration block are overlaid with their layouts, respectively. The chip size is 1 mm^2, of which 420 um$\times$320 um is for the $\Delta\Sigma$ ADC core, and

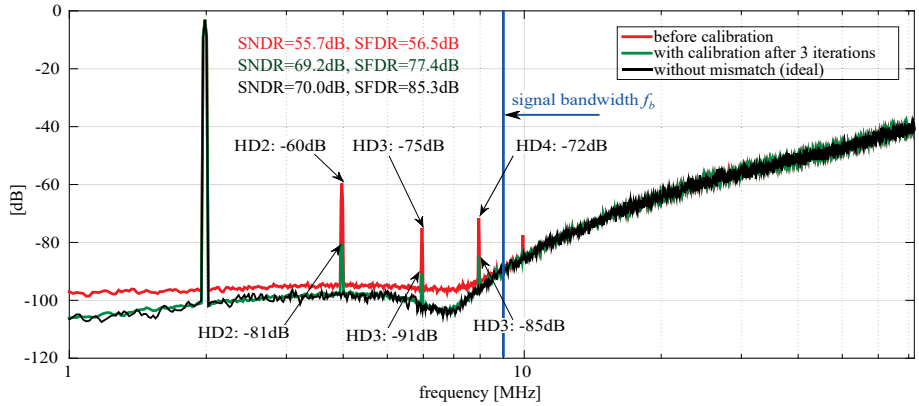

Figure 5.9: ADC output spectra of: Before and after calibration when DAC mismatch appears, and the ideal simulation result.

200 um×470 um is for the digital calibration core. The chip is bonded to a customized PCB, as shown in Fig. 5.11, and measured.

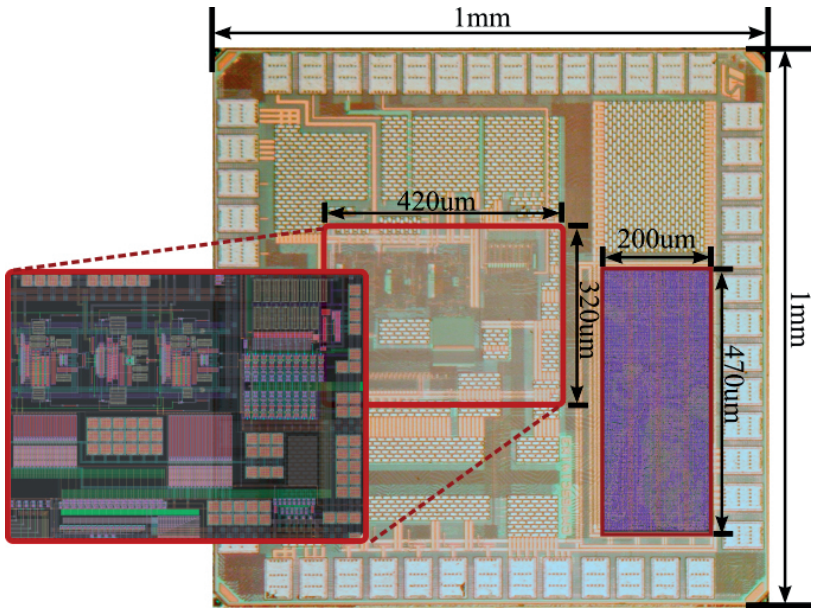

Figure 5.10: Chip microscopic photo, layout of ΔΣ ADC core and digital calibration core.

The post-layout simulation and the measurement results are plotted in Fig. 5.12. The post-layout simulation shows an SNDR of 65.5 dB and an SFDR of 77.4 dB, which degrades from an SNDR of 69.6 dB and an SFDR of 80.6 dB in a CT model simulation in MATLAB, partially due to increased thermal noise.

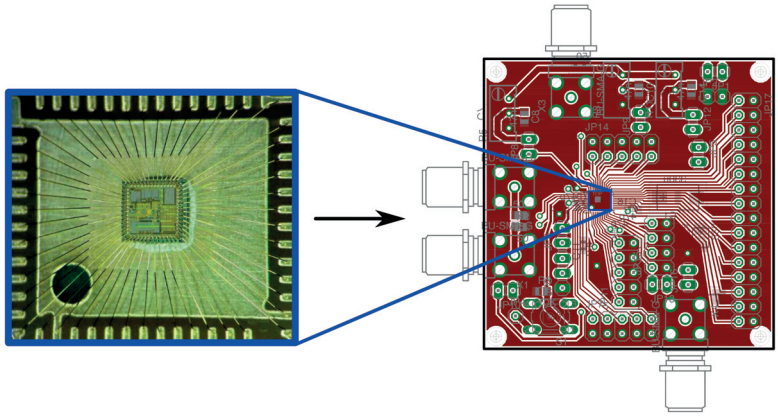

Figure 5.11: The bonded chip microscopic view and a customized PCB.

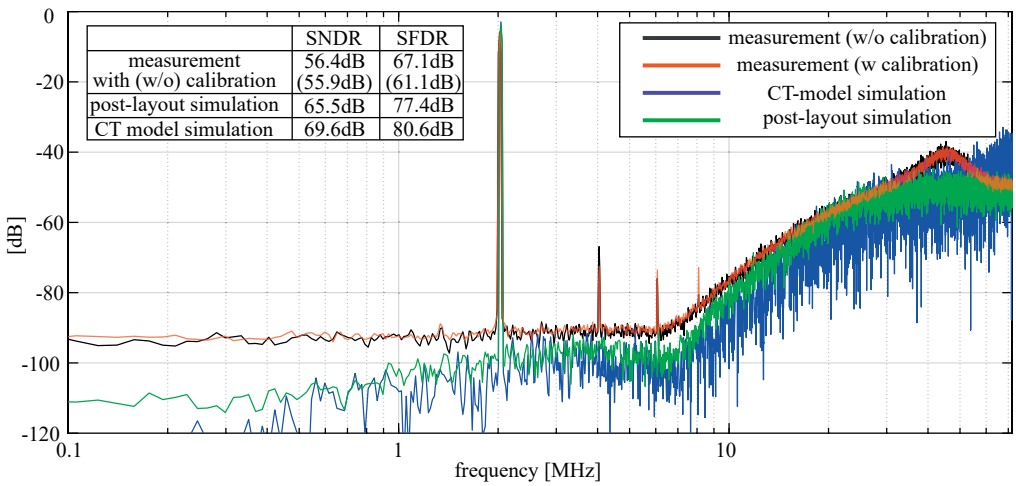

Figure 5.12: Post-layout simulation, CT model simulation, and measurement result.

The measurement results include the performance calculated directly from the $\Delta\Sigma$ ADC core. However, the on-chip digital calibration core does not correctly cancel the externally injected test signal E_t, resulting in a large residue of E_t interferes with the $\Delta\Sigma$ ADC output. Therefore, MATLAB is used for the estimation and calibration of the DAC linearity. The 4-bit quantizer outputs from the $\Delta\Sigma$ ADC core have been collected by a logic analyzer and analyzed. The function of the digital calibration core has been implemented and tested in MATLAB instead. The measurement procedure is briefly described below.

First of all, an externally generated pseudo-random test sequence E_t is injected into the system. The same E_t is input to the cross-correlation based estimator

for calculating the calibration coefficients CC, reflecting the mismatches in the out-most DAC, whose values are shown in Fig. 5.13 with all the 15 unit cells plotted, in which the y-axis shows the CC in percentage. Large mismatches among the unit cells require a larger CC to calibrate, i.e., approximately -5% calibration is required to linearize the second unit cell.

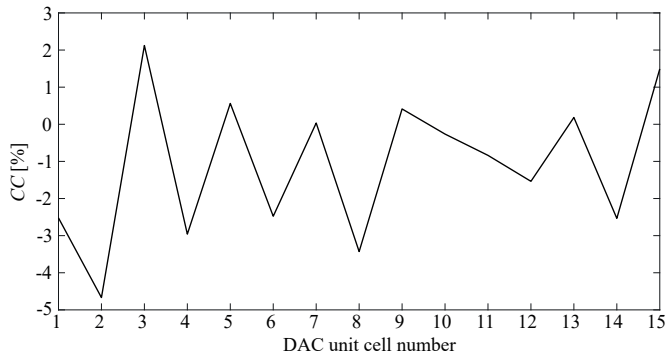

Figure 5.13: The estimated calibration coefficients CC for 15 DAC unit cells from the measurement results.

The calibration results show a small improvement of 0.5dB to the SNDR. However, it shows a larger improvement of 6 dB to the SFDR after calibration. It is partially due to a reduced third-order harmonic distortion.

Table 5.1 summarizes the key parameters used in the measurement. The supply voltages of the analog domain ($vdda$=1.3 V) and the digital domain ($vddd$=1.35 V) are slightly increased from their nominal value of 1.2 V, ensuring that the converter is stable and a moderate performance can be achieved.

Table 5.1: Summary of measurement settings and results

parameter	value
supply voltage ($vdda$)	1.30 V
supply voltage ($vddd$)	1.35 V
input V_{cm}	650 mV
amplifier V_{cm}	720 mV
QTZ reference voltage	1.18 V
input signal frequency	2.02 MHz
OSR	8
sampling frequency	144 MHz

5.6 Conclusion

In this chapter, a $\Delta\Sigma$ ADC with background calibration is explained. The simulation results are illustrated, and the chip measurement results are shown.

This work presents a digital calibration technique in CT $\Delta\Sigma$ ADC. The converter is clocked at 144 MHz, with an OSR of only 8. Non-idealities in outer-most DAC are measured and removed in the background by a digital calibration core, which is implemented in a single chip together with the $\Delta\Sigma$ ADC core.

The digital calibration is an attractive method for efficiently improving the $\Delta\Sigma$ ADC linearity when the tuning in the analog domain is not feasible. The cross-correlation method does not involve large power consumption and chip area overhead, which can be placed aside with the ADC core.

Besides, low OSR $\Delta\Sigma$ ADC does not allow the randomized method for linearizing the DAC. The digital calibration method presented in this research shows a feasible solution to low OSR designs.

A test chip has been implemented in 65 nm CMOS and measured. Even though the integrated digital calibration module for calibrating the outer-most DAC in the digital domain does not work as expected, the MATLAB calibration module still proves that the distortion tones can be partially reduced using the proposed algorithm. As a result, an improvement to the SFDR of the converter is observed.

Chapter 6

Summary of Included Papers and Author Contributions

Paper I: Digital Background Calibration in Continuous-time $\Delta\Sigma$ Analog to Digital Converters

Summary

This paper presents a research work of a CT Delta-Sigma A/D converter that is designed, simulated, and implemented in 65 nm CMOS. The converter is clocked at 144 MHz with a low OSR of only 8. The low OSR imposes low efficiency for the DEM to linearize the DAC, thus requiring a background digital calibration technique. A digital background calibration core is designed and integrated with the ADC in a system-on-chip solution to measure and then remove non-idealities in the outer-most multi-bit feedback DAC in the background.

This paper presents the architecture and circuit level design of a third-order, four-bit feedback, single-loop CT Delta-Sigma ADC. The digital implementation and mathematical calculations have been explained for showing the effectiveness of linearizing the DAC in a low OSR Delta-Sigma ADCs. The maximum simulated SNDR is 67.1 dB within 9 MHz signal bandwidth.

Author Contributions

I have designed, simulated, and chip-level implemented the CT Delta-Sigma ADC in 65 nm CMOS. I was partially involved in developing the digital calibration core. I carried out the top-level layout of integrating the Delta-Sigma ADC core and the digital calibration core, designed in separate circuit design tools, into a single chip.

Paper II:
A continuous-time delta-sigma ADC with integrated digital background calibration

Summary

This paper is an extended version of paper I, with detailed descriptions of the component-level implementation of the proposed digital background calibration technique. Compared with paper I, the detailed digital circuit implementation is presented. The division block implementation based on the Newton-Raphson equation is described, and the utilization of clock gating for saving dynamic power dissipation is presented.

The component-level implementations of the core building blocks in the proposed third-order, four-bit feedback, single-loop CT Delta-Sigma ADC, such as amplifiers, Flash quantizer, and DAC, are presented in this research paper. The converter simulation results are shown, and the effectiveness of the digital background calibration block is verified.

Author Contributions

I have drawn new figures to represent the individual block schematics in the Delta-Sigma ADC and explained the operations of the digital background calibration core. I have presented the DT to CT conversion using mathematical equations and carefully organized the paper for an enhanced illustration.

Paper III:
A 5 GHz CT $\Delta\Sigma$ ADC with 250MHz Signal Bandwidth in 28 nm-FDSOI CMOS

Summary

This paper presents a continuous-time Delta-Sigma ADC designed and simulated in 28 nm FD-SOI CMOS. The ADC is clocked at 5 GHz with a signal bandwidth of 250 MHz, for an OSR of only 10. A 4^{th} order loop filter is adopted to enhance quantization noise shaping in the presence of a low OSR. The excess loop delay exceeds one clock cycle, requiring two additional feedback paths to restore the nominal noise transfer function.

The conversion from a high-level model to component-level implementation has been presented in this research paper. The Delta-Sigma ADC design is shown that includes multiple high-speed design methodologies for achieving an optimized design for use in high-performance base stations in the future. The loop filter is built with inverter-based integrators, and the transistors are tuned by adjusting body-biasing voltages. The current-mode logic is used in the digital part to improve the signal transition speed. The Delta-Sigma ADC has a simulated SNDR of 73.1 dB for a power consumption of 232 mW in simulation.

Author Contributions

I designed, simulated, and laid-out the complete Delta-Sigma ADC core in 28 nm FD-SOI CMOS. I studied the state-of-the-art high-performance Delta-Sigma ADCs and utilized the fast-speed inverter-based integrators in the design based on the suggestions from my supervisors. I calculated the transformation from DT to CT ADC architecture using impulse-invariant transformation, with the considerations of the different excess loop delays in the ADC loop.

I synthesized and placed-and-routed the SPI module, using a source code provided by Ericsson Research, Ericsson AB, Lund, Sweden. I study the controlling method of this SPI module for controlling the on-chip memory that collecting the data from the Delta-Sigma ADC's output and reading-out the stored data in slow-speed sequentially. I managed to integrate the memory into the same chip design and connected it to the Delta-Sigma ADC core. I also designed the PCB for this ADC chip and soldered the components on the manufactured PCB for measurements (measurement results are not shown in the attached paper).

Paper IV:
A 10-bit Split-Capacitor SAR ADC with DAC Imbalance Estimation and Calibration

Summary

This paper presents a 10-bit SAR ADC core design sampled at 200 MS/s. To reduce area and power consumption, the ADC adopts a split-capacitor DAC. The gain error is estimated by injecting a PRBS signal into the equal-weighted capacitors on each split capacitor array and detected at the ADC output. The DAC imbalance estimation and correction in the proposed SAR ADC is performed by an off-chip post-processor developed in MATLAB.

This paper shows a practical way of estimating and calibrating the DAC-imbalance in a split capacitor array and shows the capabilities of being placed in a larger Time-Interleaved SAR ADC architecture. The presented SAR ADC core lies in a 7-channel Time-Interleaved SAR ADC chip, which has been designed and fabricated in a 22 nm FD-SOI CMOS process. A single SAR ADC core achieves an SNDR of 48.7 dB and an SFDR of 66.7 dB for input frequencies up to sampling frequency. The power consumption is 4.3 mW, and the FoM_s is 152 dB.

Author Contributions

In this work, I learned the functionality of different measurement tools in the lab. I performed the measurements of the fabricated SAR ADC, previously designed and taped-out by Ericsson Research, Ericsson AB, Lund, Sweden. I was involved in the designs of the DAC imbalance estimation and calibration post-processor in MATLAB, to estimate and calibrate the bridge attenuation coefficient in the split capacitor architecture. I wrote this paper based on simulation and measurement results.

Paper V:
Asynchronous vs. Synchronous CMOS SAR ADCs - A Comparison

Summary

In this paper, an improved 10-bit ASAR ADC core has been implemented based on the 10-bit SSAR ADC design. Similar to the previous SSAR design, seven ASAR sub-ADC cores are time-interleaved, designed, and simulated in 22 nm FD-SOI CMOS. The schematic of the ASAR ADC control logic is shown and compared with the SSAR ADC control logic schematic.

The two ADCs are compared in this paper, in terms of design robustness and circuit speed, in the same technology node and under a similar simulation testbench. In the ASAR ADC, the maximum sampling frequency for nominal SNDR performance, assessed both with and without transient noise, is slightly higher. The ASAR ADC displays a graceful SNDR degradation as the sampling frequency increases further instead of an abrupt SNDR collapse in the SSAR ADC. Together with the benefits of a lower external clock frequency, this establishes the superiority of the ASAR ADC, with only a minor increase in design complexity.

Author Contributions

In this work, I did the schematic and the layout design of the ASAR ADC, with a reference of the previously designed SSAR ADC. The ASAR ADC chip has already been manufactured in 22 nm FD-SOI CMOS. I performed extensive simulations for comparing the ASAR ADC and the SSAR ADC and concludes the overall superiority of ASAR ADC. I synthesized an on-chip memory component using the scripts in the earlier design and built an interface circuit between the ASAR ADC and the memory. I have analyzed the component-level simulations and achieved satisfying results. Lastly, I was partially involved in the PCB design of this chip. The chip will be measured as soon as the PCB is ready, and a suitable lab is available.

Paper VI:
A Design Method to Minimize the Impact of Bit Conversion Errors in SAR ADCs

Summary

This paper analyzes the bit conversion errors in high-speed SAR ADCs and proposes a design method to minimize their impact on ADC performance. By closely examining the existing design, the cause of bit conversion errors occurs in SAR ADCs are found. Due to the parallel signal processing paths of the comparator differential outputs in the existing design, large Sparkle-code errors occur that suspends the current and the subsequent charge redistribution in the CDAC. Besides, the use of SR latch in the SAR comparator may cause errors if the previous decisions are not updated before latched by the following digital control logic. All these bit conversion errors cause abrupt SNDR degradation when the SAR ADC sampling frequency increases.

The proposed improved SAR ADC design removes the SR latch from the output stage of the differential comparator. While using only a single-ended comparator output to generate the differential signals for the internal capacitive DAC, sparkle-code errors are avoided, and conversion errors from a previous bit conversion due to memory effects in the SR latch are eliminated. The 10-bit synchronous SAR ADC has been modeled in MATLAB and subsequently implemented at the circuit level in a 22 nm FD-SOI CMOS. The improved SAR ADC shows a graceful SNDR degradation at increased sampling frequencies, vastly improving the ADC performance compared to when sparkle-code errors, or conversion errors due to an invalid comparator output, are allowed to occur.

Author Contributions

In this work, I simulated the SAR ADC circuit and pinpointed an issue that Sparkle-code errors maybe generated from the invalid CDAC control codes. I created a MATLAB model to understand the root cause of the problem and improved the previous SAR ADC design based on the analysis. I ran extensive simulations to confirm that removing the SR latch and processing a single-ended comparator's output improves the circuit robustness, causing CDAC's charge redistribution to a default direction whenever a bit conversion error occurs.

Chapter 7

Conclusion and Future Work

The bandwidth increase in communication systems imposes enormous demands on the performance of their building blocks. The ADC is one of the critical blocks in communication devices that advanced rapidly in the previous decades. The emerge of the 5G network requires high-speed, high-performance ADCs, an attractive topic in research and industry. In this research work, two SAR ADCs and two $\Delta\Sigma$ ADCs have been designed in component-level, simulated, and fabricated in the advanced CMOS technologies. The ADC architectures have been shown, the detailed circuit designs have been explained, and tunability to counter react the non-idealities in the ADCs due to the Process, Voltage, and temperature variations, have been addressed. The benefits and drawbacks of each design have been explained.

The SAR ADCs belong to the Nyquist-rate ADC category, which is very attractive due to their digital friendly architecture and time-interleaving capability. The split-capacitor array in the CDAC in a SAR ADC is an attractive technique to reduce the total capacitance. As a result, the loads to the driving switches are decreased to reduce the SAR ADC's power consumption. However, influenced by parasitic capacitance, an imbalance between the two DAC arrays in the split-capacitor CDAC appears, limiting the maximum ADC resolution. Thus, the DAC imbalance estimation and calibration are performed in a post-processor in the digital domain, currently implemented using MATLAB.

A reference SSAR ADC design uses an external high-speed clock to synchronize the SAR ADC's internal comparator and its digital control logic. The SAR control logic design can be implemented using digital cells, but the trade-off is higher power consumption and the potential risk of experiencing high-weight

bits conversion errors due to insufficient comparison time. In contrast, an ASAR ADC is designed based on the experiences gained from the SSAR ADC design. It dynamically generates an internal clock to the comparator, guaranteeing high-weigh bits to be correctly converted, showing a graceful SNDR degradation at a higher sampling frequency than the synchronous version.

In the presented work, two $\Delta\Sigma$ ADCs are designed. $\Delta\Sigma$ ADCs belong to the oversampled ADC category, which is challenging when operated in a high sampling frequency for a moderate signal bandwidth. One of the designs is a high-speed $\Delta\Sigma$ ADC, implemented in 28 nm FD-SOI CMOS. This ADC design incorporates various techniques for achieving high-speed, such as inverter-based integrators in the loop-filter and current-mode logic in the digital logic. Larger than one clock cycle excess loop delay is compensated by introducing a direct feedback loop using an un-clocked DAC around the quantizer.

The second design evaluates the effectiveness of a digital background calibration technique, which is a $\Delta\Sigma$ ADC clocked at 144 MHz with a low OSR of only 8. A pseudo-random test sequence is injected and cycled through all the DAC unit cells, and the cross-correlation between the ADC output and the known sequence is calculated in the digital domain. A digital calibration circuit and the $\Delta\Sigma$ ADC are combined and implemented in a single chip in 65 nm CMOS, simulated and measured.

The future ADC designs can be inspired by the analysis presented in this dissertation, to design a high-performance ADC that will be implemented in a sophisticated larger system. One choice is improving the single-channel SAR ADC's performance and time-interleaving a larger number of channels for an widen bandwidth and increased ADC resolution. Another choice is to design a high-performance $\Delta\Sigma$ ADC, which will still be an interesting topic in the foreseeable future. For reaching wide-bandwidth and high-accuracy at the same time, high-order and aggressive noise shaping are inevitable. The current design already involves extensive tuning both in analog and in the digital domain. The new design will be optimized for better robustness and stability in terms of architecture selection and partially self-calibration, targeting high-speed, high-accuracy applications. Furthermore, Pipeline ADCs are very attractive, which already show huge potentials in communication devices and will be studied in the future.

Appendix

Appendix A

Coefficient Calculations in DT to CT DSM Architecture Transformation with 4^{th} Order CRFF LF

This Appendix explains the CT DSM coefficient calculations in a 4^{th} order CRFF CT DSM LF, transformed from a set of coefficients from an equivalent 4^{th} order CRFF DT DSM architecture. A similar principle applies to other DSM architectures as well.

The original DT DSM architecture is shown in Fig. A.1. It has a DAC that feedbacks the quantizer digital output signal into the analog domain then feed-forward to a summation node through four feed-forward paths a_{DT1} to a_{DT4}. An additional feedback path g_{DT} feeds the third integrator output signal back into the second integrator input node, acting as a resonator.

In contrast to the DT DSM that process discrete-time signals, the transformed CT DSM architecture shown in Fig. A.2 processes the continuously varying signals, meaning that the signals are changing from time to time. The method to map the CT DSM with the original DT DSM is the impulse-invariant transformation [68]. The CT DSM coefficients are calculated so that the impulse response H_{CT} of the open-loop filter in CT and H_{DT} in DT DSM architecture are equivalent at the quantizer sampling instant.

An important consideration during a DT to CT DSM transformation is the

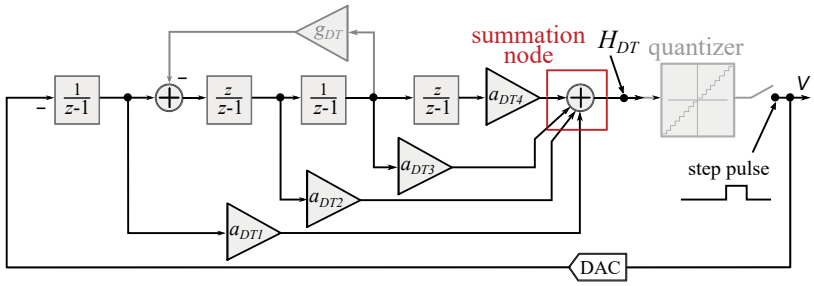

Figure A.1: 4^{th} order CRFF DT $\Delta\Sigma$ DSM architecture.

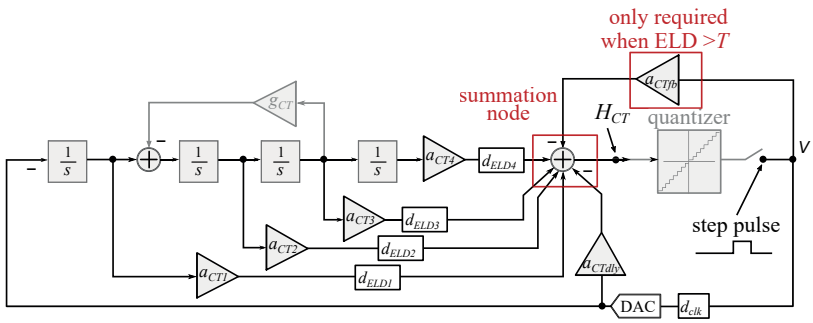

Figure A.2: 4^{th} order CRFF CT $\Delta\Sigma$ DSM architecture, with each feed-forward loop delay included due to the finite GBW of integrators.

ELD, which is termed as a combination of the delay required for a practical quantizer to resolve a decision and the inevitable delays in the feedback paths, including the DACs and the integrators.

The coefficients mapping from a 3^{rd} order CIFB DT to CT DSM architecture has been discussed in [54]. In this Appendix, the analysis extends further to a 4^{th} order CRFF CT DSM architecture. The coefficients are calculated under two different lengths of ELDs: an ELD less than or equal to T; and an ELD larger than T. Before discussing the details of DT to CT DSM coefficient calculations in the prior two scenarios, the original DT DSM coefficients are explained first.

A.1 The DT DSM Open-Loop Transfer Function

The proposed 4^{th} order, single resonator CRFF DT DSM architecture, is shown in Fig. A.1. The z-domain open-loop transfer function H_{DT}, observed from the

quantizer input, is:

$$H_{DT}(z) = \frac{-a_{DT1}}{(z-1)} + \frac{a_{DT2}(z-1-g_{DT}z)}{(z-1)[(z-1)^2+g_{DT}z]} - \frac{a_{DT3}z}{(z-1)[(z-1)^2+g_{DT}z]} - \frac{a_{DT4}z^2}{(z-1)^2[(z-1)^2+g_{DT}z]} \quad (A.1)$$

The Eq. A.1 is then mapped to DT domain $H_{DT}[n]$ using the z-transformation. The very small resonator coefficient g_{DT} is temporarily set to zero in the following calculations, which shows a very small difference between the resulting CT DSM compared with the DT DSM. The $H_{DT}[n]$ is:

$$H_{DT}[n] = -a_{DT1} - a_{DT2} \cdot n - a_{DT3} \cdot (\frac{n^2}{2} - \frac{n}{2}) - a_{DT4} \cdot [\frac{1}{6} \cdot (n^3 - n)] \quad (A.2)$$

where the N is the sample number.

Table A.1 lists the coefficients for each term in $H_{DT}[n]$:

Table A.1: Terms and coefficients in $H_{DT}[n]$

$H_{DT}[n]$ term	coefficient
n^3	$-\frac{a_{DT4}}{6}$
n^2	$-\frac{a_{DT3}}{2}$
n	$-a_{DT2} + \frac{a_{DT3}}{2} + \frac{a_{DT4}}{6}$
1	$-a_{DT1}$

A.2 DT to CT DSM Transformation

Fig. A.2 shows a CRFF CT DSM architecture. Contrary to the CRFF DT DSM architecture, the ELDs are the important parameters for calculating the

coefficients. There is an additional delay when the DAC output signal is fed back to the first CT integrator input. The feedback signal then passes through the integrators, whose outputs are scaled and fed-forward to the summation node through the gain paths from a_{CT1} to a_{CT4}.

Note that the four feed-forward path delays may not be equal since the finite GBW of the integrators introduce delays. These delays are described as d_{ELD1} to d_{ELD4} in the feed-forward paths. Furthermore, a fixed delay of d_{clk} is inevitably added between the quantizer and the feedback DAC. It could be set to half clock period delay ($0.5T$), meaning that the DAC and the quantizer are clocked at the opposite clocking edges, e.g., the quantizer is clocked at the clock rising edge while the DAC is clocked at the clock falling edge.

Usually, such a $0.5T$ delay between the quantizer and feedback DACs is sufficient for allowing the quantizer to complete a conversion, which leads to a scenario that the ELD is less than or equal to T, which will be discussed in Section A.2.1.

On the other hand, in a high-speed CT DSM, $0.5T$ may not be sufficient for reading out the properly settled quantizer outputs. A d_{clk} close or equal to T is the only viable choice, which eventually introduces a larger than one clock period ELD in the feedback loops after adding the d_{ELD1} to d_{ELD4}. This scenario will be discussed in Section A.2.2.

A.2.1 DT to CT Transformation - ELD Less than or Equal to One Clock Period

Typically, the ELD is not larger than T, meaning that the loop delay from the digital quantized signal is settled and feedback to the quantizer input node is within T. In this scenario, the impulse response of a CT DSM can perfectly match to the impulse response of the original DT DSM architecture by adding one additional feedback path a_{CTdly} to the summation node, as shown in Fig. A.2. The purpose of the a_{CTdly} path is to match the first sample in the open-loop impulse response of the CT to the DT DSM.

The impulse-response of the CT DSM architecture shown in Fig. A.2 is:

$$H_{CT}(s) = \frac{a_{CT1}}{s} + \frac{a_{CT2}}{s^2 + g_{CT}} + \frac{a_{CT3}}{s(s^2 + g_{CT})} + \frac{a_{CT4}}{s^2(s^2 + g_{CT})} \tag{A.3}$$

still, assuming $g_{CT} = 0$ in the following calculations.

The DAC feedback pulses are determined first. Then, the ELDs need to be estimated to calculate the time-domain transfer function.

The DAC feedback pulses in the time domain are defined as r_{DAC}, which is the height of the feedback pulse, commonly in NRZ or in RZ shape. The two symbols, α_{clk} and β_{clk}, are denoted as the DAC feedback pulse start and stop time, respectively, compared with the quantizer sampling instant and normalized to the T. Assume r_{DAC} is 1 between α_{clk} and β_{clk}, and 0 in the other conditions, the r_{DAC} in Laplace domain becomes R_{DAC}:

$$R_{DAC} = \frac{1}{s}(e^{-s\alpha_{clk}} - e^{-s\beta_{clk}}) \tag{A.4}$$

Based on component-level simulations, d_{ELD1} to d_{ELD4} are estimated. The start and stop times of the equivalent feedback signal, with an NRZ DAC pulse delayed by d_{clk} and four feed-forward paths delayed by $d_{ELD1,2,3,4}$, are $\alpha_{1,2,3,4} = d_{clk} + d_{ELD1,2,3,4}$ and $\beta_{1,2,3,4}$. The CT DSM open-loop LF impulse response in the time domain, including the Eq. A.4 and still disregarding the g_{CT} path, is:

$$\begin{aligned} H_{CT\_a_1}[n] &= \mathcal{L}^{-1}\{-\frac{a_{CT1}}{s^2}(e^{-s\alpha_1} - e^{-s\beta_1})\} \\ &= \begin{cases} -a_{CT1}(\gamma_1 - \alpha_1) & n = 1 \\ -a_{CT1}(\beta_1 - \alpha_1) & n \geq 2 \end{cases} \end{aligned} \tag{A.5}$$

where $\gamma_1 = min\{1, \beta_1\}$ when the DAC feedback pulses are extended beyond one clock period.

Similarly, the inverse Laplace transformation for the rest of the paths are:

$$\begin{aligned} H_{CT\_a_2}[n] &= \mathcal{L}^{-1}\{-\frac{a_{CT2}}{s^3}(e^{-s\alpha_2} - e^{-s\beta_2})\} \\ &= \begin{cases} -a_{CT2}[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}] & n = 1 \\ -a_{CT2}[(\beta_2 - \alpha_2)n + \frac{\alpha_2^2 - \beta_2^2}{2}] & n \geq 2 \end{cases} \end{aligned} \tag{A.6}$$

$$\begin{aligned} H_{CT\_a_3}[n] &= \mathcal{L}^{-1}\{-\frac{a_{CT3}}{s^4}(e^{-s\alpha_3} - e^{-s\beta_3})\} \\ &= \begin{cases} -\frac{a_{CT3}}{2}[(\gamma_3 - \alpha_3) + \alpha_3^2 - \gamma_3^2 + \frac{\gamma_3^3 - \alpha_3^3}{3}] & n = 1 \\ -\frac{a_{CT3}}{2}[(\beta_3 - \alpha_3)n^2 + (\alpha_3^2 - \beta_3^2)n + \frac{\beta_3^3 - \alpha_3^3}{3}] & n \geq 2 \end{cases} \end{aligned} \tag{A.7}$$

$$
\begin{aligned}
H_{CT\_a_4}[n] &= \mathcal{L}^{-1}\{-\frac{a_{CT4}}{s^5}(e^{-s\alpha_4} - e^{-s\beta_4})\} \\
&= \begin{cases}
-\frac{a_{CT4}}{24}[\alpha_4^4 - \gamma_4^4 - 4(\alpha_4^3 - \gamma_4^3) \\
+6(\alpha_4^2 - \gamma_4^2) - 4(\alpha_4 - \gamma_4)] & n = 1 \\
\\
-\frac{a_{CT4}}{24}[\alpha_4^4 - \gamma_4^4 - 4(\alpha_4^3 - \gamma_4^3)n \\
+6(\alpha_4^2 - \gamma_4^2)n^2 - 4(\alpha_4 - \gamma_4)n^3] & n \geq 2
\end{cases}
\end{aligned}
\tag{A.8}
$$

$$
\begin{aligned}
H_{CT\_a_{CTdly}}[n] &= \mathcal{L}^{-1}\{-\frac{a_{CTdly}}{s}(e^{-s\alpha_4} - e^{-s\beta_4})\} \\
&= \begin{cases}
-a_{CTdly} & n = 1 \\
0 & n \geq 2
\end{cases}
\end{aligned}
\tag{A.9}
$$

where $\gamma_{2,3,4} = min\{1, \beta_{2,3,4}\}$ when the DAC feedback pulses are extended beyond one clock period.

Combining the above equations Eq. A.5, Eq. A.6, Eq. A.7, A.8, and Eq. A.9, the time domain transfer function $H_{CT}(1)$ for the first sample is:

$$
\begin{aligned}
H_{CT}(1) = &- a_{CT1}(\gamma_1 - \alpha_1) - a_{CT2}[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}] \\
&- \frac{a_{CT3}}{2}[(\gamma_3 - \alpha_3) + (\alpha_3^2 - \gamma_3^2) + \frac{\gamma_3^3 - \alpha_3^3}{3}] \\
&- \frac{a_{CT4}}{24}[\alpha_4^4 - \gamma_4^4 - 4(\alpha_4^3 - \gamma_4^3) \\
&+ 6(\alpha_4^2 - \gamma_4^2) - 4(\alpha_4 - \gamma_4)] - a_{CTdly}
\end{aligned}
\tag{A.10}
$$

and $H_{CT}[n]$ for the following samples when $n \geq 2$, are:

$$
\begin{aligned}
H_{CT}[n] = &- a_{CT1}(\beta_1 - \alpha_1) - a_{CT2}[(\beta_2 - \alpha_2)n + \frac{\alpha_2^2 - \beta_2^2}{2}] \\
&- \frac{a_{CT3}}{2}[(\beta_3 - \alpha_3)n^2 + (\alpha_3^2 - \beta_3^2)n + \frac{\beta_3^3 - \alpha_3^3}{3}] \\
&- \frac{a_{CT4}}{24}[\alpha_4^4 - \beta_4^4 - 4(\alpha_4^3 - \beta_4^3)n \\
&+ 6(\alpha_4^2 - \beta_4^2)n^2 - 4(\alpha_4 - \beta_4)n^3]
\end{aligned}
\tag{A.11}
$$

The term coefficients in $H_{CT}[n]$ are combined and listed in Table. A.2: The coefficients a_{CT1}, a_{CT2}, a_{CT3}, a_{CT4} are found by mapping the coefficients of each

Table A.2: Terms and coefficients in $H_{CT}[n]$

$H_{CT}[n]$ term	coefficient
n^3	$-\frac{a_{CT4}}{6} \cdot (\beta_4 - \alpha_4)$
n^2	$-\frac{a_{CT4}}{4} \cdot (\alpha_4^2 - \beta_4^2) - \frac{a_{CT3}}{2} \cdot (\beta_3 - \alpha_3)$
n	$-a_{CT2} \cdot (\beta_2 - \alpha_2) - \frac{a_{CT3}}{2} \cdot (\alpha_3^2 - \beta_3^2) + \frac{a_{CT4}}{6} \cdot (\alpha_4^3 - \beta_4^3)$
1	$-a_{CT1} \cdot (\beta_1 - \alpha_1) - \frac{a_{CT2}}{2} \cdot (\alpha_2^2 - \beta_2^2) - \frac{a_{CT3}}{6} \cdot (\beta_3^3 - \alpha_3^3)$ $-\frac{a_{CT4}}{24} \cdot (\alpha_4^4 - \beta_4^4)$

term in $H_{CT}[n]$ (shown in Table. A.2) with the corresponding term of $H_{DT}[n]$ (shown in Table A.1), resulting in:

$$
\begin{aligned}
a_{CT4} &= \frac{a_{DT4}}{\beta_4 - \alpha_4} \\
a_{CT3} &= \frac{2a_{DT3} + (\alpha_4 + \beta_4)a_{DT4}}{2(\beta_3 - \alpha_3)} \\
a_{CT2} &= \frac{\alpha_4^3 - \beta_4^3}{6(\beta_2 - \alpha_2)} \cdot a_{CT4} - \frac{\alpha_3^2 - \beta_3^2}{2(\beta_2 - \alpha_2)} \cdot a_{CT3} + \frac{6 \cdot a_{DT2} - 3 \cdot a_{DT3} - a_{DT4}}{6 \cdot (\beta_2 - \alpha_2)} \\
a_{CT1} &= \frac{a_{DT1} - \frac{\alpha_4^4 - \beta_4^4}{24} \cdot a_{CT4} - \frac{\beta_3^3 - \alpha_3^3}{6} \cdot a_{CT3} - \frac{\alpha_2^2 - \beta_2^2}{2} \cdot a_{CT2}}{\beta_1 - \alpha_1}
\end{aligned}
\tag{A.12}
$$

Lastly, the coefficient a_{CTdly} is calculated by equating the first sample of $H_{CT}(1)$

in Eq. A.10 with $H_{DT}(1)$ using Eq. A.2 at $n = 1$:

$$\begin{aligned} a_{CTdly} =& a_{DT1} + a_{DT2} - a_{CT1}(\gamma_1 - \alpha_1) - a_{CT2}[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}] \\ & - \frac{a_{CT3}}{2}[(\gamma_3 - \alpha_3) + (\alpha_3^2 - \gamma_3^2) + \frac{\gamma_3^3 - \alpha_3^3}{3}] \\ & - \frac{a_{CT4}}{24}[\alpha_4^4 - \gamma_4^4 - 4(\alpha_4^3 - \gamma_4^3) + 6(\alpha_4^2 - \gamma_4^2) - 4(\alpha_4 - \gamma_4)] \end{aligned} \tag{A.13}$$

A.2.2 DT to CT Transformation - ELD Larger than One Clock Period

In a high-speed CT DSM, the ELD in the longest loop maybe larger than T. In other words, the delay in the feedback path, caused by the non-ideal comparator decision time and the finite GBW of the amplifiers in the integrators, maybe comparable to the clock period. Therefore, even including an additional a_{dly} path seeing from Fig. A.1, the delay of such a feedback path could still be larger than T if the d_{clk} is large, and the summation amplifier is slow.

The influence of the DT to CT DSM transformation when experiencing a more than T ELD has been discussed in [57]. It concluded that an ELD value could be larger than T, but an exact mapping from DT to CT is not feasible even with altering the feedback paths or re-calculating the coefficients of the loop filter. A solution has proposed that a fast analog feedback loop can be implemented outside the ADC loop without being limited by the latency of the quantizer and the feedback DACs.

In contrary to the analog feedback loop, an additional fast digital feedback loop a_{CTfb} that is shown in Fig. A.2 serves a similar purpose, with a prerequisite that the quantizer can complete a decision within one clock cycle. The DAC is not clocked, immediately responds to the quantizer digital outputs whenever they are ready for achieving the maximum speed of the feedback signal from the quantizer output back to the analog summation node. This path does not involve any integrator, only requiring a sufficient settling time of the feedback pulse before the quantizer's next sampling instant.

Assume that the DACs are clocked at the same clock edge as the quantizer, resulting in the $\alpha_{1,2,3,4} > 1$. Thus, Eq. A.10 evidently shows that the first sample of $H_{CT}(1)$ becomes zero. With the additional coefficient a_{CTfb}, the $H_{CT}(1)$ is realizable, guaranteeing a successful mapping between CT and DT DSM. Similar to the calculation of a_{CTdly} shown previously in Section A.2.1, the

a_{CTfb} is determined by mapping the $H_{CT}(1)$ with $H_{DT}(1)$, which is:

$$H_{CT}(1) = \mathcal{L}^{-1}\{-\frac{a_{CTfb}}{s}(e^{-s\alpha_{fb}} - e^{-s\beta_{fb}})\} = -a_{CTfb} = H_{DT}(1) \tag{A.14}$$

where the α_{fb} represents the start time of this extra fast feedback loop that has to be smaller than the T, and the β_{fb} represents the stop time of this pulse that should not be larger than $2T$.

The CT DSM transfer function $H_{CT}(n-1)$ from Eq. A.11 is mapped with $H_{DT}[n]$ from Eq. A.2, when $n > 2$. By using the similar calculations as presented in Section A.2.1, substituting $\alpha_{1,2,3,4}$ with $\alpha_{1,2,3,4} - 1$ and $\beta_{1,2,3,4}$ with $\beta_{1,2,3,4} - 1$, the CT coefficients with an ELD larger than T, are:

$$\begin{aligned}
a_{CT4} =& \frac{a_{DT4}}{\beta_4 - \alpha_4} \\
a_{CT3} =& \frac{a_{DT3} + a_{DT4} + \frac{a_{DT4}}{2} \cdot (\alpha_4 + \beta_4)}{\beta_3 - \alpha_3} \\
a_{CT2} =& \frac{a_{DT2} - \frac{1}{2} \cdot a_{DT3} - \frac{2}{3} \cdot a_{DT4} - \frac{a_{DT4}}{6} \cdot (\alpha_4^2 + \alpha_4 \cdot \beta_4 + \beta_4^2) - \frac{a_{DT4}}{2} \cdot (\alpha_4 + \beta_4)}{\beta_2 - \alpha_2} \\
&+ \frac{a_{CT3} \cdot (\beta_3 - \alpha_3) - \frac{a_{CT3}}{2} \cdot (\alpha_3^2 - \beta_3^2)}{\beta_2 - \alpha_2} \\
a_{CT1} =& \frac{a_{DT1} + a_{CT2} \cdot (\beta_2 - \alpha_2) - \frac{a_{CT2}}{2} \cdot (\alpha_2^2 - \beta_2^2) - \frac{a_{CT3}}{2} \cdot (\beta_3 - \alpha_3)}{\beta_1 - \alpha_1} \\
&+ \frac{\frac{a_{CT3}}{2} \cdot (\alpha_3^2 - \beta_3^2) - \frac{a_{CT3}}{6} \cdot (\beta_3^3 - \alpha_3^3) + \frac{a_{DT4}}{24} \cdot (\alpha_4^2 + \beta_4^2) \cdot (\alpha_4 + \beta_4)}{\beta_1 - \alpha_1} \\
&+ \frac{\frac{a_{DT4}}{6} \cdot (\alpha_4^2 + \alpha_4 \cdot \beta_4 + \beta_4^2) + \frac{a_{DT4}}{4} \cdot (\alpha_4 + \beta_4) + \frac{a_{DT4}}{6}}{\beta_1 - \alpha_1} \\
a_{CTfb} =& a_{DT1} + a_{DT2}
\end{aligned} \tag{A.15}$$

Lastly, the new coefficient of the feedback path a_{CTdly}, which is necessary for matching $H_{CT}(1)$ from Eq. A.10 with the second sample $H_{DT}(2)$ in DT DSM

(due to one clock period delay), becomes:

$$\begin{aligned} a_{CTdly} =& a_{DT1} + 2 \cdot a_{DT2} + a_{DT3} + a_{DT4} - a_{CT1} \cdot (\gamma_1 - \alpha_1) \\ & - a_{CT2} \cdot (\gamma_2 - \alpha_2 + \frac{\alpha_2^2 - \gamma_2^2}{2}) - \frac{a_{CT3}}{2} \cdot (\gamma_3 - \alpha_3 + \alpha_3^2 - \gamma_3^2 + \frac{\gamma_3^3 - \alpha_3^3}{3}) \\ & - \frac{a_{CT4}}{24} \cdot (\alpha_4^4 - \gamma_4^4) - 4 \cdot (\alpha_4^3 - \gamma_4^3) + 6 \cdot (\alpha_4^2 - \gamma_4^2) - 4 \cdot (\alpha_4 - \gamma_4) \end{aligned} \tag{A.16}$$

where $\gamma_{1,2,3,4} = min(\beta_{1,2,3,4}, 1)$.

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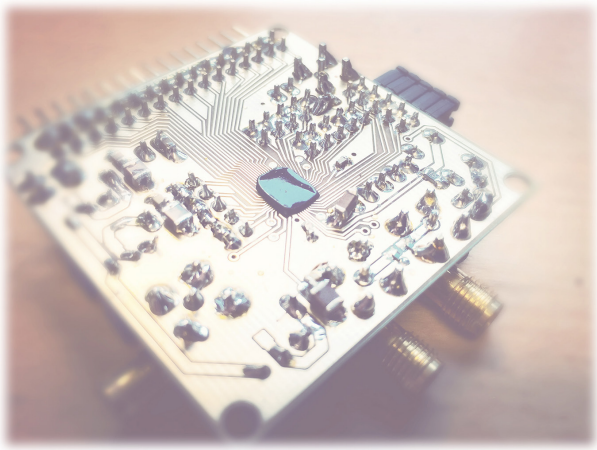

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