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InGaAs Tri-gate MOSFETs with Record On-Current

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***Abstract*—**We demonstrate InGaAs tri-gate MOSFETs with an on-current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, enabled by an inverse subthreshold slope of SS = 66 mV/decade and transconductance of g_m = 3 mS/μm, a Q-factor of 45. This is the highest reported I_{ON} for both Si-based and III-V MOSFETs. These results continue to push III-V MOSFET experimental performance towards its theoretical limit. We find an improvement in SS from 81 to 75 mV/dec. as the effective oxide thickness (EOT) is scaled down from 1.4 to 1 nm, as well as improvements in SS, g_d and DIBL from reducing the nanowire width. We also find that electron mobility remains constant as the width is scaled to 18 nm.

I. Introduction

An important path for reducing the power density in CMOS technology has been to lower the supply voltage V_{DD}. To maintain sufficient drive current, innovations are required, such as strained channels, novel channel materials and 3D device architectures [1]-[14]. For this purpose, high indium $In_xGa_{1-x}As$ is an attractive channel material due to its excellent electron transport properties, i.e. high electron mobility μ_e and long mean free path λ [6]. While the relatively low DOS of indium-rich $In_xGa_{1-x}As$ is predicted to limit I_{DS} in highly scaled devices, compared to competing technologies such as Si and Ge, this may be offset by the gain from the long λ and high μ_e of $In_xGa_{1-x}As$ [15]. Since this technology likely will be implemented in a 3D channel architecture, such as FinFETs or NWFETs, a further question concerns the dependence of λ on the channel dimensions, i.e. the influence of surface roughness on device performance.

In this work, we demonstrate tri-gate MOSFETs utilizing an $In_{0.85}Ga_{0.15}As$ nanowire (NW) as the channel. By gate oxide scaling, improvements of the surface passivation process and optimization of device dimensions, we achieve a drive current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm. This is a record value for both III-V and Si MOSFETs. We also show that, as the NW width, W_{NW}, is scaled down, electrostatic properties significantly improve, while g_m and λ do not degrade. These results continue to push the limits, as well as explore the potential, of III-V FETs.

II. Device Fabrication

The process flow and schematic images of the device are shown in Fig. 1(a)-(f). The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask, as described elsewhere [4]. Each device consists of a single NW. The composition of the NW is $In_{0.85}Ga_{0.15}As$, as determined by optical characterization [15]. Fig. 1(g) shows an SEM image of an NW with W_{NW} = 90 nm, with the {110} sidewall facets denoted [15]. The inset of Fig. 1(h) shows a schematic figure of the NW cross-section. 30 nm highly doped $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) is subsequently grown by MOCVD as the contact layer, utilizing HSQ as a dummy gate [Fig. 1(h)]. After mesa isolation, the InP in the channel is etched by HCl (10%) in order to form a ~30 nm tall plateau, with the purpose of improving the gate coverage along the bottom of the sides of the NW. 4 cycles of surface oxidation by ozone and diluted HCl etching (digital etching) are performed to reduce the dimensions of the NW. The final height of the NW is H_{NW} = 8 nm, as determined from AFM. Subsequently, Ti/Pd/Au contact metal is evaporated and patterned by lift-off. Surface passivation, by ozone cleaning and $(NH4)_2S$ (10%) for 20 min, is followed by deposition of Al_2O_3/HfO_2 gate oxide (5/35 cycles and EOT ≈ 1 nm, unless otherwise stated). A 12 hour post-deposition anneal step at 100 °C in N_2 atmosphere is performed in-situ. Thermal evaporation and patterning by lift-off of 30/10/150 nm Ni/Pd/Au as the gate metal complete the process [Fig. 1(i)].

III. Results

Fig. 2 shows transfer characteristics of a tri-gate MOSFET with L_G = 75 nm and W_{NW} = 25 nm. All normalization is done to the total gated NW periphery, i.e. the three sides of the tri-gate. Peak transconductance is $g_m \approx 3.0$ mS/μm at V_{DS} = 0.5 V. Subthreshold characteristics of the same device are shown in Fig 3. At V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, I_{ON} = 650 μA/μm. The gate current is I_G < 1 nA/μm. Minimum inverse subthreshold slope SS reaches 66 mV/decade (Fig. 4) at V_{DS} = 0.5 V, and 61 mV/decade at V_{DS} = 0.05 V. The drain-induced barrier-lowering (DIBL) is 65 mV/V, measured at I_{DS} = 1 μA/μm. The on-resistance of this device is R_{ON} = 175 Ω·μm at V_{GS} = 1 V. Output characteristics for W_{NW} = 90 and W_{NW} = 25 nm devices with L_G = 75 nm are shown in Fig. 5 and 6, respectively. The output conductance of these devices is g_d = 0.45 and 0.25 mS/μm (voltage gain is 5.5 and 10) at $V_{GS} - V_T = V_{DS}$ = 0.5 V.

Minimum SS versus L_G is shown for W_{NW} = 25 nm and W_{NW} = 90 nm devices at V_{DS} = 0.05 and 0.5 V (Fig. 7). The reduced W_{NW} offers improved resilience against short channel effects (SCEs), but at L_G = 25 nm, SS is degraded (110 mV/decade) even at W_{NW} = 25 nm. Minimum SS versus W_{NW} is shown in Fig. 8 for L_G = 75 nm devices at V_{DS} = 0.5 V. Average minimum SS improves from approximately 95 mV/dec. for W_{NW} > 90 nm to SS < 70 mV/dec. for W_{NW} < 30 nm due to enhanced electrostatic control. The lowest SS of a device at this bias is 64 mV/dec. The theoretical values

indicate *SS* obtained from a solution of Laplace's equation modeling the full 3D structure of the nanowire using COMSOL. To improve performance at short L_G, W_{NW} must be further reduced. Scaling of H_{NW} will improve *SS* but reduce the aspect ratio (AR), which is undesirable. Moreover, the implementation of a wider band gap back-barrier, such as InAlAs or a BOX layer, is also expected to improve resilience to SCEs. Fig. 9 shows median (crosses) and mean (squares) minimum *SS* for four samples with L_G = 75 nm and W_{NW} = 25-30 nm at both V_{DS} = 0.05 and 0.5 V (~40 devices each). Sample D has 5/50 cycles Al_2O_3/HfO_2. Sample C has 5/45 cycles Al_2O_3/HfO_2. Sample B and A have 5/35 cycles Al_2O_3/HfO_2. In addition, samples D, C and B where passivated with $(NH_4)_2S$ (10%) produced by Merck, while sample A was passivated with $(NH_4)_2S$ (10%) produced by Sigma-Aldrich. Fig. 10 shows mean minimum *SS* of samples D to B versus EOT (1 cycle = 1.1 Å, κ = 18 and 9 for HfO_2 and Al_2O_3). These results indicate an improvement both from oxide scaling (average *SS* improves from 81 to 75 mV/dec. for EOT from ~1.4 nm to ~1 nm), and from optimization of the surface passivation parameters (mean *SS* improves from 75 to 70 mV/dec. for sample B to A). The trend indicates that *SS* may be further improved by scaling of the EOT. We do not observe a clear trend of g_m versus EOT.

Fig. 11 shows g_d versus W_{NW} at V_{DS} = 0.5 V and $V_{GS} - V_T$ = 0.5 V for L_G = 75 nm devices. Average g_d is reduced from 0.5 mS/µm at W_{NW} = 90 nm to ~0.2 mS/µm at W_{NW} = 25 nm. The DIBL measured at 1 µA/µm is shown in Fig. 12. It is similarly reduced from 170 mV/V at W_{NW} = 90 nm, to 38 mV/V at W_{NW} = 25 nm. The threshold voltage (V_T) defined at I_{DS} = 1 µA/µm increases in narrow NWs (Fig. 13). The trend approximately follows calculated values from an effective mass quantum wire model, indicating that the V_T increase is due to quantum confinement.

Fig. 14 shows g_m versus W_{NW}. The highest g_m observed in these devices is ~3.3 mS/µm (SS_{sat} = 90 mV/dec.) at V_{DS} = 0.5 V and L_G = 50 nm. g_m increases as W_{NW} is scaled down to approximately 35 nm from planar architecture (W_{NW} = 1 µm). This may be explained by that narrow NWs are more Indium-rich, due to interactions with the HSQ mask during MOCVD growth, which may improve mobility as well as change the D_{it} distribution [15]. This shows that the improvement of g_d with W_{NW}, is in fact due to improved electrostatics. The inset of Fig. 15 shows average values of g_m versus L_G for W_{NW} = 25 nm. Dashed traces show an analytical quasi-ballistic model with λ = 140 nm fitted to the measured data.

I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm is shown in Fig. 15 versus both W_{NW} and L_G (inset). I_{ON} increases from 200 to 650 µA/µm as W_{NW} goes from 1 um (planar) to 25 nm, due to the simultaneous improvements of *SS* (100 to 66 mV/dec.) and g_m (1.1 to 3 mS/µm). I_{ON} peaks at L_G = 75 nm, which is explained by the degraded *SS* (Fig. 7) and that g_m only improves slightly (Fig. 14) for shorter L_G.

These devices exhibit quantized conductance at 10 K due to subband splitting in a 1D channel (inset of Fig. 16). From the conductance steps, the transmission is obtained. The device in Fig. 3 shows a transmission of T = 0.67, which indicates quasi-ballistic transport. Fig. 16 shows electron mobility μ_e and λ for NWs with W_{NW} = 18 – 32 nm calculated from quantized conductance. To obtain μ_e, we use the Einstein relation and a correction factor of 1.6 to account for degeneracy [15]. We note that this method is not strongly influenced by D_{it}. No dependency versus W_{NW} is observed, which correlates with g_m versus W_{NW} with W_{NW} < 35 nm, explained by small surface scattering. Since g_m is temperature-independent, the same is true for μ_e.

A benchmark of the I_{ON} (at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm) for state-of-the-art III-V planar and non-planar MOSFETs is shown in Fig. 17. The value of 650 µA/µm presented in this work is the record value of both categories. The same is true for the quality factor Q = g_m/SS, which is 45 in this work (Fig. 18). Fig. 19 compares I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm for various technologies. $I_{DS,surface}$ is I_{ON} normalized to the gated channel periphery, while $I_{DS,chip}$ is normalized to the chip surface width including the specified pitch size. $I_{ON,chip}$ in our devices is lower than that of 14 nm FinFET (570 compared to 650 µA/µm for a pitch of 42 nm), which demonstrates the importance of high AR in 3D channels, but we observe a two-fold increase in $I_{ON,surface}$ over 14 nm FinFET technology, which is due primarily to the high μ_e of $In_xGa_{1-x}As$ [16].

IV. Conclusion

We have demonstrated $In_xGa_{1-x}As$ tri-gate MOSFETs with a record on-current of 650 µA/µm at V_{DD} = 0.5 V and I_{ON} = 100 nA/µm, *SS* = 66 mV/decade and g_m = 3.0 mS/µm. From data versus NW width, we observed improvements in *SS*, DIBL and g_d for scaled down NWs. Furthermore, we observed improvements both from oxide scaling the surface passivation process. From low-temperature measurements we obtain μ_e and λ, which remain high, 2750 cm^2/Vs and 150 nm, respectively, even in scaled NWs.

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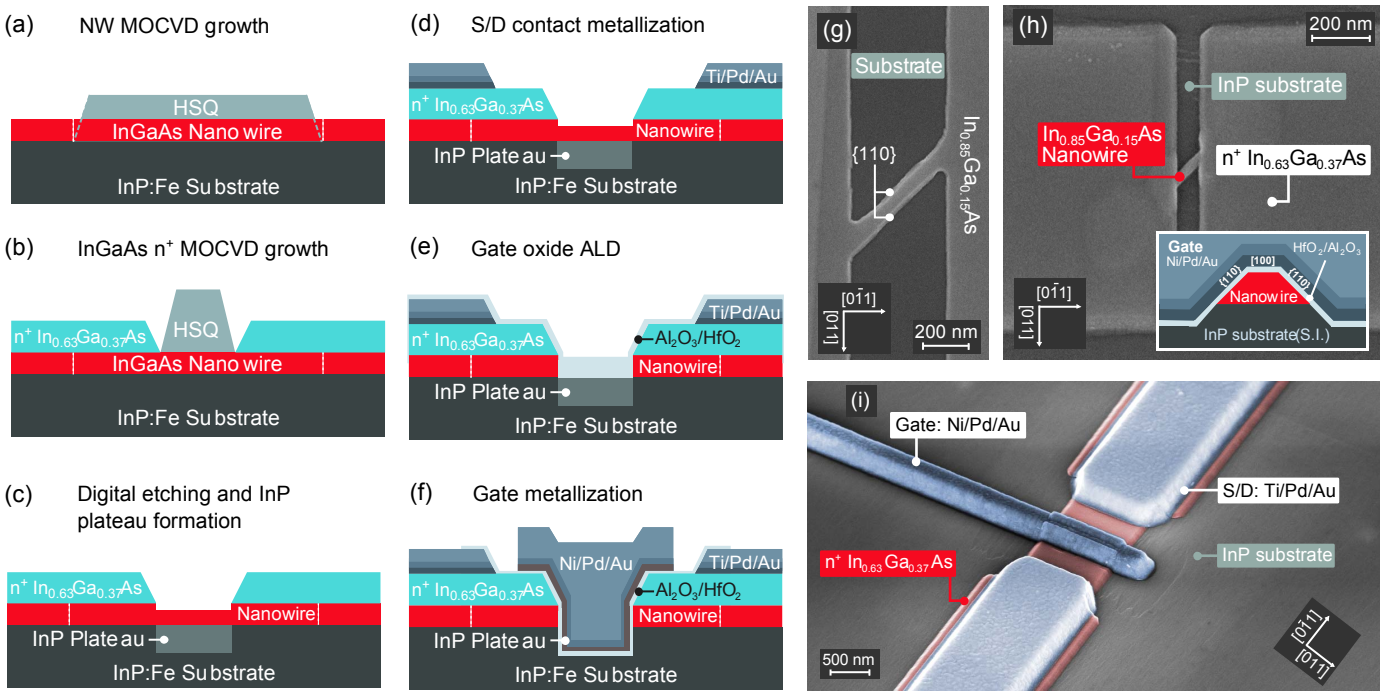

Fig. 1: Schematic figures SEM images of the device fabrication process. (a) NW formation utilizes selective area MOCVD growth with an EBL-defined HSQ hard mask. (b) Contacts are defined using an HSQ dummy gate and MOCVD regrowth of n^+ $In_{0.63}Ga_{0.37}As$. (c) NW is scaled down using "digital etching". (d) S/D metal is deposited by evaporation and lift-off. (e) A bilayer of Al_2O_3/HfO_2 is used as the gate oxide. (f) Ni/Pd/Au is evaporated as the gate metal. (g) SEM image of a 90 nm wide NW with the {110} side facets denoted. (h) The device after contact regrowth. Inset shows a schematic cross-section of the NW in the finished device. (i) False-color SEM image of the finished device. The NW is located at the center of the 1 µm wide mesa.

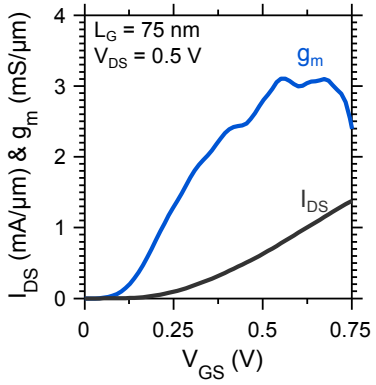

Fig. 2. Transfer characteristics for a device with W_{NW} = 25 nm.

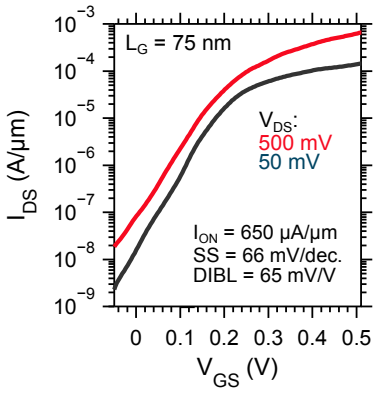

Fig. 3: Subthreshold characteristics for the same device as in Fig. 2.

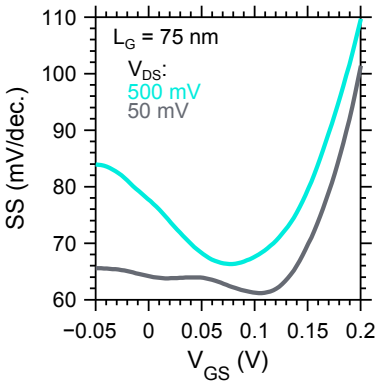

Fig. 4: Subthreshold slope versus V_{GS} for the same device as in Fig. 2.

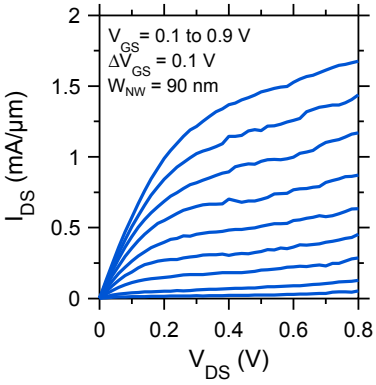

Fig. 5: Output characteristics for a device with L_G = 75 nm and W_{NW} = 90 nm.

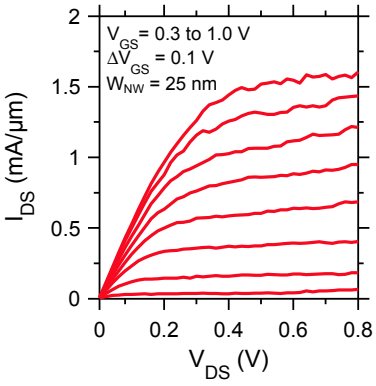

Fig. 6: Output characteristics for a device with L_G = 75 nm and W_{NW} = 25 nm.

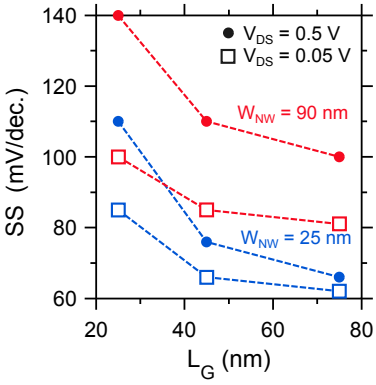

Fig. 7: Subthreshold slope for devices with different W_{NW} and L_G.

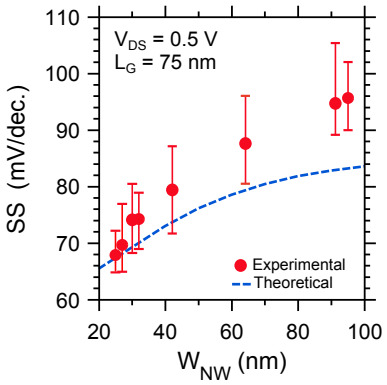

Fig. 8: Subthreshold slope versus W_{NW} at V_{DS} = 0.5 V and L_G = 75 nm.

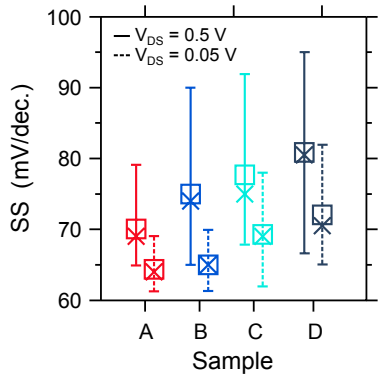

Fig. 9: Mean (squares) and median (crosses) *SS* for different samples.

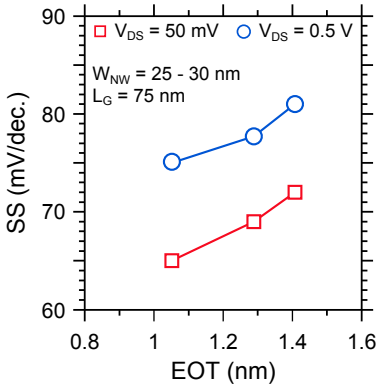

Fig. 10: Average subthreshold slope (each point is ~40 devices) versus EOT.

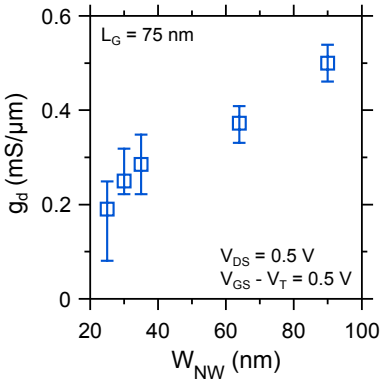

Fig. 11: Output conductance versus W_{NW}, measured at $V_{DS} = V_{GS} - V_T$ = 0.5 V.

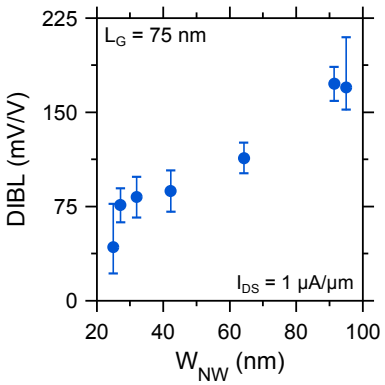

Fig. 12: DIBL versus W_{NW} measured at I_{DS} = 1 μA/μm.

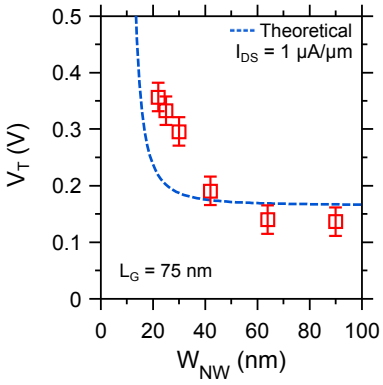

Fig. 13: Threshold voltage versus W_{NW}. Dashed traces show a QW model.

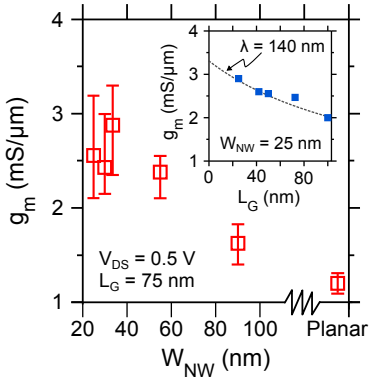

Fig. 14: Peak g_m versus W_{NW} and (inset) L_G, all measured at V_{DS} = 0.5 V.

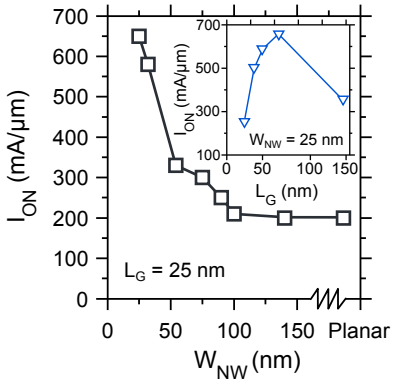

Fig. 15: I_{ON} versus W_{NW} and L_G at I_{OFF} = 100 nA/μm.

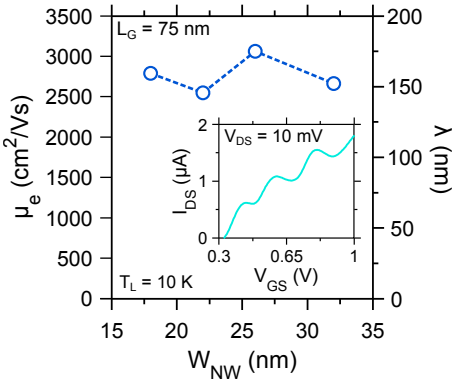

Fig. 16: μ_e and λ, measured from quantized current (inset), versus W_{NW}.

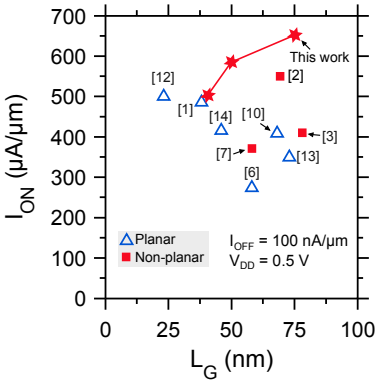

Fig. 17: Benchmark of I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm.

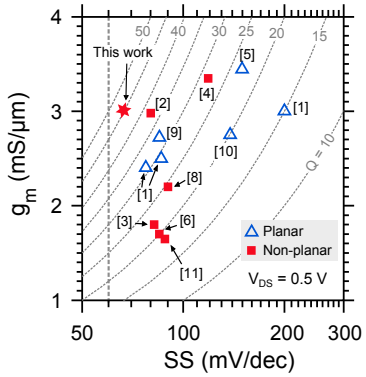

Fig. 18: Benchmark of the quality factor g_m/SS at V_{DS} = 0.5 V.

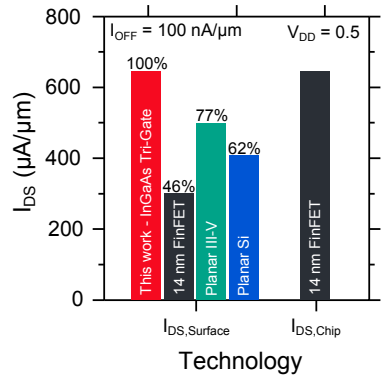

Fig. 19: Benchmark of various technologies.