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High-Performance Lateral Nanowire InGaAs MOSFETs with Improved On-Current

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***Abstract*—We report on $In_{0.85}Ga_{0.15}As$ MOSFETs utilizing selectively grown lateral nanowires as the channel. These devices exhibit on-current of I_{ON} = 565 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, which is higher than all other reported values for III-V FETs. This is enabled by a transconductance of 2.9 mS/µm and a minimum SS_{sat} of 77 mV/decade. A ballistic top-of-the-barrier model is used to model these devices and to predict their ultimate performance, which is approximately twice that of the fabricated devices.**

***Index Terms*—MOSFET, III-V, InGaAs, Nanowire**

I. Introduction

Indium-rich III-Vs have been considered as a replacement for silicon as the channel in CMOS technology [1]. This is due to their excellent electron transport properties, such as high mobility, which enables increased transconductance g_m at a given L_G and may allow a reduction of the supply voltage V_{DD} to 0.5 V. For instance, there have recently been several reports on $In_xGa_{1-x}As$ MOSFETs with g_m of above 3 mS/µm [2]-[3]. However, to achieve high I_{ON} at a specified I_{OFF} and V_{DD} = 0.5 V, which is a primary metric for CMOS applications, the subthreshold slope must be near the thermal limit of 60 mV/decade. This is a challenge in III-V technology due to e.g. the high-k oxide interface quality. Moreover, the narrow band gap of $In_xGa_{1-x}As$ causes, for instance, band-to-band-tunneling in the off-state which makes reaching lower I_{OFF} such as 1 and 10 nA/µm (low-power and general purpose limits, respectively) difficult. For this reason, 3D channel architectures, such as various implementations of FinFETs and Tri-gate devices, are promising to improve electrostatic integrity at scaled down gate-lengths [4].

In this work, we report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs with a tri-gate architecture and a record I_{ON} of 565 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, together with a combination of g_m = 2.9 mS/µm and minimum SS of 77 mV/decade. Compared to our previous work, we have here optimized the nanowire dimensions, as well as examined the influence of gate length scaling [5]. We also explore the ultimate potential of these devices by comparing with a modeled fully ballistic device.

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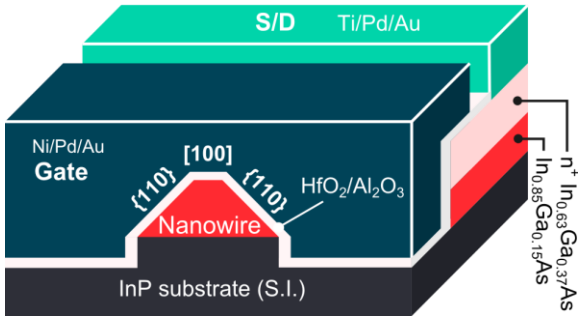

Fig. 1. Schematic figure of the fabricated device. The crystal facet are deduced from facet angels and the NW orientation.

TABLE I
COMPARISON OF THEORETICAL PERFORMANCE WITH RECORD FABRICATED III-V DEVICES

Metric	Experimental	Theoretical
I_{ON} (I_{OFF} = 100 nA/µm)	565 µA/µm	1200 µA/µm
I_{ON} (I_{OFF} = 10 nA/µm)	360 µA/µm [5]	930 µA/µm
I_{ON} (I_{OFF} = 1 nA/µm)	---	670 µA/µm
$g_{m,peak}$ (V_{DS} = 0.5 V)	2.9 mS/µm	6 mS/µm
SS_{min} (V_{DS} = 0.05 V)	68 mV/dec.	60 mV/dec.
SS_{min} (V_{DS} = 0.5V)	77 mV/dec.	60 mV/dec.

II. Device Fabrication

Lateral $In_{0.85}Ga_{0.15}As$ nanowires (NWs) are formed on semi-insulating InP:Fe (100) by selective area growth using hydrogen silsequioxane (HSQ) as a hard mask, as described elsewhere [6]. The composition of the NWs is determined by optical characterization [7]. The direction of the NW is ⟨010⟩. The main focus of this work is on devices consisting of a single NW with width, W_{NW}, and height of 28 and 8 nm, respectively, and with gate length, L_G, of 75 nm. To explore the scaling properties, devices with L_G = 50 – 150 nm, and W_{NW} = 28 – 140 nm are also fabricated. A 30 nm highly doped $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) raised contact layer is regrown using an HSQ dummy gate hard mask. The direction of the dummy gate is ⟨110⟩. Subsequently, the InP in the channel is etched down by HCl solution. This is to ensure proper gating of the lower edge of the nanowire. The dimensions of the nanowire are reduced by 4 cycles of Ozone oxidation and diluted HCl oxide etch. 50 nm Ti/Pd/Au

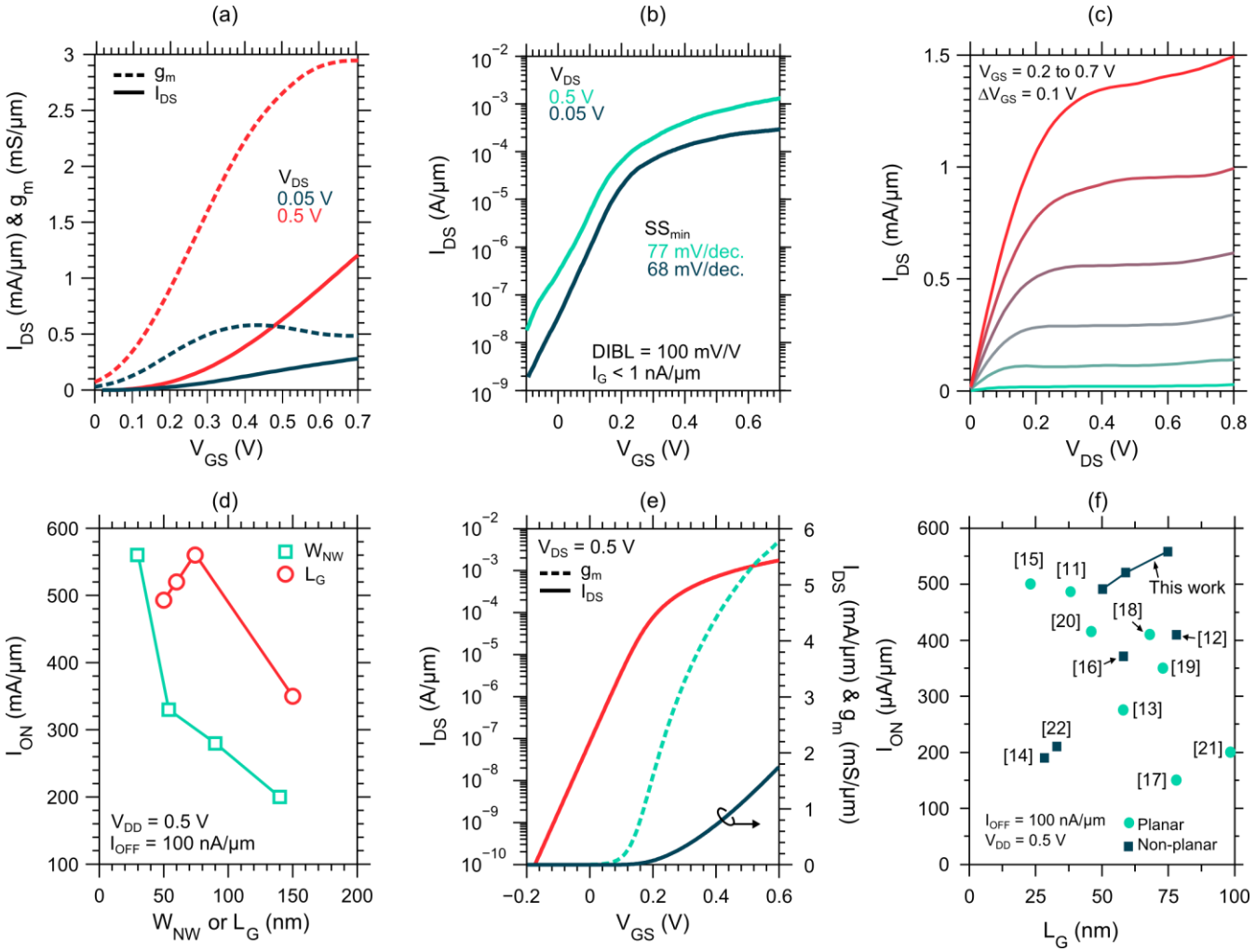

Fig. 2. (a) Transfer, (b) subthreshold and (c) output characteristics of the same L_G = 75 nm device. (d) I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 versus W_{NW} (squares) and L_G (circles). Squares have a fixed L_G = 75, and circles have a fixed W_{NW} = 28 nm. (e) Transfer and subthreshold performance of a fully ballistic ideal device using a top-of-the-barrier model. (f) A benchmark of I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V for state-of-the-art III-V planar and non-planar MOSFETs.

source/drain metal is deposited by thermal evaporation. Prior to ALD deposition of Al_2O_3/HfO_2 (10/40Å, EOT ≈ 1.5 nm) at 300/100°C, sulphur passivation in $(NH_4)_2S$ (10%) is performed for 20 min. Following, an in-situ post-deposition annealing step is performed at 100°C for 12 hours in N_2 atmosphere, which is found to improve the subthreshold slope. Finally, 150 nm Ni/Pd/Au is patterned and thermally evaporated as the gate-metal and gate pad using lift-off. Since the gate was defined in the contact regrowth step, gate metallization is self-aligned. Fig. 1 shows a schematic image of the fabricated device, and the facets of the NW, which have 45° facet angles, as we have previously shown [7]. The distance between S/D contact metal and the gate is 700 nm. The width of the contacts is 1 μm.

III. Results

Fig. 2(a)-(b) show transfer and subthreshold characteristics for a device with L_G = 75 nm. The data is normalized to the gated perimeter according to the shape in Fig. 1. The peak transconductance is g_m = 2.9 mS/μm at V_{DS} = 0.5 V. Minimum inverse subthreshold slope (SS_{sat}) is 77 mV/decade, and the drain-induced barrier lowering (DIBL), measured at I_{DS} = 1 μA/μm, is 100 mV/V. The gate-leakage current I_G is below 1 nA/μm. At V_{DS} = 50 mV, minimum SS is 68 mV/decade. The on-current, measured as I_{DS} at a fixed voltage swing of 0.5 V from I_{OFF} = 100 nA/μm and V_{DS} = 0.5 V, is I_{ON} = 565 μA/μm. The output characteristics of an L_G = 75 nm device is shown in Fig. 2(c). The on-resistance is R_{ON} = 180 Ωμm, and the contact resistance is approximately R_C = 20 Ωμm, as determined from transmission line measurements.

Fig. 2(d) shows I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 versus both the width of the nanowires, W_{NW} (with L_G = 75 nm for all devices) and L_G (with W_{NW} = 28 nm for all devices). I_{ON} significantly improves as W_{NW} is scaled down from 140 nm to 28 nm, which is primarily due to an improvement of SS, from > 100 mV/decade to approximately 80 mV/decade, as an effect of improved electrostatic control. The optimal I_{ON} is found at L_G = 75 nm for these devices. At shorter L_G, short-channel effects begin to degrade performance through a degradation of the subthreshold slope. This can be offset by, e.g. further scaling of the NW. The peak transconductance is

weakly increasing with the reduction of gate length.

The ideal device performance was calculated using a fully ballistic top-of-the-barrier model and is shown in Fig. 2(e). The gate length is assumed long enough to suppress any short channel effects. For the evaluation of device density of states, a 2-band non parabolic quantum wire model was used [8]. Quantum well band bending was approximately taken into account through a first order perturbation scheme.

The nanowire was modeled as a 28 × 8 nm rectangular wire (which is more voluminous than the fabricated NWs, due to their 45° facet angles), with a bulk effective mass $m^* = 0.027m_0$ and a bulk bandgap of E_g = 0.44 eV, roughly corresponding to $In_{0.9}Ga_{0.1}As$. The oxide capacitance was calculated from the tri-gate configuration, with t_{ox} = 4.7 nm and $\varepsilon_{r,ox}$ = 15.9 [9]. Extrinsic resistances are 0 Ω.

Ideal nanowire device performance is compared to that of fabricated III-V MOSFETs with record I_{ON} in table 1. Currently, I_{OFF} = 1 nA/µm has not been demonstrated experimentally in non-planar InGaAs MOSFETs. The g_m and SS values are those reported in this work. Ideal g_m and I_{ON} (at 100 nA/µm) are 6 mS/µm and 1200 µA/µm, respectively. The difference of about a factor 2 compared to our devices is explained mainly by quasi-ballistic transport, e. g. a transmission less than 1, as well as non-ideal electrostatics partly due to traps (D_{it}), in the fabricated devices [10]. We have previously shown that the transmission, *T*, in devices similar to those reported here is approximately 70% [7]. Therefore, to improve device performance, device dimensions, W_{NW} and L_G must be optimized, EOT must be reduced and the oxide interface quality improved. *T* is inversely proportional to L_G, and W_{NW} also influences *T* since smaller W_{NW} typically correlates to lower mobility and mean free path.

Finally, we benchmark our results with state-of-the art III-V planar and non-planar MOSFETs [Fig. 1(f)] [11]–[22]. The I_{ON} (at 100 nA/µm) of 565 µA/µm reported in this work is the record value for both planar and non-planar devices.

IV. Conclusion

We have reported $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs with record I_{ON} at 100 nA/µm. This was enabled by a transconductance of 2.9 mS/ µm and minimum SS of 77 mV/decade. We also compared record III-V MOSFET performance to an ideal fully ballistic device using a top-of-the-barrier model. Fabricated device performance was found to have reached approximately half of that of the ideal device.

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