

Design Space Exploration of Digital Circuits for Ultra-low Energy Dissipation

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Energy dissipation of a circuit is of utmost importance in the cellular or medical implanted devices. As the operations in these devices depend on the energy that can be provided by the battery encased with them. The energy measure is most important in determination of best suited design for an electronic device that is to be used in medical implants. The relation between dynamic energy and the supply voltage V_{DD} leads to the fact that supply voltage reduction yields quadratic reduction in energy dissipation. This is one of the most effective knob to play with when reduction in energy is needed. The side effect of V_{DD} reduction is an increase in the delays of the gates or the designed circuit. Rigorous voltage supply scaling is employed to achieve low energy dissipation. This reduces the ratio between on-current I_{on} and off-current I_{off} in the transistor. Hence, the transistor operates in the sub-threshold (sub- V_T) domain or weak inversion region.

In order to exhaustively analyze the energy dissipation and the critical path delay of a given design with a certain architectures, a gate-level sub- V_T characterization flow is applied. The benefit of such a flow is that it characterizes the circuit with respect to the sub- V_T domain. This characterization is necessary as the energy minimum operating point (E_{min}) lies somewhere in sub- V_T domain, as shown in the Figure 1. This shows, that the dynamic energy (E_{dyn}) scales down quadratically with the scaling of supply voltage V_{DD} . On the other hand, the leakage energy increase exponentially at lower voltages, this is due to the fact that the gates become very slow and leakage dominates throughout the circuit. Therefore, there lies a sweet spot for the total energy dissipation (E_T), where the sum of dynamic energy and leakage energy amounts to a local minimum, which is described as the energy minimum voltage point (EMV).

This work include a proposed energy model for designs to be characterized for sub- V_T domain operation. The present model encompasses single V_T implementations and

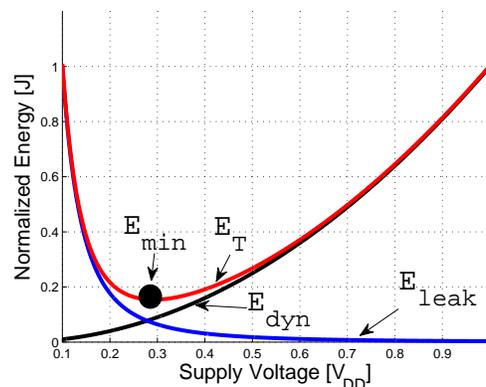


Figure 1: Energy Dissipation in circuit

multi- V_T implementations. The energy modeling is based on the 65 nm CMOS standard cells provided by the technology vendor. The energy model has been used to evaluate various techniques and constraints for a circuits operated in the sub- V_T domain. The work describes how the energy dissipation of architectures vary w.r.t. switching activity, μ_e . The simulation results based on the sub- V_T energy model, show that higher μ_e in a given design causes high energy dissipation that in turn moves the energy minimum voltage point (EMV) to lower voltages.

Deep pipelining together with supply voltage scaling have high benefits with respect to energy dissipation. The simulation results based on the sub- V_T energy model, show that designs with high combinational logic gates the pipeline reduce the switching activity μ_e , furthermore, there is reduction in leakage currents. All of these reductions result in the form of low energy dissipation in sub- V_T domain.

Four half band digital (HBD) filter structures are evaluated for minimum energy dissipation in the sub- V_T domain for a throughput constrained system. All architectures i.e., unfolded by 2,4,8, and the basic HBD filter, are implemented and simulated using 65 nm Low-Leakage High-Threshold (HVT) standard cells. The application of a sub- V_T energy model reveals that it is beneficial to use unfolded implementation to achieve low energy dissipation per sample at EMV, when compared to the energy dissipated by a basic simplified HBD filter implementation. However, there is a limit to the unfolding factor, where the energy dissipation benefits start to diminish.

In order to examine the effect of various available threshold options all filter structures are implemented and simulated using 65 nm HVT, Standard-Threshold (SVT) and Low-Threshold (LVT) standard cells. Secondly, the design space is increased by utilization of a combination of HVT + SVT and also HVT + LVT cells. The analysis with sub- V_T energy model leads to the conclusion that different architectures are suitable for different constraints. A suitable design is a synergy between parallelism, and utilization of various threshold options. However, with stringent low energy dissipation requirements combined with moderate throughput requirements unfolded architectures synthesized with SVT cells are the most appropriate option. In this analysis the multi- V_T , implementations did not show a major advantage over single V_T implementations.

The simulation results are validated by silicon measurements and demonstrate that low-power standard threshold logic (SVT) and different architectural flavors are suitable for a low-power implementation. Silicon measurements prove functionality down to 350 mV supply, with a maximum clock frequency of 500 kHz, having an energy dissipation of 102 fJ/cycle.

Finally, a dual- V_T (DVT) approach is shown to results both in higher performance and reliability. The Signal-to-Noise Margin (SNM) of the NAND3 and NOR3 gates show an improvement of 47% over the same setting with standard-cell library (SCL) gates. The overall performance gain of a DVT-inverter and DVT-NAND3 gates is 45 % and 67 %, respectively, compared to the gates in the SCL. Furthermore, the Monte-Carlo simulations confirm a lower worst-case delay and noise-margins. Additionally, the proposed technique is highly area efficient.