# Effect of Gate Oxide Defects on Tunnel Transistor RF Performance

Hellenbrand, Markus; Memisevic, Elvedin; Svensson, Johannes; Krishnaraja, Abinaya; Lind, Erik; Wernersson, Lars-Erik

*Published in:*
2018 76th Device Research Conference (DRC)

*DOI:*
10.1109/DRC.2018.8442145

2018

*Document Version:*
Peer reviewed version (aka post-print)

# Effect of Gate Oxide Defects on Tunnel Transistor RF Performance

M. Hellenbrand, E. Memisevic, J. Svensson, A. Krishnaraja, E. Lind, and L.-E. Wernersson
*Lund University, Department of Electrical and Information Technology*
*Ole Römers väg 3, 22363 Lund, Sweden*
*Email: markus.hellenbrand@eit.lth.se*

**Overview**
Tunnel field-effect transistors (TFETs) are designed for low off-state leakage and low drive voltages. To investigate how capable TFETs are of RF operation, we measured their scattering parameters and performed small-signal modeling. We find that in the low frequency ranges, gate oxide defects have a major influence on the RF performance of these devices, which can be modeled by a frequency-dependent gate-to-drain conductance $g_{gd,\omega}$. This model is based on charge trapping in gate oxide defects and was studied before for metal-oxide-semiconductor capacitors [1].

**Devices and Measurement**
All TFETs in this work are based on vertical III-V nanowire structures. To achieve sufficiently high RF gain, all measured devices consisted of arrays of up to 2000 nanowires. Arrays this large deteriorate the inverse subthreshold slope $S$ from typical values below 60 mV/decade for devices with only a few nanowires to about 75 to 200 mV/decade (Fig. 1(b)). The maximum intrinsic transconductance for most of the measured RF devices was about 113 µS/µm at $V_{DS}$ = 0.5 V. A schematic structure of one nanowire inside an array is depicted in Fig. 1(a) and details about the fabrication can be found in [2] and [3]. The RF measurement setup was calibrated off-chip, all measurements were de-embedded by dedicated open and short structures on the respective sample, and modeling was performed according to the model in Fig. 1(c), which also presents representative values for all small-signal parameters. The difference in the real parts of the $y$-parameters with and without frequency dependence is evident in Fig. 2(a).

**Modeling and Physical Explanation**
Electrons can tunnel into and out of gate oxide defects from the channel and from the gate contact, and the tunnel time constant of this process, modeled as the frequency-dependent conductance $g_{gd,\omega}$, causes a phase shift relative to the small-signal voltage excitation. Above a certain frequency, the time constants of all defects is too long for the defects to respond to the small-signal excitation so that the effect decreases at higher frequencies. The phase shift effectively constitutes a loss in the RF power gain $U$ (clearly visible in Fig. 2(c)) and a shift of the real parts of the $y$-parameters (Fig. 2(a)). This sensitivity to oxide defects can be used as a general material characterization method. In the case of TFETs, a frequency dependence only occurs in $g_{gd}$, not in $g_{gs}$, and with the example of $\mathrm{Re}(y_{11}) \approx \omega\, g_{gd,\omega} + \omega^2 (C_{gs}+C_{gd})^2 R_g$ with the parameters from the model in Fig. 1(c) (without $R_s$ and $R_d$), the shift from the frequency-dependent part of $g_{gd}$ is evident. Constant contributions to $g_{gd}$ or $g_{gs}$, representing gate leakage, were found to be negligible besides the frequency-dependent component of $g_{gd}$.
The asymmetry between source and drain provides insight into the charge distribution and transport mechanism of TFETs, since it indicates that the tunnel junction on the source side decouples the small-signal responses between source and channel. Furthermore, it indicates that the majority of the channel charge is supplied by the drain side, since increasing $V_{DS}$ depletes the drain side of the channel of charge so that the same variation due to gate oxide defects has less impact and $g_{gd,\omega}$ decreases (Fig. 3(a)). The opposite happens when the amount of charge in the channel is increased by increasing the gate bias $V_{GS}$ for a constant $V_{DS}$. This lowers the barrier from the drain towards the channel, allowing more charge carriers to enter the channel, and $g_{gd,\omega}$ increases with the charge (Fig. 3(b)).
The same asymmetry between source and drain and the same bias dependence were observed for the intrinsic capacitances in TFETs, where the gate-to-source capacitance $C_{gs}$ turned out to be much smaller than the gate-to-drain capacitance $C_{gd}$[4]. Different from $g_{gd,\omega}$, however, the intrinsic $C_{gd}$ eventually becomes zero at high $V_{DS}$ or low $V_{GS}$, when the channel is completely depleted of charge. The reason why $g_{gd,\omega}$ does not become zero in the same manner is probably the large parasitic capacitance between the gate metal contact and the n+ InAs drain layer (cp. Fig. 1). Since the gate oxide is not only adjacent to the channel, but also to the gate-drain spacer, there are parasitic losses in these layers as well, which remain present even when the channel is depleted of carriers.

In summary, we have analyzed and explained the effect of gate oxide defects on the RF performance of TFETs.

[1] Y. Yuan et al., IEEE-EDL, vol. 32, p. 485, (2011).
[2] E. Memisevic et al., Nano Lett., vol. 17, p. 4373, (2017).
[3] E. Memisevic et al., IEEE-TED, vol. 64, p. 4746, (2017).
[4] M. Hellenbrand et al., submitted to IEEE-EDL, (Feb. 2018).
This work was supported in part by the Swedish Foundation for Strategic Research and the Swedish Research Council, and in part by the European Union Seventh Framework Program E2SWITCH under Grant 619509.

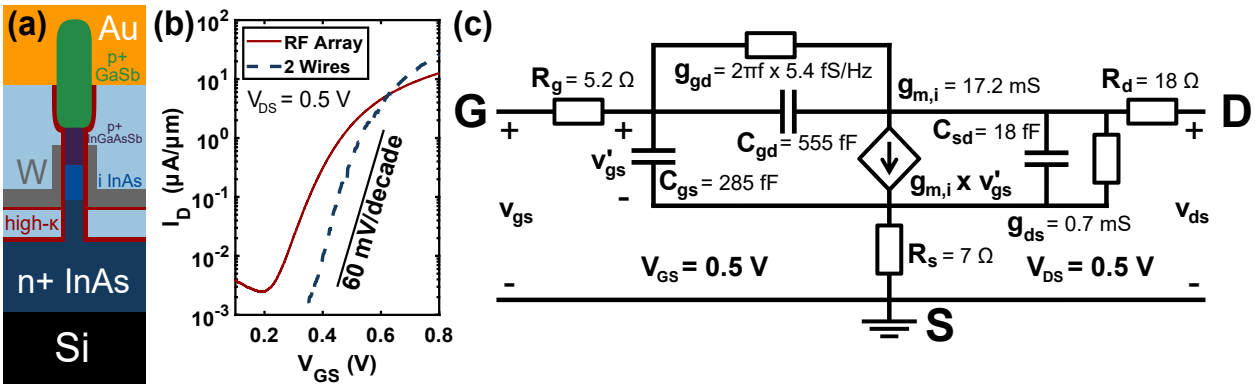


Fig. 1: (a) Schematics of a single nanowire inside an array. (b) Example transfer curves for an RF array (minimum $S$ = 75 mV/decade) and a device with two nanowires (minimum $S$ = 53 mV/decade). (c) Small-signal model with representative values. Note the frequency dependence of $g_{gd}$ and the absence of $g_{gs}$.

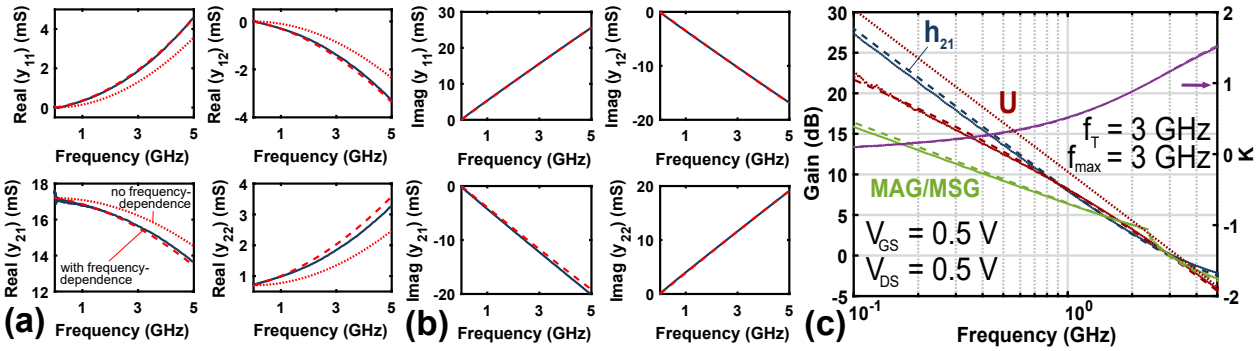


Fig. 2: Full small-signal model for a TFET, solid lines are the measured values. (a) Real parts of the $y$-parameters with and without frequency dependence as red, broken and red, dotted lines, respectively. The difference is clearly visible. (b) Imaginary parts not affected by frequency-dependence. (c) The unitary power gain $U$ is greatly affected by the frequency dependence in $g_{gd}$, but MAG, MSG, and $h_{21}$ remain unchanged.

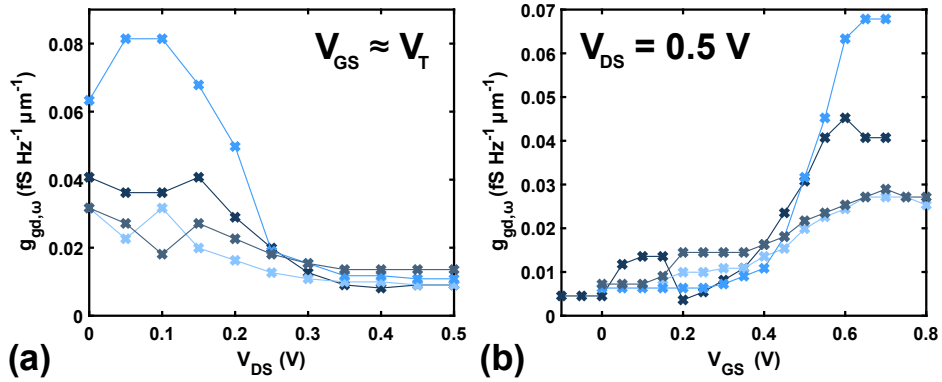


Fig. 3: Bias dependence of the frequency-dependent parts of the small-signal conductances, normalized to the total gate width. Different curves represent different transistors. (a) $g_{gd,\omega}$ decreases with increasing $V_{DS}$ because the drain side of the channel is depleted and the variations due to gate oxide defects have less impact. (b) $g_{gd,\omega}$ increases with increasing $V_{GS}$, since charge is accumulated in the channel.