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2018

Document Version:
Peer reviewed version (aka post-print)

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I. INTRODUCTION

Due to their ability to reach steeper inverse subthreshold slopes S than conventional metal-oxide semiconductor field-effect transistors (MOSFETs), tunnel FETs (TFETs) are promising candidates to play an important role in low-power electronics such as for example Internet of Things (IoT) applications. For RF operation, an outstanding off-state, and thus S, is not critical, but it will be for IoT applications that are not active all the time. To investigate the suitability of our TFETs for RF applications and to facilitate the optimisation of TFET RF properties, we performed scattering parameter (s-parameter) measurements on vertical III-V nanowire TFETs. The tunnel junction in the measured transistors was realised by an InGaAsSb/InAs heterostructure, which resulted in sub-60 mV/decade operation for transistors with only a few nanowires [1]. To compensate for the low currents in TFETs and to enable measurable RF gain, transistors with arrays of 2000 nanowires needed to be fabricated. Due to processing and growth variations, not all of the nanowires exhibited the same threshold voltage [2] so that the inverse subthreshold slope was degraded to values between 75 and 200 mV/decade in the RF transistors.

II. RESULTS

The measurement setup was calibrated off-chip and open and short structures were fabricated on-chip to de-embed the metal contact pads of the transistors. Fig. 1 and 2 summarise the measurement results [3]. Excellent agreement between measured and modelled values (e.g. gains and stability factor in Fig. 1(b)) was achieved at all bias points, which allows the accurate determination of the intrinsic small-signal parameters. Fig. 2 presents a detailed study of the intrinsic gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs}, both for varying gate-to-source voltages V_{GS} (Fig. 2(a)) and drain-to source voltages V_{DS} (Fig. 2(b)). It is obvious that for changes

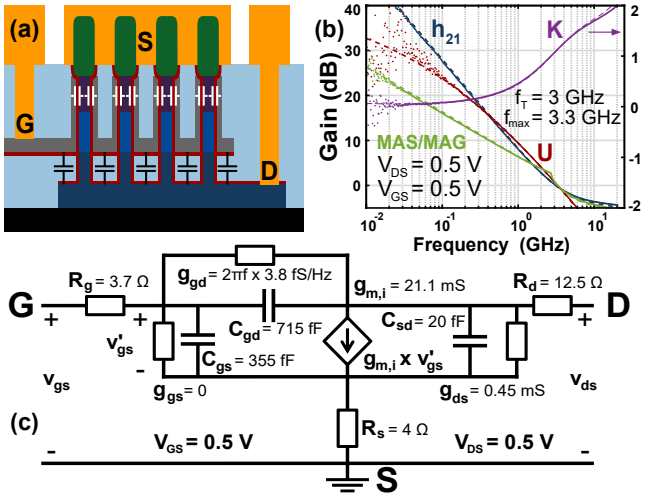

Fig. 1. (a) Schematic layout of the measured TFETs. The capacitor symbols indicate the largest parasitic contributions. (b) Measured and modelled gains for a TFET. (c) Small-signal model with example values.

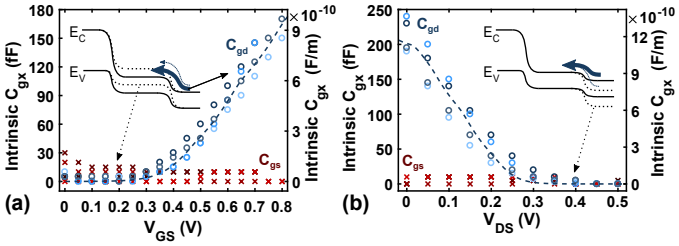

Fig. 2. Intrinsic capacitances as a function of (a) V_{GS} and (b) V_{DS}. The insets schematically show the energy band diagrams for different bias points; broken lines for low and solid lines for high capacitances. Broken lines for C_{gd}: Modelled intrinsic values.

in both voltages, C_{gd} largely dominates over C_{gs}, which constitutes a large Miller capacitance with detrimental effects on circuit applications. The large C_{gd} also limits the maximum cut-off frequency f_T and the maximum oscillation frequency f_{max} to values of about 3 GHz (Fig. 1(b)). The origin of the capacitance asymmetry is the tunnel junction, which effectively decouples source and channel, whereas on the drain side, electrons respond much more directly to variations in the small-signal bias. This behaviour can easily be modelled, the result of which is plotted as broken lines in Fig. 2. Fig. 1(c) provides the small-signal model that was used for parameter extraction along with example values.

Different from Fig. 2, which only shows the intrinsic C_{gs} and C_{gd}, the values provided in Fig. 1(c) also contain the parasitic components of the capacitances, the origins of which are the too thin bottom spacer (for C_{gd}) and an overlap of the gate over the InGaAsSb source segment (for C_{gs}). The first optimisation step for both will consist in increasing and decreasing the spacer thickness and the overlap, respectively. The intrinsic C_{gd} can be reduced by a reduction of the channel length. The third major factor limiting f_T and f_{max} besides the two capacitances is the frequency dependence of the gate-to-drain conductance g_{gd}, the origin of which most likely are gate oxide defects. Minimising these three while maintaining a constant transconductance, should increase f_T and f_{max} to about 40 to 50 GHz.

III. CONCLUSIONS

By means of s-parameter measurements, we identified the origins of three of the major limiting factors of high-frequency TFET operation. To the first degree, all three can be optimised straightforwardly, which emphasizes the suitability of TFETs as low-power electronics components.

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