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A Filtering Technique to Lower *LC* Oscillator Phase Noise

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Abstract—Based on a physical understanding of phase-noise mechanisms, a passive *LC* filter is found to lower the phase-noise factor in a differential oscillator to its fundamental minimum. Three fully integrated *LC* voltage-controlled oscillators (VCOs) serve as a proof of concept. Two 1.1-GHz VCOs achieve −153 dBc/Hz at 3 MHz offset, biased at 3.7 mA from 2.5 V. A 2.1-GHz VCO achieves −148 dBc/Hz at 15 MHz offset, taking 4 mA from a 2.7-V supply. All oscillators use fully integrated resonators, and the first two exceed discrete transistor modules in figure of merit. Practical aspects and repercussions of the technique are discussed.

Index Terms—Analog integrated circuits, CMOS oscillators, noise filtering, optimization, phase noise, radio frequency, spiral inductors, voltage-controlled oscillators.

Fig. 1. Basic *LC* oscillator. (a) Ideal negative resistance. (b) Nonlinear negative resistance.

I. INTRODUCTION

A SINGLE-CHIP radio remains a challenging problem due to technology limitations on passive component quality and lack of efficient optimization procedures. Of all RF blocks, voltage-controlled oscillators (VCOs) have received the most attention in recent years, as evidenced by the large number of publications reporting improved performance [1], [2], higher operating frequency [3], or use of a different passives technology to achieve the stringent requirements of wireless standards [4]. Integrated oscillator circuits published so far use tuning inductors that are either fully integrated, partly integrated, or discrete, with quality factors spanning a large range. However, lacking a clear understanding of the physical processes of phase noise, it is difficult to compare the relative merits of these VCOs in a normalized sense.

In this paper, we present a technique to lower the phase noise of differential oscillators to its fundamental minimum permitted by the resonator quality factor and allocated power consumption. The technique is based on a recently attained understanding of physical processes of phase noise in differential oscillators [5].

In Section II, we look at the bare-bone oscillator design problem starting from first principles. Section III discusses the particular features of current-biased differential *LC* oscillators, while Section IV describes the filtering technique proposed. Sections V and VI are concerned with the efficient implementation of the *LC* passives to achieve best performance. In Section VII, measurement results from three different oscillators are presented as a proof of concept to the technique

presented in Section IV. A discussion of the results and extensions to this work are discussed in length in Section VIII.

II. FUNDAMENTALS OF *LC* OSCILLATORS

Phase noise in *LC* feedback oscillators is usually captured by Leeson's proportionality [6]

$$\mathcal{L}(\omega_m) \propto \frac{1}{V_0^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{Q} \cdot \frac{1}{\omega_m^2}. \tag{1}$$

In this formulation, phase noise is given as kT/C noise that is shaped in frequency by the *LC* tank and normalized to the power in the oscillation amplitude. Phase noise is scaled by a circuit specific noise factor F, the constant of proportionality that comprises noise contributions from various circuit elements. Being circuit specific, the noise factor F needs to be identified for each oscillator topology in terms of device sizes, current, and other circuit parameters.

The noise factor of an *LC* oscillator is analogous to the noise factor of any other RF circuit. The difference, however, is that in *LC* oscillators, the noise factor is equal to the total oscillator phase noise normalized to phase noise due to the resonator loss, whereas in other RF circuits, the noise factor is the total noise of the circuit normalized to the noise of the system characteristic impedance, usually 50 Ω.

An ideal *LC* oscillator is composed of an inductor and a capacitor. The noise factor of such a circuit is equal to one if the tank is lossless, while the oscillator has no phase noise since the tank quality is infinite. Since practical *LC* tanks are lossy, a means of providing negative resistance is required to sustain the oscillation. Consider the oscillator shown in Fig. 1(a), where
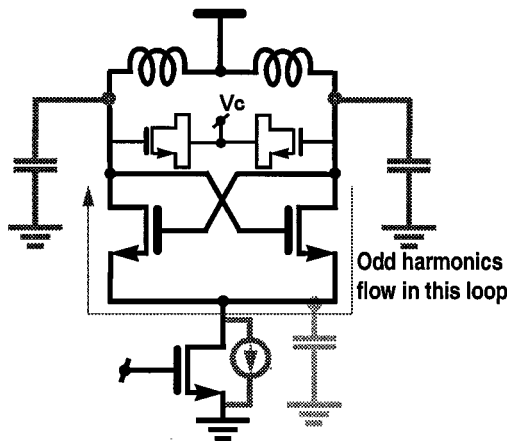
Fig. 2.   Current-biased differential *LC* oscillator.

the resonator has a finite loss resistance. An ideal negative resistance compensates the sinewave signal current through the tank loss resistor. The noise of the negative resistance is equal but uncorrelated to the noise in the resonator loss. This gives rise to a noise factor of 2, the sum of the unity noise factors of both resistors. In practice, a nonlinear active circuit, as shown in Fig. 1(b), provides the negative resistance. The average negative resistance over a full cycle is equal to the tank loss even though it might well be operative only over small portions of the oscillation cycle. Assuming the noise factor of the nonlinear active circuit to be γ, the noise factor of the whole oscillator becomes $1 + \gamma$. Note that this is the fundamental minimum noise factor for a negative-resistance *LC* oscillator. As we will show later, bias circuits significantly add to this noise factor.

The cross-coupled differential pair (Fig. 2) gives a small-signal negative differential conductance of $-g_m$ across the tuned circuit. If this overcomes the positive loss conductance of the tuned circuit, then the natural response of the circuit is a growing oscillation eventually limited in amplitude by circuit nonlinearity. When the differential pair is biased at low currents, this nonlinearity stems from bias current exhaustion. Suppose the oscillation amplitude is larger than the voltage required to commutate the differential-pair current, $\sqrt{2}(V_{\mathrm{GS}} - V_{\mathrm{t}})$. The differential pair sustains the oscillation by injecting an energy-replenishing square-wave current into the *LC* resonator. The bandpass resonator responds to the fundamental frequency in the current waveform and rejects harmonics with a differential voltage amplitude of oscillation [7], [8]

$$V_0 = \frac{4IR}{\pi}. \tag{2}$$

In that the amplitude is proportional to the tail current, this is known as the "current-limited" regime. As the tail current is raised in value, the amplitude also rises until, approaching a single-ended amplitude of V_{DD}, negative peaks momentarily force the current-source transistor into triode region. This is a self-limiting process. Raising the gate bias on the current source forces this FET to spend a greater fraction of the oscillation cycle in triode, resulting in no appreciable rise in the amplitude. This is called the "voltage-limited" regime, whose onset is defined by entry of the current-source transistor into triode region.

In a recent paper, Rael has analyzed the physical mechanisms of phase noise at work in the differential *LC* oscillator [5]. He has proven from first principles that Leeson's hypothesized proportionality specified in (1) really holds, and that this oscillator's noise factor F is

$$F = 1 + \frac{4\gamma IR}{\pi V_0} + \gamma \frac{4}{9} g_{m\mathrm{bias}} R \tag{3}$$

where I is the bias current, γ is the channel noise coefficient of the FET (equal to 2/3 for long-channel FET, and larger than that for shorter channels), and $g_{m\mathrm{bias}}$ is the transconductance of the current-source FET.

The expression in (3) describes three noise contributions, respectively, from the tank resistance, the differential-pair FETs, and from the current source. Note that thermal noise in the differential-pair FETs produce oscillator phase noise that is independent of the FET size. In typical oscillators operating at high current levels with moderate-to-high resonator quality factors, the current-source contribution dominates other sources of phase noise.

Suppose that the current-source contribution, the third term, is removed from (3). Since (2) tells us that the oscillation amplitude is directly proportional to the current I, the oscillator noise factor simplifies to its minimum value

$$F_{\min} = 1 + \gamma. \tag{4}$$

This can be understood by considering the circuit in steady state. A cross-coupled differential pair biased at the balance point by an ideal *noiseless* current presents a negative resistance $-g_m$, with a noise voltage spectral density of $4kT\gamma/g_m$ due to the FET pair. However, if the differential pair is switched to one side or the other, there is no differential output noise. Therefore, the oscillation *samples* the FET noise at every differential zero crossing, that is, at twice the oscillation frequency. Meanwhile, the fundamental component of the differential-pair current relative to the oscillation voltage presents a steady-state negative conductance exactly equal to the resonator loss conductance. Fig. 3 shows an equivalent circuit representing these two actions. Noise sampled by the switching differential pairs of mixers is analyzed in [9]. Although the noise is cyclostationary [10], its spectrum is white. The analysis shows that the noise spectral density is the same as that due to a linear resistor R, equal in magnitude to the effective steady-state negative resistance, but with a noise factor of γ:

$$\hat{i}_n^2 = 4kT\gamma \frac{2I}{\pi V_0} = \frac{4kT\gamma}{R}. \tag{5}$$

Referring to Fig. 1(b), it is now evident how (4) arises. In a sensibly designed oscillator circuit, with a supply voltage of about 3 V and moderate bias current, the third term in (3) can raise the noise factor by as much as 75%.

III. ROLE OF THE CURRENT SOURCE

Consider the differential *LC* oscillator where the current source is replaced by low impedance to ground, in the extreme case a short circuit [Fig. 4(a)]. This circuit still produces steady-state oscillation. Let us take a closer look at the roles of
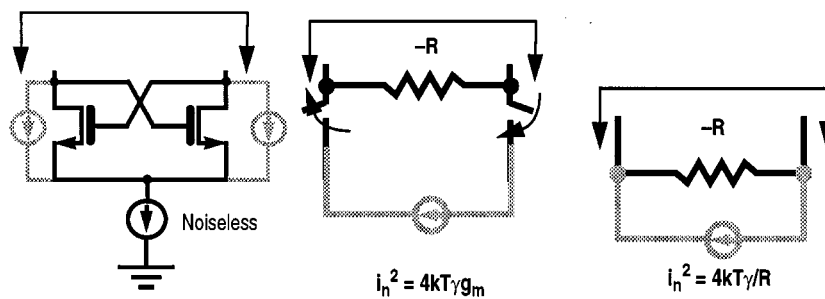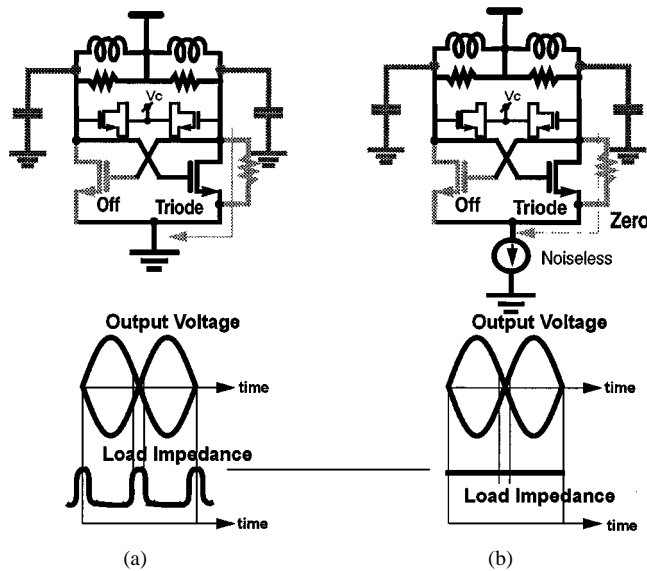
Fig. 3.   Model of the switch noise.

Fig. 4.   Role of the current source. (a) No current source. (b) Ideal noiseless current source.

the two transistors across the oscillation cycle. First, note that the oscillator topology forces V_{GD} of the two FETs to be equal in magnitude but with opposite signs to the differential voltage across the resonator. At zero differential voltage, both switching FETs are in saturation, and the cross-coupled transconductance offers a small-signal *negative* differential conductance that induces startup of the oscillation. As the rising differential oscillation voltage crosses V_t, the V_{GD} of one FET exceeds $+V_t$, forcing it into the triode region, and the V_{GD} of the other FET falls below $-V_t$, driving it deeper into saturation. The g_{DS} of the FET in triode grows with the differential voltage, and adds greater loss to the resonator because the current flowing through it is in-phase with the differential voltage. In the next half cycle, g_{DS} of the other FET adds to resonator loss. The two FETs lower the average resonator quality factor over a full oscillation cycle.

Now, suppose an ideal noiseless current source is present in the tail of the differential pair, as shown in Fig. 4(b). Close to zero differential voltage, the two FETs conduct and present a negative conductance across the resonator. Suppose that in the balanced condition when each FET carries $I/2$, the W/L is chosen such that $(V_{GS} - V_t) < V_t$. When the differential voltage drives one FET into triode, it turns off the other FET. As no signal current can flow through the g_{DS} of the triode FET, this

FET does not load the resonator, thus preserving quality factor of the unloaded resonator. The differential pair injects noise into the resonator only over the short window of time while both FETs conduct. Referring to the earlier analysis, this means that the noise factor is $1 + \gamma$ for phase noise, which is the *fundamental minimum* for a practical oscillator.

Rael's analysis [5] shows how current-source noise creates phase noise in the oscillator. The switching differential pair, which is acting as a single-balanced mixer for noise in the current source, commutates and upconverts low-noise frequencies (modeled by a single tone) into two correlated AM sidebands around the fundamental. Therefore, low-frequency noise in the current source does not directly produce phase noise.[1] Noise frequencies around the oscillation frequency are translated far away from the passband of the tuned circuit. However, noise frequencies around the second harmonic downconvert close to the oscillation frequency, and upconvert to around the third harmonic, where they are rejected by the bandpass characteristic of the *LC* tank. A tone injected into the tuned circuit passband may be decomposed into half AM and half PM sidebands around the oscillation frequency [11]. Thus, fundamentally, half the noise in the current source lying at frequencies close to the second harmonic produces phase noise. Odd harmonics of the commutating waveform might downconvert higher noise frequencies close to the oscillation, but for a first-order calculation, these are ignored because the mean square contributions fall off rapidly $(1/3^2, 1/5^2, 1/7^2, \ldots)$. The role of noise around even harmonics of the oscillation was first noted based on the similarity between the switching pair of an oscillator and a commutating mixer [12], and then on an analysis of the time-domain waveforms [13].

The current source plays a twofold role in the differential *LC* oscillator: it sets the bias current, and it also inserts a high impedance in series with the switching FETs of the differential pair. In any balanced circuit, odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path, through the resonator capacitance and the switching FETs to ground. Therefore, strictly speaking, the current source need only provide high impedance to *even harmonics* of the oscillation frequency, of which the second harmonic is usually dominant. Shrinking the requirement of high impedance to a narrow band of frequencies offers some unique opportunities to realize this concept.

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[1]It does so indirectly. As discussed later, a nonlinear capacitor across the tuned circuit converts AM sidebands into FM, which is phase noise.
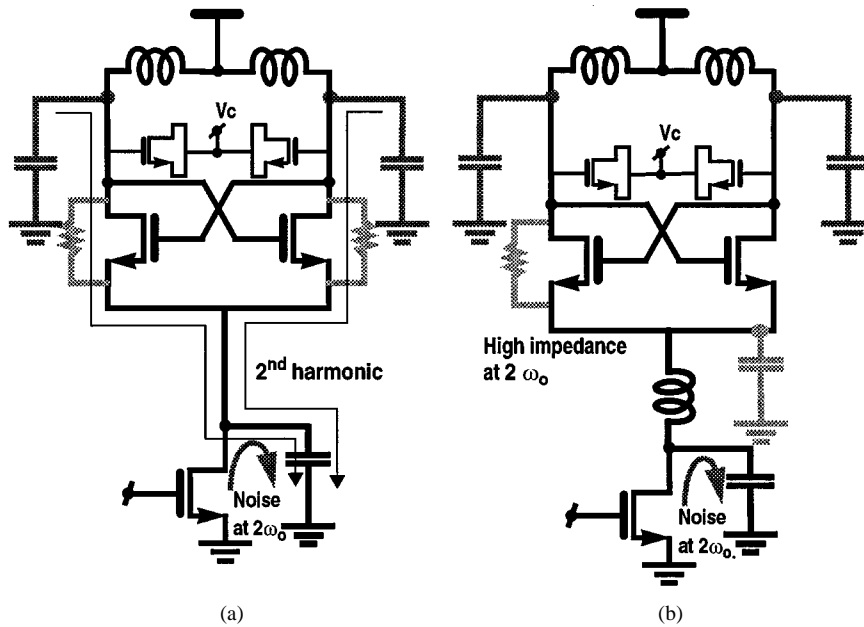
Fig. 5.   Tail-biased VCO with noise filter. (a) Capacitor alone. (b) Complete noise filter.

IV. Noise Filtering

To recapitulate, for the current source: 1) Only thermal noise in the current-source transistor around the second harmonic of the oscillation causes phase noise, and 2) a high impedance at the tail is only required at the second harmonic to stop the differential-pair FETs in triode from loading the resonator. This suggests use of a narrowband circuit to suppress the troublesome noise frequencies in the current source—making it appear noiseless to the oscillator—which gives a high impedance in the narrow band of frequencies where it is important. Placing a large capacitor in parallel with the current source, as shown in Fig. 5(a), shorts noise frequencies around $2\omega_0$ to ground. Then, to raise the impedance, an inductor is inserted between the current source and the tail, as shown in Fig. 5(b). The inductance is chosen to resonate at $2\omega_0$ in parallel with whatever capacitance is present at the common sources of the differential pair. The impedance at the tail is limited only by the quality factor of the inductor. The inserted inductor and the large capacitor comprise what we term a *noise filter*.

A variant of the tail-biased *LC* oscillator described in the literature is the top-biased differential *LC* oscillator, where the current source is connected from the positive supply to the center tap of the differential inductor (Fig. 6). If the junction capacitors to ground are ignored, these two oscillators are identical in that the bias current source is in series with the supply-voltage source, and the position of the two can be exchanged without affecting the circuit topology. However, the two circuits are different when the junction capacitors are included. These differences have some practical consequences. For instance, the top-biased oscillator is more immune to substrate noise because the current source is placed in an n-well, rather than in the substrate. Also, the top-biased oscillator upconverts less flicker noise into phase noise, but further discussion on this is outside the scope of this paper.

One important consequence of the difference is in the noise-filter circuit for the top-biased oscillator. As before, a large ca-
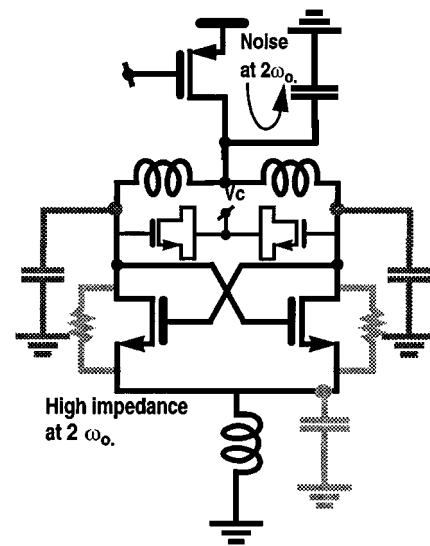

Fig. 6.   Top-biased VCO with noise filter.

pacitor in parallel with the current source shunts noise frequencies around the second harmonic to ground. However, the filter inductor must be inserted at the common source point of the switching pair to resonate in parallel with the capacitance at that node at $2\omega_0$. This blocks second-harmonic current from flowing through the grounded junction capacitors comprising the resonator, and through the switching FETs to ground.

A properly designed noise filter brings down the noise factor of the differential *LC* oscillator to its fundamental minimum of $1 + \gamma$. Once the constant of proportionality F is minimum, (1) prescribes that, given a resonator Q and current limited operation, for least phase noise the oscillation amplitude V_0 must be as large as possible. The positive peak of the oscillation at the drains of the M1, M2 is limited by breakdown. The negative peak can, in principle, be as low as a forward-bias junction voltage below ground. The instantaneous negative voltage
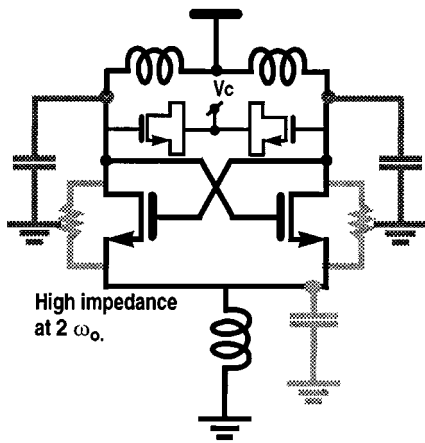
Fig. 7.   Voltage-biased VCO with noise filter.

is absorbed across the filter inductor, and the large filter capacitor holds the V_{DS} constant across the current-source FET, maintaining it in saturation. In practice, the highest differential voltage swing across the *LC* resonator is roughly $2V_{DD}$ peak.

In the extreme, if a very large gate bias is applied to the current-source FET, it is continuously in triode region and almost appears as a short circuit to ground (an example is given in [14]). This reverts to the voltage-biased oscillator [Fig. 4(a)]. Without a noise filter, the FETs will load the resonator throughout the oscillation while the differential resonator voltage is larger than V_t. A noise filter in the tail tuned to the second harmonic removes this loading (Fig. 7). This circuit oscillates with the largest possible amplitude because there is no current-source FET in series with the differential pair to take up voltage headroom. As there is no second harmonic with dc content, the circuit biases at a current that relates to the differential oscillation amplitude according to (2), because whatever this current, it is commutated into the resonator by the periodic FET switching. In other words, with the noise filter the circuit acts as if biased by a tail-current source that consumes zero voltage headroom, yet produces the largest possible amplitude. As a result, the phase noise of this topology is least, although its current is largest.

V. DISCRETE FREQUENCY TUNING

A CMOS oscillator must be designed with a large tuning range to overcome process variations, which create a large spread in the center frequency from wafer to wafer. The simplest way to do so is with a strong varactor, that is, one that gives a large capacitance swing relative to the fixed resonator capacitance as the tuning voltage is swept over its full range limited by the power supply V_{DD}. Irrespective of how the varactor is realized, whether by a MOS capacitor or a p-n junction [15], the larger its area the stronger it is. The resulting high sensitivity of frequency tuning, though, is at the price of worse phase noise.

Varactor capacitance depends continuously on control voltage. Clearly, additive noise on the control voltage will convert through frequency modulation into phase noise sidebands. However, the varactor whose *incremental* capacitance is a function of the instantaneous voltage across it offers an *average* capacitance to the resonator that depends on the envelope

and duty cycle of the oscillating waveform. As described in Section IV, even if the control voltage is noiseless, the varactor will detect envelope fluctuations due to AM noise on the oscillation, and by modulating the *average* capacitance convert this into FM noise [5], [16]. This process may add several decibels to the phase-noise sidebands.

In previous work, we have suggested that by a combining discrete and continuous tuning, it is possible to lower FM sensitivity while spanning a wide tuning range [15]. For instance, a 3-b binary-weighted switched-capacitor array [Fig. 8(a)] tunes the oscillator center frequency to eight discrete frequencies. Then, a small-size MOS varactor interpolates continuously around these frequencies, giving rise to a family of overlapping tuning curves which guarantee continuous frequency coverage over the tuning range, as shown in Fig. 8(b). This requires a mixed analog–digital phase-locked loop (PLL), whose design has been described elsewhere [17] to tune such a VCO operating at a lower frequency.

VI. HIGH-Q RESONATOR INDUCTOR

It was the intent of this work to show how a noise filter can lower phase noise to a record level in a prototype CMOS oscillator with fully on-chip resonator. From (1), it is seen that F must be low (the task of the noise filter), the amplitude V_0 should be large, and the inherent quality factor of the resonator Q must also be large. The latter two yield quadratic improvement in phase noise, and are also related in that the higher the resonator Q, the higher the amplitude for a given bias current. In an entirely integrated resonator, losses in the on-chip spiral inductor usually limit Q.

Before describing the design of the spiral, it is necessary to first specify the IC fabrication process. The ST Microelectronics BiCMOS6M process used here offers four layers of metal, and a substrate resistivity of 15 Ω·cm. The metal-4 film is almost 2.5 μm thick, while the lower layers of metal are all about 0.8 μm thick.

The inductor is designed using a custom fast simulator that models self-inductance, parasitic capacitance, and all losses, including dissipation due to displacement and eddy currents in the substrate [18]. The differential resonator uses a single balanced octagonal spiral with a center tap. Although the obvious geometrical symmetry of this structure is discussed in the literature [19], we believe its main benefit is that it offers higher Q than two independent spirals in series, each of half the required inductance. For the same dimension of the inner hollow area, the differential spiral requires roughly $1/\sqrt{2}$ the length of metal of two spirals in series, which lowers metal loss, and it occupies a smaller footprint over the substrate, which lowers substrate losses.

The balanced spiral in metal 4 implements a total differential inductance of 26 nH, and is optimized for 1.1 GHz. At this frequency, simulation shows that displacement current loss is important in the lightly doped substrate. Simulations also show that a metal-1 patterned shield is more effective in blocking displacement currents from entering the substrate than a polysilicon shield [20]. However, the shield geometry must be designed very carefully because the high conductivity of metal,
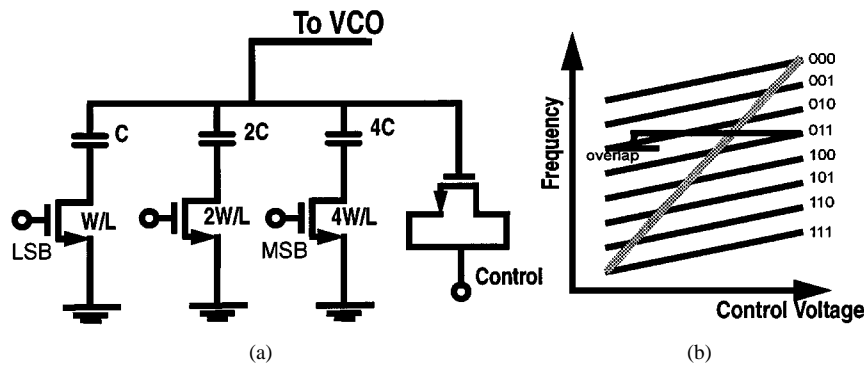
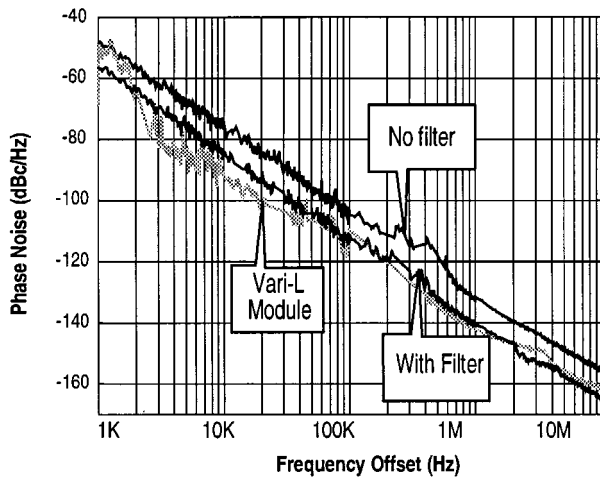Fig. 8.   (a) Tuning arrangement. (b) Resulting tuning characteristics.

Fig. 9.   Phase-noise measurement of tail-biased VCO with and without noise filter, compared against VARI-L module.

Fig. 10.   Phase-noise measurement of top-biased VCO, with and without noise filter.

which improves shielding of the electric field, makes it more susceptible to strong eddy currents induced by the magnetic field under the inductor. The shield is patterned as a checkerboard of small squares connected diagonally with narrow tracks, which locally cancel the magnetic fields induced by miniature loops of current within the squares. The patterning ensures there is no closed loop of metal at the scale of the inductor, which might allow image current to flow. The simulated Q of this inductor at 1.1 GHz is about 13, which is verified by measurement.

VII. PROTOTYPE OSCILLATOR

A tail-biased differential oscillator is implemented in 0.35-μm CMOS. The oscillator consumes 3.7 mA from 2.5-V supply. Measured phase noise 3 MHz away from a 1.2-GHz oscillation is −153 dBc/Hz, as shown in Fig. 9. A reference oscillator, which is identical except it has no noise filter, is fabricated on the same wafer. Its phase noise at 1.2 GHz and the same offset is 7 dB worse.

A top-biased oscillator was also fabricated on the same wafer. This circuit tunes from 1 to 1.2 GHz, also consuming 3.7 mA. Measured phase noise at 3 MHz offset is −152 dBc/Hz, an 8-dB improvement over its reference oscillator, Fig. 10. The noise filter uses a 10-nH square on-chip spiral and a 40-pF MiM capacitor. A third oscillator implemented in the same process
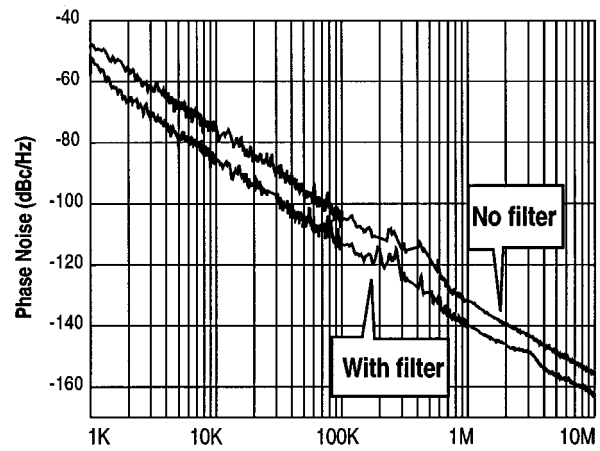
oscillates at 2.1 GHz. Consuming 4 mA from 2.7-V supply, its measured phase noise at 3 MHz offset is −134 dBc/Hz. The 5.5-nH on-chip differential inductor has a Q at 2 GHz of about 10.

The phase noise of a commercially available discrete transistor module oscillator, the Vari-L VCO190-1100AT, that tunes over the same frequency range, was measured on the same instrument, and is plotted alongside. The VCO core of the module is estimated to consume one-third the total current [21], which is roughly the same current as the 1-GHz VCOs described above, but from a 5-V supply. Measured phase noise at 1 GHz and 3 MHz offset is −150 dBc/Hz (Fig. 9).

Now, let us use Leeson's proportionality (1) combined with Rael's noise factor (4) to manually calculate this oscillator's phase noise. The foundry specifies $\gamma = 4/3$ for the FETs, and the various other parameters are $L = 13$ nH, $Q = 14$ at 1.2 GHz, $I = 3.7$ mA, $f_0 = 1.2$ GHz, $f_m = 3$ MHz, and $V_{DD} = 2.5$ V. The calculated $\mathcal{L}(f_m) = -153.2$ dBc/Hz is remarkably close to the measured value. This further validates the phase-noise analysis in [5].
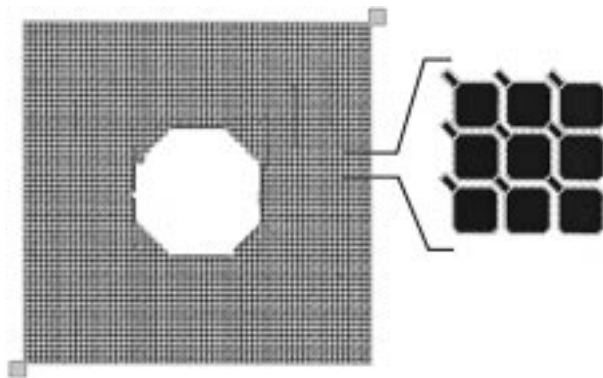
Fig. 11 shows the chip photograph of one of the oscillators.

VIII. DISCUSSION AND EXTENSIONS

It is not easy to compare the performance of different oscillators. The oscillator design space entails phase noise, power consumption, and oscillation frequency, and to a lesser degree,
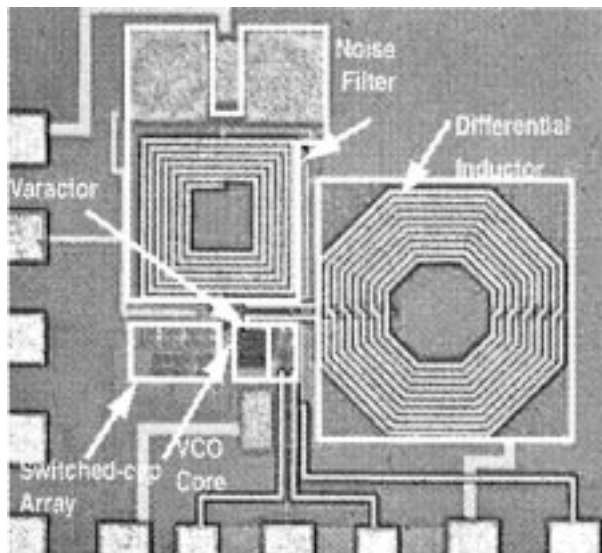
(a)

(b)

Fig. 11. (a) Die photo of one of the oscillators (b) Close-up of metal shield pattern under octagonal inductor.

tuning range. The best definition of a normalized figure of merit (FOM) proposed so far is [21]

$$\text{FOM} = \left(\frac{f_0}{f_m}\right)^2 \frac{1}{\mathcal{L}(f_m) \cdot V_{\text{DD}} \cdot I} \qquad (6)$$

where I is the oscillator current. This definition's appeal arises from the fact that it relates and normalizes the quantities given in (1) which determine phase noise. For a differential oscillator biased at the tail current that just gives the largest amplitude, this expression simplifies to

$$\text{FOM} \propto \frac{Q^2}{F} \qquad (7)$$

where the constants of proportionality are physical constants. The FOM therefore depends strongly on resonator Q, and how closely F approaches the fundamental lower limit of $1 + \gamma$. However, it is implied that the differential oscillator biases at the optimum current

$$I_{\text{opt}} = \frac{\pi V_{\text{DD}}}{\omega_0 L Q}. \qquad (8)$$

This current may not be low enough for the intended application. At a given oscillation frequency, this current is lowered
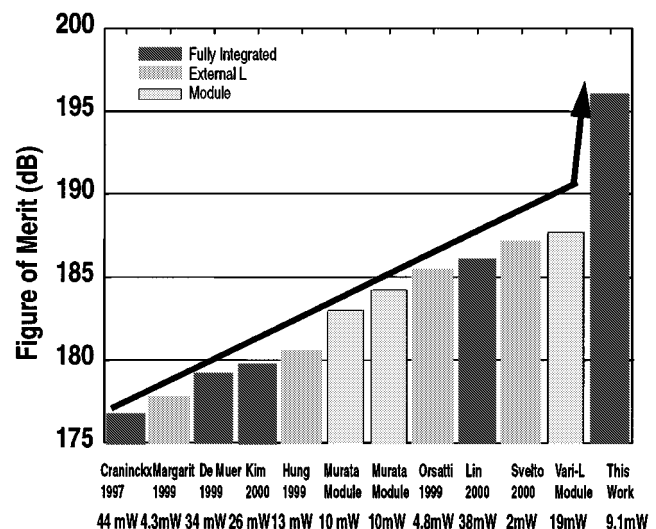

Fig. 12. Comparison of state-of-the-art FOM.

with V_{DD}, and by a resonator inductor with the largest $L \times Q$ product. The latter depends on how the inductor is fabricated. It may be deduced from (7) and (8) that an inductor that minimizes bias current does not necessarily lead to the highest FOM. This is because the quality factor of integrated inductors varies considerably with their size due to substrate losses [18]. This explains why many standalone VCOs in the literature report an impressive FOM, but at a large bias current. The inductor described in Section VI illustrates a compromise between these two requirements to obtain a high FOM at reasonable current, while holding down the actual phase noise to a low value.

The chart in Fig. 12 compares the FOM of various RF oscillators using resonators that are fully integrated, partly integrated, or discrete. The FOM of the 1.2-GHz tail-biased noise-filtered oscillator described above is 196 dB. The next best FOM is 7 dB *lower* for a widely used discrete module in cellular handsets. The next best fully integrated oscillator is a bipolar circuit [22] with an FOM 10 dB *below ours*. This circuit is an example of high FOM attained with large bias current.

Does the noise filter adversely affect power-supply rejection in this differential oscillator? Consider the tail-biased differential oscillator (Fig. 2) without noise filter or parasitic capacitances. If the varactor is biased with respect to V_{DD}, fluctuations at any frequency in V_{DD} with respect to ground cannot modulate the varactor, creating no FM. Furthermore, the current source in the tail when biased at constant V_{GS} will not permit any AM. However, low-frequency noise on V_{DD} passes through the resonator inductors to modulate the voltage on the FET drains, and voltage-dependent junction capacitors to ground there will create FM noise.

With the filter present [Fig. 5(b)], the oscillator responds in exactly the same way to low-frequency noise on the supply. At high frequencies, the filter capacitor bypasses the current-source FET and couples supply fluctuations directly into the filter inductor. The oscillator can only respond with a common-mode current, which as explained earlier must be either dc or at even harmonics. But the filter inductor in parallel resonance with the tail capacitance blocks any second harmonic. In this way, the
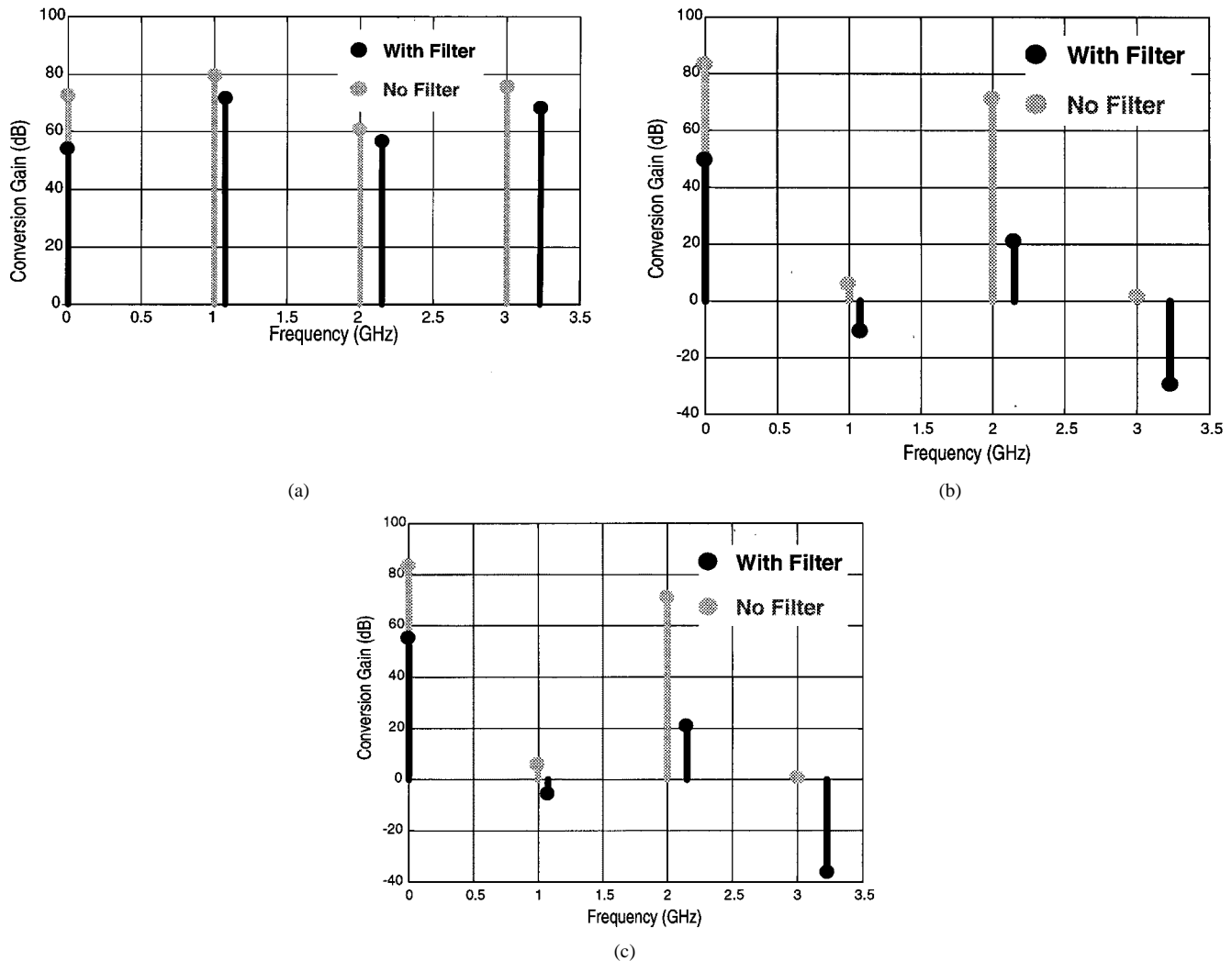
Fig. 13.   (a) Simulated conversion gain of switching differential-pair noise to phase noise at 10-kHz offset. (b) Simulated conversion gain of current-source noise to phase noise at 10-kHz offset. (c) Simulated conversion gain from V_{DD} noise to phase noise at 10-kHz offset.

oscillator better rejects noise on the power supply. The same analysis applies to the top-biased oscillator, where the grounded filter capacitor shunts power-supply noise and the series inductor blocks noise currents.

Cadence SpectreRF is found to be a useful and accurate aid in understanding mechanisms of phase noise. It allows the simulation of conversion gain from voltage noise at any node in the oscillator to phase noise. Fig. 13(a) plots the simulated conversion gain from gate-referred voltage noise in one of the differential-pair FETs to phase noise, versus discrete frequencies of voltage noise which will produce close-in phase noise. The noise filter reduces upconversion of low-frequency noise, but does not affect the noise at harmonics of the oscillation frequency very much. As predicted by [5], this simulation shows that noise in the differential-pair FETs close to the oscillation frequency is mainly responsible for phase noise. Fig. 13(b) shows that the noise filter dramatically lowers the conversion gain of noise in the current source at frequencies around the second harmonic. Finally, Fig. 13(c) shows that the noise filter improves power-supply rejection at all frequencies. In sum, these simulations verify the qualitative description in Section IV that with the filter present, only noise in the

differential pair and the resonator loss matters. As a side note, when second harmonics no longer flow in the resonator, the oscillation frequency increases slightly [23].

For completeness, we now summarize previous work suggestive of filtering in oscillators, and compare it with the ideas presented here. It has been proposed [24] to add an inductor in series with the current source biasing each delay stage in a ring oscillator, with the object of improving sinusoidal purity of the signal and the output impedance of the current source at high frequency. However, there is no recognition of the inductor's benefits on internally generated phase noise.

Other work [8] recommends a large capacitor in parallel with the current source, because, it is argued, this shrinks the duty cycle of switching current in the differential pair, which lowers the instantaneous FET current at differential zero crossing, thus lowering phase noise due to the differential-pair FETs. This is implemented in [25] to lower the upconversion of flicker noise into phase noise. However, this argument overlooks the effect described in Section IV, that the large capacitance at the tail offers a low impedance path for the triode-region FET in the differential pair to load the resonator and degrade Q. Moreover, although outside the scope of this paper, it should be noted that
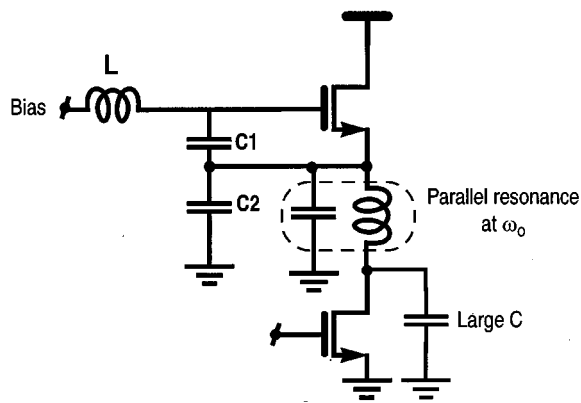
Fig. 14. Colpitts oscillator with noise filter applied to the current source.

the tail capacitance leads to greater upconversion of flicker noise from the differential pair into oscillator phase noise [5], [26]. Our analysis shows that a large filter capacitor alone can only lower thermally generated phase noise if the current source contributes such a large phase noise [third term in (3)] that its elimination by the capacitor outweighs the higher phase noise due to degraded Q. We believe that in practice this is unlikely.

It is straightforward to extend the noise filter to other oscillators. The voltage-biased oscillator is improved as shown in Section IV. Other differential oscillators such as the complementary differential [27] and quadrature oscillators [14] fall into the category of top-biased, tail-biased, or voltage-biased, and the appropriate filter improves their phase noise.

Fig. 14 shows a noise filter at the bias current source in a Colpitts oscillator. The capacitor C_2 should remain unaffected by insertion of the filter, which means that additional capacitance may be required to cancel the inductor reactance at the oscillation frequency. Here, given the single-ended FET circuit, the filter inductor tunes the parasitic capacitance to the oscillation frequency instead of the second harmonic as in differential oscillators. SpectreRF simulations confirm that the noise filter lowers phase noise in the Colpitts oscillator.

IX. CONCLUSION

We have presented a technique to lower the noise factor of *LC* oscillators to its fundamental minimum. The technique is based on physical understanding of phase-noise mechanisms in *LC* oscillators and is extendable to other topologies, as we showed. As a result, we were able to implement fully integrated oscillators with on-chip resonators that outperform discrete transistor module oscillators.

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