Teaching Top Down Design of Analog/Mixed Signal ICs Through Design Projects

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Published in:
FIE 2007: 37th annual Frontiers in education conference - global engineering: knowledge without borders, opportunities without passports, Proceedings

2007

Teaching Top Down Design of Analog/Mixed Signal ICs Through Design Projects

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Abstract – **This paper describes a project course that focuses on the design of analog and mixed signal circuits through a systematic top down design flow. In the project, the student will be involved in the planning, modeling, circuit level design, physical level implementation and measurement verification of for example a successive approximation (SA) ADC or a class-D audio amplifier. Throughout the project, the project members will improve their design skills and create an understanding for the importance of a systematic top-down design methodology at the different levels of the design flow.**

Index Terms – IC design, IC projects, top down design.

INTRODUCTION

IC design projects are important parts of the electrical engineering education that are often specifically asked for by representatives of the IC design industry, for example when recruiting master thesis workers. In the projects, the students get a chance to use their prior knowledge and practice real world situations like team work and work planning that span beyond the typically well-defined problems taught in traditional courses. They are allowed to make mistakes that could be very expensive in the real world, and learn from them. Altogether, the projects create an understanding and experience in the design of mixed signal System-On-Chips (SOCs) that are hard to teach in any other way. Despite all their benefits, we have throughout the years found several problems like:

- The prior knowledge and motivation of the students are very different. It is hard to find tasks simple enough for poor students, yet challenging enough for the motivated.
- Students tend to not follow their own time plans for the project, often as a result of competing examinations in other courses. The result is that they get to short time for the final verification of their design.
- One or a few students make the work for the whole group, and the others do not learn anything.
- Students lack a structured way of working.
- The project supervisors have a too heavy workload.

This paper presents a new course organization for the 2006 projects, where a structured top down design flow is stressed, through a new lab course, the design of the course material as well as the examination.

The rest of this paper is organized as follows. In section II, the traditional view of top-down design is given for completeness, in section III the currently implemented course organization is explained, in sections IV and V we exemplify by giving some more details about two different design projects. Finally we conclude and give some further suggestions for future improvements of this course.

BOTTOM UP VERSUS TOP DOWN DESIGN

The constantly larger mixed signal integrated circuits and the pressure to get the designs right in a minimum of design spins drive the need for improved design methodology among circuit design engineers. Mixed signal circuits are characterized by a medium to high amount of complexity, and typically high accuracy requirements exists for some of its circuit elements. While design automation is practical and essential in digital design, analog circuits are not well suited for automation. Analog designs are typically transformed from concept to implementation by hand, which makes the design slow and error prone as compared to digital circuit design. As an alternative to design automation, analog designers have to develop a systematic design methodology that is more efficient.

The traditional bottom up design process starts with the design of individual blocks which are then combined to form the system. The block design starts with a specification and ends with a transistor level implementation. Each block is verified against their specification. Once verified separately, the blocks are combined and verified together at the transistor level. This approach has several important problems [1]:

- System level verification has to be done using slow transistor level simulations.
- Little if any architectural / structural exploration is performed, high level improvements are often missed.
- Several expensive steps like system-level verification and test development has to be performed sequentially which increases the overall design time.

In a top-down design the process from concept to transistor level design is systematic. A set of principles for an effective top-down design is outlined in [1]:

- The design shall be able to be simulated by all members of the design team in all types of its description (behavioral, schematic, layout).
- During the design process each change to the design is verified against the previously verified design as dictated by the verification plan.
- A design process that includes careful verification planning where risks are identified up-front and modeling plans are developed to mitigate the risks.
- A design process that have multiple steps, starting with simple models that are refined as details become available.
- Specifications and plans are manifested as executable models and scripts that can be used in the design process, rather than as written documents.

A comprehensive verification strategy including simulation and modeling plans is needed. The plans specify which test to run, how to perform them, and which blocks that shall be at transistor level during the test. For blocks represented by models, the effects that must be included in the model are identified for each test. The simulation plan is applied initially to the high-level description of the system where it can be quickly debugged. Once validated, it can be applied in transistor level simulations. Mixed level simulations verify the block function in the system context. Each level is fully designed before moving on to designing the next level. By doing so, the design is partitioned into smaller blocks that can be designed in parallel. Following a top down design methodology both minimizes the risk for, and the impact of changes that come late in the design cycle.

COURSE ORGANISATION

The eight-week full-time course is divided into three phases. A study, planning and modeling phase with two labs on behavioral modeling and mixed level simulation is followed by the schematic and layout level implementation, and finally the fabrication and measurement verification. The course flow is illustrated in figure 1.
Different project assignments have been given in the past, for example the design of an SA-ADC or a class-D amplifier. In these projects of medium complexity, the students are faced with both traditional analog design problems like noise, bandwidth and distortion, but also mixed signal issues like for example timing between analog and digital parts, circuit structuring and crosstalk.

I. Prerequisites

The basics of analog circuit design such as circuit elements, noise, distortion and bandwidth are taught in the courses *Analog Electronics* and *Advanced Analog Design*. The course *Analog IC Design* focuses on the analog design flow and integrated analog building blocks such as amplifying stages and current mirrors etc. The course *Integrated A/D and D/A Converters* cover data converters, mixed level modeling and simulation using Verilog-A and spectreVerilog. The digital design flow is taught in the course *Digital IC Design*.

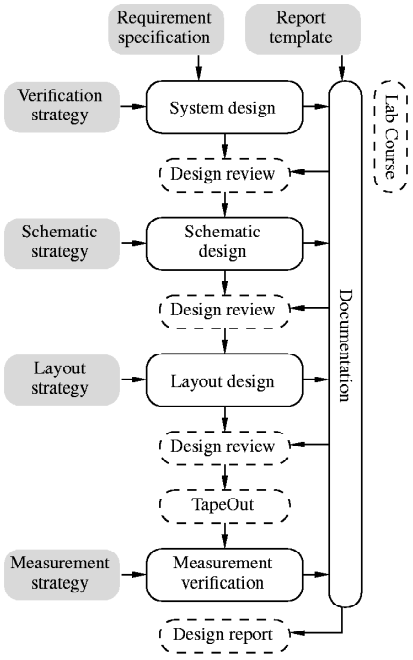

FIGURE 1
THE COURSE FLOW, DOCUMENTATION AND EXAMINATION SUPPORTING TOP DOWN DESIGN IN THE ANALOG / MIXED SIGNAL IC PROJECT COURSE.

II. Course material

As input to the project work there are six documents as illustrated in figure 1. The **requirement specification** describes the project assignment, the electronic input and output interfaces as well as the dynamic range, bandwidth and power requirements of the system. It is the task of the group to break down the requirement specification into requirements for each building block in the system design phase. The **project report template** is assisting the student to systematically document the results from each phase of the project. It is important that the student reflects upon the design methodology in the project report, and that it is clear which considerations that were made during the different phases of the project. The **verification strategy** is divided into a modeling plan and a simulation plan guiding the students on how to model and verify their blocks and systems. The **schematic strategy**, **layout strategy** and **measurement strategy** documents are all assisting the student with theoretical and practical information on for example design methodology, how to organize the design database, how to make and verify layouts and how to verify the fabricated circuits by measurements.

III. Pass requirements

The examination that contains six compulsory parts (marked with dashed boxes in figure 1) is done continuously during the project. First of all, in the system design phase, a **lab course** on Verilog-A modeling and mixed level simulations with spectreVerilog is completed. At the end of each design phase, a **design review** is held, where the supervisor simulates and

verifies the operation of the circuit model as specified in the verification strategy. At the design reviews the documentation is checked to make sure that the students document their work continuously. It is not recommended to start the next design phase before passing the preceding design review. Before **tape out**, the project must pass all three design reviews according to the verification plan. After fabrication, the students shall do a **measurement verification** of their chip. Finally, the design project is summarized and conclusions are drawn in the **project report**.

IV. Project management

The project management is performed by the supervisor, normally a doctoral student. All actual design work is performed by the students. The role of the supervisor is to act technical expert, motivating coach and the one that controls that the verification strategy and the time plan are followed. Some of the course related material is available on the homepage [2]. FAQ information can also be posted there.

PROJECT EXAMPLE 1: A CLASS-D AUDIO AMPLIFIER

The project goal is to design a class-D amplifier with high efficiency and acceptable distortion, using a top down design flow. Class-D amplifiers are used in many applications and are today making their way into applications such as portable computers, musical instruments, wireless communication devices, battery-powered portable products, high-end professional amplifiers, advanced TVs and other home multimedia systems. The class-D amplifiers have higher efficiencies than classical amplifier topologies, such as class-A and class-AB, but require fast transistors to switch the Pulse Width Modulated (PWM) signal. This makes class-D amplifiers ideal to integrate on chip to extend battery life, save space, and reduce cooling cost. The output stage of the class-D amplifier consists of CMOS power transistors operating as switches, working either fully on or off. This gives a high efficiency since ideally no voltage drop occurs over the transistor in the on-state, and no current is conducted in the off-state. In reality, losses are introduced by the finite on-resistance of the transistors and the power required for switching. The signal can be represented by the high frequency switching (square) waveform using PWM, see Fig. 3. The PWM-signals are generated in the analog domain by a triangular wave and a comparator. The amplifier must be able to supply 160 mA current into headphones, typically 16 . The triangle wave generator shall operate at a frequency of 1.0 MHz, which is rather high compared with discrete class-D audio amplifiers, which generally operate at a few 100 kHz. A higher frequency pushes unwanted frequency contents up in frequency and makes filtering of the output signal easier.

II. Circuit Topology

The system contains the following important blocks (Fig. 2): triangle wave generator (implemented as a smith trigger with a capacitive load integrating the square wave to a triangle wave), comparator, amplifiers (two stage operational amplifiers), filters, delay circuit, buffers, and H-bridge. The frequency behavior of the amplifier is simulated with SpectreRFs periodic AC analysis. The simulated open-loop DC gain is 65 dB and the phase margin is 74 with a closed-loop gain of 17 dB.

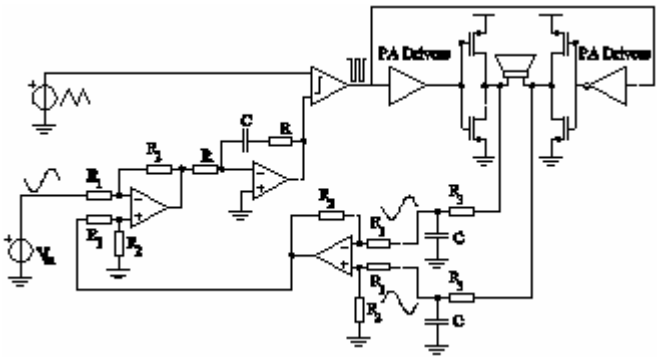

FIGURE 2

OVERVIEW OF THE CLASS-D AMPLIFIER

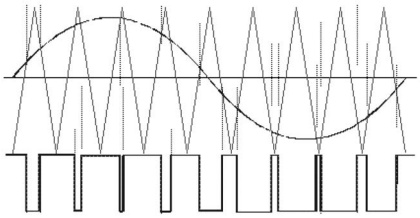

FIGURE 3

TRIANGULAR WAVE AND COMPARATOR INPUT ABOVE. COMPARATOR OUTPUT BELOW

The difference between the input and fed back signal is integrated and compared with a triangle wave in the comparator. The result from a typical comparison with a sine wave input is shown in Fig. 2. If the sine wave is higher than the triangle wave, the output will be high, otherwise it will be low. Due to the high modulation frequency, the comparator must be fast. As can be seen the width of the pulses at the output is modulated, but not the amplitude, hence the name pulse width modulation. The PWM signal is then fed to a time delay circuit, a part of the PA driver in Fig. 1, to make sure that the large nMOS and pMOS transistors in the H-bridge are not conducting at the same time. This is very important to reduce power consumption and most of all, prevent the chip from a breakdown due to the short circuit currents. The delay circuit is simply a number of inverters connected in series with skewed transition points achieving pulse shrinking and widening. The nMOS and pMOS transistors in the output stage are 5.75 mm and 15 mm wide, respectively, which can deliver 160 mA to the load. After the delay circuit, the signal is buffered by drivers to the output stage. They are needed to drive the large gate capacitance of the output transistors in the H-bridge. Just as the delay circuit, the driver stages consist of several inverter stages but in increasing sizes. The signal is inverted and fed to the right side of the H-bridge, see Fig. 1. An H-bridge is simply two large inverters whose purpose is to drive a heavy load, which is a low impedance loudspeaker. The H-bridge works like this: When the PWM signal is low,

the pMOS transistor on the left side and the nMOS transistor on the right side conduct. The current will then flow from the left supply through the load, to the right side ground. As the signal changes and goes high, the nMOS transistor on the left side and the pMOS transistor on the right side conduct. Thus, the current will then flow in the other direction.

III. Measurement Results

The triangle wave generator was measured with an oscilloscope. The frequency was initially a bit lower than simulated, but was easily adjusted to 1.0 MHz by applying a different bias to the charge pump in the oscillator.

To measure the harmonic distortion an audio analyzer from Audio Precision was used. The output from the H-bridge was low-pass filtered by a fourth order filter with a -3dB frequency of 50 kHz. This is needed to avoid high frequency signals interfering with the measurement. The lowest measured THD+N was 0.2 % at 1 kHz, 210 mW(rms). The efficiency was measured by measuring the current drawn from the supply with a multi meter. The measured efficiency was 71%. The amplifier has also been used to play music on and was able to drive a 4 load speaker.

PROJECT EXAMPLE 2: A HIGH-SPEED SA-ADC

Successive-Approximation A/D converters (SA-ADC) are one of the oldest and simplest ADC architectures. Yet, they are still the most commonly used and their simplicity makes them well suited for low power and low voltage applications. The reason SA-ADCs are well suited for mixed signal education projects is that they contain most design difficulties (such as co-timing and co-simulation of analog and digital blocks) and many analog and digital circuit techniques (such as digital controllers, switched capacitor circuits, amplifiers and comparators) commonly used in other applications while still having a moderate complexity necessary for the students to get an acceptable workload. The students are assigned the design and speed optimization of an 8 bit charge redistributing SA-ADC. After successful design and simulations, it is fabricated in a 0.35 m CMOS process with 3.3V supply voltage. The clock frequency is targeted at 100 MHz, making the design challenging in this technology. The SNDR shall be larger than 46 dB. This specification is then broken down by the students into noise, distortion and bandwidth requirements on the main building blocks.

II. Circuit Topology

The SA-ADC system, illustrated in figure ?? consists of three main building blocks. They are a binary weighted switched-capacitor array used as a charge redistributing DAC and embedded passive sampling circuit, a comparator and a digital control unit. An SA-ADC converts one digital bit per clock cycle using the well known binary search algorithm, which is implemented in the digital controller. By switching the correct amount of capacitance to well known voltage levels, the input signal can be compared to different signal levels by the comparator, and the logic will successively exclude half the remaining input signal range from the binary search, and finally the closest digital level corresponding to the analog input signal has been found. Both the conversion rate and accuracy is determined by the analog building blocks. The speed is limited by the RC time constants needed for settling of the comparator of the SC DAC and the metastability and hysteresis of the comparator. The main design difficulties in the digital part are correct timing and the speed optimisation of the critical path (in order for to give the analog time constants as much of the conversion time as possible).

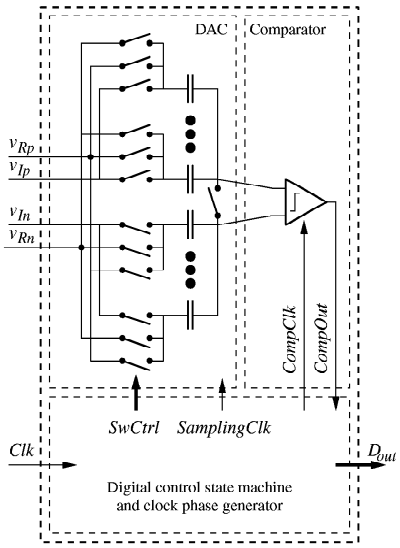

FIGURE 4

SA-ADC SYSTEM BLOCK SCHEME.

CONCLUSION AND FUTURE WORK

By going through all the steps of the design flow the students get a valuable experience from most aspects of the design of a complex mixed signal SoC. They gain understanding of the importance of a systematic top-down design methodology. A new course organization is presented, where the lab course is intended to teach high level modeling and structuring of a complex design to make it easier for the students to work in a structured way in their project. The quite extensive written course material is intended to reduce the supervisor workload as well as to support a structured way of working. To force the students to work continuously with their project and to find design errors as early as possible, the examination has been divided into three design reviews.

As improvements for future projects we suggest to let the students review each-others projects and to improve the lab course with a lab assignment on the final steps of the design, layout and post layout verification. That would increase the interaction between the student groups and reduce the supervisor workload during the final hours of the project.

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