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A 30 GHz 90-nm CMOS Passive Subharmonic Mixer with 15 GHz Differential LO

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Abstract—A new passive subharmonic mixer topology is presented and compared to a previously published passive topology. The comparison is conducted using simulations at 30 GHz with a 90-nm CMOS design kit.

The advantage of the new passive subharmonic mixer is that it only requires a differential local oscillator (LO) signal, compared to the previously published mixer that requires a quadrature LO signal. The mixer consists of two cascaded passive mixers with an interstage second order filter suppressing harmonics while providing some 10 dB of voltage gain at the LO frequency.

The noise performance of the differential mixer is slightly worse than for the quadrature one, with a simulated down conversion SSB NF of 10 dB compared to 7 dB. The voltage conversion gain is −1 dB for both mixers, all with a 1 V LO amplitude.

I. Introduction

A wide range of applications use frequency bands located at several tens of gigahertz, e. g. automotive radar (24 GHz and 77 GHz) and WLAN/WPAN (60 GHz). To make these applications penetrate the mass market the cost of the chip sets must be reduced, which is a drive and motivation to use CMOS technology also when implementing the analog and RF parts [1], [2].

The motivation to integrate automotive radar, also in the low cost segment cars, is high. The injuries from car collisions cost the society a lot both in medical bills and in human tragedies. Just in the United States (US) alone motor vehicle accidents accounted for 42,000 deaths, more than 5.3 million injuries, and over $231 billion in economic losses in year 2000 [3]. The consumer electronics, WLAN/WPAN applications, is extremely cost sensitive, and to succeed a low cost solution is a must.

A drawback when it comes to high speed CMOS processes is the low supply voltage. It reduces the available dynamic range of receivers and the achievable output power of the transmitters. To overcome these disadvantages a beamforming transceiver can be used [4], [5]. Combining a beamforming transceiver and phased array antenna the system will have an increased antenna directivity (∝ the number of antennas) compared to a single antenna element [6]. The increased antenna directivity increases the strength of the signal to receive and at the same time reduces the level of interferers from other directions.

In Fig. 1 the proposed beamforming transmitter architecture is presented. The phase shifting to control the direction of the

beam is performed in the local oscillator (LO) path, by means of a quadrature to differential vector modulator (VM) [7], [8], one modulator for each transmitter path. A subharmonic mixer, presented in this paper, upconverts the phase shifted signal to twice the LO frequency. A power amplifier (PA) driver and a frequency doubling PA then converts the signal to four times the LO frequency and transforms the differential to a single-ended signal [9]. The LO thus runs at a quarter of the carrier frequency, which increases the tuning range of the LO and the robustness to parasitics. Furthermore, the vector modulator
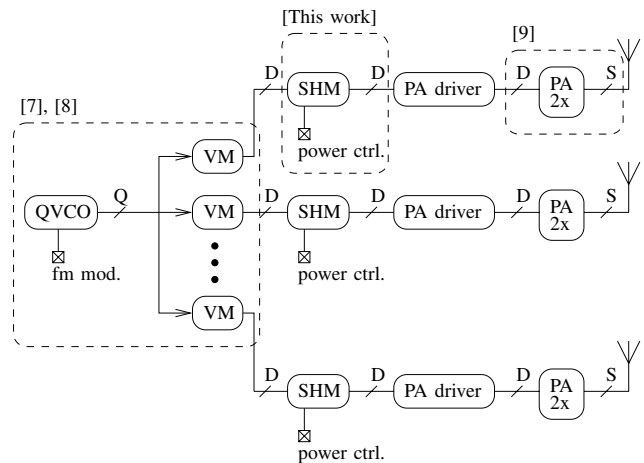

Fig. 1. Proposed beamforming architecture with LO phase shifting. Q means quadrature signals, D differential, and S single-ended

could be simplified, as 360° at the the output corresponds to 90° at the LO, and thus it is sufficient to be able to steer the phase across one quadrant. The frequency (phase) modulation is inserted on the control voltage of the QVCO. The IF port of the subharmonic mixer is used to control the output power, and also to reduce the level of the side lobes.

Two of the three main building blocks have been presented earlier [7]–[9]. In this paper the third block, the subharmonic mixer (SHM), is addressed. A subharmonic passive mixer driven with quadrature LO was presented in [10]. It shows good performance but it is not suitable for a beamforming transmitter due to the quadrature LO needed. In a beamforming transmitter there are many transmit paths, and distributing the quadrature (phase shifted) LO across the chip to the mixers with sufficient signal quality is non-trivial and requires significant chip area and power consumption [11]. Distributing

a differential signal is much easier. The demands on the vector modulators are also relaxed, since implementing vector modulators with differential output is less difficult than with quadrature output. An active SHM with differential LO was presented in [12]. The design uses two inductors, as does the proposed topology in Fig. 2(b). The hardware cost for the two mixers are about the same but the passive has less power consumption and is less complex. When used in a direct conversion receiver the passive mixer also has a $1/f$ noise advantage.

Therefore a comparison between the topology in [10], Fig. 2(a), and a novel topology presented in Fig. 2(b) is conducted.

II. SUBHARMONIC MIXER TOPOLOGIES

The comparison is performed using a 90-nm CMOS design kit with BSIM4.3 transistor models [13]. The non-quasi static model of the transistors is used, Table I shows the BSIM4 user switch settings. All simulations were performed with the Cadence SpectreRF simulator.

TABLE I
BSIM4.3 TRANSISTOR MODEL SWITCHES

acnqsmod = 1	trnqsmod = 1	rgatemod = 0	mobmod = 2
rdsmod = 1	igcmod = 1	igbmod = 1	capmod = 2
rbodymod = 1	diomod = 2	pemod = 1	geomod = 3
rgeomod = 1			

To determine the dimensions of the transistors and the LO bias voltage, parametric sweeps were performed and the voltage conversion gain (CG) and the single sideband noise figure (SSB NF) were plotted. The finger width was fixed to 2 μm and the number of fingers was changed to change the width of the transistor. The transistor length was the minimum, 90 nm. To fit into the beamforming architecture presented in the introduction the LO frequency was 15 GHz, RF was 30 GHz, and the IF was zero. The LO was applied through a 5 pF DC-block capacitance while the bias was fed through a 10 kΩ resistor with an effective resistance of 3.8 kΩ at 15 GHz. The LO amplitude was held constant at 1 V peak, which can be achieved in a 1.2 V process. The higher the LO amplitude the better performance of the mixer. When simulating down-conversion a differential capacitive load of 500 fF was applied at the IF side, and a resistive load of 300 Ω was applied at the RF side in up conversion simulations.

A. Quadrature LO SHM

The dimensions of the transistors and the LO bias voltage were determined through a two-dimensional parametric sweep. In Fig. 3 the SSB NF and CG are plotted. The width was swept from 10 μm to 100 μm in steps of 10 μm. The NF decreases with increasing width, while the CG just drops slightly. Only the CG at 10 μm and 100 μm are plotted. At 100 μm the decrease in NF has flattened out, and the width of the transistors was thus chosen to 100 μm. The CG is largest at zero LO bias while the NF reaches its minimum at 420 mV, thus a trade-off has to be made. Making the degradation from
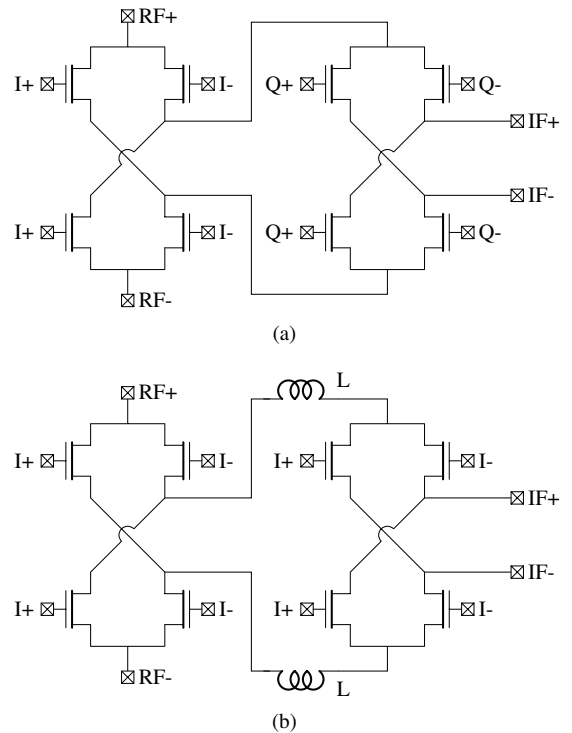
Fig. 2. The two passive subharmonic mixer topologies. a) Quadrature LO. b) Differential LO

their optimum equal, a bias level of 210 mV was chosen, with a corresponding degradation of 0.6 dB. It can also be seen
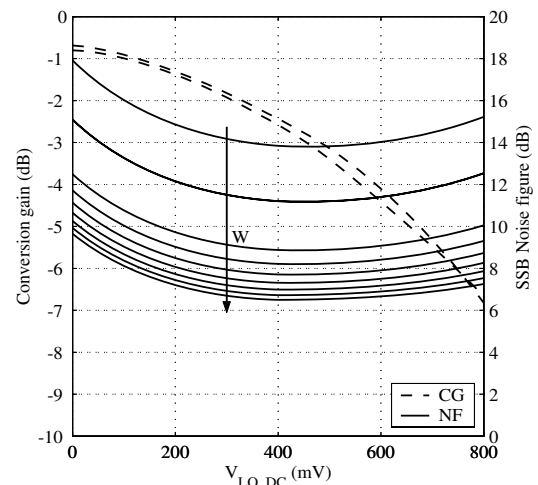
Fig. 3. Simulation of down conversion voltage gain and SSB noise figure of the quadrature LO SHM, at an IF of 10 MHz. The width is swept from 10 μm to 100 μm in steps of 10 μm

that the LO bias voltage and transistor size are orthogonal with respect to CG and NF.

With the transistor sizes and LO bias voltage now set, CG and NF versus frequency, and linearity were investigated. The 1-dB compression point referred to the RF side is 0.8 dBm, while CG and SSB NF remain constant at -1.4 dB and 7.0 dB, respectively, up to 1 GHz IF frequency the degradation is less than 1 dB. The up-conversion comparison between the two

topologies with respect to noise, gain, and compression point is presented in Section II-C.

An LO signal with perfect quadrature is difficult to achieve and route across the chip. The sensitivity against quadrature phase error, θ, was therefore simulated, see Fig. 4. The quadrature phase error stretches from 0 to 360 degrees and one can see that the order of $Q+$ and $Q-$ is arbitrary (works well at $180°$ error), which can be valuable if the locking order of the QVCO is difficult to assure. It is also clear that the CG deteriorates as θ approaches 90 and 270 degrees, thus a modification of the mixer is required to work with differential LO signals.
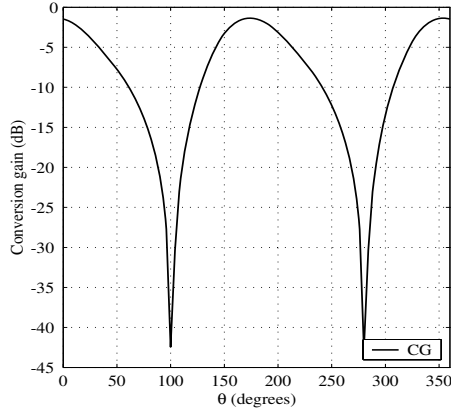

Fig. 4. Conversion gain vs. quadrature phase error

B. Differential LO SHM

In the previous section it was observed that the effects of transistor width and LO bias voltage on CG and NF were orthogonal. Thus the transistor width and inductance are chosen first through a two dimensional parametric simulation. The LO bias voltage is then chosen through a separate simulation. The inductance and transistor width are connected together in the interstage filter function and thus have to be changed simultaneously. The inductors are spiral inductors supplied by the foundry, swept from 200 pH to 1 nH. Their Q-value at 15 GHz is above 18 for all sizes. Two-dimensional contour plots of the SSB NF and CG are presented in Fig. 5. The plots are normalized relative to the optimum value since the LO bias was not yet optimized. The conversion gain is best for a seemingly constant LC-product, corresponding to a peak in the filter function at the LO frequency, see Fig. 7. The SSB NF is also in this case the lowest for large transistors. A transistor width of 100 μm and an inductance of 225 pH were chosen, indicated by the cross (X) in Fig. 5.

The LO bias level was swept and then set to 370 mV, which gives a CG and SSB NF of -0.43 dB and 9.9 dB, respectively, see Fig. 6. For the bias point selected the CG and NF deviates less than 0.5 dB from their optimum values. The noise figure of this mixer is 2.9 dB worse than the quadrature LO one.

The compression point at the RF side is -6.2 dBm. The CG and SSB NF are rather constant up to 1 GHz IF frequency, deviates less than 1 dB.
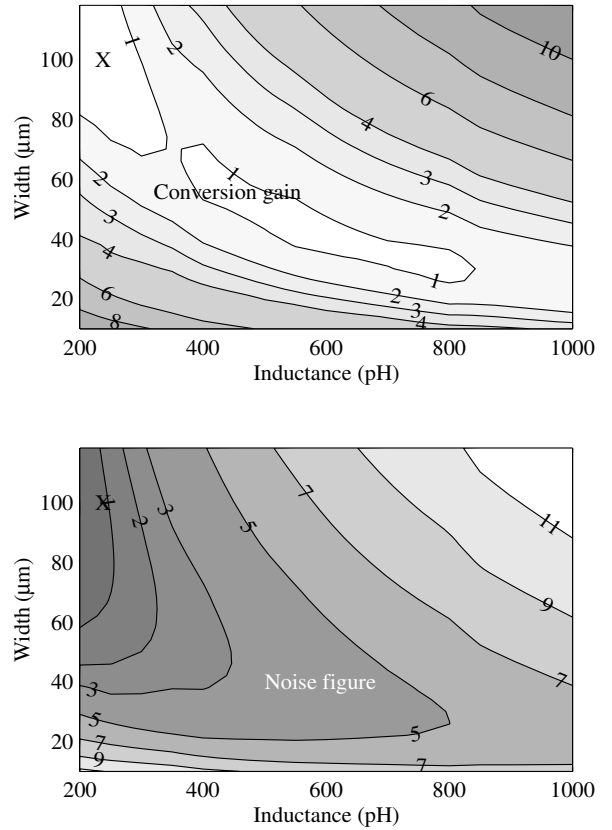

Fig. 5. Simulation of the differentially driven SHM as the transistor width and the inductance are swept, at 10 MHz IF. Top: Relative voltage conversion gain. Bottom: Relative single sideband NF
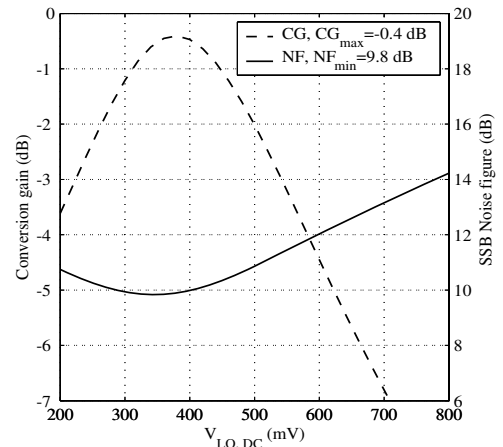

Fig. 6. Down conversion CG and SSB NF for the differentially driven SHM versus LO bias voltage, IF is 10 MHz

C. Up Conversion Comparison

The up conversion performance for both topologies is evaluated with respect of noise, gain, and 1-dB compression point (Fig. 8). The load at the RF side is 300 Ω, emulating the load of a tuned 30 GHz PA driver following the SHM. The SSB noise figure is 4 dB higher for up conversion than down conversion, 11 dB and 14 dB for the quadrature and differential LO SHM respectively. The 3-dB difference between the two topologies remain.
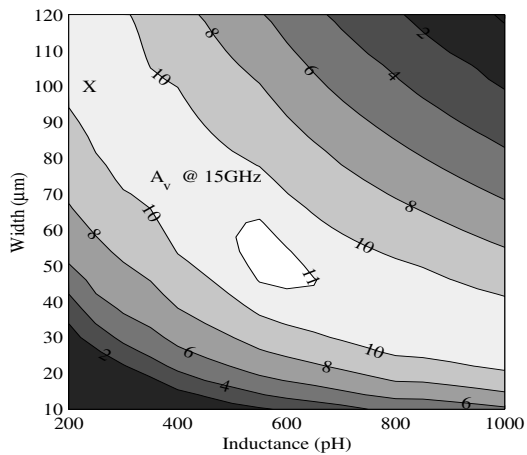
Fig. 7. Voltage gain for the 15 GHz tone of the interstage second order filter

The voltage conversion gain, simulated with one RF tone and a DC IF input voltage, is 0.14 dB and -1.59 dB for the quadrature and differential LO SHM respectively. In Fig. 8 output power vs. input DC voltage is plotted and the 1-dB compression points are extracted, -2.7 dBm and 0.17 dBm for the quadrature and differential LO corresponding to an output voltage of 220 mV and 320 mV respectively over a 300 Ω load.
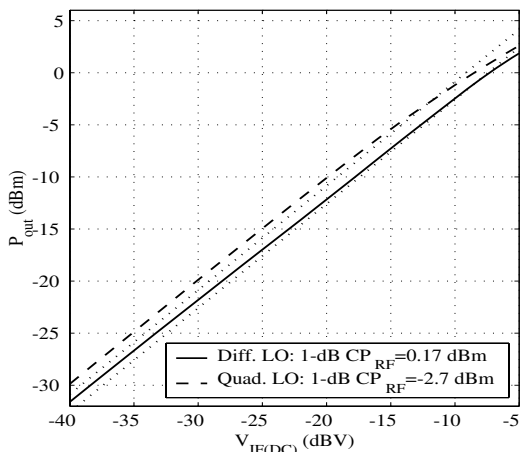

Fig. 8. Up-conversion output power vs. DC IF input voltage

D. Summary

The performance and design parameters of the two SHM are summarized in Table II.

III. CONCLUSION

A comparison between two passive SHM has been performed, one with quadrature LO and one with differential LO. The new mixer topology with differential LO uses a second order interstage filter to suppress high order harmonics and provide some 10 dB of voltage gain for the desired signal at the LO frequency. In a beamforming transceiver, with multiple receive and transmit paths, the LO generation (with or without phase shift) is performed at one place on the chip. The LO therefore needs to be distributed to all the mixers in the transceiver (Fig. 1), which is much easier with a differential than with a quadrature LO signal.

The differential subharmonic mixer, however, has some penalties in noise figure and chip area, but in a beamforming application the advantage of having of having differential LO signals is so large that these penalties in most cases can be accepted.

IV. ACKNOWLEDGMENT

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