LUND UNIVERSITY

Differential measurement and parameter extraction of symmetrical inductors

Troedsson, Niklas; Wernehag, Johan; Sjöland, Henrik

Link to publication

Differential Measurement and Parameter Extraction of Symmetrical Inductors

Niklas Troedsson, Johan Wernehag and Henrik Sjöland

Department of Electroscience,

Lund University,

Box 118, 221 00 Lund, Sweden

email: {Niklas.Troedsson, Johan.Wernehag, Henrik.Sjoland}@es.lth.se

Abstract

Measurements and extraction of Q-value and self-resonance frequency of on-chip differential symmetrical inductors have been performed. Both 1-port and 2-port measurements have been carried out. In the 1-port measurements a high frequency broadband 180° hybrid was used to generate differential signals. The inductor was then excited by the same kind of signals in the measurement as when used in a real differential circuit. The measurement results agree well with simulations using FastHenry in combination with the free inductor optimization program Indentro, verifying these tools.

1 Introduction

Symmetrical inductors are essential in RFICs, which typically use differential topologies to improve the performance by suppressing even order non-linearities and substrate interference. Differential inductors are common in *e.g.* differential oscillators [1] and low noise amplifiers [2].

Modern RF CMOS processes have high silicon substrate resistivity as well as thick top metal options, significantly increasing the performance of monolithic inductors. To design first time right and thereby reducing the design costs, accurate inductor models are needed for simulations. Earlier work has therefore developed such models based on 2-port measurements, for both single ended inductors [3] [4] [5] [6] and differential ones [7] [8].

2 Indentro

The inductor optimization program Indentro [9] is used for comparison to our measurements. Its theory of equivalent distributed capacitances [1] is in this paper verified with measured on-chip inductors. Indentro uses simple lumped Π-models to optimize the geometry of spiral and symmetrical inductors. The models are depicted in Fig. 1.

Thanks to the simplicity of the algorithm, and using fast empirical and semi-empirical formulas to calculate the lumped Π-model, Indentro reduces the optimization time greatly compared to field solvers. When a suitable geometry has been found using the fast formulas, an accurate Π-model is created using FastHenry for the inductive and resistive parts, and the equivalent dis-

(a) Symmetrical: Differential Mode

(b) Spiral: Single-ended Mode

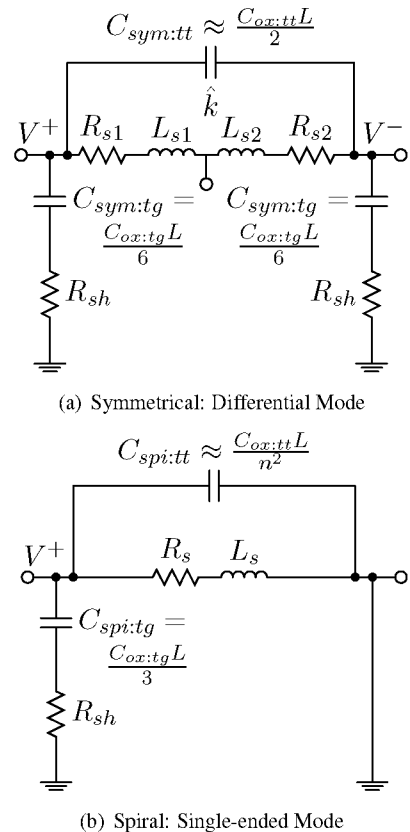Figure 1. Inductor Π-models. R_{sh} is the shield resistance. L the total length of the inductor

tributed capacitances from Indentro. This final equivalent lumped Π-model is valid for a single frequency only, and when sweeping the frequency a new Π-model is therefore calculated for each frequency.

2.1 Equivalent Distributed Capacitances

As can be seen in Fig. 1(a) a differentially excited symmetrical inductor has an equivalent distributed capacitance between the two outer terminals of $C_{sym:tt} \approx C_{ox:tt}L/2$ and terminal to ground $C_{sym:tg} \approx C_{ox:tg}L/6$, where L is the total length of the inductor. For spiral inductors, excited single-endedly, $C_{spi:tt} \approx C_{ox:tt}L/n^2$, where n is the number of turns, and $C_{spi:tg} \approx C_{ox:tg}L/3$. The capacitances $C_{ox:tt}$ and $C_{ox:tg}$ are given in (F/m) and are calculated with concise expressions using microstrip theory, whereas the corresponding division factors are eval-
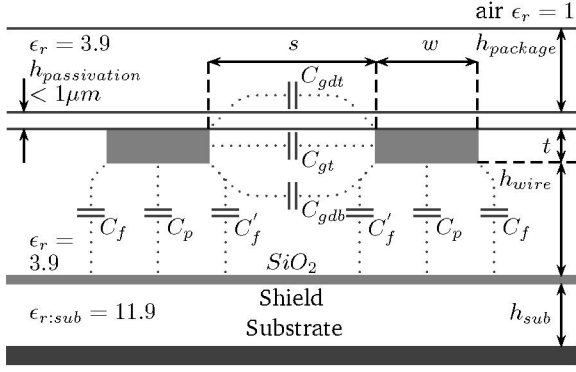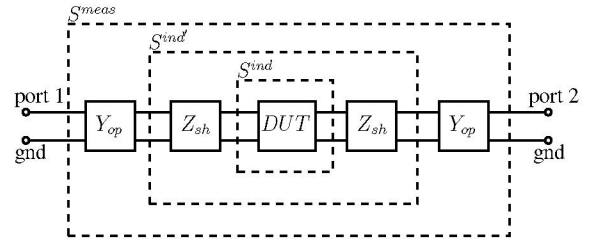
Figure 2. Capacitances of two microstrips

Figure 3. De-embedding scheme for the pads (open) and the feeding structures (short) in the S-parameter plane

Figure 4. The calibration structure for open pads on-chip
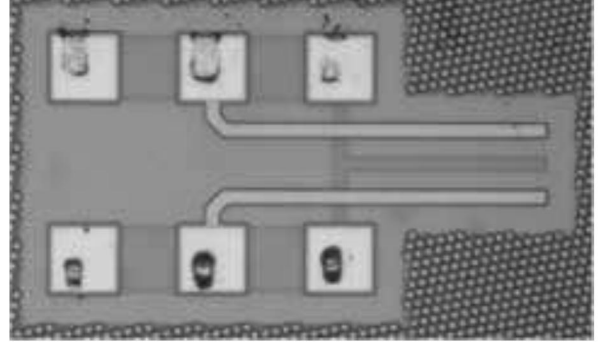
uated using the principle of conservation of energy [1].

2.2 $C_{ox:tt}$ For Naked versus Molded Die

It is assumed that the isolation material on top of the metal has infinite thickness. This is a fairly good assumption if the die is placed in a molded plastic package. However, with the die naked as in the case of probing this is not true, since the passivation material is usually less than $1\mu m$ thick. The capacitance, $C_{ox:tt}$, thus changes significantly. A change of $C_{ox:tt}$ is particularly hazardous for symmetrical inductors. The influence of this capacitance is large due to the low division factor of 2, compared to spiral inductors which have a factor close to the number of turns squared, n^2, see Fig. 1. As can be seen in Fig. 2, for a very thin passivation layer, and $h_{package} = 0$, the field lines C_{gdt} travel mostly through air with $\epsilon_{air} = 1$ rather than SiO_2 dielectric with $\epsilon_r \approx 4$.

We now evaluate the difference in $C_{ox:tt}$ between a naked die and a molded one. The total capacitance between the strips are:

$$C_{ox:tt} = C_{gdt} + C_{gt} + C_{gdb} \qquad (1)$$

Unless the strips are thick and narrow, and has a small spacing, C_{gdt} and C_{gdb} dominate over C_{gt}. Thus for strip lines with a thin passivation layer, and under the assumption that $C_{gdt} \approx C_{gdb}$ we get:

$$C_{ox:tt} \approx C_{gdt:mold}\frac{\epsilon_{air}}{\epsilon_r} + C_{gdb} \approx C_{gdt:mold}\left(1 + \frac{\epsilon_{air}}{\epsilon_r}\right) \qquad (2)$$

Compared to $C_{ox:tt} \approx 2C_{gdt:mold}$ the capacitance $C_{ox:tt}$ decreases by a factor of (3) for a naked die compared to a molded package that Indentro assumes.

$$C_{sym:tt:die} = C_{sym:tt}\frac{1 + \frac{\epsilon_{air}}{\epsilon_r}}{2} \approx C_{sym:tt}\frac{1}{1.6} \qquad (3)$$

The change of value of $C_{sym:tt:die}$ will be used later on when comparing the results of Indentro and Fast-Henry to the measurements. The change is less for inductors with thick metal and small spacing, when C_{gt} has more influence.

3 De-embedding

The de-embedding is a two step procedure, first the open-pad admittance (capacitance) is subtracted [10], then the impedance of the short circuit path [11] [10]. Fig. 3 shows the two de-embedding steps and parameter names used.

There is an open structure for calibration on-chip, Fig. 4, with Ground-Signal-Ground (GSG) configuration. The pads have the same dimensions as those connecting to the inductor in Fig. 6. The de-embedding is performed according to (4):

$$Y^{ind'} = Y^{meas} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot Y_{op} \qquad (4)$$

The short circuit structures were simulated with Fast-Henry. The two structures are plotted in Fig. 5, where the darker wires are in thick top metal layer, used for power grids and high quality inductors, and the lighter are in metal 1. The series inductance and resistance for the differential 1-port signals is simulated with a through from port to port, and for the 2-port as a short between signal and ground at the end of the wires.

The simulated impedance of the feeding paths is subtracted from $Z^{ind'}$ [11] [10], and Z^{ind} is finally calculated as:

$$Z^{ind} = Z^{ind'} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot Z_{sh} \qquad (5)$$
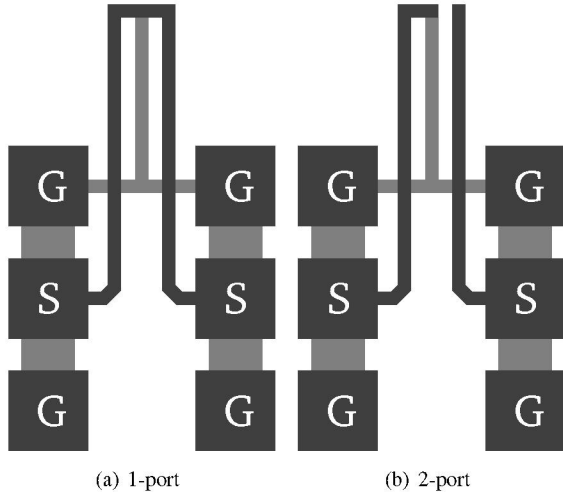
(a) 1-port   (b) 2-port

Figure 5. Structures of simulated short for 1-port and 2-port

Table 1. Octagonal Inductor Geometries Under Measurement

Inductor	Radius	Width	Spacing	Turns
No. I	$140\mu m$	$10\mu m$	$4\mu m$	8
No. II	$100\mu m$	$4.5\mu m$	$8.5\mu m$	6
No. III	$90\mu m$	$3\mu m$	$8\mu m$	6

4 Measurements and Results

Three symmetrical inductors on four different chips have been measured. Two chips were measured with a 1-port method, and the other two with a 2-port. A die photo of two of the inductors can be seen in Fig. 6, and their geometries are presented in Table 1.

The inductors are not optimized for high Q-value, but in order to verify the results of Indentro they have rather been chosen with different parameter settings in terms of radius, width, spacing, and number of turns.

A $0.18\mu m$ CMOS process with 6 metal layers and high substrate resistivity (10Ω-cm) was used, including a thick top metal option for inductors and power lines. The $2\mu m$ thick top metal of aluminum is located approximately $5\mu m$ above the metal 1 shield of the test inductors.

The measurements have been conducted with a HP8720C Vector Network Analyzer (VNA), which measures from 50 MHz-20 GHz. Infinity probes from Cascade Microtech[1] was used. The probe measurements seemed to be sensitive to skating distances, and efforts were therefore made to maintain an equal skating length of $25\mu m$ for reproduceability of the results.

The VNA and probes were calibrated with an Impedance Standard Substrate (ISS), which provides open,

[1]The probes are in a GSG configuration with a pitch of 100 μm. The frequency range is from DC to 40 GHz. The contact resistance is less than 50 mΩ on aluminum pads.

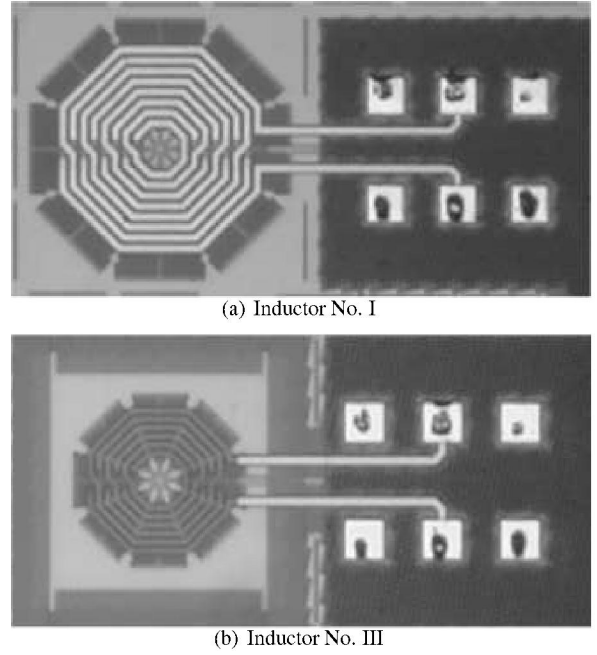(a) Inductor No. I

(b) Inductor No. III

Figure 6. A photograph of two of the inductors. The skating marks from the probes are clearly visible

short, load, and through structures. WinCal from Cascade Microtech was used to calibrate the VNA and collect the data. The de-embedding of the measured data followed the procedure in Section 3, with an open pad structure on-chip and simulated short structures with FastHenry (one for 1-port and another for 2-port).

4.1 1-port Measurement

The measured and corrected curves were limited to the balun's frequency range, 2 GHz-18 GHz. To get the best differential signal from the balun three different cables was tested on different outputs of the balun, thus a total of six combinations were tested. The 1-port measurements were compensated for the error in phase and magnitude of the $180°$ hybrid before extracting the differential Q-value.

4.2 Results

The differential Q-value and self-resonance frequency, f_{sr}, were extracted from the three inductors described in Table 1 and the results are plotted in Fig. 7. The Q-value was calculated by:

$$Q = -\frac{\Im m(Y_{in})}{\Re e(Y_{in})} \qquad (6)$$

where we have used $Y_{in} = Y_{11}$ for 1-port measurements, and $Y_{in} = Y_{11} - Y_{12}$ for 2-port. The self-resonance frequency can be found as the frequency where Q equals zero (13 GHz for inductor II). As can bee seen, the 1-port and 2-port measurements are in alignment with the simulation results by Indentro and FastHenry. Since the die

is naked and not molded the capacitance $C_{sym:tt}$, calculated by Indentro, has been compensated with (3) for a better agreement in terms of Q-value and self-resonance frequency.

5 Conclusion

Measurements of inductors on a lightly doped CMOS substrate have been carried out with 1-port and 2-port techniques. Q-value and f_{sr} have been compared with Indentro, a free inductor design tool, and the agreement is good up to $f_{sr}/2$.

References

[1] N. Troedsson and H. Sjöland, "A Distributed Capacitance Analysis of Co-Planar Inductors for a CMOS QVCO with Varactor Tuned Buffer Stage," *Analog Integrated Circuits and Signal Processing, AICASP*, vol. 42 (1), pp. 7–19, January 2005.

[2] F. Tillman, N. Troedsson, and H. Sjöland, "A 1.2 Volt 1.8 GHz CMOS Quadrature Front-End," *IEEE Symposia on VLSI Circuits*, 2004.

[3] A. Watson, P. Francis, K. Hwang, and A. Weisshaar, "Wide-band distributed modeling of spiral inductors in RFICs," *2003 IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1011–1014, June 2003.

[4] W. Ni, X. Yuan, Y. Tretiakov, R. Groves, and L. Larson, "Design and Modeling of a High-Q On-Chip Hairpin Inductor for RFIC Applications," *2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 547–550, June 2003.

[5] Y. Cao, R. Groves, X. Huang, N. Zamdmer, J.-O. Plouchart, R. Wachnik, T.-J. King, and C. Hu, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 38 (3), pp. 419–426, March 2003.

[6] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33 (5), pp. 743–752, May 1998.

[7] W. Yin, S. Pan, and L. Li, "Experimental characterisation of on-chip octagonal double-helix inductors on silicon substrates," *IEEE Proceedings - Microwaves, Antennas and Propagation*, vol. 150 (4), pp. 265–268, Aug 2003.

[8] Z. Huszka, "3-port characterization of differential inductors," *Proceedings of the 2004 Meeting Bipolar/BiCMOS Circuits and Technology, 2004*, pp. 269–272, Sep 2004.

[9] N. Troedsson, http://www.indentro.com.

[10] R. Thüringer, "Characterization of integrated lumped inductors and transformers," Diplomarbeit, Technischen Universität Wien, April 2002.

[11] T. E. Kolding, "A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements," *IEEE Transactions on Electronic Devices*, vol. 47, pp. 17–27, April 2000.
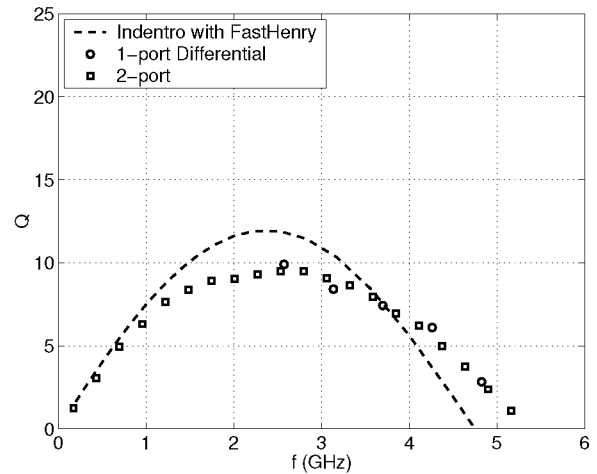
(a) Inductor No. I
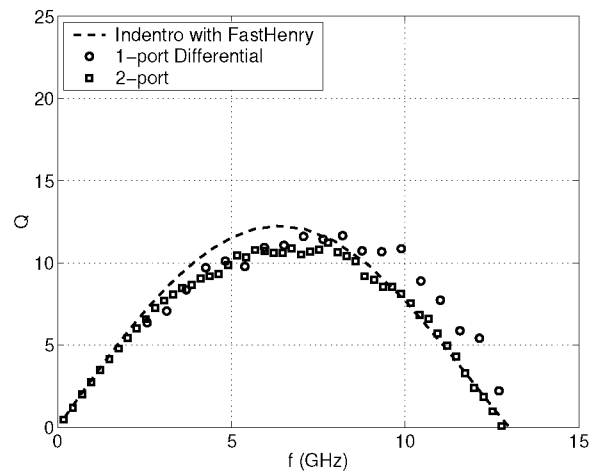
(b) Inductor No. II
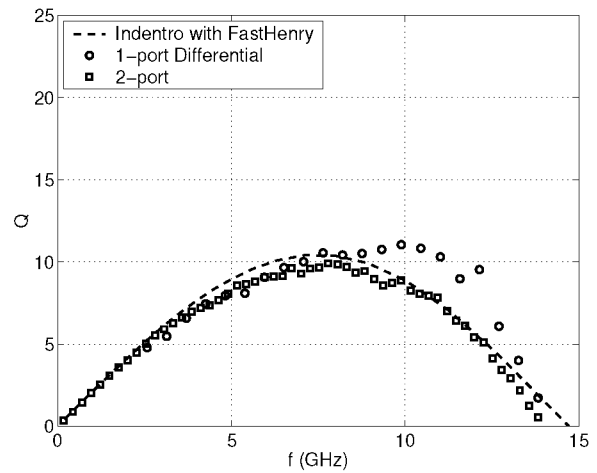
(c) Inductor No. III

Figure 7. Comparison between Indentro with FastHenry, and 1-port and 2-port measurements