Electron Tunneling and Field-Effect Devices in mm-Wave Circuits

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Electron Tunneling and Field-Effect Devices in mm-Wave Circuits

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Doctoral Thesis

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Abstract

Short high-frequency electromagnetic pulses, also referred to as wavelets, are considered for use in various short-range impulse based ultra-wideband applications, such as communication, imaging, radar, spectroscopy, and localization. This thesis investigates field-effect and tunneling based semiconductor devices and their operation in millimeter-wave (mm-wave) impulse transceivers. The main research contribution of this work is the demonstration of a novel high performance InGaAs MOSFET and its integration in a wavelet generator.

The first topic of this thesis is the design and fabrication of a gated tunnel diode (GTD) device. The main feature of the GTD is the ability to switch it between positive differential output conductance (PDC) and negative differential output conductance (NDC). This makes it a versatile element, which can be used to improve circuit functionality.

The second topic is the design and fabrication of an epitaxially regrown InGaAs MOSFET. The device architecture was developed with the aim of minimizing the on-resistance (Ron) to increase the on-state current and extrinsic transconductance (gm,ext.). A 55-nm-gate length MOSFET yields gm,ext.=1.9 mS/μm at VGS=0.5 V and VDS=1 V, Ron=199 Ωμm, an extrapolated fmax of 292 GHz, and ft of 244 GHz. The device performance is analyzed by constructing a small-signal model, which includes the influence of impact ionization, band-to-band tunneling, and the wideband frequency response of gate oxide border traps. Vertical gate-all-around nanowire MOSFETs integrated on a Si platform are also investigated and exhibit gm,ext.=0.155 mS/μm, fmax=9.3 GHz, and ft=14.3 GHz.

The regrown MOSFET is furthermore combined with an RTD to form a switchable NDC component, which is integrated in parallel to an inductive coplanar waveguide to form an oscillator circuit. By switching the output of the RTD-MOSFET between NDC and PDC it is possible to kick-start and rapidly quench the oscillator to produce mm-wave wavelets. The wavelet generator delivers coherent 41-ps-short wavelets with a peak output power of 7 dBm at a rate of 15 Gpulses/s. The wavelets are generated at an energy consumption of 1.9 pJ/pulse.

Key words: Wavelet generator, MOSFET, impulse radio, ultra-wideband, resonant tunneling diode, negative differential conductance oscillator, nanowire, high frequency characterization

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The first topic of this thesis is the design and fabrication of a gated tunnel diode (GTD) device. The main feature of the GTD is the ability to switch it between positive differential output conductance (PDC) and negative differential output conductance (NDC). This makes it a versatile element, which can be used to improve circuit functionality.

The second topic is the design and fabrication of an epitaxially regrown InGaAs MOSFET. The device architecture was developed with the aim of minimizing the on-resistance (R_{on}) to increase the on-state current and extrinsic transconductance ($g_{\mathrm{m,ext.}}$). A 55-nm-gate length MOSFET yields $g_{\mathrm{m,ext.}}$=1.9 mS/μm at V_{GS}=0.5 V and V_{DS}=1 V, R_{on}=199 $\Omega\mu$m, an extrapolated f_{max} of 292 GHz, and f_{t} of 244 GHz. The device performance is analyzed by constructing a small-signal model, which includes the influence of impact ionization, band-to-band tunneling, and the wideband frequency response of gate oxide border traps. Vertical gate-all-around nanowire MOSFETs integrated on a Si platform are also investigated and exhibit $g_{\mathrm{m,ext.}}$=0.155 mS/μm, f_{max}=9.3 GHz, and f_{t}=14.3 GHz.

The regrown MOSFET is furthermore combined with an RTD to form a switchable NDC component, which is integrated in parallel to an inductive coplanar waveguide to form an oscillator circuit. By switching the output of the RTD-MOSFET between NDC and PDC it is possible to kick-start and rapidly quench the oscillator to produce mm-wave wavelets. The wavelet generator delivers coherent 41-ps-short wavelets with a peak output power of 7 dBm at a rate of 15 Gpulses/s. The wavelets are generated at an energy consumption of 1.9 pJ/pulse.

Populärvetenskaplig sammanfattning

Arbetet i denna avhandling berör elektroniska komponenter och hur de kan användas i kretsar för trådlös kommunikation. Den huvudsakliga slutsatsen av arbetet är att innovativa och icke konventionella komponenter kan bidra till att förbättra presentanda och minska effektförbrukningen i system för kommunikation på korta avstånd. Framförallt har en krets tillverkats som genererar extremt korta och högfrekventa elektromagnetiska pulser med frekvens upp till 100 GHz, pulslängd ner till 33 ps och med en repetitionshastighet på upp till 15 Gbit/s. För att möjliggöra detta så har en ny typ av transistor utvecklats. Den främsta egenskapen hos denna transistor är att den opererar vid en väldigt hög hastighet samtidigt som den konsumerar mycket lite energi.

Första gången människan kommunicerad trådlöst, om man bortser från ljud och skrift, var när Guglielmo Marconi skickade elektromagnetiska pulser genom luften år 1894. Dessa pulser skapades genom elektromagnetiska urladdningar som kopplades via en sändande antenn ut i etern och vidare till en mottagande antenn där signalen registrerades. Sedan dess har den trådlösa teknologin utvecklats i rasande takt och har gett upphov till olika produkter så som radar, television och mobiltelefoni. Metoderna har förfinats och gjorts allt mer raffinerade och idag kan man trådlöst skicka mer information per sekund än som kunde lagras totalt på en persondator i början av 1990-talet.

För att fortsätta utvecklingen så krävs nya elektroniska komponenter som kan operera vid högre hastighet och vid mindre effektförbrukning. I detta arbete har fyra olika komponenter studerats. De första två är transistorer byggda från material i grupp 13 och 15 i det periodiska systemet, dessa material benämns även som grupp III och V och har egenskaper som gör att det går att tillverka snabbare och strömsnålare transistorer än med konventionell kiselteknologi. Användningen av III-V material gör att nya komponentstrukturer måste utvecklas. I denna avhandling undersöks en transistor där extra ledande material har tillförts för att minska effektförbrukningen och en transistor där den kontrollerande elektroden omsluter hela den kanal där strömmen färdas, vilket gör att strömmen går att styra på ett mycket effektivt sätt.

Den tredje komponenten baseras på det kvantmekaniska fenomenet tunnling, som innebär att en ström kan flyta genom en region där den enligt klassisk mekanik inte borde kunna existera. Den fjärde komponenten baseras på samma fenomen, men där har en tredje elektrod integrerats för extra funktionalitet.

Tunnlingskomponenterna besitter negativ resistans vilket gör att de kan användas för att tillföra energi i en krets. Genom att integrera en tunnlingskomponent i en resonanskrets så kan en elektromagnetisk svängning produceras. Arbetet i denna avhandling visar att genom att använda en transistor i serie med tunnlingskomponenten så kan svängnin-

gen strypas på ett effektivt sätt när transistorn slås mellan lågt och högt motstånd. Resultatet blir då korta högfrekventa pulser som kan användas för att skicka data mellan en sändare och mottagare, vilket illustreras av Fig. 1. Den framtagna kretsen kan även användas i en mottagare genom att rekonfigurera den elektriska styrsignalen till kretsen. Detta gör att sändare och mottagare kan bestå av samma krets, vilket minskar storleken på systemet och tillverkningskostnaden.

De korta högfrekventa pulserna som sändaren producerar kan även användas i system som mäter avstånd, position, eller som används för att se genom objekt som inte är transparenta för synligt ljus.

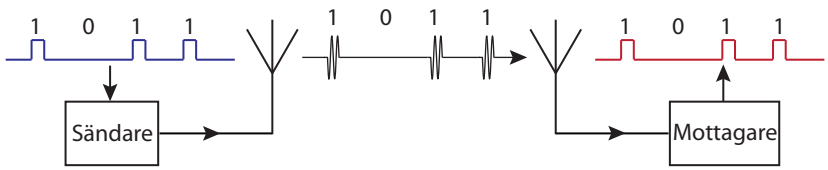

Figure 1: Illustration av hur kretsen som utvecklats i detta arbete kan användas i ett system för trådlös kommunikation.

Preface

This thesis summarizes my academic work for the Doctoral degree in Physics. The work has been done within the Nanoelectronics group at Lund University. The content of this thesis is divided into two parts. The first part serves as an introduction to the second part which constitute of the research papers included in this thesis.

List of papers

I. **M. Egard**, M. Ärlelid, E. Lind, G. Astromskas, and L.-E. Wernersson, "20 GHz Wavelet Generator using a Gated Tunnel Diode", *Microwave and Wireless Components Letters, IEEE*, vol. 19, no. 6, pp. 386-388, June 2009.

I did the circuit design, fabrication, measurements, modeling, and I wrote the paper.

II. M. Ärlelid, **M. Egard**, E. Lind, and L.-E. Wernersson. "Coherent V-Band Pulse Generator for Impulse Radio BPSK", *Microwave and Wireless Components Letters, IEEE*, vol. 20, no. 7, pp. 414-416, July 2010.

I did the fabrication and took part in writing the paper.

III. M. Ärlelid, **M. Egard**, L. Ohlsson, E. Lind, and L.-E. Wernersson. "Impulse-Based 4 Gbps Radio Link at 60 GHz", *Electronic Letters*, vol. 47, no. 7, pp. 467-468, March 2011.

I did the fabrication and took part in writing the paper.

IV. **M. Egard**, M. Ärlelid, E. Lind, and L.-E. Wernersson. "Bias Stabilization of Negative Differential Conductance Circuits Operated in Pulsed Mode", *Transactions on Microwave Theory and Techniques, IEEE*, vol. 59, no. 3, pp. 672-677, March 2011.

I did the circuit design, fabrication, measurements, modeling, and I wrote the paper.

V. M. Ärlelid, **M. Egard**, L. Ohlsson, E. Lind, and L.-E. Wernersson. "A 400 Msamples/s Super-Regenerative Receiver", manuscript.

I did the fabrication and took part in writing the paper.

VI. **M. Egard**, L. Ohlsson, B. M. Borg, F. Lenrick, R. Wallenberg, L.-E. Wernersson, and E. Lind "High Transconductance Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET", *International Electron Devices Meeting, IEDM 2011, IEEE*, pp. 13.2.1-13.2.4, Dec. 2011.

I planned and coordinated the project, did the device design, fabrication, measurements, modeling, and I wrote the paper.

VII. **M. Egard**, L. Ohlsson, M. Ärlelid, B. M. Borg, F. Lenrick, R. Wallenberg, L.-E. Wernersson, and E. Lind "High-Frequency Performance of Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET", *Electron Device Letters, IEEE*, vol. 33, no. 3, pp. 369-371, March 2012.

I planned and coordinated the project, did the device design, fabrication, measurements, modeling, and I wrote the paper.

VIII. **M. Egard**, M. Ärlelid, L. Ohlsson, E. Lind, and L.-E. Wernersson. "$In_{0.53}Ga_{0.47}As$ RTD-MOSFET mm-Wave Wavelet Generator", in press *Electron Device Letters, IEEE*, 2012.

I planned and coordinated the project, did the circuit design, fabrication, measurements, modeling, and I wrote the paper.

IX. **M. Egard**, S. Johansson, A.-C. Johansson, K.-M. Persson, A. Dey, B. M. Borg, C. Thelander, L.-E. Wernersson, and E. Lind. "Vertical InAs Nanowire Wrap Gate Transistors With $f_t > 7$ GHz and $f_{max} > 20$ GHz", *Nano Lett.*, vol. 10, no. 3, pp. 809-812, Feb. 2010.

I did the measurements, modeling, and I wrote the paper.

X. S. Johansson, **M. Egard**, S. Ghalamestani, M. Borg, M. Berg, L.-E. Wernersson, and E. Lind. "RF-Characterization of Vertical InAs Nanowire Wrap Gate Transistors Integrated on Si Substrates", *Transactions on Microwave Theory and Techniques, IEEE*, vol. 59, no. 10, pp. 2733-1738, Oct. 2011.

I did the S-parameter measurements, modeling, and I wrote parts of the paper.

The following lists other contributions to scientific journals, conferences, or patent applications that are related to the topic of this thesis. However, they have not been included here as they are beyond the scope of this thesis or have overlapping content with the previous listed articles. The author changed his last name from Nilsson to Egard during the course of his PhD studies.

11. M. Ärlelid, **M. Nilsson**, G. Astrsomskas, E. Lind and L.-E. Wernersson. "High Tuning-Range VCO Using a Gated Tunnel Diode", oral presentation at the *International Conference on Solid State Materials and Devices 2007*, pp. 798-799 Sept. 2007.

12. **M. Nilsson**, M. Ärlelid, E. Lind, G. Astromskas and L.-E. Wernersson. "20 GHz Gated Tunnel Diode Based UWB Pulse Generator", oral presentation at the *International Symposium on Compound Semiconductors 2008*, pp. Tu 1.6.1-1.6.2, Sept. 2008.

13. L.-E. Wernersson, M. Ärlelid, **M. Egard**, and E. Lind. "Gated Tunnel Diode in Oscillator Applications with High Frequency Tuning", *Solid-State Electronics*, vol. 53, no. 3, pp. 292-296, March 2009.

14. **M. Egard**, M. Ärlelid, E. Lind, G. Astromskas, and L.-E. Wernersson. "20 GHz Gated Tunnel Diode Based UWB Pulse Generator", *Physica Status Solidi (c)*, vol. 6, no. 6, pp. 1399-1402, April 2009.

15. **M. Egard**, M. Ärlelid, E. Lind, P. Caroff, G. Astromskas, M. Borg, and L.-E. Wernersson. "60 GHz Wavelet Generator for Impulse Radio Applications", oral presentation at the *38th European Microwave Conference, EuMC 2009, IEEE*, pp. 1908-1911, Sept. 2009.

16. M. Ärlelid, **M. Egard**, E. Lind, and L.-E. Wernersson. "60 GHz Ultra-Wideband Impulse Radio Transmitter", oral presentation at the *International Conference on Ultra-Wideband, ICUWB 2009, IEEE*, pp. 185-188, Sept. 2009.

17. **M. Egard**, M. Ärlelid, E. Lind, and L.-E. Wernersson. "A 12.5 Gpulses/s 60 GHZ Bi-Phase Wavelet Generator", oral presentation at the *34th International European Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE 2010*, pp. 51-52, May 2010.

18. **M. Egard**, M. Ärlelid, E. Lind, and L.-E. Wernersson. "Gated Tunnel Diode with a Reactive Bias Stabilizing Network for 60 GHz Impulse Radio Implementations", oral presentation at the *68th International Device Research Conference, DRC 2010, IEEE*, pp. 161-162, Aug 2010.

19. L.-E. Wernersson, **M. Egard**, M. Ärlelid, and E. Lind. "Tunneling-Based Devices and Circuits", invited presentation at the *68th International Conference on IC Design and Technology, ICICDT 2010. IEEE*, pp. 190-193, July 2010.

20. M. Ärlelid, **M. Egard**, E. Lind, and L.-E. Wernersson. "A 60 GHz Superregenerative Oscillator for Implementation in an Impulse Radio Receiver", best student paper award presentation at the *International Conference on Ultra-Wideband, ICUWB 2010, IEEE*, pp. 1-4, Sept. 2010.

21. M. Ärlelid, **M. Egard**, L. Ohlsson, E. Lind, and L.-E. Wernersson. "60 GHz Impulse Radio Measurements", oral presentation at the *International Conference on Ultra-Wideband, ICUWB 2011, IEEE*, pp. 536-440, Sept. 2011.

22. D. Sjöberg, **M. Egard**, M. Ärlelid, G.P. Vescovi, and L.-E. Wernersson. "Design and Manufacturing of a Dielectric Resonator Antenna for Impulse Radio at 60 GHz", oral presentation at the *3rd European Conference on Antennas and Propagation, EuCAP 2009, IEEE*, pp. 3549-3553, March 2009.

23. L. Ohlsson, D. Sjöberg, M. Ärlelid, **M. Egard**, E. Lind, and L.-E. Wernersson. "Admittance Matching of 60 GHz Rectangular Dielectric Resonator Antennas for Integrated Impulse Radio", poster presentation at the *Loughborough Antennas & Propagation Conference, LAPC 2010, IEEE*, pp. 253-256, Nov. 2010.

24. **M. Egard**, L. Ohlsson, B. M. Borg, L.-E. Wernersson, and E. Lind "Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET with Selectively Regrown Source and Drain Contact Layers", late news presentation at the *69th International Device Research Conference, DRC 2011, IEEE*, pp. 1-2, June 2011.

25. E. Lind, **M. Egard**, S. Johansson, A.-C. Johansson, K.-M. Persson, A. Dey, B. M. Borg, C. Thelander, and L.-E. Wernersson. "High Frequency Performance of Vertical InAs Nanowire MOSFET", oral presentation at the *22nd International Conference on Indium Phosphide and Related Materials, IPRM 2010, IEEE*, pp. 1-4, July 2010.

26. S. Johansson, S. G. Ghalamestani, **M. Egard**, B. M. Borg, M. Berg, L.-E. Wernersson, and E. Lind. "High-Frequency Vertical InAs Nanowire MOSFETs Integrated on Si Substrates", oral presentation at the *38th International Symposium on Compound Semiconductors, ISCS 2011, IEEE*, pp. 471-472, May 2011.

27. S. Johansson, **M. Egard**, S. G. Ghalamestani, B. M. Borg, M. Berg, E. Lind, and L.-E. Wernersson. "High-Frequency Characterization of Vertical InAs Nanowire Wrap-Gate FETs on Si(111) Substrates", late news presentation at the *38th International Conference on Solid State Materials and Devices, SSDM 2011*, pp. KM-4-3, Sep. 2011.

28. S. Johansson, S. G. Ghalamestani, **M. Egard**, B. M. Borg, M. Berg, L.-E. Wernersson, and E. Lind. "High-Frequency Vertical InAs Nanowire MOSFETs Integrated on Si Substrates", *Physica Status Solidi (c)*, vol. 9, no. 2, pp. 350-353, Feb. 2012.

Patent applications

29. **M. Egard**, E. Lind, and L.-E. Wernersson. "Process for Manufacturing a Semiconductor Device and an Intermediate Product for the Manufacture of a Semiconductor Device", Patent Cooperation Treaty (PCT) application EP2011/059190, submitted to *European Patent Office (EPO)*, June 2011.

30. **M. Egard**, M. Ärelid, and L.-E. Wernersson. "Transceiver Module", Patent Cooperation Treaty (PCT) application EP2011/058847, submitted to *European Patent Office (EPO)*, May 2011.

31. L.-E. Wernersson, E. Lind M. Ärlelid, **M. Nilsson**. "Ultrabredbandig Sändare och Mottagare", Swedish patent application SE 0700531-7, submitted to *Patent och Registreringsverket*, Feb. 2007.

Contents

Acknowledgments

Five years goes by in a hurry, but looking at what I have experienced during this period it rather feels like a very long time. I have many people to thank for these experiences and I would like to acknowledge a few of all of you that have been a part of my life during this time.

I started my PhD studies in spring of 2007 when professor Lars-Erik Wernersson gave me the opportunity to look into the exciting field of nanoelectronics. The first project was the gated tunnel diode, which you, Lars-Erik, started to develop during your own PhD studies, and I could actually feel that it was almost as you handed me your baby to look after and take care of. Many projects later I would like to thank you for your expertise, inspiration, and encouragement.

My assistant supervisor Erik Lind is the second person that deserves a special recognition. I have really enjoyed working with you, especially on the MOSFET projects were you have been a solid rock that I, among others, have relied on. To quote one of you former master students "Erik is the best that FTF has ever produced". I would also like to thank my second assistant supervisor, professor Henrik Sjöland, for sharing your wisdom regarding high-frequency electronics.

Mats Ärlelid, dear colleague, I have heard people describing us as an old married couple, arguing and finishing each other sentences. Family is very important to me and I am really happy that we will be able to continue working together.

Lars Ohlsson, you have been an extremely valuable addition to the Wavelet generator team and it has been great working with you. You also deserve extra credit for not complaining when I ask you to run tests in the laboratory, one idea stupider than the other.

Mattias Borg, Gvidas Astromskas, Philippe Caroff, and Johannes Svensson, you have all contributed to the work of this thesis with your expertise in epitaxial growth, and as always, no device is better than the material it is fabricated from. A great example of this are the Nanowire MOSFETs, and I would like to thank Karl-Magnus Persson, Sofia Johansson, Anil Dey, Ann-Charlotte Johansson, Sepideh Ghalamestani, Martin Berg, and Claes Thelander for developing such great devices.

Apart from assisting in the diploma work of Lars Ohlsson I have also been assisting Giuliano Vescovi, Kristveig Thorbergsdottir, Johannes Bengtsson, and Elvedin Memisevic. You have all contributed to the research at the department in an excellent way and I would like to take the opportunity to thank the teachers, fellow PhD students, and staff at Solid State Physics for producing such great students. It has been a fantastic environment to work in, with extremely intelligent and productive people wherever I have turned. I would especially like to recognize Kristian Storm for always being eager to help me with challenges that I have faced during this work, which are mostly related to the painstaking task of semiconductor device fabrication. Fortunately, I have always had the staff of the Lund Nano Lab to assist me; it has been a pleasure to work in such great facilities.

Now to the persons that have helped me staying sane during this work. Whether it is a lively after work, barbecue at the beach, road trip to Hamburg, or chilling in a hot tube in the back of your garden, you, my friends, always make me feel at ease. The same goes for my in-laws Ann and Nils-Gustav, and my parents Gunnel and Jan who have always been there for me. I cannot thank my younger brothers Robert and Tommy enough, you are the best, and both of you have actively helped me with the work presented in this thesis, which I think is really cool.

I have understood that I give a very calm and professional impression at the department. The person that makes this possible is my wife Jessika, as she gets to deal with the opposite sides of my personality at home. Isabelle and Jessika, you are the love and joy of my life.

Mikael Egard

- *Det ser ut som om någon har slirat med moppen på ditt prov*
Robert Nilsson age 15 during his "prao" at Solid State Physics

List of Acronyms

BER	Bit error rate
BSN	Bias stabilizing network
BTBT	Band-to-band-tunneling
CPW	Coplanar Waveguide
DBH	Double barrier heterostructure
EBL	Electron beam lithography
ED	Energy detector
EII	Electron impact ionization
EIRP	Equivalent isotropically radiated power
EOT	Equivalent oxide thickness
FCC	Federal Communications Commission
GAA	Gate all around
GTD	Gated tunnel diode
HEMT	High electron mobility transistor
HBT	Heterojunction bipolar transistor
IR	Impulse radio
ITRS	International Technology Roadmap for Semiconductors
MBE	Molecular beam epitaxy
MIM	Metal-insulator-metal
mm-wave	Millimeter wave
MOCVD	Metalorganic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
NDC	Negative differential conductance
NW	Nanowire
OFDM	Orthogonal frequency-division multiplexing

PA	Power amplifier
PDC	Positive differential conductance
PRF	Pulse repetition frequency
QTD	Quenchable tunnel diode
RTD	Resonant tunneling diode
S	Scattering
SCR	Space charge region
SNR	Signal to noise ratio
SRO	Super-regenerative oscillator
UWB	Ultra-wideband
VLSI	Very-large-scale integration
VNA	Vector network analyzer
WLAN	Wireless local area network

List of Symbols

A_{RTD}	Resonant tunneling diode area
C_{ce}	Collector emitter capacitance
C_{gp1}	Contact layer-to-gate overlap capacitance
C_{gp2}	Contact-to-gate fringing capacitance
C_{ox}	Gate oxide capacitance
C_{s}	Bias stabilizing capacitance
C_{sc}	Semiconductor capacitance
D_{it}	Interface trap density
ΔI	Peak to valley current difference
ΔV	Peak to valley voltage difference
ϵ_{ox}	Oxide permittivity
E_{p}	Energy consumption per wavelet
f_0	Fundamental oscillation frequency
f_{max}	Maximum oscillation frequency
f_{t}	Current gain cut-off frequency
g_{L}	Load conductance
g_{m}	Intrinsic transconductance
$g_{\mathrm{m,ext}}$	Extrinsic transconductance
G_{o}	DBH large signal output conductance
g_{o}	DBH small signal output conductance
g_{i1}	Transconductance related to gate-drain potential
g_{i2}	Transconductance related to gate-source potential
$g_{\mathrm{o,min}}$	DBH minimum small signal output conductance
h_{21}	Current gain
I_{off}	Off-state current

I_{on}	On-state current
J_{p}	RTD peak current
J_{v}	RTD valley current
k_{B}	Boltzmann constant
L_{c}	Contact length
L_{b}	Bias inductance
L_{g}	Gate length
L_{gc}	Gate to contact spacing
L_{tw}	Gate overhang length
L_{t}	Coplanar waveguide inductance
m^*	Effective mass
N_{bt}	Border trap density
P_{peak}	Peak output power
Q_{tank}	Tank circuit quality factor
R_{access}	Access resistance
R_{c}	Collector resistance
R_{cn}	Contact resistance
R_{e}	Emitter resistance
R_{g}	Gate resistance
R_{gc}	Gate to contact resistance
R_{on}	On-resistance
SS	Subthreshold swing
t_{c}	Contact layer thickness
τ_{i}	Time constant related to EII and BTBT
T_{L}	Lattice temperature
t_{ox}	Oxide thickness
t_{r}	Support layer height
μ	Mobility
U	Unilateral power gain
$v(0)$	Oscillator initial condition

V_{DBH}	Voltage drop across the DBH
V_{dd}	Supply voltage
v_{inj}	Injection velocity
V_{p}	RTD peak current voltage
V_{v}	RTD valley current voltage
V_{th}	Threshold voltage
W_{g}	Gate width
ω_0	Angular frequency
Y_{xy}	Admittance

Introduction

Introduction

Chapter 1

Background and Motivation

Electromagnetic wireless communication has been around since the discovery of wireless telegraphy back in the 19th century [1]. This marked the beginning of an era, which to present day has given us innovations such as television, radar, mobile phone, etc. The impact of these technologies on our society cannot be underestimated, with that said, we have just started to see the possibilities that wireless data communication will be able to provide. In the recent decade, new technologies for high data rate communication at short distances have emerged. Bluetooth and wireless local area network (WLAN) are two examples. These solutions have given us a glimpse of what a truly wireless environment would bring, an environment where all our gadgets talk to us and to each other, without the inconvenience of wires. Bluetooth marked the beginning of this era with its data rate of 1 Mbit/s, WLAN has pushed the rate to more than 100 Mbit/s. In the search for new technologies that will increase the bit rate and lower the power consumption, spread spectrum techniques such as Ultra-wideband (UWB) communication are highly interesting and are explored in the industry, at universities, and at research institutes. UWB communication in the 3.1-10.6 GHz band now delivers 480 Mbit/s, and with the new IEEE standard for the 60 GHz band, UWB will offer data rates of 2 Gbit/s and higher [2].

One factor that has made it possible to increase the speed of wireless communication is the increase in transistor performance. Faster transistors translate into higher data rates and lower power consumption per bit. Microelectronics, and in recent years nanoelectronics, has provided us with generation after generation of high performance transistors. However, conventional Si transistor technology is running out of steam and that is why novel device concepts are being investigated. The resonant tunneling diode (RTD), the gated tunnel diode (GTD), the regrown metaloxide−semiconductor field-effect transistor (MOSFET), and the nanowire (NW) MOSFET presented in this thesis are examples of such devices. This thesis especially focuses on the use of these devices in circuits generating wavelets, which is a short burst of electromagnetic energy that can be used as the basis for UWB communication. The outline of this thesis is;

Chapter 1 presents the concept of ultra-wideband communication and how the wavelet

generator contributes to this field of research.

Chapter 2 introduces the theory of resonant tunneling diodes and describes the operation, fabrication, and characterization of the gated tunnel diode.

Chapter 3 gives an introduction to the field of III-V MOSFETs. Device architecture considerations are discussed in detail and related to the fabrication of a regrown MOSFET. This chapter also covers high-frequency characterization of electronic devices.

Chapter 4 describes the series integration of a resonant tunneling diode and the regrown MOSFET.

Chapter 5 covers the design and fundamental operation of the wavelet generator. Measurement results are accompanied by analytical modeling of the circuit operation.

Chapter 6 summarizes the thesis and discusses future applications and challenges for the wavelet technology.

1.1 60 GHz ultra-wideband communication

As given by the name "Ultra-Wideband" communication, this technique of transmitting data makes use of a very wideband frequency spectrum. This is in contrast to conventional narrow band carrier modulation methods. According to Shannon's law

$$C = BW \log_2(1 + \frac{S}{N}), \tag{1}$$

which describes the channel capacity C (bit/s), either an increase in the signal power S (W) or the bandwidth BW (Hz) gives an increased upper bound on the data rate when transmitting in an channel with white additive Gaussian noise N (W). Equation (1) further states that for a fixed signal to noise ratio (S/N) the upper bound on the data rate is proportional to the bandwidth. This is why huge channel capacities can be achieved without utilizing higher order modulations that require large S/N ratios. This illustrates one of the benefits of UWB communication.

Besides the achievable data rates, one very interesting benefit of spreading the transmitted energy over a large bandwidth is that it reduces the interference to other communication systems, as the signal power at one discrete spectral component is low. How much power an UWB signal is allowed to carry at a certain frequency is regulated by the Federal Communication Commission (FCC) in the US, and corresponding authorities in the rest of the world. For the 3.1 to 10.6 GHz band the FCC decided in 2002 that a signal is considered UWB if its bandwidth exceeds 500 MHz or 20% of its center frequency, and that it is not allowed to exceed -41.3 dBm/MHz at any frequency in this band [3]. UWB communication in the 3.1 to 10.6 GHz band has not been the expected success, much due to additional constraints imposed by the regulatory document. The maximum achievable data rate that is targeted as of now is 480 Mbit/s [2, 4]. Instead, industry and the research community is turning their attention

Table 1: Available unlicensed spectrum at 60 GHz

	Unlicensed spectrum (GHz)
North America	57-64
Europe	59-66
Australia	59.4-62.9
Korea	57-64
Japan	59-66

to the 60 GHz band with its 5 GHz of almost worldwide unlicensed bandwidth [5, 6], which is listed in Table 1. Besides the band being worldwide unlicensed and accepted, the high frequency decreases the critical dimensions of the antennas to millimeter size. Combining several antennas and controlling the phase among the multiple outputs provides the possibility to only transmit power in the desired direction [2]. This decreases intersymbol interference, interuser interference, and destructive interference (fading) from multipath components [7].

At 60 GHz the free-space path loss

$$L = 20 \log_{10} \frac{4\pi d}{\lambda}, \tag{2}$$

where d is the distance and λ is the wavelength, is 28 dB larger than at the 2.4 GHz WLAN band, and combined with an increased material attenuation at higher frequencies restricts the targeted 60 GHz communication scenarios to line-of-sight and in-the-room [5]. Examples of applications where 60 GHz communication could have, and already has, a great impact are simple docking solutions for downloading high definition content or wireless connection to a display.

When UWB communication was first introduced the idea was to generate short pulses in the time domain that translates into a wideband signal in the frequency domain, this is known as UWB Impulse Radio (IR) communication. However, the regulation describing the transmission of UWB signals allows for the transmission of any signal that fulfills the emission regulations, which makes techniques such as Orthogonal Frequency Division Multiplexing (OFDM) interesting [5]. OFDM uses the robustness of standard digital coding to modulate a continuous carrier signal, the data is then transmitted in N different sub-channels using orthogonal carrier signals to avoid interference. Two frequencies are considered orthogonal when they are separated by $\Delta f = 1/T_0$, where T_0 is the time it takes to transmit a symbol on the corresponding carrier [8]. Designing the subchannels correctly will make the transmitted signal as a whole fulfill the requirements for a signal to be considered UWB. The OFDM way of UWB communication is a complex solution as it deals with the parallel transmission in N subchannels. This requires sophisticated transmitter and receiver circuits, which

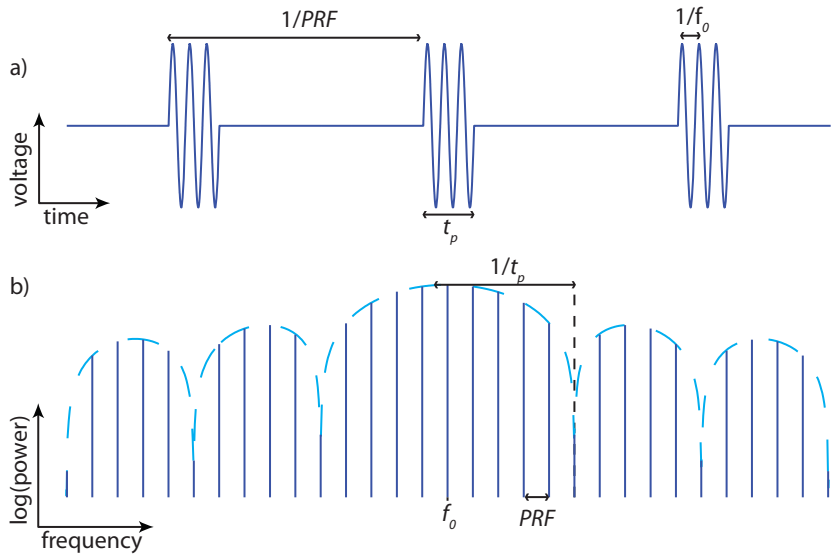

Figure 2: Illustration of a sequence of wavelets (a) in the time domain and (b) in the frequency domain.

have large power consumption, but high bit rates, high spectral efficiency, and low bit error rate (BER) [7].

1.1.1 Ultra-wideband impulse radio communication

UWB IR communication is based on the transmission of short pulses representing the data, much like the first spark radio transmitters designed by Marconi [1]. The benefit of UWB IR communication is that high bit rates may be achieved using low-complexity transmitter layouts with a very low power consumption. The duration of the transmitted pulses are typically a few hundred picoseconds long [8] and one or several pulses can be used to represent each bit, a higher energy per bit decreases the BER. Different techniques to modulate the data using IR UWB exist, examples are pulse position modulation (PPM), pulse amplitude modulation (PAM), and phase shift keying (PSK). The simplest system relies on non-coherent receiver schemes where energy detection is used, PSK implementations requires coherent systems, which decreases the BER, but requires more complex receiver structures.

It should also be mentioned that UWB IR is relatively immune to multipath fading, as compared to continuous wave carrier based narrow band radio, which experience deep fades. The reason is that the transmitted UWB IR pulses are very short in time and space, hence the multipath reflections will not overlap the main part of the pulse [9, 10].

Besides high speed data communication, UWB IR is considered for applications

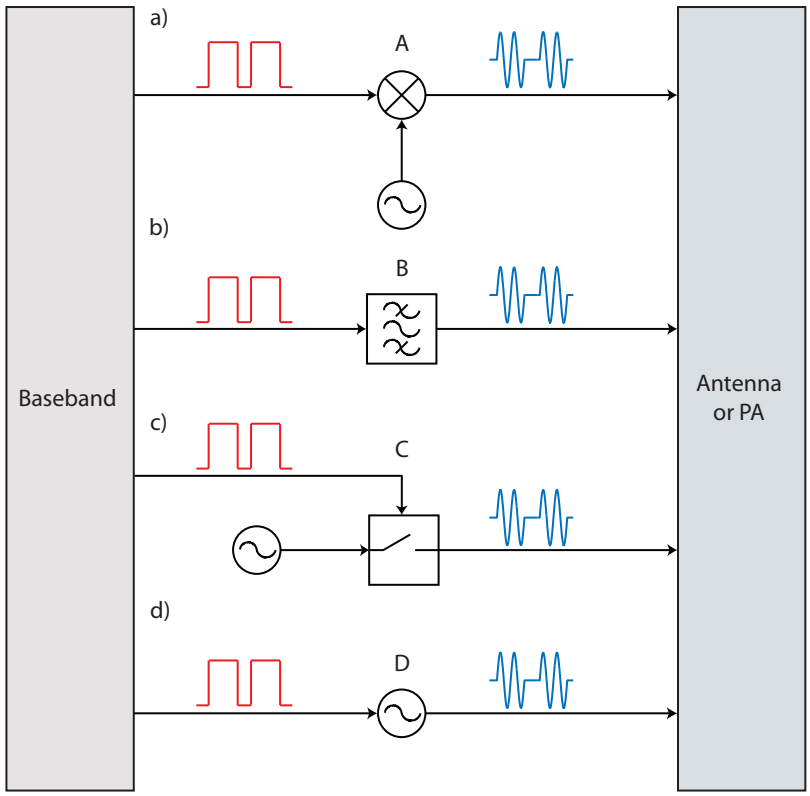

Figure 3: Illustration of 4 different wavelet generator implementations, (a) upconversion of a baseband pulse, (b) filtering a baseband pulse, (c) passing a continuous oscillator signal through a series of switches, and (d) switching an oscillator on and off.

in radar [11], spectroscopy [12], localization [13], and imaging [14]. Different applications have different requirements when it comes to range, pulse length, and pulse repetition time, but they are all based on the same basic circuit topology.

1.2 High frequency wavelet generators

Two different types of techniques are commonly used for generating pulses in UWB IR systems, the first category includes pulses generated by digital circuits. These pulses are created by controlling the delay among individual baseband signals and combining them into the desired output waveform [15]. Compact pulse generators may be created using this technique, it is however challenging to obtain high output power in the 60 GHz band [16, 17].

The second category of UWB IR signals consists of pulses, or wavelets as they are also denoted, which are generated from a carrier signal. An illustration of such a signal is shown in Fig. 2(a). The spectral shape is given by the center frequency of the carrier signal f_0, the pulse length t_{p}, and the pulse repetition frequency (PRF), as given by Fig. 2(b). The spectral shape is also determined by the envelope of the pulse in the time domain.

Different examples of wavelet generators are illustrated in Fig. 3. The input signal to all different types of wavelet generators is a baseband pulse and the wavelet is delivered to a power amplifier (PA) or directly to an antenna. Figure 3(a) describes the solution presented by Wentzloff *et al.* in [18], where a baseband or Gaussian pulse is upconverted to the desired center frequency. This gives good control of the output wavelet characteristics such as the center frequency. A second alternative is to generate a very short baseband pulse that has frequency components in the targeted band [19–21], as illustrated in Fig. 3(b). This pulse is then passed through a filter with the appropriate characteristics to form the high frequency wavelet. Figure 3(c) describes another option, which is to pass a continuously running oscillator signal through a series of switches, which may include gain [14, 22]. High frequency pulses are generated by turning these switches on and off, using the baseband signal to represent the data that is to be transmitted.

The wavelet generator investigated in this thesis belongs to the group which are illustrated in Fig. 3(d). These wavelet generators operate by using the baseband signal to switch a circuit between an oscillating state and a non-oscillating state. Example of other implementations that fall in the same category are given in reference [23–26].

When comparing the solutions, presented in Fig. 3, it is possible to identify benefits of the implementation illustrated in Fig. 3(d):

- No need for any high frequency upconversion. Designing high frequency mixers that has a high conversion efficiency is a challenging task.

- No need for high frequency band pass filtering, which would add insertion loss or increase the power consumption.

Table 2: State of the art mm-wave wavelet generators

Type	Technology	f_0 (GHz)	t_p (ps)	P_peak (dBm)	E_p (pJ/pulse)
B	InP130nm HEMT [19][1,2]	82.5	80	-22	63
C	SiGe BiCMOS130nm [22][2]	60.5	350	9	(150mW)
C	SiGe BiCMOS130nm [14]	90	26	<17.2	(450mW)
D	CMOS65nm SOI [23][1,2]	56	250	5.3	12.6
D	CMOS65nm SOI [26][1]	60	500	5	5.0
D	GaAs Paper II[1]	60	33	-13	4.6
D	InP Paper VIII[1]	70	41	7	1.9

[1]Coherent signal. [2]Baseband generator included.

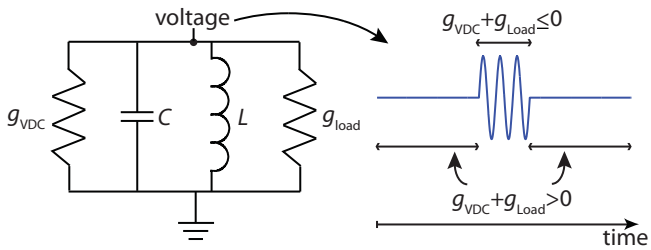

Figure 4: Switchable oscillator circuit.

- No need for high frequency switches. To get enough attenuation of the signal typically several switches are required, each consuming power.
- All the generated energy is synthesized directly at the RF frequency, no energy is lost in filters, mixers or switches. This gives the possibility to realize efficient transmitters.

These benefits are further accentuated in Table 2, which lists state of the art mm-wave wavelet generators based on the techniques described in Fig. 3. The benchmarking contains center frequency (f_0), wavelet length (t_p), wavelet peak output power (P_peak), and energy consumption per wavelet (E_p). Table 2 also indicates if the wavelet generators produce coherent signals, which is required to retain phase information, and if the baseband signal generator is included in E_p. The wavelet generators considered in this thesis are represented by Paper II and Paper VIII, they compare favorably, especially when a short t_p is required.

The wavelet generators developed in this work are thoroughly analyzed in Chap-

ter 5, a brief introduction to the concept is given here and is illustrated by Fig. 4. The generalized circuit consists of two reactive elements, one inductor (L) and one capacitor (C), a load given by g_{load}, and a variable conductance (g_{VDC}), which may be switched between negative and positive differential conductance. When g_{VDC} is switched to negative values such that it compensates for resistive losses in the circuit, i.e. $g_{\mathrm{VDC}}+g_{\mathrm{load}}<0$, the circuit will be unstable and oscillations are produced. The frequency of the oscillation is determined by the resonance frequency of the reactive elements, which is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

Switching g_{VDC} to a positive value will add loss to the circuit and the oscillation will decay, hence, the circuit in Fig. 4 has the functionality of the wavelet generator in Fig. 3(d).

This thesis mainly focuses on developing devices with the property of the variable conductance in Fig. 4. These devices are based on the negative differential conductance of a resonant tunneling diode, which is the first topic of the next chapter.

Chapter 2

The Gated Tunnel Diode

The gated tunnel diode (GTD) considered in this chapter is an example of a variable conductance device that can be used in wavelet generating circuits. It is based on the negative differential conductance (NDC) property of a resonant tunneling diode, which has been utilized in various electronic circuits such as high frequency oscillators [27], low power memory cells [28], and analog to digital converters [29]. In order to make the RTD more flexible as a circuit element it may be combined with a transistor, which provides the possibility to tune the NDC property. Examples are given in [30] where a RTD has been integrated in series with a heterojunction bipolar transistor, and in [31] where the RTD has been integrated in parallel with a field effect transistor.

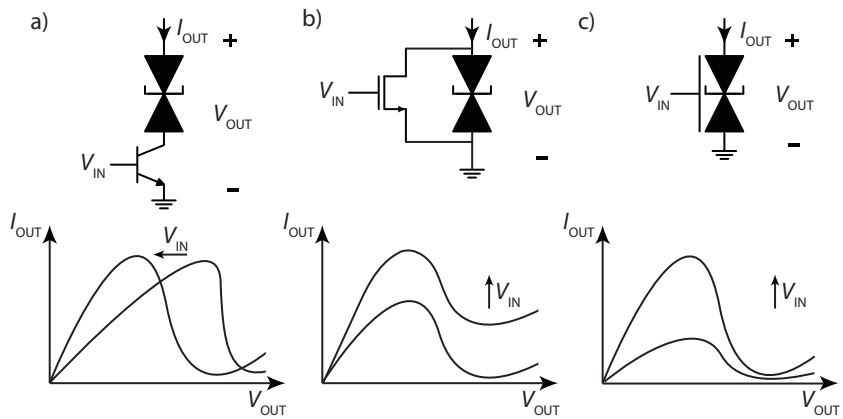

Figure 5: (a) and (b) shows the circuit layout and output characteristics of a series and parallel integration of a transistor and an RTD, respectively. (c) Symbol representing the GTD together with an illustration of its output characteristics.

A schematic layout of these devices and their corresponding output characteristics are shown in Fig. 5(a) and (b). These configurations require performance matching of the transistor and the RTD, and design for additional voltage drop across the transistor. The GTD presented here controls the conducting area of an RTD by an integrated

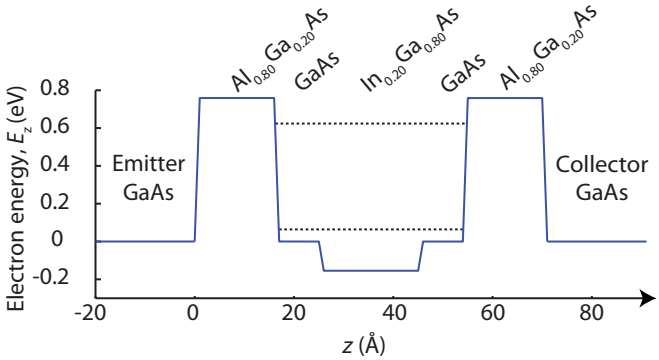

Figure 6: Conduction band diagram of the GaAs DBH used in this thesis, the complete epitaxial structure is given in Table 3.

metal gate, which provides the possibility to directly modulate the output conductance, as illustrated in Fig. 5(c).

This chapter describes the basic principle and operation of an RTD, and the fabrication and modeling of the GTD. The GTD is further analyzed in Chapter 5, where the possibility of switching the output conductance between positive and negative values is used to generate wavelets.

2.1 The resonant tunneling diode

A resonant tunneling diode consists of a double-barrier heterostructure (DBH). The conduction band diagram of the GaAs based DBH that are considered in this thesis is given in Fig. 6. The confinement potential, formed by the conduction band offset between the materials of the DBH, creates quasi-bound states at certain energies E_{n}, these are indicated by the dashed lines in Fig. 6. Resonant tunneling from the emitter to the collector through the DBH may occur when the energy of an electron outside the DBH coincide with that of a quasi bound state inside the DBH.

In the simple model considered here the wavefunction of an electron outside the DBH is represented by a plane wave with a crystal momentum vector $\bar{k}$, the spatial coordinate vector $\bar{r}$, and the amplitude vector A. If a translation invariant DBH is considered it is possible to separate the motion in the x and y plane into plane waves that are independent of the wavefunction in the z direction [32]. This makes it possible to write the wavefunction as

$$\Psi = a{\cdot}e^{(ik_{\mathrm{x}}x)}b{\cdot}e^{(ik_{\mathrm{y}}y)}\phi(z) \tag{4}$$

with the energy

$$E(\bar{k}) = \frac{\hbar^2(k_{\mathrm{x}}^2 + k_{\mathrm{y}}^2)}{2m^*} + E_{\mathrm{n}},\ n = 1, 2, 3... \tag{5}$$

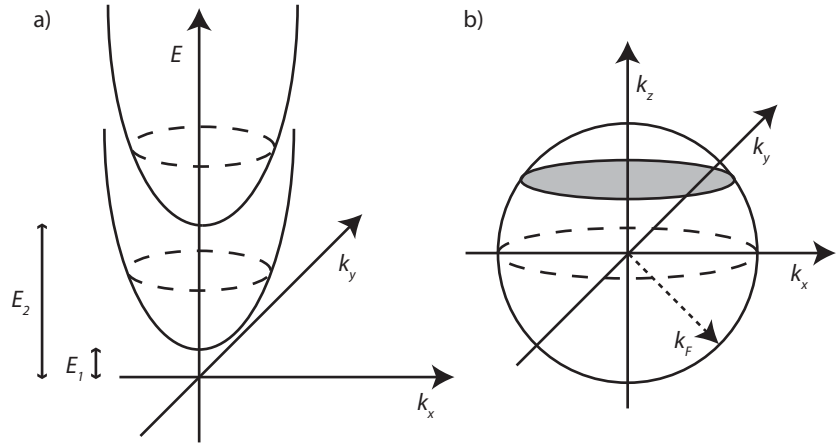

Figure 7: (a) Illustration of the available energies inside the potential confinement. (b) The shaded surface represents electronic states available for transmission through the DBH at a certain energy E_{z}. k_{F} is the Fermi wavenumber corresponding to the Fermi energy.

Here, m^* is the effective mass of the electron and a and b are the amplitude of the plane waves in the x and y direction, respectively. In this model k_{x} and k_{y}, which are the lateral crystal momentums, are conserved together with E_{z}. This implies that the restriction on the crystal momentum in the z-direction

$$k_{\mathrm{z}} = \frac{\sqrt{2m^* E_{\mathrm{n}}}}{\hbar}, \tag{6}$$

has to be fulfilled in order to have transmission through the DBH. Figure 7(a) shows an illustration of the available energies between the barriers, as a function of k_{x} and k_{y}. The electronic states that are available for tunneling at E_{n} are depicted in Fig. 7(b).

The probability for an electron to be transmitted from the emitter side to the collector side, through the DBH structure in Fig. 6, can be calculated using the transfer matrix approach [33]. Details regarding the calculations are presented in appendix A and the result is shown in Fig. 8, where it is seen that the transmission probability approaches unity for energies corresponding to a resonant state. Off resonance the probability instead approaches that of the tunneling probability through a barrier with a thickness corresponding to the total thickness of the two barriers forming the potential confinement of the DBH. This is represented by the dashed trace in Fig. 8, which was also calculated using the transfer matrix method. Thus, a resonant tunneling structure resembles a Fabry-Perot interferometer where constructive interference leads to a transmission maximum. Here it is the wavefunctions of the tunneling electrons that interfere constructively to give a transmission maximum. A more thorough introduction to the resonant tunneling phenomena may be found in [34], and for a

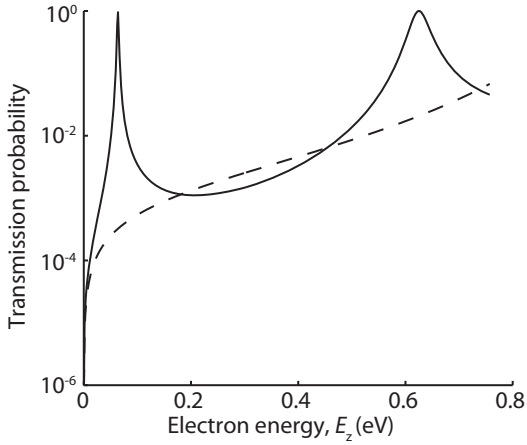

Figure 8: The solid trace shows the result of the calculation of the transmission probability through the DBH given in Fig. 6, the method used is described in more detail in appendix A. The transmission through a 3.2-nm-thick $Al_{0.8}Ga_{0.2}As$ barrier is illustrated by the dashed line.

deeper understanding of the theory [33] is recommended.

The current density through the DBH may be calculated using the Esaki-Tsu formula:

$$J = \frac{m^* e k_B T_L}{2\pi^2 \hbar^3} \int_0^\infty \mathrm{d}E_\mathrm{z} T(E_\mathrm{z}, V_\mathrm{DBH}) \ln\left(\frac{1 + e^{(\mu_E - E_\mathrm{z})/k_\mathrm{B}T_\mathrm{L}}}{1 + e^{(\mu_\mathrm{E} - E_\mathrm{z} - eV_\mathrm{DBH})/k_\mathrm{B}T_\mathrm{L}}}\right) \quad (7)$$

Here, T_L is the temperature, k_B is the Boltzmann constant, V_DBH is the voltage applied across the DBH, and μ_E and μ_C are the chemical potentials at the emitter and collector side, respectively. Equation (7) includes two terms that are integrated with respect to E_z, the first is the transmission probability considered earlier and the second is a function which accounts for the net amount of carriers available for tunneling at a certain E_z. Both these terms are functions of the applied bias V_DBH.

Figure 9 shows the conduction band diagram under different bias conditions and the corresponding current density transmitted through the RTD for the DBH structure defined in Fig. 6. A factor η=0.27 has been used to relate V_DBH to V_CE, which is the voltage drop across the DBH and the adjacent spacer layers. The value of η was estimated from 2D simulations using the software ATLAS by Silvaco. As the bias is increased the energy difference between the resonant level and the conduction band edge on the emitter side is decreased, as depicted in Fig. 9(a). Figure 9(b) illustrates the DBH at V_CE=0.40 V, increasing the bias beyond this point will cause the resonant level to be below the energy of electrons eligible for transmission from the emitter to the collector. This is when the current starts to decrease and the NDC property of the RTD presents itself, as seen in Fig. 9(d).

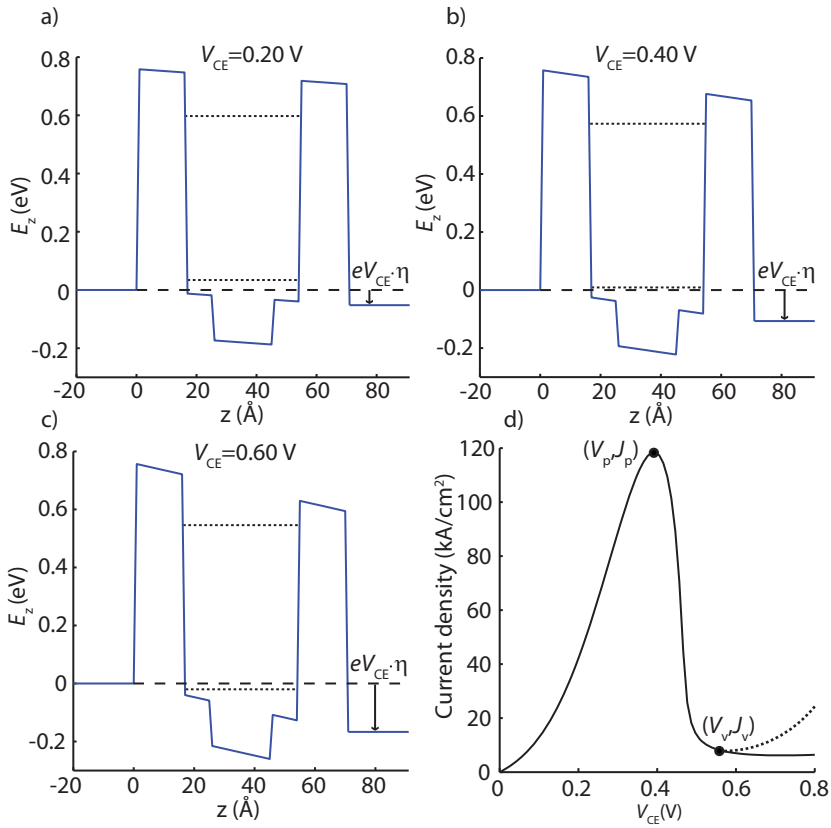

Figure 9: (a)-(c) Conduction band minimum of the DBH described in Fig. 6, the resonant states are indicated by dashed lines. The corresponding current density is shown in (d).

Important metrics of an RTD is the peak current density ($J_{\rm p}$) and peak voltage ($V_{\rm p}$), which are indicated in Fig. 9(d). The transfer matrix method is useful to predict the peak current density (the experimental value for this structure is $J_{\rm p}$=120 kA/cm^2), but as the solution is not made self-consistent it does not predict $V_{\rm p}$ in a good way. Also, the transfer matrix method does not include scattering, which is why the current remains essentially flat as the first resonant level is pulled below the conduction band edge on the emitter side. The dashed trace in Fig. 9(d) illustrates the increase in current experimentally observed, and the definition of the valley current density ($J_{\rm v}$) and the valley voltage ($V_{\rm v}$).

When designing high speed RTDs several factors needs to be considered and trade-offs have to be made. The most important parameters used to evaluate RTDs are listed below. These parameters are chosen based on their influence on the performance of high frequency oscillators incorporating RTDs, which will be further discussed in Chapter 5.

- The peak to valley current difference ($\Delta I = I_{\rm p} - I_{\rm v}$) and voltage difference ($\Delta V = V_{\rm v} - V_{\rm p}$) both need to be large in order to maximize the output power from the RTD. However, the output conductance $g_{\rm o} \approx \Delta I/\Delta V$ needs to be large enough to compensate for losses in the circuit.
- The output capacitance of the device, $C_{\rm ce}$, should be as small as possible to maximize the oscillation frequency.
- $V_{\rm p}$ should be as small as possible to limit the DC power consumption.

A large ΔI requires a large $J_{\rm p}$, which is obtained by decreasing the thickness of the DBH barriers to maximize the tunneling current, and by increasing the amount of electrons available for tunneling, i.e. increasing the doping on the emitter side. However, it is important to make sure that $J_{\rm v}$ is not severely deteriorated as a result of increased scattering due to nonuniformity in the epitaxial layers forming the DBH.

One important trade-off when considering the parameters listed above is that the RTD area ($A_{\rm RTD}$) should be large to provide high output power, but small to enable a high oscillation frequency. The capacitance per area unit ($C_{\rm ce}/A_{\rm RTD}$) is minimized by having a thick space charge region (SCR) layer on the collector side of the DBH, but this in turn increases $V_{\rm p}$, as there will be an additional voltage drop across the SCR. The $In_{0.2}Ga_{0.8}As$ notch included in the design of the DBH presented here acts to lower $V_{\rm p}$, as the notch lowers the first bound state of the DBH. Several more trade-offs and considerations needs to be taken into account when designing RTDs and a detailed discussion is found in [34].

2.2 Fabrication of the gated tunnel diode

As mentioned earlier, it is possible to gain additional circuit functionality from an RTD if a third terminal is integrated with the RTD. The gated tunnel diode (GTD) presented in this section is such a device. The device processing is illustrated in Fig. 10

Table 3: Epitaxial structure

Layer	Material	Thickness (Å)	Dopant level (cm^{-3})
Contact layer	$In_{0.5}Ga_{0.5}As$	300	$3{\cdot}10^{19}$
Contact layer	$In_xGa_{(1-x)}As^*$	300	$3{\cdot}10^{19}$
Emitter	GaAs	4000	$2{\cdot}10^{18}$
Tungsten gate			
Emitter	GaAs	100	$2{\cdot}10^{17}$
Emitter	GaAs	200	$5{\cdot}10^{17}$
Spacer	GaAs	50	$2{\cdot}10^{16}$
Barrier	$Al_{0.8}Ga_{0.2}As$	16	$2{\cdot}10^{16}$
Well	GaAs	9	$2{\cdot}10^{16}$
Notch	$In_{0.2}Ga_{0.8}As$	20	$2{\cdot}10^{16}$
Well	GaAs	9	$2{\cdot}10^{16}$
Barrier	$Al_{0.8}Ga_{0.2}As$	16	$2{\cdot}10^{16}$
Spacer	GaAs	50	$2{\cdot}10^{16}$
SCR	GaAs	1000	$2{\cdot}10^{17}$
Collector	GaAs	10000	$5{\cdot}10^{18}$
0	GaAs	Substrate	S.I.

$^*x = 0 \rightarrow 0.5$ linearly graded.

and the layers of which the GTD consists are shown in Table 3. The DBH is grown by molecular beam epitaxy (MBE). An electron beam lithography (EBL) defined W grating is then deposited on top of the MBE grown substrate by electron beam evaporation, Fig. 10(a) shows the sample after the lift-off process is completed. The tungsten grating will act as the gate of the device. The sample is then cleaned and the native oxide is removed in a HCl etch, before the sample is transferred to a metalorganic chemical vapor deposition (MOCVD) reactor. Figure 10(b) shows the sample after overgrowth. The overgrowth has been optimized to give a self aligned mesa on top of the tungsten grating [35]. The complete epitaxial structure is shown in Table 3, the $In_{0.5}Ga_{0.5}As$ layer is included to decrease the contact resistance of the device. The contacts, which are denoted as the emitter (on top of the self aligned mesa) and the collector contact, are defined by EBL and deposited by thermal evaporation, the fabricated structure is described by Fig. 10(c). The Ti/Pd/Au metal stack gives ohmic contacts with a specific contact resistivity of 50-80 $\Omega\mu m^2$, as deduced from the transmission line method.

To minimize the gate to collector capacitance most of the W frame is removed,

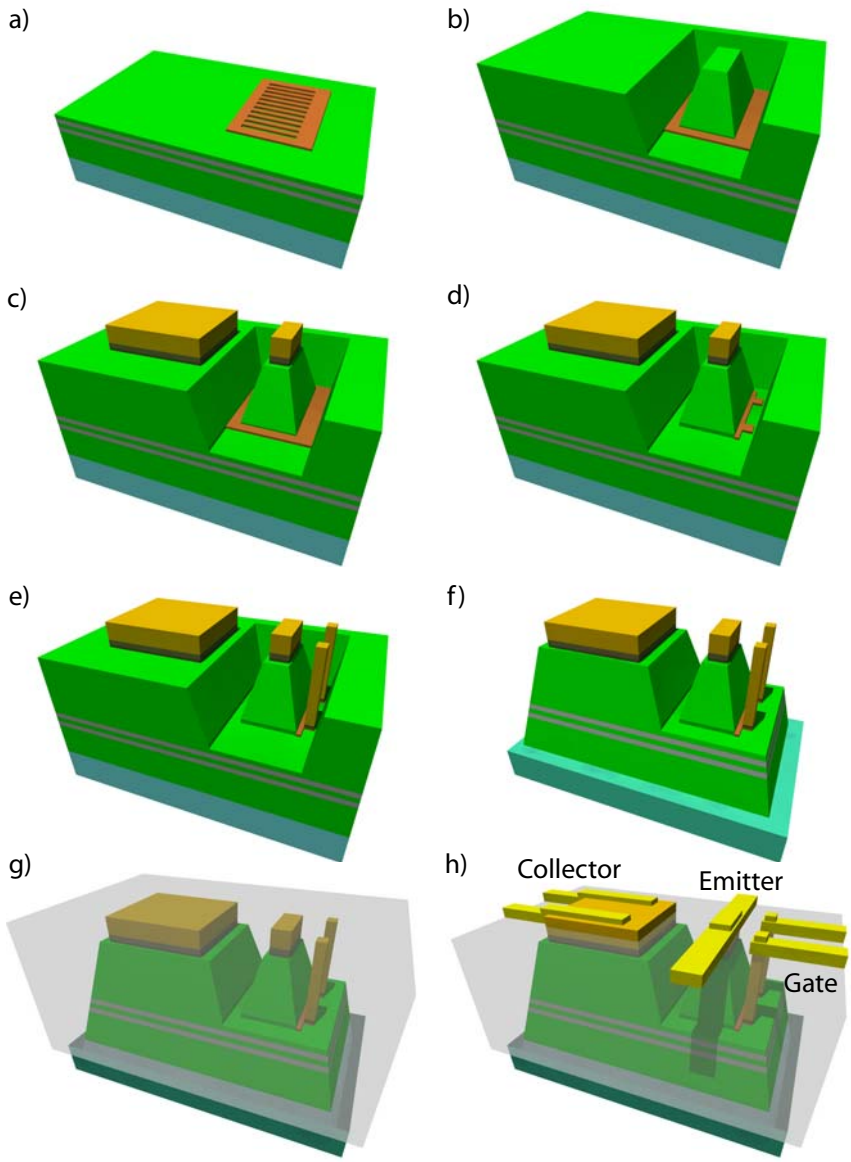

Figure 10: Illustration of the GTD during different steps of the fabrication process.

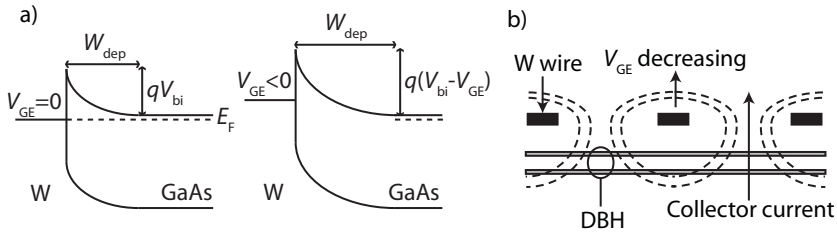

Figure 11: (a) Schematic band diagram and (b) cross section of the active region of the GTD. The dashed line illustrate the depletion of carriers associated with the W-GaAs Schottky contact and how it is influenced by the gate potential.

as illustrated in Fig. 10(d). This is done by defining a resist mask using EBL and removing the W by reactive ion etching in SF_6 chemistry. A slow (1.5 nm/s) wet-etch process is then used to remove the parts of the contact layer that is not covered by the ohmic contacts, which is done in order to avoid short circuiting between the gate and the ohmic contacts through the $In_xGa_{(1-x)}As$ layer. The wet etch also removes parts of the semiconductor material underneath the gate, this will further decrease the gate to collector parasitic capacitance. Gate pillars are then deposited by thermal evaporation, as shown in Fig. 10(e), and the device mesa is isolated by wet-etching, Fig. 10(f) shows the GTD resting on the semi-insulating substrate. The low-κ dielectric bisbenzocyclobutene (BCB) is used to passivate and to planarize the devices, as illustrated in Fig. 10(g), and the sample is then dry etched to reveal the top parts of the contacts. The completed device is shown in Fig. 10(h), where Au measurement pads have been integrated with the device terminals labeled collector, emitter, and gate. The here described fabrication process was used, with minor modifications, in Paper I-V.

The output current is passed from the collector to the emitter contact. The gate is connected to the W grating and it forms a Schottky contact with the GaAs as illustrated in Fig. 11(a). By controlling the potential on the gate it is possible to control the depletion width W_{dep} of the Schottky contact, which in one dimension is given by:

$$W_{\mathrm{dep}} = \sqrt{\frac{2\epsilon_s}{qN_{\mathrm{D}}}(V_{\mathrm{bi}} - V_{\mathrm{GE}})} \tag{8}$$

This modulates the active conducting area of the DBH, as illustrated in Fig. 11(b), and hence the output current.

2.3 Characterization of the gated tunnel diode

2.3.1 DC characterization

Figure 12(a) shows the measured DC output characteristics of a GTD and Fig. 12(b) depicts the gate leakage current (I_{G}). From Fig. 12(a) it is seen that it is possible to

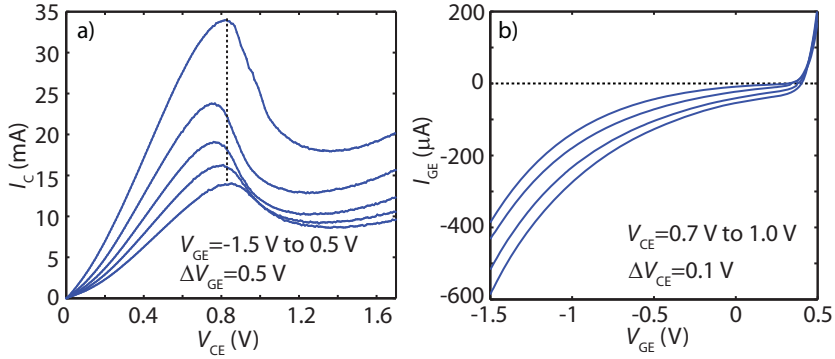

Figure 12: (a) Measured DC output characteristics of the GTD, (b) gate leakage. The device has 55 W fingers with a width of 80 nm, length of 2 μm and thickness of 20 nm. The spacing between the fingers is 250 nm and the total active device area is 36 μm^2.

switch the output conductance of the device from positive to negative values by controlling the gate voltage along the dotted line in Fig. 12(a). At low V_{GE} the V_{p} is shifted to higher V_{CE} due to the decreased potential in the DBH region. At high I_{C} the V_{p} increases as a consequence of the parasitic series resistance in the RTD. This phenomenon is exploited in the circuit implementations presented in Chapter 5.

The transconductance (g_{m}) is fairly low, as the device has not been optimized to give high gain. Instead the parameters listed in Section 2.1, which relates to how well the GTD performs in a high frequency oscillator circuit, have been considered. This also applies to the design of the Schottky contact gate leakage current in Fig. 12(b), which is fairly high due to the high doping concentration at the emitter side of the DBH. The high doping concentration ensures a high J_{p}, as discussed in Section 2.1.

2.3.2 RF characterization and equivalent circuit model

Figure 13 shows the current gain (h_{21}) and maximum unilateral power gain (U) as a function of frequency. The result is obtained from S-parameter measurements using standard open and short de-embedding of the measurement pad parasitics. The current gain cut-off frequency (f_{t}) and the maximum oscillation frequency (f_{max}) are 30 GHz and 11 GHz, respectively. This is sufficient for the device to be able to respond to Gbit/s data signals, which is the requirement when considering the circuit applications in Chapter 5.

To characterize the GTD in the NDC region requires a shunt resistor integrated close to the GTD to make sure that the total output conductance is positive. Without this resistor the GTD would oscillate with the bias network, as will be further described in Section 5.1.1, making S-parameter characterization impossible. By characterizing this resistor individually and subtracting its influence on the measurement,

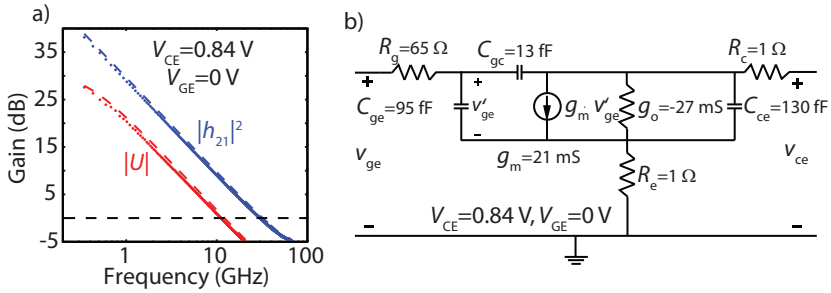

Figure 13: (a) Gain factors calculated from S-parameter measurements on a GTD with 55 W fingers, each with a width of 80 nm, length of 2 μm and thickness of 20 nm. The spacing between the wires is 250 nm and the total active device area is 36 μm. The dashed trace represents the result from the small signal equivalent model shown in (b).

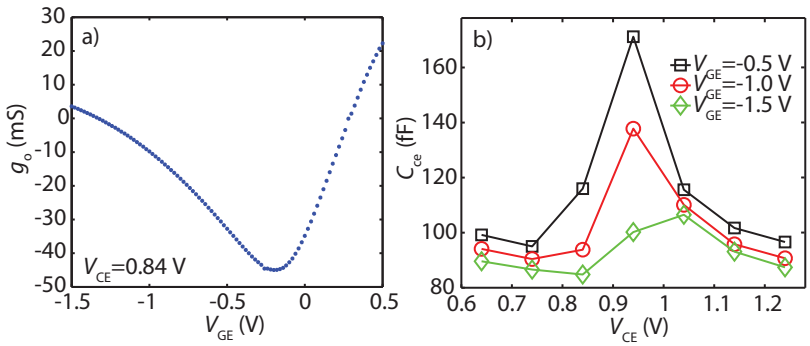

Figure 14: (a) Measured intrinsic output conductance as function of V_{GE} and (b) measured output capacitance as a function of V_{CE}.

it is possible to obtain the true GTD response [36]. This technique was also used for the DC measurements presented in Fig. 12. The S-parameter measurement is used to create an equivalent small signal model of the GTD to be used in circuit simulations and to improve the understanding of the device performance. The model in Fig. 13(b) was extracted according to the approach outlined in Section 3.4, it resembles that of a standard field-effect transistor with an output conductance (g_{o}), which may be negative. Figure 14(a) shows the extracted g_{o} as a function of V_{GE}, demonstrating that the device may be switched between positive differential conductance (PDC) and NDC by controlling the gate potential. The measured intrinsic output capacitance C_{ce} is shown as a function of V_{CE} in Fig. 14(b). Besides the geometrical depletion capacitance, C_{ce} also consists of a quantum capacitance originating from the charging and discharging of the quantum well [36], which is seen in Fig. 14(b) as an increase in C_{ce} when the

GTD is biased in the NDC region.

Other reports of gated tunnel diodes are found in reference [37, 38]. These devices have mainly been developed for digital applications, the main argument is increased circuit functionality per occupied area. However, they have been outperformed in terms of manufacturing cost and power consumption, by conventional CMOS logic. When considering high frequency wavelet generator circuits the GTD shows promising features, which will be analyzed in Chapter 5 where the circuit performance is evaluated based on the RTD parameters defined and analyzed in Section 2.1.

Chapter 3

The Regrown MOSFET

The previous chapter presented a device which combined an RTD with a Schottky field-effect gate to form a GTD. This device has many interesting properties, but also some limitations. These are mainly related to the choice of material for the DBH structure. In the case of the GTD, the design is limited to a material system that allows for the integration of a Schottky gate, which in the work presented here was GaAs. It is well known that the best performing DBHs are found in the InGaAs/AlAs [39] or in the InAs/AlSb material systems [40], much due to the decreased contact resistance as compared to GaAs. However, high In content materials do not form good Schottky barriers with metals and a GTD in this material system would have a to large leakage current at the input.

Chapter 4 considers a variable conductance component implemented as a series integration of an InGaAs RTD and an InGaAs metal-oxide-semiconductor field-effect-transistor (MOSFET). The primary purpose of the MOSFET is to operate as a variable resistance, hence it has been designed to have a low on-resistance R_{on}, i.e. a high on-current (I_{on}), and a high off-resistance, i.e. a low off-current (I_{off}). This chapter analyses the MOSFET from the perspective of its operation in conventional digital logic for very large scale integration (VLSI). The conclusions derived are then used when analyzing the RTD-MOSFET variable conductance component in Chapter 4.

3.1 MOSFETs for VLSI

One of the most high-tech products, in terms of the amount of money spent on research and development, commercially available today is the "Ivy Bridge" Intel computer processor. It consists of 1.4 billion transistors with a physical gate length (L_{g}) of $\approx$25 nm, equivalent to roughly 250 atoms. This transistor is designed according to the requirements stated in the international technology roadmap for semiconductors (ITRS) [41] at the 22 nm node. Looking back at the development of previous generations of transistors they have all faced tough challenges, however, innovation inspired by business (the total semiconductor market value was $300 billion in 2010) is a powerful force and semiconductor engineers have managed to deliver improved transistor performance according to Gordon Moore's observation of the doubling of the transistor count every 18-24 months. Examples of major innovations in the latest generations up to the 22 nm node are:

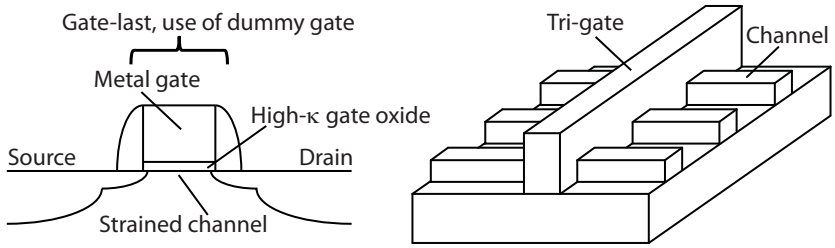

Figure 15: Illustration of major innovations in CMOS transistor fabrication from the 90 nm node generation up to the 22 nm node generation.

- Introduce strain to boost charge transport [42].
- Introduce high-κ gate dielectric for improved charge control [43].
- Replace polysilicon gate with metal gate to enable charge control [44].
- Introduction of gate-last processing to facilitate high-κ integration [44].
- 3-D architecture, Tri-gate devices for improved electrostatic control [45].

These innovations are illustrated in Fig. 15 and described in this section. The fundamental challenge is to be able to increase the performance of the transistor while minimizing the power consumption, both in the on-state and off-state. The remainder of this section lists how the above innovations has contributed to solve these challenges, the discussion is based on two key transistor metrics, the on-current ($I_{\rm on}$) and the subthreshold swing (SS), Figure 16(a) illustrates the impact of these two parameters on the transfer characteristic. The transistor is used as a logic gate having two states "1" and "0", which are controlled by the gate-source voltage $V_{\rm GS}$ and distinguished by the threshold voltage ($V_{\rm th}$). The aim is to get the transistor to work as an ideal switch, which only consumes power in the on-state. The subthreshold swing is a measure of the ability to switch the transistor off, a smaller SS means less current consumption in the off-state. A high $I_{\rm on}$ is desired as this current will be used to drive the input of subsequent gates, as will be considered next.

Increase the current

The transistor switching performance is illustrated by the one stage inverter delay:

$$\tau = \frac{C_{\rm output} V_{\rm dd}}{I_{\rm on}}. \tag{9}$$

Here, $C_{\rm output}$ consists of both the intrinsic and parasitic capacitances at the output of the inverter in Fig. 16(b). The parasitic capacitances originating from interconnects ($C_{\rm wire}$) and fringing fields from gate sidewalls might not scale well with $L_{\rm g}$

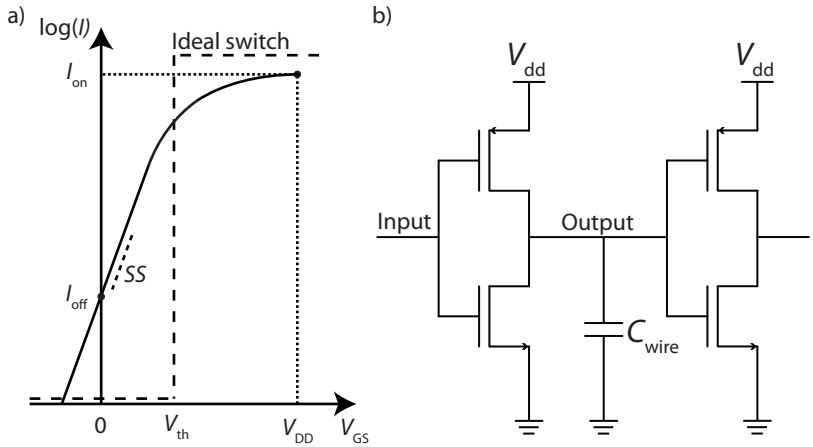

Figure 16: (a) Illustration of the transfer characteristics of a MOSFET switch. (b) CMOS inverter.

and inverter performance is primarily increased by decreasing the supply voltage $V_{\rm dd}$ and increasing the on-state current [46], which is equivalent to increasing the transconductance ($g_{\rm m} = {\rm d}I_{\rm D}/{\rm d}V_{\rm GS} \approx I_{\rm on}/V_{\rm dd}$) [47]. Technology generations up to the 250 nm node have been scaled according to the constant field approach [48], which implies a decrease in $V_{\rm dd}$ by $1/\alpha$ as L_g is scaled by $1/\alpha$. This has not been possible in later generations as this would have manifested itself as a too low drive current, hence a generalized scaling theory has been introduced [48], which is closer to the constant voltage scaling where $V_{\rm dd}$ has been kept constant at 1 V as $L_{\rm g}$ is scaled by $1/\alpha$. The reason for the deviation is mainly related to the gate oxide tunneling leakage current, which depends on the thickness of the gate oxide ($t_{\rm ox}$). Inability to scale $t_{\rm ox}$ by $1/\alpha$, hence the gate oxide capacitance $C_{\rm ox} \propto 1/t_{\rm ox}$, manifests itself as less induced charge in the channel $q{\cdot}N_{\rm s} \propto C_{\rm ox}(V_{\rm dd} - V_{\rm th})$, which will cause the on-state current density, given by

$$I_{\rm on}/W_{\rm g} = qN_{\rm s}{\cdot}v_{\rm s},\ v_{\rm s} = \mu{\cdot}E, \tag{10}$$

to decrease, wheras it should be constant according to constant field scaling. Here, $W_{\rm g}$ is the width of the transistor, $N_{\rm s}$ is the induced carrier concentration, $v_{\rm s}$ is the velocity near the source edge, and E is the horizontal electric field along the channel. The introduction of strain in the channel to increase the mobility (μ) and hence $I_{\rm on}$, and the introduction of high-κ gate oxide to increase the gate coupling without scaling $t_{\rm ox}$, has made it possible to stay on the ITRS track [45]. As the standard polysilicon gate experience problems with Fermi level pinning when integrated with high-κ dielectric, it has been replaced by a metal gate and an added benefit of this is the increased flexibility when designing the work function of the gate to obtain the required $V_{\rm th}$ [44]. The introduction of the high-κ/metal-gate stack also inspired the development of the

gate-last process, in which the gate dielectric is deposited after the high temperature dopant activation anneals [44]. This increases the stability of the high-κ-metal gate stack and also provides the possibility of choosing the gate metal from a wider range of materials.

Recently Intel has announced that their Ivy Bridge 22 nm node process, which is in production, includes a 3-D architecture known as a Tri-gate [45]. The Tri-gate controls the channel from 3 sides, as illustrated in Fig. 15. This boosts $I_{\rm on}$ by increasing $C_{\rm ox}$ and hence $qN_{\rm s}$ at a given $L_{\rm g}$.

To further improve the drive current of high performance digital circuits the industry is considering replacing Si as the channel material, especially InGaAs is considered a good candidate due to the superior mobility and high source injection velocity ($v_{\rm inj}$) as compared to Si [49]. These properties are correlated with a small effective mass which limits the density of states and hence the current, however, when considering thin channel FETs this effect might not be severe and significantly improved on-state performance is still expected from III-V materials, especially for low supply voltage applications [49]. These materials are likely to be introduced as the $L_{\rm g}$ approaches 10 nm and at these short gate lengths the injection velocity becomes an important parameter as the current is no longer governed by the long channel mobility (10) but rather the saturated velocity ($v_{\rm sat}$)

$$I_{\rm on}/W_{\rm g} = qN_{\rm s}{\cdot}v_{\rm sat} \tag{11}$$

or ballistic transport

$$I_{\rm on}/W_{\rm g} = qN_{\rm s}{\cdot}v_{\rm inj}. \tag{12}$$

Another factor limiting the drive current is the resistance between the source/drain contact and the channel ($R_{\rm access}$). As $L_{\rm g}$ is scaled closer to the ballistic limit $R_{\rm access}$ will become a larger fraction of the total on-resistance ($R_{\rm on}$), which decreases the energy efficiency and degrades the drive current and the transconductance.

Minimize the subthreshold swing

The off-state current is limited by thermionic emission of charges from the source into the channel. The potential barrier limiting the current is controlled by $V_{\rm GS}$ and the current in the subthreshold regime is proportional to $\exp(q(V_{\rm GS}-V_{\rm th})/(k_{\rm b}T_{\rm L}))$, the room temperature limit of the switching of current in the subthreshold regime is 60 mV/dec. To realize this ideal operation requires a good electrostatic coupling between the gate and the channel, which is not possible if the MOS interface suffers from a high density of interface trap states ($D_{\rm it}$), which screens the vertical field. By keeping a thin interfacial layer of SiO_2 between the Si channel and the high-κ gate dielectric it has been possible to keep $D_{\rm it}$ at an acceptable level.

It is also imperative that the device does not suffer from short channel effects, i.e. drain induced leakage currents. To ensure that the device electrostatics is controlled by the gate potential and not the drain potential it is essential that the channel is kept thin. The restriction on the channel thickness may be relaxed if the channel is controlled

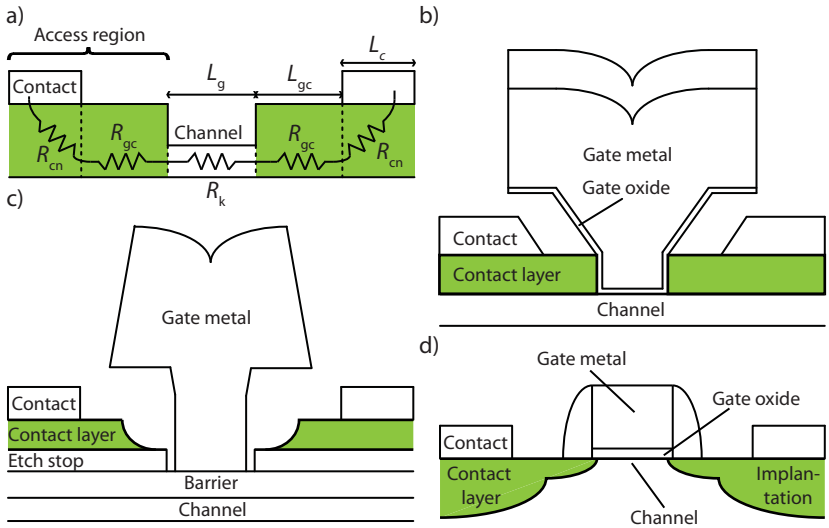

Figure 17: (a) Resistive contributions to the on-resistance of a FET. (b) Shows a schematic cross-section of the MOFET described in this thesis and (c) and (d) shows a standard HEMT and Si MOSFET, respectively.

from more than one side. The Tri-gate transistor is such a device and it has demonstrated improved subthreshold characteristics for both Si and III-V channels [50, 51]. A step further is to use a gate all around (GAA) design to gain ultimate electrostatic control of the channel [52].

The future introduction of III-V materials will make it possible to use quantum confinement in the channel by heterostructure engineering. This is a simple way of thinning the channel to ensure good 2-D electrostatics. On the down side, III-V materials have a slightly higher permittivity which makes them more susceptible to short channel effects and the lower band gap also gives a larger lower bound on the minimum I_{off} [53].

3.2 III-V MOSFET device architecture

To further increase I_{on} and decrease SS requires new innovations that goes beyond what is currently regarded as "business as usual", III-V channel material is one such example. High electron mobility transistors (HEMTs) has for a long time demonstrated the superiority of the III-V channel materials as compared to Si [54, 55]. One of the reasons that HEMTs have not found their way into VLSI applications is that the scaling of these devices to short gate lengths implies a reduction of the thickness of the Schottky gate barrier layer, which at short gate lengths results in a large gate leakage current [49]. There is currently a big effort at both universities and in industry

across the globe to find a suitable high-κ dielectric that limits the gate leakage current and gives good control of the charges in III-V channels.

A second big challenge is to integrate this high quality gate dielectric while maintaining a low on-resistance device architecture. Figure 17(a) illustrates the different resistive contributions to the on-resistance

$$R_{\rm on} = R_{\rm access} + R_{\rm k},\ R_{\rm access} = 2{\cdot}R_{\rm cn} + 2{\cdot}R_{\rm gc}, \tag{13}$$

of a FET, where $R_{\rm cn}$ is the contact resistance, $R_{\rm gc}$ is the gate-to-contact resistance, and $R_{\rm k}$ is the channel resistance. The lateral dimensions associated with these resistive contributions are the contact length $L_{\rm c}$, and the gate to contact spacing $L_{\rm gc}$.

Scaling scenarios target a $R_{\rm access}$ of 145-228 $\Omega\mu$m at the 15 nm node with $2{\cdot}L_{\rm c}$= 20 nm [41,56]. This challenge is one of the main motivations behind the design of the regrown MOSFET reported in this thesis, which is shown in Fig. 17(b) together with a schematic layout of a standard HEMT in Fig. 17(c), and a standard Si MOSFET in Fig. 17(d), for comparison. The following considerations, labeled A to E, were taking into account when developing the regrown MOSFET fabrication process.

A. Avoid heterostructure barriers in the path of the current $\Rightarrow$ Epitaxial regrowth of source and drain access regions

HEMT devices rely on a heterostructure barrier Schottky gates, these devices are fabricated by performing a gate recess etch which is selective to the barrier on top of which the gate contact is formed. This means that the heterostructure barrier will also be present in the source and drain access regions, as shown in Fig. 17(c), which may be avoided by epitaxially regrowing the source and drain access regions. Metal-organic chemical vapor deposition is the preferred choice for selective area regrowth due to the possibility of growing under high ambient pressure, which gives a long diffusion length of the precursor molecules and hence high uniformity growth.

B. Minimize the gate-to-contact resistance $\Rightarrow$ Self-aligned device

When scaling transistors to short gate lengths it is important that the parasitic resistance originating from $L_{\rm gc}$, is kept small. The $L_{\rm gc}$ is targeted to be 15 nm at the 15 nm node [41, 56]. This implies that the highly conductive access regions must be self-aligned to the gate in order to have a reliable fabrication process. This is hard to realize for short gate length devices relying on recess etch to form the gate. Si based devices traditionally use ion implantation to form the self-aligned access regions, as illustrated in Fig. 17(d). This approach would be a desirable choice for III-V MOSFETs, as many of the well established fabrication processes in the Si industry could be reused for the III-V channels. However, studies has shown that it might be a tough challenge to implant high quality, shallow, abrupt, and highly doped junctions in III-V materials and this is especially true for the low thermal budget processing required for $\rm In_{\it x}Ga_{1-\it x}As$ compounds [57, 58].

C. The device should be scalable to short gate lengths $\Rightarrow$ Surface channel device

The excellent performance of HEMTs are mainly attributed to the high quality interface between the channel and the Schottky barrier. This knowledge has inspired the development of MOSHEMTs [59], where the gate oxide is separated from the channel by a heterostructure barrier to give improved transport properties. The equivalent oxide thickness (EOT) is given by the barrier and the gate dielectric, which requires that these layers are kept very thin [43]. It might be a challenging task to manufacture these devices in a controlled way at very short $L_{\rm g}$. It would be desirable to have the gate oxide directly on the channel to improve the gate to channel coupling. This has been the traditional CMOS approach facilitated by the high quality Si-SiO_2 interface, and lately the Si-SiO_2-high-κ interface. To find a high quality MOS gate stack is the main challenge for the In compound transistors.

D. High quality MOS interface $\Rightarrow$ Gate-last process

As mentioned earlier, Si based MOSFETs rely on ion implantation processes, which are followed by high temperature annealing to activate the dopants and to form the intended doping profile. High temperature annealing is also used to improve ohmic contacts. A fabrication scheme where no high-temperature annealing is used after the formation of the gate is referred to as a gate-last process and the benefit of such a processes is that the temperature budget for the MOS interface can be designed independently of the temperature during the formation of the contacts and the access regions. Moderate annealing has shown to improve the quality of the MOS interface [60].

E. The device should be high frequency compatible $\Rightarrow$ Trade off between $R_{\rm access}$ and parasitic gate capacitance ($C_{\rm gp}$)

Transistors for VLSI applications are mainly evaluated based on the highest $I_{\rm on}$ for a fixed off-current. Less attention is paid to parasitic capacitance contribution, as discussed in Section 3.1. The trade-off between $R_{\rm access}$ and $C_{\rm gp}$ is more important for analog applications, where the transistor is used to deliver gain at high frequencies. This is illustrated by the expression for the current gain cut-off frequency of a standard FET

$$\frac{1}{2\pi f_{\rm t}} = \frac{C_{\rm gs}+C_{\rm gd}}{g_{\rm m}}(1+(R{\rm s}+R_{\rm d})g_{\rm ds})+(R_{\rm s}+R_{\rm d})C_{\rm gd}, \qquad (14)$$

which includes the source and drain resistances, $R_{\rm s}$ and $R_{\rm d}$, and the gate-drain and gate-source capacitances, $C_{\rm gd}$ and $C_{\rm gs}$. This is further discussed in the following section together with a description of the key features of the fabrication process and how they affect this trade-off.

3.2.1 The regrown InGaAs MOSFET, design and fabrication

A thorough description of the fabrication of the regrown MOSFET is found in Papers VI and VII, this section addresses fabrication considerations related to the design trade-off between low $R_{\rm access}$ and low $C_{\rm gp}$. Figure 18 shows a schematic cross-section of the regrown MOSFET, indicating key design parameters. Here $L_{\rm c}$ is the contact

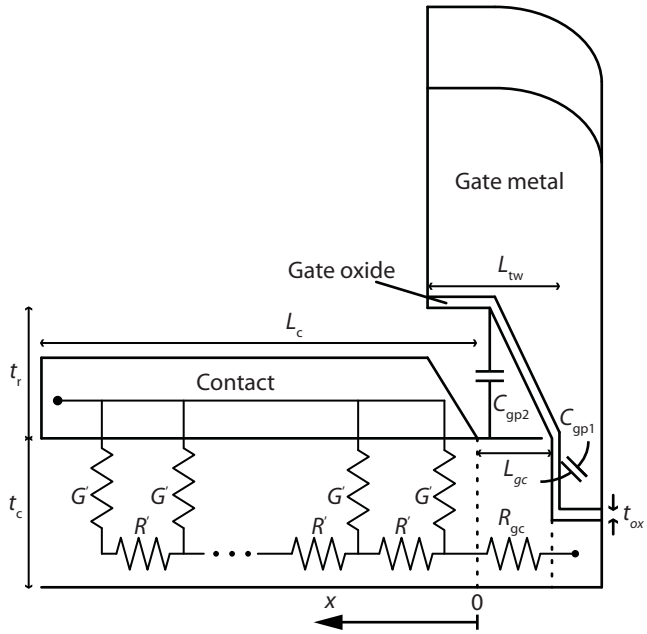

Figure 18: Schematic cross-section of the regrown MOSFET indicating the key dimensions related to the resistive and capacitive parasitic of the device.

length, $L_{\rm gc}$ is the gate to contact spacing, $L_{\rm tw}$ is the T-gate overhang, $t_{\rm r}$ is the stem height of the T-gate, and $t_{\rm c}$ is the thickness of the access region semiconductor material.

The presented device topology possesses the numerous benefits discussed in the previous section, all of which minimizes $R_{\rm access}$. One of the key properties is the absence of heterostructure barriers in the access regions. Hence, it is possible to model $R_{\rm access}$ using a simple one layer distributed transmission line model, as presented in Fig. 18, contrary to the more complex models used for heterostructure FETs [61]. Here G' is the distributed contact to contact layer conductance per unit length, and R' is the distributed contact layer resistance per unit length. The differential equation

$$\frac{d^2V(x)}{dx^2} - R'G'V(x) = 0,\ V(0) = V_0,\ \frac{-1}{R}\frac{dV(x)}{dx} = I_0 \tag{15}$$

governs the voltage drop $V(x)$ at a distance x underneath the contact, assuming that the resistance in the metal is negligible. The solution to (15) is,

$$R_{\rm cn} = \frac{V_0}{I_0} = \frac{R_{\rm sh}L_{\rm t}}{W_{\rm g}}\coth\left(\frac{L_{\rm c}}{L_{\rm t}}\right),\ L_{\rm t} = \sqrt{\frac{\rho_{\rm c}}{R_{\rm sh}}}, \tag{16}$$

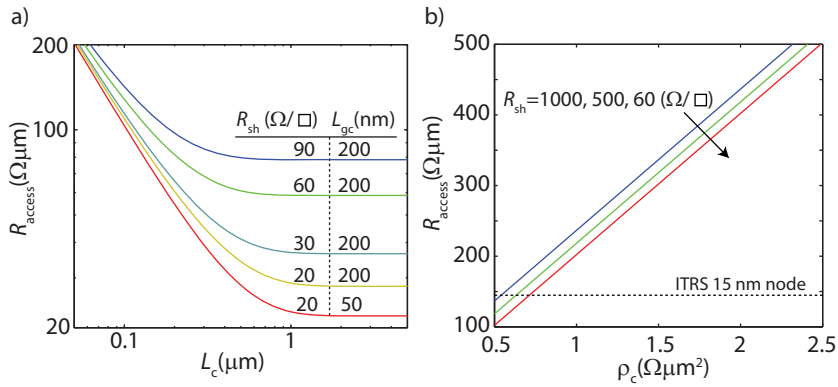

Figure 19: (a) R_{access} as a function of L_{c} for different L_{gc} and R_{sh}. (b) R_{access} as a function of ρ_{c}, L_{gc}=15 nm and L_{c}=10 nm.

Table 4: The influence on R_{access}, C_{gp1}, and C_{gp2}, by increasing the listed design parameters.

	t_{c}	t_{r}	t_{ox}	L_{c}	L_{gc}	L_{tw}
R_{access}	↓	0	↑	↓	↑	↑
C_{gp1}	↑	0	↓	0	0	0
C_{gp2}	0	↓	0	↑	↓	↑

where R_{sh} is the semiconductor sheet resistance, ρ_{c} is the specific contact resistivity, L_{t} is the transfer length, which is defined as the point where the current has decreased by a factor e, and W_{g} is the width of the contact. The total R_{access} is

$$R_{\mathrm{access}} = 2 \cdot (R_{\mathrm{cn}} + R_{\mathrm{gc}}) = 2 \cdot \frac{R_{\mathrm{sh}} L_{\mathrm{t}}}{W_{\mathrm{g}}} \coth\left(\frac{L_{\mathrm{c}}}{L_{\mathrm{t}}}\right) + 2 \cdot R_{\mathrm{sh}} \cdot L_{\mathrm{gc}}. \qquad (17)$$

Figure 19(a) shows R_{access} as a function of L_{c} for different L_{gc} and R_{sh}. At long L_{c} both R_{sh} and L_{gc} have a great influence on R_{access}, but as L_{c} is scaled below L_{t}, ρ_{c} becomes the single dominant factor. This is further analyzed in Fig. 19(b), which shows R_{access} as a function of ρ_{c} for different R_{sh}, given L_{c}=10 nm and L_{gc}=15 nm as targeted at the 15 nm node [41]. When considering devices this compact, R_{sh} has only a small influence on R_{access} and ρ_{c} is recognized as the single most important parameter to minimize R_{access}. A ρ_c below 0.7 $\Omega\mu\mathrm{m}^2$ is required to fulfill the target at the 15 nm node. Contacts to InAs, which fulfill this requirement, have been reported in [62] for an active doping concentration of $8.2{\cdot}10^{19}$ cm^{-3}.

As shown in Fig. 19(a), the access resistance is minimized by increasing t_{c} (decreasing R_{sh}) and decreasing L_{gc}. This is in contrast to the parasitic capacitance

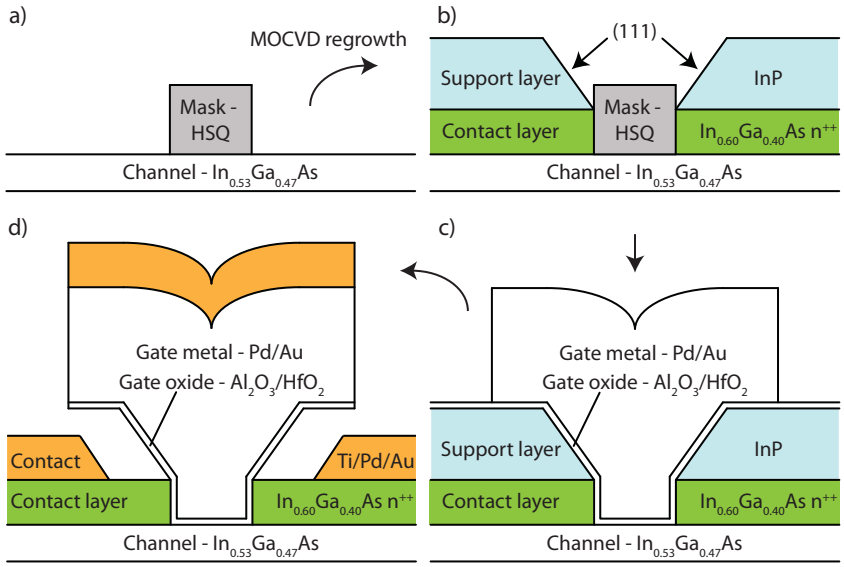

Figure 20: Illustration of the fabrication of the regrown MOSFET, (a) formation of HSQ dummy gate, (b) after regrowth, (c) after deposition of gate metal, and (d) completed device.

which is increased by increasing t_{c} and decreasing L_{gc}. The parasitic capacitance may be separated into the semiconductor to gate capacitance (C_{gp1}) and the gate to contact/contact layer fringing capacitance (C_{gp2}), as illustrated in Fig. 18. To minimize C_{gp1} implies decreasing the contact layer to gate overlap, which can be done without deteriorating R_{access} if the contact layer is buried fully or partly below the gate. Another option is to remove and replace the high-κ spacer. To ensure that C_{gp2} is kept small t_{r} should be large and L_{tw} small, as these parameters have no impact on R_{access}. To further decrease C_{gp2} requires that L_{gc} is kept large to separate the gate from the contact. Table 4 summarizes the influence of the design parameters on R_{access} and C_{gp}.

The regrown MOSFET fabrication scheme is described here to illustrate the possibilities and constraints of the design parameters listed in Table 4. Figure 20 summarizes the fabrication process, where the first step is to define a hydrogen silsesquioxane (HSQ) dummy gate on top of the channel, as shown in Fig. 20(a). The HSQ dummy gate will be used as a hard mask when selectively regrowing the source and drain access region. The gate length is defined by the width of the HSQ dummy gate and this process is scalable to HSQ line widths below 10 nm [63]. Figure 20(b) shows the samples after MOCVD regrowth of the contact layer and the support layer, the thickness t_{c}, defined in Fig. 18, is determined by the growth time of the contact layer. By orientating the HSQ lines in different crystal directions on the surface of the channel

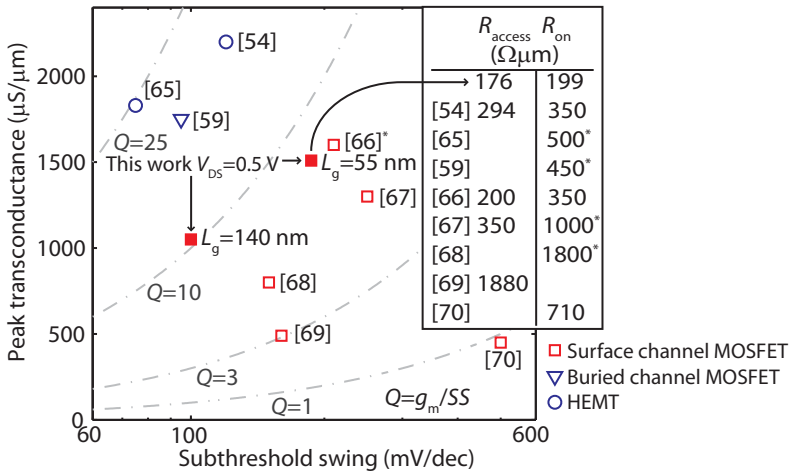

Figure 21: Benchmarking of state of the art InGaAs FETs. *Extracted from graphical representation of data.

it is possible to control the development of the facet adjacent to the dummy gate. If the HSQ lines are parallel to the (001) direction, the vertical facet will be (111), under certain growth conditions, where the V/III ratio plays an important role [64]. The selective growth also gives the opportunity to grow the support layer thicker than the height of the HSQ dummy gate, which increase the gate stem height t_{r}.

The HSQ dummy gate is then removed and the samples are transferred to an atomic layer deposition system, where the gate oxide of thickness t_{ox} is formed. The properties of the gate oxide also determines C_{gp1}. Gate metal is then deposited and L_{tw} is defined by lithography, as shown in Fig. 20(c), and increasing L_{tw} will decrease the gate resistance R_{g} but increase C_{gp2}. For VLSI applications L_{tw} should be small enough to comply with the required gate to contact length L_{gc}, which at the 15 nm node is 15 nm [56]. The gate oxide and the support layer is then removed by wet etching. The L_{gc} is determined by L_{tw} and the tilt of the sample when evaporating the source and drain contacts and L_{c} is defined by lithography. Figure 20(d) shows the completed device.

The described fabrication steps provide the opportunity to control the dimensions indicated in Fig. 18, which gives the flexibility to design a device that is optimized either for analog or digital applications. Analog devices are typically wide and require a T-gate to minimize the gate resistance to increase the high frequency gain. Digital devices are rather designed to occupy as small area as possible, and to minimize R_{access}, whereas the trade-off between C_{gp} and R_{access} is an important parameter for high frequency analog devices.

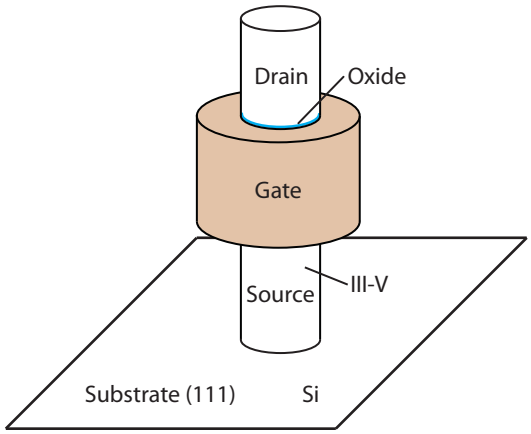

Figure 22: Illustration of a vertical nanowire MOSFET.

3.2.2 III-V FET benchmarking

The performance of the regrown MOSFET is reported in Paper VI and Paper VII, Fig. 21 presents a comparison with state of the art InGaAs FETs [54, 59, 65–70]. The result is that the regrown MOSFET shows the lowest reported $R_{\rm on}$ and $R_{\rm access}$, which is attributed to the epitaxial regrowth of the source and drain access regions.

The regrown MOSFET also shows the highest Q=$g_{\rm m}/SS$ for surface channel devices in part due to the use of a gate-last process. The HEMT and buried channel devices demonstrate the potential of the III-V technology and the importance of having a good quality gate interface to the channel.

3.3 Nanowire MOSFET

Papers IX and X presents vertical nanowire (NW) MOSFETs which combines III-V channel material with a GAA architecture, as depicted in Fig. 22, which is a schematic illustration of the basic device configuration where the current is flowing perpendicular to the surface of the substrate. The nanowires are epitaxially grown from a seed particle, which allows for integration of high quality InAs MOSFETs on a Si substrate, as reported in Paper X. The vertical geometry also has other interesting features such as the possibility for vertical stacking of transistors, control of $L_{\rm g}$ by the thickness of the deposited gate metal, and radial and axial epitaxial channel engineering to improve transistor performance [71]. The processing required to fabricate NW MOSFETs has a number of challenges such as accurate positioning of the gate to the channel, and trade-off between access resistance in the thin wire and parasitics due to overlapping gate-source and gate-drain electrodes [72].

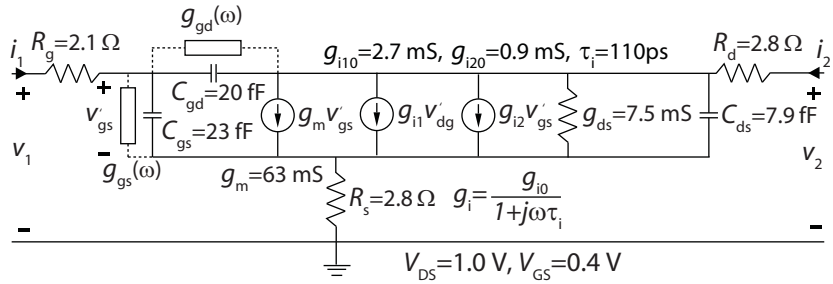

Figure 23: Small signal model of the regrown MOSFET with L_g=55 nm and W_g=21.6 μm. The value of the circuit elements are deduced from S-parameter measurements.

3.4 Small-signal modeling

The devices presented in the papers included in this thesis were evaluated by scattering (S)-parameter measurements using a vector network analyzer (VNA). The measurements are done by imposing a voltage wave on the device under test and measuring the ratio between transmitted, or reflected, and incident voltage. This is done at an interface with known impedance, which is usually 50 Ω. The measured S-parameters can then be converted into different sets of parameters to facilitate the analysis of the data, admittance (Y)-parameters are commonly used for field-effect transistors. Based on these measurements it is possible to create small-signal models that may be used when designing circuits by computer aided software simulations. Such models could be a "black box" representation of the device, relating input to output, but if the model is based on the physics of the device it may also be used to investigate factors that limit the device performance and the implications that these limitations have on the circuits they are integrated into. An example of such a physics based model is shown in Fig. 23, representing the regrown MOSFET reported in Papers VI and VII, the model accounts for impact ionization, band-to-band tunneling and the wideband response of gate oxide border traps. These phenomena are further described and analyzed in Section 3.4.1 and Section 3.4.2.

The MOSFET model was extracted using the following approach:

1. Suggest a physics based model for the device.
2. Derive analytical expressions for the intrinsic Y-parameters of the suggested model.
3. Estimate the parasitic source and drain resistances (R_s and R_d) from DC measurements and subtract them from the measured S-parameters.
4. Compare the measured Y-parameters with the analytical expressions and isolate the device elements one by one.

5. Minimize the relative error

$$\epsilon = 100 \cdot \frac{1}{4} \sum_{ij} \left(\sum_{freq} \frac{\left| Y_{ij}^{\mathrm{mod}} - Y_{ij}^{\mathrm{meas}} \right|^2}{\left| Y_{ij}^{\mathrm{meas}} \right|^2} \right) \frac{1}{N_{freq}} \tag{18}$$

between the measured and modeled data by using R_{s} and R_{d} as parameters for the optimization.

The derived Y-parameters of the model in Fig. 23 are:

$$Y_{11} = \frac{i_1}{v_1}|_{v_2=0} = g_{\mathrm{gd}}(\omega) + g_{\mathrm{gs}}(\omega) + R_{\mathrm{g}}\omega^2(C_{\mathrm{gs}} + C_{\mathrm{gd}})^2 + j\omega(C_{\mathrm{gs}} + C_{\mathrm{gd}}) \tag{19}$$

$$Y_{12} = \frac{i_1}{v_2}|_{v_1=0} = -g_{\mathrm{gd}}(\omega) - R_{\mathrm{g}}\omega^2 C_{\mathrm{gd}}(C_{\mathrm{gd}} + C_{\mathrm{gs}}) - j\omega C_{\mathrm{gd}} \tag{20}$$

$$\begin{aligned} Y_{21} = \frac{i_2}{v_1}|_{v_2=0} &= g_{\mathrm{m}} - g_{\mathrm{i1}} + g_{\mathrm{i2}} - \omega^2 C_{\mathrm{gd}} R_{\mathrm{g}}(C_{\mathrm{gs}} + C_{\mathrm{gd}}) \\ &- j\omega R_{\mathrm{g}}(g_{\mathrm{m}} - g_{\mathrm{i1}} - g_{\mathrm{i2}})(C_{\mathrm{gs}} + C_{\mathrm{gd}}) - j\omega C_{\mathrm{gd}} \end{aligned} \tag{21}$$

$$\begin{aligned} Y_{22} = \frac{i_2}{v_2}|_{v_1=0} &= g_{\mathrm{ds}} + g_{\mathrm{i1}} + R_{\mathrm{g}}\omega^2 C_{\mathrm{gd}}^2 \\ &+ \omega^2 R_{\mathrm{g}}^2 C_{\mathrm{gd}}(C_{\mathrm{gs}} + C_{\mathrm{gd}})(g_{\mathrm{m}} - g_{\mathrm{i1}} - g_{\mathrm{i2}}) + j\omega(C_{\mathrm{ds}} + C_{\mathrm{gd}}) \\ &+ j\omega R_{\mathrm{g}} C_{\mathrm{gd}}(g_{\mathrm{m}} - g_{\mathrm{i1}} - g_{\mathrm{i2}}) - j\omega^3 R_{\mathrm{g}}^2(C_{\mathrm{gs}} + C_{\mathrm{gd}})C_{\mathrm{gd}}^2 \end{aligned} \tag{22}$$

The expressions in (19-22) have been simplified under the condition

$$\omega^2(C_{\mathrm{gs}} + C_{\mathrm{gd}})^2 R_{\mathrm{g}}^2 << 1, \tag{23}$$

which is valid for the model in Fig. 23 in the 10 MHz to 30 GHz frequency range considered here. To further simplify the expressions the effect of oxide border traps have only been included in the derived Y-parameters where it most significantly affects the device response, this is further discussed in Section 3.4.2.

The gate source capacitance is obtained from

$$C_{\mathrm{gs}} = \frac{\Im(Y_{11}) + \Im(Y_{12})}{\omega} \tag{24}$$

and the remaining parameters in Fig. 23 are deduced accordingly. This approach is similar to the one presented in [73].

Figure 24(a) and (b) shows the measured and extracted Y-parameters and S-parameters, corresponding to the small signal model in Fig. 23. The absolute square of the relative error averaged over all measured frequencies is less than 0.1% as calculated from (18).

A similar approach as the one described here was used in modeling of the nanowire MOSFET in Papers IX and X, the GTD model in Paper IV, and the GTD model in Section 2.3.2.

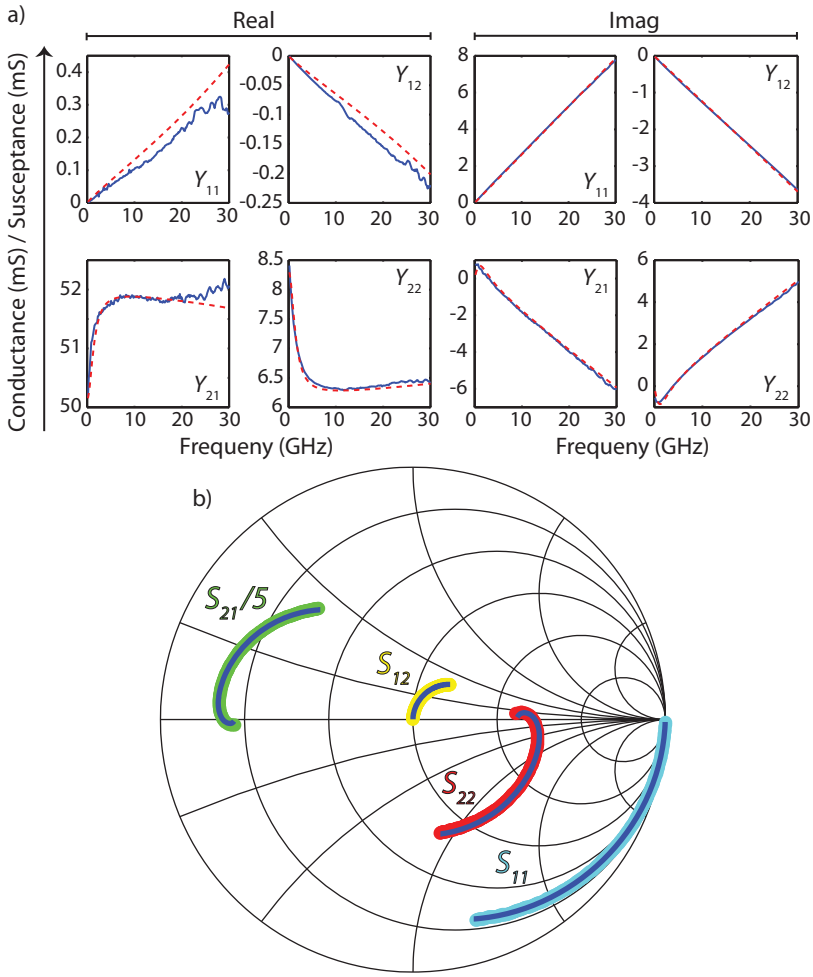

Figure 24: (a) Measured Y-parameters of the regrown MOSFET, the dashed trace corresponds to the model in Fig. 23. (b) Measured S-parameters, the solid blue trace corresponds to the model in Fig. 23.

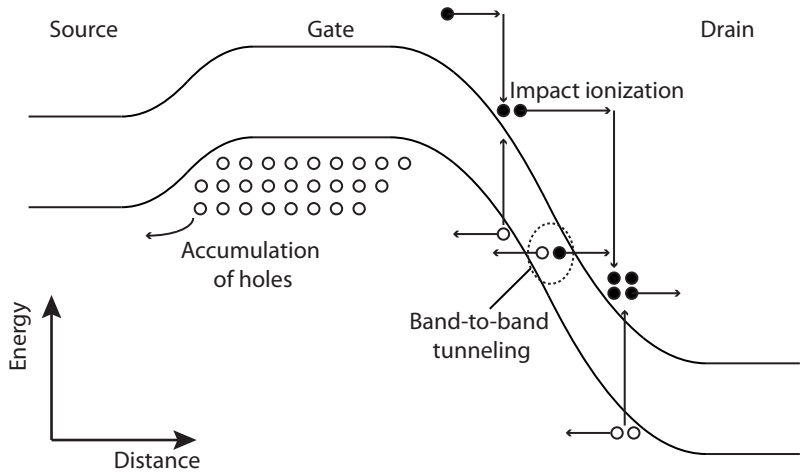

Figure 25: Schematic band diagram illustrating impact ionization, band to band tunneling, and the accumulation of holes in the gate-source region.

3.4.1 Modeling of impact ionization and band to band tunneling

The S-parameters S_{21} and S_{22}, shown in Fig. 24(b), experience a change of phase at low frequencies. This phenomenon is also observed in Paper VI-X and is attributed to two effects that are present at the output of FETs at high gate-drain electric fields, namely electron impact ionization (EII) and band-to-band tunneling (BTBT).

EII is the process in which an electron is accelerated by the electric field in the gate-drain region. If the electron gains enough kinetic energy it may, upon impact with an atom, transfer this energy to another electron, which is then lifted to the conduction band, as illustrated in Fig. 25. This electron may in turn be accelerated by the electric field and transfer its energy to a new electron. EII is observed already at low drain-gate potentials (V_{DG}) in small band gap semiconductors as the required energy to ionize an electron is related to the magnitude of the band gap. The EII current also depends on the initial amount of electrons entering the gate-drain region.

BTBT is the process in which an electron tunnels from the valence band into the conduction band, in the gate-drain region. At high enough V_{DG} the bands bend and present a tunneling path, as illustrated in Fig. 25. The tunneling distance is decreased as V_{DG} is increased and the tunneling barrier height is dependent on the band gap.

The holes generated by these processes drift towards the source region where they accumulate before they recombine with an electron, or are injected into the source, as illustrated in Fig. 25. The positive charge in the gate-source region gives a feedback effect, which increases the drain current. Hence, the small signal model describing these phenomenons needs to include two elements, one that is related to the electric field at the output and one that is dependent on the gate-source potential. The model in

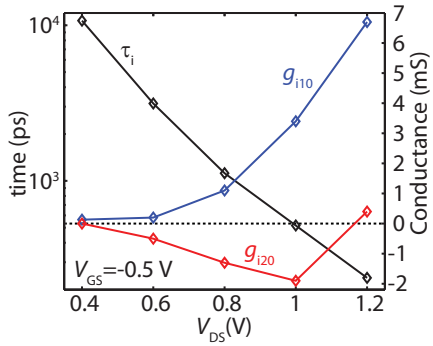

Figure 26: (a) Extracted parameters of (25) and (26) as a function of $V_{\rm DS}$ for a regrown MOSFET with $L_{\rm g}$=55 nm and $W_{\rm g}$=21.6 μm.

Fig. 23 implements EII and BTBT as two voltage dependent current sources controlled by $v_{\rm dg}$ and $v_{\rm gs}$, the corresponding transconductances are

$$g_{\rm i1} = \frac{g_{\rm i10}}{1 + j\omega\tau_{\rm i}} \tag{25}$$

and

$$g_{\rm i2} = \frac{g_{\rm i20}}{1 + j\omega\tau_{\rm i}}, \tag{26}$$

respectively. The current source, $g_{\rm i2}v_{\rm gs}$, also includes the dependence on the initial current entering the gate-drain region [74]. The time constant $\tau_{\rm i}$ represents the effective rate of the process. By incorporating these two current sources it is possible to obtain a good fit between the measurement and the model, as shown in Fig. 24. Figure 26(a) shows the parameters of (25) and (26), as a function of $V_{\rm DS}$, deduced from S-parameter measurements using a similar approach as in Paper X. The extracted data shows that $\tau_{\rm i}$ decreases for increasing $V_{\rm DS}$, this is equivalent to an increased rate of the EII and/or BTBT process. The parameter $g_{\rm i10}$, which represents the electrons generated in the gate-drain region, increases with increasing $V_{\rm DG}$ and the current source modeling the influence of the initial electron current and the hole feedback effect ($g_{\rm i20}$) is negative for small $V_{\rm DS}$ and turns positive as $V_{\rm DS}$ is increased to 1.2 V. This is possibly related to the decreasing influence of the hole feedback effect and the increasing influence of the primary current, which indicates that the dominating process is EII at high $V_{\rm DS}$. Both $g_{\rm i1}$ and $g_{\rm i2}$ are dependent on the same effective generation rate $1/\tau_{\rm i}$.

3.4.2 Modeling of border traps

The real part of the Y-parameters Y_{11} and Y_{12}, shown in Fig. 24(a), experience an almost linear dependence on frequency, instead of the expected square behavior of the input low pass filter, or constant frequency dependence due to conductive gate

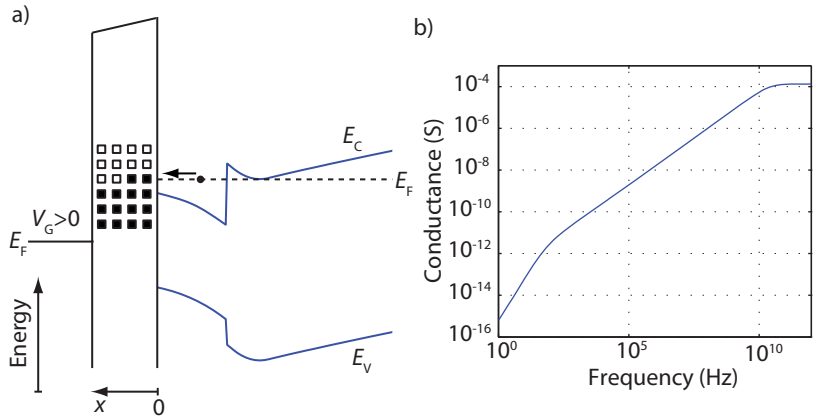

Figure 27: (a) Schematic band diagram illustrating the charge exchange between border traps and the semiconductor surface. (b) Gate oxide conductance calculated from (28). A constant $N_{\rm bt}$ of $9 \cdot 10^{19}$ cm^{-3} eV^{-1} was used, which was obtained from fitting to the measured Y-parameters in Fig. 24.

leakage. This phenomenon is also observed in Paper VII, IX, and X. In the case of the regrown MOSFET, the input is isolated by a 7-nm-thick gate oxide, which gives an insignificant DC gate leakage, less than 10 pA/μm, and the frequency response in Fig. 24(a) is instead attributed to the wideband nature of gate oxide border traps. These traps are present throughout the gate oxide and they exchange charges with the semiconductor surface through tunneling, as illustrated in Fig. 27(a). The time constant associated with this process is given by

$$\tau(x) = \tau_0 e^{2\kappa x},\ \kappa = \sqrt{2m^*(E_{\rm c}^{\rm ox} - E)}/\hbar, \tag{27}$$

where m^* is the electron effective mass in the dielectric, E is the electron energy and $E_{\rm c}^{\rm ox}$ is the energy barrier presented by the gate oxide [75]. Following the approach in [76] it is possible to calculate the admittance Y of the gate oxide by modeling the border traps as a distributed RC network. The resulting differential equation is

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\epsilon_{\rm ox}} + \frac{j\omega q^2 N_{\rm bt}}{1 + j\omega\tau_0 e^{2\kappa x}},\ Y(x=0) = j\omega C_{\rm sc}, \tag{28}$$

where $N_{\rm bt}$ is the border trap density, $C_{\rm sc}$ is the semiconductor capacitance, and $\epsilon_{\rm ox}$ is the permittivity of the gate oxide. Solving this equation under the condition of a constant $N_{\rm bt}$ gives the conductance shown in Fig. 27(b). Three distinct regions can be observed. The low cut off frequency is the frequency at which all border traps at a certain E are able to follow the applied voltage, hence it depends on $t_{\rm ox}$. The high cut-off frequency is the frequency at which none of the border traps are able to respond

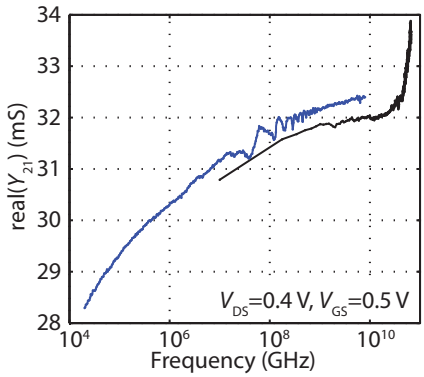

Figure 28: Measured $\Re(Y_{21})$ as a function of frequency for a regrown MOSFET with $L_{\rm g}$=140 nm and $W_{\rm g}$=21.6 μm. The blue and black traces are obtained from network analyzers with a frequency range of 20 kHz to 8 GHz and 10 MHz to 67 GHz, respectively.

to the applied voltage. The intermediate region where border traps at increasing depth respond to lower and lower frequencies has a very wide bandwidth and overlaps with the frequencies of the measured S-parameters in Fig. 24. The effect of border traps is included by adding the calculated gate oxide conductance in two equal parts, $g_{\rm gd}(\omega)$ and $g_{\rm gs}(\omega)$, to the small signal model in Fig. 23. It is especially important to include this effect when modeling the unilateral power gain, as the conductances at the input, $\Re(Y_{11})$ and $\Re(Y_{12})$, have a large impact on the result, given by

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(\Re(Y_{11})\Re(Y_{22}) - \Re(Y_{12})\Re(Y_{21}))}. \tag{29}$$

Paper VII also addresses the fact that for high $V_{\rm GS}$ the transconductance extracted from DC measurements differs from the transconductance extracted from S-parameter measurements. This is likely due to the increased trapping by gate oxide border traps at high $V_{\rm GS}$. The trapped charges screen the gate field and decrease the gate to channel coupling, which decreases the transconductance. Only a small fraction of these border traps are able to respond at the frequencies at which the transconductance is extracted from the S-parameter measurements. Figure 28 presents a measurement of $\Re(Y_{21})$ ($\approx$transconductance) from 20 kHz to 67 GHz on a regrown MOSFET. It is seen that the transconductance decreases with decreasing frequency. This effect has also been reported in [77].

Chapter 4

The InGaAs MOSFET and RTD

Chapter 3 discussed the considerations that were taken into account when designing the regrown MOSFET. The motivation of this design is to minimize the on-resistance to improve transistor performance both for digital and analog applications. However, the main purpose of the regrown MOSFET for the work of this thesis is its operation in a high frequency wavelet generator, where it is integrated in series with an RTD to form a variable negative differential conductance component. The RTD-MOSFET operation differs from that of the GTD, but the basic concept, of switching the output of the device between PDC and NDC using an isolated input, is the same. An important difference is that the RTD is designed separately from the FET, which provides the possibility to choose the ΔV, ΔI, C_{ce}, and V_{p} that gives the optimum performance for a specific application, which was not possible when designing the GTD.

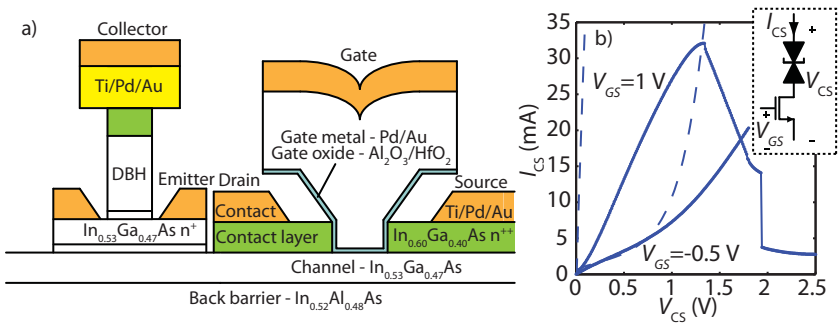

Figure 29: (a) Schematic cross-section of the RTD-MOSFET component. (b) Measured I_{CS} as a function of V_{CS}, the dashed trace is the output characteristics of the MOSFET. The RTD area is 26.4 μm^2 and the dimensions of the MOSFET are L_{g}=55 nm and W_g=160 μm. The inset shows the configuration of the RTD-MOSFET component.

Figure 29(a) shows a schematic cross-section of the RTD-MOSFET component. The RTD is fabricated in parallel with the regrown MOSFET. The collector contact is defined by lithography and is used as a mask when isolating the DBH mesa by means of wet etching. The emitter contact is deposited by thermal evaporation at the same time as the source and drain contacts. Paper VIII contains a thorough description of

Table 5: Epitaxial structure

Layer	Material	Thickness (Å)	Dopant level (cm^{-3})
SCR	$In_{0.53}Ga_{0.47}As$	1000	$2{\cdot}10^{17}$
Spacer	$In_{0.53}Ga_{0.47}As$	30	N.I.D
Barrier	AlAs	14	N.I.D
Well	$In_{0.53}Ga_{0.47}As$	9	N.I.D
Notch	InAs	20	N.I.D
Well	$In_{0.53}Ga_{0.47}As$	9	N.I.D
Barrier	AlAs	14	N.I.D
Spacer	$In_{0.53}Ga_{0.47}As$	30	N.I.D
Emitter	$In_{0.53}Ga_{0.47}As$	200	$4{\cdot}10^{18}$

the fabrication process.

The purpose of the MOSFET is to act as a variable resistor, which short circuit at high V_{GS} and limits the current through the RTD at low V_{GS}. Figure 29(b) shows the measured collector to source current (I_{CS}) as a function of the collector to source voltage (V_{CS}) and the dashed trace represents the measured output characteristics of the MOSFET. The MOSFET has a gate length of 55 nm and a width of 160 μm, to enable low resistive losses. The short gate length gives rise to short channel effects, which limit the off-state performance, and Impact ionization and BTBT, which were described in Section 3.4.1, are also present and adds to the off state current at high V_{DS}.

The epitaxial layers of the MBE grown DBH are shown in Table 5, they were designed based on the considerations in Section 2.1. A 100 nm thick space charge region was included to obtain high frequency operation at high output power, the InAs notch was incorporated to lower V_{p}, and the emitter side doping was kept high to increase J_{p}.

The DBH design in Table 5 shows a J_{p} of 1.22 mA/μm^2, high performance InGaAs RTDs with 1.2 nm thick AlAs barriers delivers a J_{p} as high as 24 mA/μm^2 [78]. The higher J_{p} comes at the expense of a higher J_{v}, however, as long as ΔI is increased for a given A_{RTD} it is beneficial to thin down the AlAs barriers to improve the oscillator output power of the RTD, which will be further discussed in the next chapter.

Chapter 5

The Wavelet Generator

From the moment the resonant tunneling diode was first proposed [79], it has been recognized as a circuit element capable of generating high frequency signals, due to its inherent NDC property that extends from DC well into the THz region [27, 40]. Various oscillator circuits utilizing the RTD has been implemented, and might be categorized as follows;

- Relaxation oscillators [80].
- Transmission line resonators [81].
- Antenna coupled quasioptical cavity resonators [27].
- LC-tank oscillators [82].

The relaxation oscillators are characterized by having an large inductive element in series with the RTD. The inductance counteracts any rapid current change through it, which is used to switch the RTD through the NDC region to generate sharp transitions. The relaxation oscillator is described in more detail in Paper IV. An RTD transmission line oscillator circuit is based on a configuration which has three possible operating points when biased in the NDC region. When triggered to switch between these points the circuit generates a pulse that is sent through a short or open circuit terminated transmission line. As the pulse is reflected it induces another switching through the NDC region, which in turn generates a new pulse that is sent through the transmission line. The length of the transmission line hence determines the oscillation frequency. Antenna coupled quasioptical cavity resonators are based on an RTD connected to an antenna, commonly an inductive slot antenna that is integrated into a resonator cavity. The properties of the RTD, antenna, and cavity determines the oscillation frequency. The to date highest oscillation frequency generated from an RTD oscillator was obtained by integrating an $In_{0.53}Ga_{0.47}As$ RTD with a slot antenna, it delivered 0.1 μW at 1.11 THz [39]. The circuits considered in this thesis belong to the LC-tank category of oscillators. In such a circuit the available energy oscillates between energy stored in inductive and capacitive circuit elements on-chip.

While the GTD and RTD-MOSFET devices may be applied in various circuits utilizing NDC, it is as the key component in high-frequency wavelet generators that they demonstrate unique features. The following sections describe the basic design and operation of a NDC driven wavelet generator and different alternatives of stabilizing the

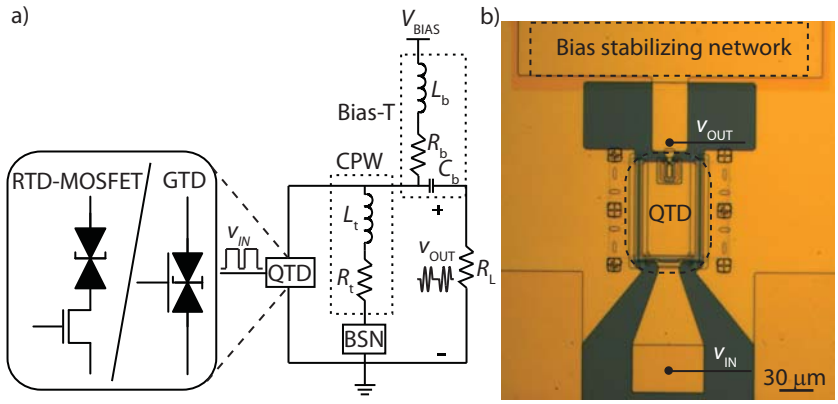

Figure 30: (a) Equivalent circuit of the wavelet generator. (b) Optical micrograph of the wavelet generator illustrating the different components. This particular image shows an RTD-MOSFET with a capacitive bias stabilizing network and a CPW of type A.

Table 6: Extracted small signal equivalent model of CPWs with different length

CPW type	length (μm)	L_t (pH)	R_t (Ω)
A	55	8	0.15
B	85	23	0.20

operation point of the circuit. This is followed by a detailed description of the startup and decay time of the oscillator. The last section gives a brief introduction to the use of the wavelet generator circuit as a super-regenerative oscillator detector.

5.1 Wavelet generator operation

Figure 30(a) shows the layout of the wavelet generator, and Fig. 30(b) shows the corresponding optical micrograph. The wavelet generator consists of three parts; a bias stabilizing network (BSN), a coplanar waveguide (CPW), and a quenchable tunnel diode (QTD), which is integrated in parallel to the CPW. Here, the QTD is either the GTD, which was described in Chapter 2 or the RTD-MOSFET, which was described in Chapter 4, however, the discussion in this chapter applies to NDC circuit elements in general. The wavelet generator is loaded by a 50 Ω measurement load (R_L) and biased through a bias-T, which is characterized by L_b, C_b, and R_b. An equivalent small signal model of the CPW is given by L_t and R_t. Table 6 shows the value of these elements extracted from S-parameter measurements on CPWs of two different lengths. The inductive CPW and the capacitive QTD forms a resonance

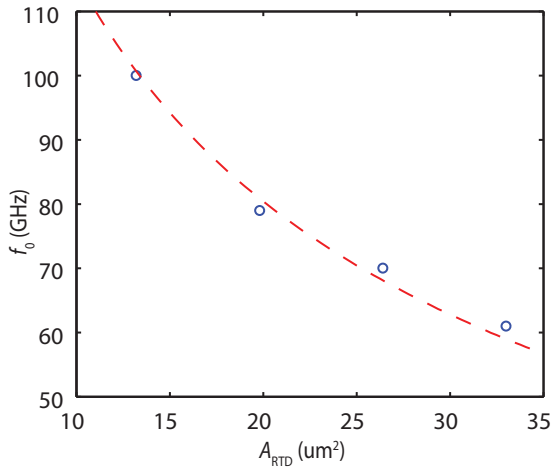

Figure 31: Measured oscillation frequency of fabricated RTD-MOSFET wavelet generators with CPW B (circles). The dashed trace is calculated from (30).

circuit at the output node, which will oscillate with the frequency

$$f_0 \approx \frac{1}{2\pi L_\mathrm{t}} \cdot \sqrt{\frac{L_\mathrm{t}}{C_\mathrm{ce}/((R_\mathrm{on}+R_\mathrm{e}+R_\mathrm{c})G_\mathrm{o}+1)^2} - R_\mathrm{t}^2}, \tag{30}$$

if the RTD presents enough NDC to compensate for the resistive losses in the circuit [83], which requires that

$$\frac{G_\mathrm{o} + (R_\mathrm{e}+R_\mathrm{c}+R_\mathrm{on})(G_\mathrm{o}^2+(\omega_0 C_\mathrm{ce})^2)}{((R_\mathrm{e}+R_\mathrm{c}+R_\mathrm{on})G_\mathrm{o}+1)^2} + \frac{1}{R_\mathrm{L}} + \frac{R_\mathrm{t}}{R_\mathrm{t}^2+(\omega_0 L_\mathrm{t})^2} = 0, \tag{31}$$

where G_o is the large signal output conductance of the DBH. Figure 31 shows the measured oscillation frequency of the RTD-MOSFET wavelet generator for different area of the RTD (A_RTD), the dashed trace is calculated by solving (30) and (31). The maximum frequency of oscillation of the RTD is given by the frequency at which the RTD no longer presents NDC at its output:

$$f_\mathrm{maxRTD} = \frac{|g_\mathrm{o}|}{2\pi C_\mathrm{ce}} \sqrt{\frac{1}{|g_\mathrm{o}|\,(R_\mathrm{e}+R_\mathrm{c})} - 1}. \tag{32}$$

In general it is beneficial to choose the smallest practical L_t and the largest A_RTD, i.e C_ce, when designing for a specific f_0, as this will maximize the available output power. This is discussed in Section 5.1.3.

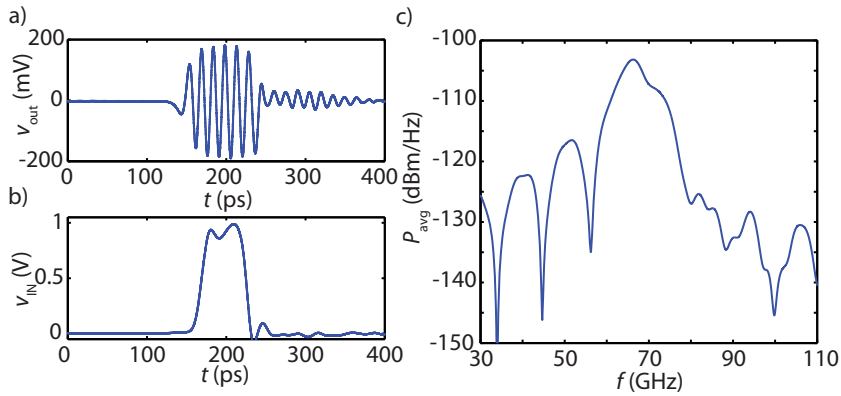

Figure 32: (a) Output signal from the RTD-MOSFET wavelet generator. (b) Input signal to the wavelet generator. (c) Fourier transform of the signal shown in 32(a).

Wavelet generator operation is achieved by applying a baseband signal to the input, which switches the output of the QTD between PDC and NDC. This turns the oscillator on and off, as illustrated in Fig. 30(a) and as shown in the measurement in Fig. 32(a). Figure 32(b) shows the corresponding input signal, and Fig. 32(c) is a Fourier transform of the output signal in Fig. 32(a).

5.1.1 DC stabilization

As discussed earlier, an RTD has the inherent property that it exhibits NDC at DC as well as at high frequencies. NDC at DC is an attractive property in the sense that the device may be used in applications where it is desirable to have a bistable load line configuration, for instance A/D converters [29] or memory cells [84]. However, when constructing high-frequency LC-tank oscillators it is necessary to have a stable bias point in the NDC region, any low frequency bias network oscillations need to be suppressed. Figure 33(a) shows an RTD oscillator circuit biased through a bias-T with a large inductor $L_{\rm b}$. This is the same circuit as in Fig. 30(a), except that the QTD has been replaced by an RTD, which is done in order to simplify the analysis of the bias stability. A DC blocking capacitor $C_{\rm s}$ has also been included in Fig. 33(a) to limit the power consumption. As described in Section 5.1 the oscillator circuit in Fig. 30 will oscillate at a frequency given by the QTD and the CPW, if the bias point is kept stable. In order to investigate the bias stability of the oscillator circuit in Fig. 33(a) it is simplified under the assumption of low frequency operation, the resulting circuit is shown in Fig. 33(b). The impedance between $V_{\rm bias}$ and ground is

$$Z_{\rm B} = R_{\rm e} + R_{\rm c} + R_{\rm b} + \frac{1}{g_{\rm o} + j\omega C_{\rm ce}} + j\omega L_{\rm b}. \tag{33}$$

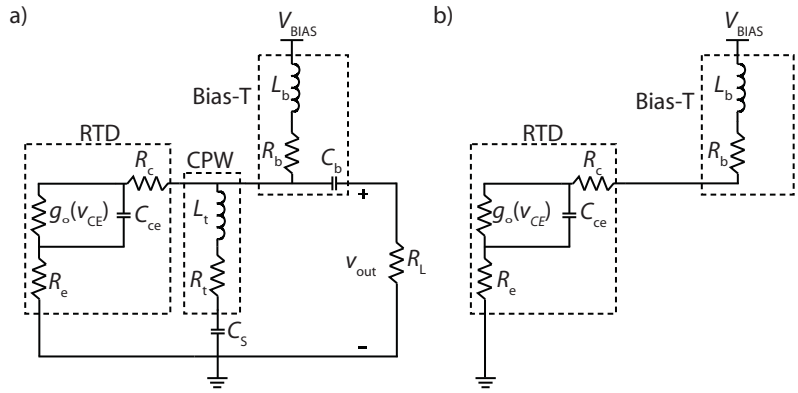

Figure 33: (a) Shows an RTD oscillator circuit that is equivalent to the QTD oscillator circuit presented in Fig. 30. (b) Simplification of the circuit in Fig. 33(a) under the assumption of low frequency oscillations.

If $\Re(Z_{\rm B}) \leq 0$, at the resonance frequency, given by the imaginary part of (33), the RTD will oscillate with the bias network [85]. Solving $\Re(Z_{\rm B}) = 0$ gives the maximum frequency of operation

$$f_{\rm M} = \frac{|g_{\rm o}|}{2\pi C_{\rm ce}} \sqrt{\frac{1}{|g_{\rm o}|\,(R_{\rm e} + R_{\rm c} + R_{\rm b})} - 1} \tag{34}$$

and solving $\Im(Z_{\rm B}) = 0$ gives the resonance frequency

$$f_{\rm B} = \sqrt{\frac{1}{C_{\rm ce} L_{\rm b}} - \frac{g_{\rm o}^2}{C_{\rm ce}^2}}. \tag{35}$$

The condition for maintaining a stable operating point is then rewritten as $f_{\rm M} < f_{\rm B}$, which is translated into the inequality

$$C'_{ce} > A_{\rm RTD} \cdot g_{\rm o}'^2 \cdot L_{\rm b}, \tag{36}$$

where $C'_{\rm ce}$ and $g'_{\rm o}$ are per RTD area unit. To obtain a stable bias point either $L_{\rm b}$ should be small or $A_{\rm RTD}$ should be small. In practical circuits it is hard to make $L_{\rm b}$ small enough, which imposes constraints on $A_{\rm RTD}$. The RF output power is proportional to $A_{\rm RTD}$, which means that bias network stability can only be achieved by imposing constraints on the available output power, which makes RTD circuits less attractive as a high-frequency source.

The operating point will not be stable if $f_{\rm M} > f_{\rm B}$, which will cause oscillations in the bias network. Depending on the ratio between $g_{\rm o}$ and the positive resistances in the circuit, the oscillations will be either sinusoidal or growing exponential [85], where the

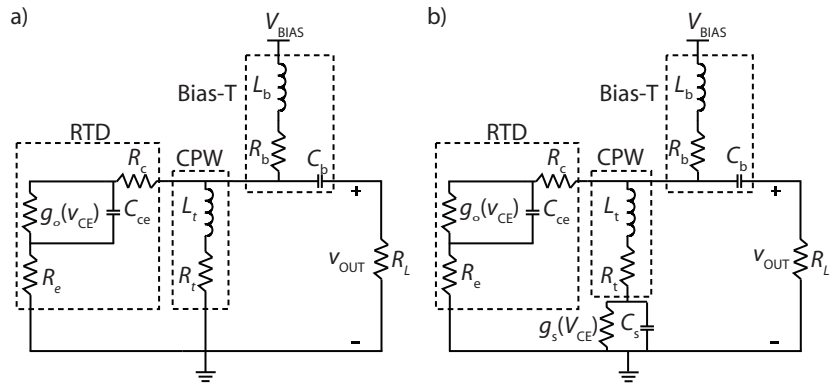

Figure 34: (a) Oscillator circuit which achieves bias stability by short circuiting the CPW to ground, in (b), bias stability is provided by an on-chip bias stabilizing network consisting of a Schottky diode, which is modeled by $g_{\rm s}(V_{\rm ce})$, and a MIM capacitor.

growing exponential solution results in what is known as a relaxation oscillator [86], which is further considered in Paper IV.

It is important to be able to implement RTD circuits without having to rely on small device areas to ensure a stable operating point. A straightforward approach is to make the bias point stable by introducing an element in parallel to the RTD that ensures that the output node conductance is larger than zero at $f_{\rm B}$. The simplest approach is to short circuit the CPW to ground as shown in Fig. 34(a), this approach was used in Paper I. To ensure that the operating point is kept stable requires that

$$|\Re(Y_{\rm RTD})| = \left|\frac{g_{\rm o}(g_{\rm o}(R_{\rm e}+R_{\rm c})+1)+(\omega_{\rm B}C_{\rm ce})^2(R_{\rm e}+R_{\rm c})}{((R_{\rm e}+R_{\rm c})g_{\rm o}+1)^2}\right| < \frac{1}{R_{\rm t}} \qquad (37)$$

is fulfilled. This configuration however imposes the restraint that it is not possible to design the CPW and the current limiting element independently. Figure 34(b) illustrates an approach where this is possible. By implementing a bias stabilizing network consisting of a Schottky diode, and a large metal-insulator-metal (MIM) capacitor ($C_{\rm s}$), it is possible to design the CPW solely for high-frequency operation and the Schottky diode conductance $g_{\rm s}(V_{\rm CE})$ for bias stabilization [47], this approach was used in Paper II and III. The lowest power consumption is achieved by using the smallest possible Schottky diode area that still fulfills (37), with $R_{\rm t}$ replaced by $1/g_{\rm s}(V_{\rm CE})+R_{\rm t}$. Figure 35(a) shows a measurement where the Schottky diode area has been matched to the NDC of the RTD. The MIM capacitor $C_{\rm s}$ is large enough to keep $g_{\rm s}$ from loading the circuit at f_0, but it also has other purposes as will be discussed. The circuit shown in Fig. 34(b) is fabricated by processing the CPW, the Schottky diode, and the MIM capacitor in parallel to the QTD. C_s has a value of 300-700 pF and is implemented in Au-HfO_2-Au MIM stack, where the thickness of the HfO_2 is

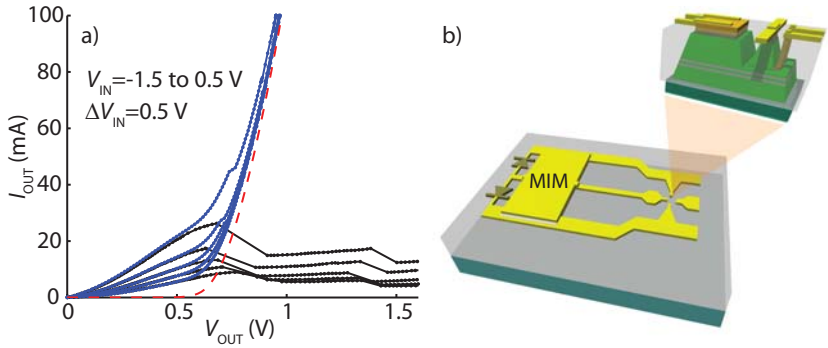

Figure 35: (a) DC output characteristics of the GTD (black trace) and the GTD shunted by a Schottky diode (blue trace). The non ideal GTD IV-characteristics is due to bias network oscillations. The dashed red trace shows the DC characteristics of the Schottky diode. (b) Schematic layout of the fabricated GTD oscillator circuit, including Schottky diode and MIM capacitor BSN.

15-20 nm, the area of the capacitor is 0.02-0.05 mm^2, and the relative permittivity of the HfO_2 layer is roughly 20. The capacitor was evaluated by S-parameter measurements. An illustration of the fabricated GTD wavelet generator circuit is shown in Fig. 35(b), which relates to the illustrations in Fig. 10 in Chapter 2, where the fabrication of the GTD was described.

The previous discussion applies if a continuous oscillator signal is desired, the bias point needs to be kept stable at all time. However if the circuit is to be used solely as a wavelet generator, then the conductance that was introduced in parallel to the QTD may be neglected, hence limiting the DC power consumption to that of the QTD. This is the approach in Paper III-IV and VIII. Thus, the circuit in Fig. 33(a), that was found to have constraints on its available output power, is now considered again but this time only from a wavelet generator perspective.

A large signal model of the GTD wavelet generator is shown in Fig. 36. If this circuit is biased in the NDC region, with the intention of generating a continuous RF signal, the result will be a low frequency bias network oscillation. However, if the circuit is operated as a wavelet generator, then it will be able to produce short pulses of RF signal. This is thoroughly analyzed in Paper IV, a brief description is given here, which is illustrated by the insets of Fig. 36, where the actual high frequency oscillation has been neglected for clarity. The GTD is biased in the PDC region in such a way that a decrease in the input voltage will switch the output of the device to NDC, which triggers high frequency oscillations, as discussed in Section 5.1. The input pulse, shown to the left in Fig. 36, is translated into a decrease in the output current of the GTD, which cannot be supported by the large bias inductor L_{b}. If C_{s} is large enough to support an increase in current that is equal to the decreases in the

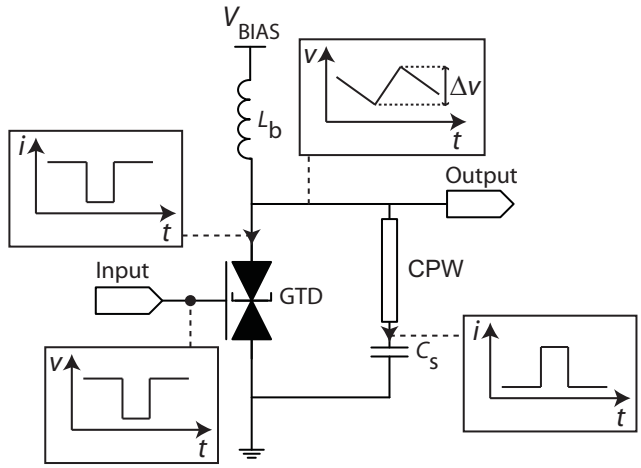

Figure 36: Large signal equivalent model of the GTD wavelet generator, without bias stabilizing Schottky diode. The insets illustrate the currents and voltages in the circuit when triggered by the baseband pulse shown at the input.

current through the GTD, without a significant increase in the voltage at the output node, then the bias point will be quasi-stable and RF oscillations will be produced. The change in voltage across C_s during a pulse of length t_p is

$$\Delta v \approx \Delta i \cdot t_\mathrm{p} / C_\mathrm{s}. \tag{38}$$

A large C_s and small t_p will ensure that any modulation of the oscillation frequency or output voltage during t_p is kept at an acceptable level. This technique provides the possibility to generate wavelets at the lowest possible power consumption, as it is only the active device that consumes current.

5.1.2 Startup and decay of wavelets

When designing wavelet generators it is important to have exact control of the startup and decay behavior of the oscillator. This allows for direct shaping of the wavelets, which may be used to optimize the spectral efficiency of the output signal. A rapid startup and decay also gives the possibility of generating very short wavelets, which is important for high bit rate impulse radio transmitters.

Paper I describes the startup and decay lapse of the QTD wavelet generator when triggered by an input pulse with a relatively slow rise time. The startup behavior is investigated by considering the circuit in Fig. 37(a), which is a simplified version of the GTD wavelet generator model in Fig. 30(a), including the GTD model in Fig. 13(b).

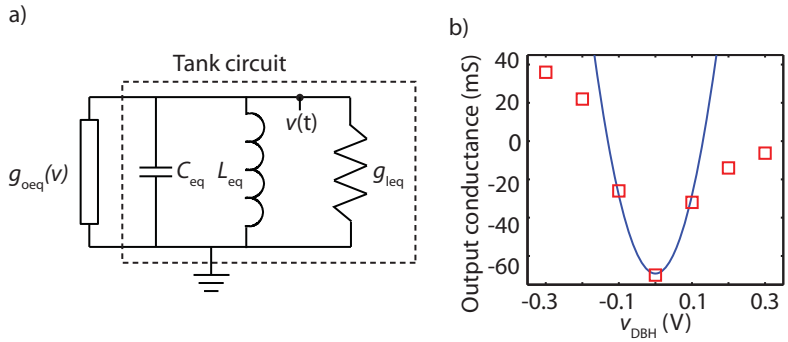

Figure 37: (a) Simplified version of the output circuit of Fig. 30(a). (b) The solid trace shows $g_{\rm o}(v_{\rm DBH})$ derived from the third order polynomial in (42), the parameters used are ΔI=12 mA, and ΔV=260 mV. The squares shows the intrinsic output conductance extracted from S-parameter measurements on the GTD biased at $V_{\rm IN}$=0 V.

The circuit elements in Fig. 37(a) are

$$C_{\rm eq} = C_{\rm ce}/(((R_{\rm e}+R_{\rm c})G_{\rm o}+1)^2+(\omega_0 C_{\rm ce}(R_{\rm e}+R_{\rm c}))^2), \tag{39}$$

$$L_{\rm eq} = (R_{\rm t}^2+(\omega_0 L_{\rm t})^2)/(\omega_0^2 L_{\rm t}), \tag{40}$$

and

$$g_{\rm leq} = 1/R_{\rm L} + R_{\rm t}/(R_{\rm t}^2+(\omega_0 L_{\rm t})^2), \tag{41}$$

which is the equivalent load seen by the GTD at $f_0 = \omega_0/2\pi$. The equivalent output conductance of the DBH of the GTD ($g_{\rm o}(v_{\rm DBH})$) is derived from a third order polynomial representation of the current through the DBH, given by

$$i_{\rm DBH} = g_{\rm omin} v_{\rm DBH} + 2\frac{\Delta I}{(\Delta V)^3} v_{\rm DBH}^3. \tag{42}$$

Here, $g_{\rm omin} = -3\Delta I/2\Delta V$ is the negative differential conductance of the DBH when biased in the middle of the NDC region, ΔI and ΔV are the peak to valley current and voltage difference, respectively [86]. Figure 37(b) shows the DBH output conductance ${\rm d}i_{\rm DBH}/{\rm d}v_{\rm DBH} = g_o(v_{\rm DBH})$ calculated from (42) and the output conductance extracted from S-parameter characterization of the GTD reported in Section 2.3. Differentiating (42) with respect to time gives

$$\frac{{\rm d}i_{\rm DBH}}{{\rm d}t} = \dot{v}_{\rm DBH}(g_{\rm omin} + 6\frac{\Delta I}{(\Delta V)^3} v_{\rm DBH}^2) = \dot{v}_{\rm DBH} g_{\rm o}(v_{\rm DBH}). \tag{43}$$

The resistances $R_{\rm e}$ and $R_{\rm c}$ are accounted for by deriving the equivalent output conductance $g_{\rm oeq}(v)$ of the GTD

$$g_{\rm oeq}(v) = \frac{g_{\rm o}(v)+(R_{\rm e}+R_{\rm c})(g_{\rm o}(v)^2+(\omega C_{\rm ce})^2)}{((R_{\rm e}+R_{\rm c})g_{\rm o}(v)+1)^2+(\omega C_{\rm ce}(R_{\rm e}+R_{\rm c}))^2}. \tag{44}$$

The difference between v and v_{DBH} is a linear voltage drop across R_{e} and R_{c} and will not affect the analysis of the startup and decay time.

By Taylor expanding (44) to second order

$$g_{\mathrm{oeqT}}(v) = g_{\mathrm{oeq}}(0) + g''_{\mathrm{oeq}}(0)v^2/2 \tag{45}$$

the time differentiate of the current through the GTD may be written as

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{GTD}} = g_{\mathrm{oeqT}}(v)\dot{v}, \tag{46}$$

and summing the currents at the output node of Fig. 37(a) and differentiating with respect to time gives

$$C_{\mathrm{eq}}\ddot{v} + (g_{\mathrm{leq}} + g_{\mathrm{oeqT}})\dot{v} + \frac{1}{L_{\mathrm{eq}}}v = 0. \tag{47}$$

Defining $v_0 = \sqrt{-2(g_{\mathrm{leq}} + g_{\mathrm{oeq}}(0))/g''_{\mathrm{oeq}}(0)}$, $\epsilon = -(g_{\mathrm{leq}} + g_{\mathrm{oeq}}(0))\sqrt{L_{\mathrm{eq}}/C_{\mathrm{eq}}}$, and replacing v with $v_{\mathrm{o}}y$ makes it possible to write (47) as

$$\ddot{y} + \epsilon\omega_0(y^2 - 1)\dot{y} + \omega_0^2 y = 0, \tag{48}$$

which is transformed into the van der Pol equation

$$\omega_0 t \to \tau, y(t) \to x(\tau) \Rightarrow \ddot{x} + \epsilon(x^2 - 1)\dot{x} + x = 0 \tag{49}$$

that can be solved using the averaging method [87]. The amplitude r and phase φ are functions of time

$$x(\tau) = r(\tau)\cos(\tau + \varphi(\tau)) \tag{50}$$

$$\dot{x}(\tau) = -r(\tau)\sin(\tau + \varphi(\tau)) \tag{51}$$

and together with the fact that the time differentiate of (50) has to be equal to (51), makes it possible to write

$$\dot{r} = -\epsilon\sin(\tau + \varphi)(r^2\cos^2(\tau + \varphi) - 1)r\sin(\tau + \varphi) \tag{52}$$

$$\dot{\varphi} = -\frac{\epsilon}{r}\cos(\tau + \varphi)(r^2\cos^2(\tau + \varphi) - 1)r\sin(\tau + \varphi). \tag{53}$$

As r and φ are assumed to vary slowly compared to one cycle of oscillations, i.e $\epsilon < 1$, (52,53) are averaged over $\varphi \to 2\pi + \varphi$. The result is

$$\dot{r} = \frac{1}{2}\epsilon r(1 - \frac{r^2}{4}) \tag{54}$$

$$\dot{\varphi} = 0. \tag{55}$$

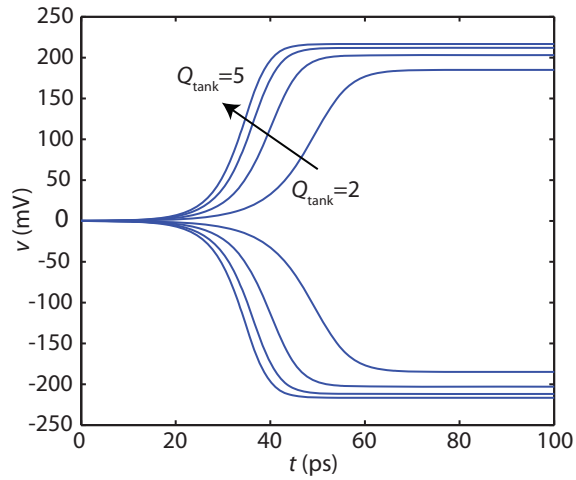

Figure 38: Envelope of the oscillator signal calculated from (57).

Separating variables of (54) and integrating results in

$$r(\tau) = \frac{r(0)e^{1/2\epsilon\tau}}{\sqrt{1+\frac{1}{4}r(0)^2(e^{\epsilon\tau}-1)}}, \tag{56}$$

where the initial condition $r(0)$ has been introduced. Transforming back to voltage gives

$$v(t) = \frac{2v_0}{\sqrt{1+\left(\left(\frac{2v_0}{v(0)}\right)^2-1\right)e^{-\epsilon\omega_0 t}}}\cos(\omega_0 t+\varphi), \tag{57}$$

which describes the voltage at the output node of Fig. 37(a) as a function of time, φ is set by its initial value $\varphi = \varphi(0)$. The startup of oscillations is mainly determined by two factors, the initial condition $v(0)$ and the damping factor ϵ, which may be rewritten as

$$\epsilon = -\left(g_{\mathrm{oeq}}(0)\sqrt{\frac{L_{\mathrm{eq}}}{C_{\mathrm{eq}}}}+\frac{1}{Q_{\mathrm{tank}}}\right),\ Q_{\mathrm{tank}} = 1/(g_{\mathrm{leq}}\omega_0 L_{\mathrm{eq}}). \tag{58}$$

Here the quality (Q)-factor of the tank circuit (Q_{tank}), shown in Fig. 37(a), has been included. The Q-factor is defined as the ratio between maximum instantaneous energy stored in the tank circuit and the energy dissipated per cycle. To ensure rapid startup Q_{tank} should be large and hence g_{leq} small, i.e. low tank circuit loss. Figure 38 shows the result of (57) for different Q_{tank} illustrating its influence on the startup time. The value of the reactive elements were kept constant in the calculations, increasing L_{eq}

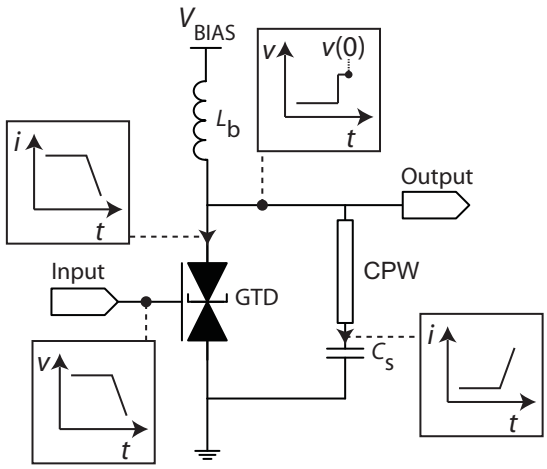

Figure 39: Large signal equivalent model of the GTD wavelet generator. The insets illustrate the currents and voltages in the circuit when triggered by the the falling edge of a baseband pulse, as depicted at the input.

by a factor β while keeping $L_{\rm eq}/C_{\rm eq}$ constant to maintain f_0 can decrease the startup time for circuit configurations were $g_{\rm oeq}$ does not scale with $C_{\rm eq}$. This is not the case for the oscillator considered here as both g_o and $C_{\rm ce}$ are proportional to $A_{\rm RTD}$ and increasing $L_{\rm eq}$ by β would only have a small impact on the startup time.

The calculated 10% to 90% startup time of the GTD oscillator when loaded by $R_{\rm L}$ =50 Ω ($Q_{\rm tank}$=2.4) is 20 ps. However, faster startup may be achieved by adjusting the initial condition $v(0)$ in (57), which is the approach in Paper II-IV, and VIII. This is realized by controlling the rise time of the input signal to the wavelet generator, as illustrated by the insets of Fig. 39, describing the current and voltage in different nodes as the input is triggered by a negative baseband pulse. The input signal causes the current through the GTD output to decrease and forces an equivalent increase in current to $C_{\rm s}$, as the current cannot be supplied by the large inductance $L_{\rm b}$. This rapid increase of current through $L_{\rm t}$ calls for a rapid increase of the voltage at the output node of the wavelet generator

$$v_{\rm out} = L_{\rm t}\frac{di_{L_{\rm t}}}{dt}. \tag{59}$$

Here, $di_{L_{\rm t}}/dt$ may be altered by adjusting the rise time of the input baseband pulse, which effectively allows for direct control of the initial condition $v(0)$ governing the startup of oscillations. Figure 40(a) shows experimental data, where the output signal of the oscillator is measured for three different rise times of the input baseband pulse, shown in Fig. 40(b). The calculated startup condition is shown in Fig. 40(c) and it is clearly seen that the output signals have different startup time depending on the rise time of the input signal ($t_{\rm rin}$), i.e. the initial condition of the oscillation. For the input

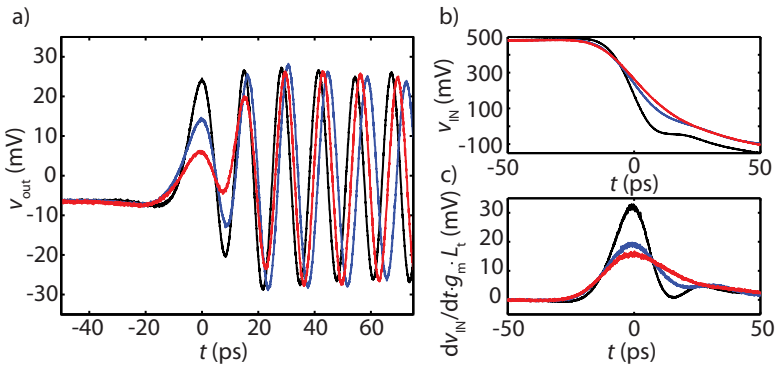

Figure 40: (a) Measured output signal of the GTD wavelet generator when triggered by the baseband pulses shown in (b), the calculated initial condition is shown in (c). Three different values of t_{rin} is used to illustrate the significance of controlling the initial condition of the oscillator.

pulse with t_{rin}=12 ps (20% to 80%) the initial condition is almost set to the amplitude of the steady state oscillation and the startup time of the oscillator is then limited to the rise time of the input signal. The time constant of the input low pass filter of the GTD is

$$t_{\mathrm{rg}} \approx \ln(9) C_{\mathrm{ge}} (R_{\mathrm{e}} + R_{\mathrm{g}}), \tag{60}$$

which for the circuit and bias condition of the measurement in Fig. 40 is calculated to 3 ps and has no significant influence on the startup of the oscillator.

As discussed previously, a high Q_{tank} ensures rapid startup of the QTD wavelet generator. However, when considering the decay of the oscillator a low Q_{tank} is required to rapidly quench the oscillation, as given by

$$v(t) = 2v_0 e^{\frac{-\omega_0}{2Q_{\mathrm{tankPDC}}} t} \cos(\omega_0 t),\ Q_{\mathrm{tankPDC}} = 1/((g_{\mathrm{leq}} + g_{\mathrm{oeqPDC}})\omega_0 L_{\mathrm{eq}}), \tag{61}$$

which is the solution to (47) when g_{oeqT} has been replaced by the the output conductance of the GTD when biased in the PDC region (g_{oeqPDC}). Here, g_{oeqPDC} is approximated to be constant with respect to v_{OUT}. The maximum amplitude of the output signal is equal to $2v_0$ at the instance the oscillator is switched off, as given by (57). Figure 41 depicts the result of (61) for different Q_{tankPDC}. Equation (61) illustrates that even though a high Q_{tank} is used to ensure rapid startup, the oscillations may be rapidly quenched by a low tank Q-value as the circuit is switched off. This is due to the output circuit being loaded by g_{oeqPDC} when the QTD is switched to the PDC region.

Figure 42 shows a measured wavelet from a GTD wavelet generator, the imposed envelope represent the result of (57) and (61), starting from the initial condition indicated in the figure. The parameters used in the calculations are those of the GTD

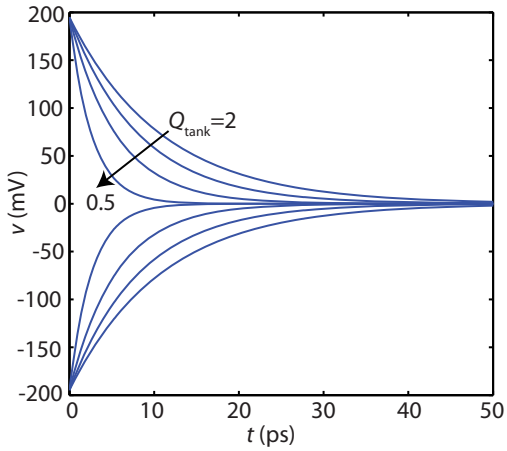

Figure 41: Envelope of the oscillator calculated from (61) for different Q_{tank}.

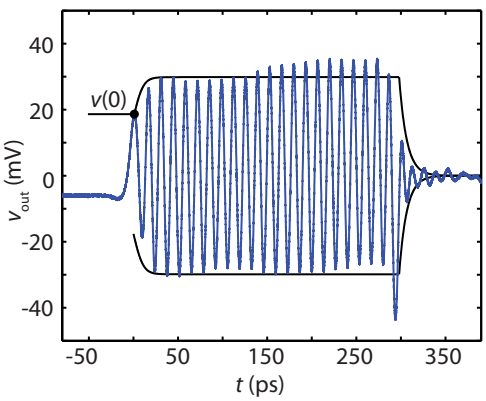

Figure 42: Output signal from the GTD wavelet generator. The envelope is calculated from (57) and (61). The measured data has not been compensated for measurement losses and the calculated envelope has been rescaled to show the agreement between the measured and modeled startup and decay behavior.

small-signal model in Fig. 13(b), CPW B in Table 6, g_{oPDC}=5 mS and the third order polynomial given by the parameters listed in the caption of Fig. 37(b). The good agreement between theory and experiment confirms the operation of the wavelet generator.

5.1.3 Output power and design considerations

The peak output power of the wavelet generator delivered to the load g_{L} is given by

$$P_{\mathrm{peak}} = 2v_0^2 g_{\mathrm{L}} \approx \frac{g_{\mathrm{L}}}{2}(\Delta V)^2 - \frac{g_{\mathrm{L}}}{3}\frac{(\Delta V)^3}{\Delta I}, \tag{62}$$

neglecting the loses in the QTD and CPW. Equation (62) shows that a large ΔI and ΔV maximizes the output power, hence, A_{RTD} should be as large as possible. The optimum load is derived as $g_{\mathrm{L}} = -g_{\mathrm{omin}}/2$, which gives P_{peak}=(3/16)$\Delta I \Delta V$. Based on these derivations the efficiency of the oscillator does not depend on A_{RTD} as both P_{peak} and the DC power consumption scales linearly with A_{RTD}.

In conclusion, the optimum wavelet generator performance, in terms of output power and the possibility to generate short wavelets, is achieved by implementing the smallest practical L_{t} and choosing the largest A_{RTD} given the desired f_0. This maximizes P_{peak}, Q_{tank}, and g_{oPDC}, which allows for rapid startup and decay of the wavelets. To improve the efficiency, given a desired P_{peak} and f_0, V_{p} and J_{v} should be as small as possible, as discussed in Section 2.1. These conclusions are based on the analytical derivations in this chapter, starting from the third order polynomial description of the RTD current in (42), which is valid to a first order of approximation. To obtain a more reliable and optimized design it is recommended to use computer aided simulations incorporating the small-signal models that were developed as a part of this thesis.

The wavelet generator theory described in this chapter applies to NDC oscillators in general. The GTD and RTD-MOSFET wavelet generators are two examples and alternative implementations are possible. The NDC element could be a Gunn diode [88, 89] or a transistor implementation [25, 90] and the variable resistance could be realized using any type of switch with a high dynamic range. The main benefit of the QTD wavelet generator presented here is the extremely fast startup and decay of coherent wavelets and the possibility of only consuming energy during the generation of the wavelet.

5.2 Super regenerative oscillator detector

The QTD wavelet generator has many features which makes it suitable for use as an impulse transmitter. In addition, the same circuit topology may be used as an impulse receiver by simply reconfiguring the input control signal, which allows for savings in terms of size and manufacturing cost.

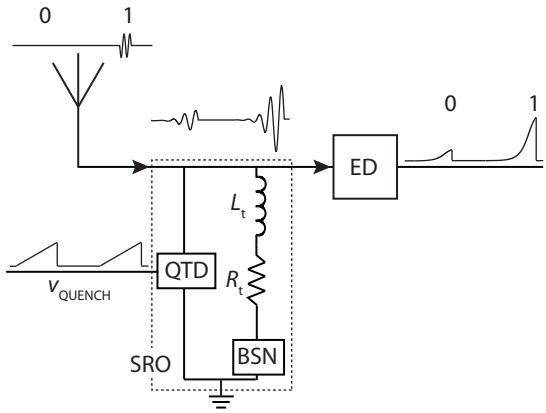

Figure 43: Illustration of a receiver topology based on the QTD super-regenerative oscillator.

The receiver topology is known as a super regenerative oscillator (SRO) detector and is reported in Paper V. Figure 43 shows the QTD circuit configuration and its functionality in an non-coherent receiver, where the control signal (V_{QUENCH}), as compared to the QTD wavelet generator, is a sawtooth wave with a slow rise time. This signal turns the output conductance of the SRO from positive to negative, which will start a slow build up of oscillation, governed by ϵ in (57). If energy is received at the output node during the early phase of the build-up it will speed up the process, much like the initial condition $v(0)$ of (57), and if no energy is received the build-up will be purely from noise. The SRO output during build-up from noise and build-up from received wavelet is illustrated in Fig. 43. An energy detector (ED) transforms the signal into an envelope, which is delivered to an analog-to-digital converter that returns a "1" if a wavelet was received and a "0" if no wavelet was received.

The SRO may be programmed to detect in different time slots making it possible to get time resolution already in the RF front-end. The time resolution may be further improved by relating the amplitude of the envelope of the SRO at a given time to the actual time in the sample when the energy was received.

Chapter 6

Conclusions and Outlook

The work of this thesis has demonstrated field-effect and tunneling based devices in millimeter wave (mm-wave) impulse radio circuits. The main research results are that novel device concepts can be used to improve and even create new circuit functionality. An example is the quenchable tunnel diode wavelet generator, which shows promising features for use in mm-wave communication, as well as in other applications as illustrated in Fig. 44. The figure represents, from top to bottom, on-off keying communication, radar, spectroscopy, localization, and imaging. The ultra-short mm-wave wavelets may be used to increase bit rates, improve ranging accuracy, enhance positioning exactness, perform time resolved wideband characterization, and improve range resolution. These are important properties, but it is the possibility of combing them with a small energy consumption that makes the research presented here attractive for the applications described by Fig. 44. The next step will be to integrate the wavelet generator with a suitable antenna that supports the very wideband nature of the wavelets, which may be done by embedding the antenna as a part of the circuit. This is the main goal for the continuation of the project.

The RTD-MOSFET wavelet generator shows superior features when compared to the GTD wavelet generator. This is mainly related to the choice of DBH materials, and to the excellent properties of the demonstrated $In_{0.53}Ga_{0.47}As$ MOSFET. The novel device architecture was designed with minimization of the on-resistance as the main target, which was achieved by using epitaxial regrowth of the source and drain access regions. The fabricated devices show the lowest R_{on} reported for any InGaAs FET.

The future development of MOSFETs for VLSI will include III-V channel materials. However, many challenges remain, such as the impact of gate oxide border traps on high frequency performance, and increased off-state current due to impact ionization and band-to-band-tunneling. These phenomena were investigated in this work and should be subjected to continued investigations, preferably by temperature dependent S-parameter characterization. The technique of epitaxial regrowth of MOSFET access regions, which was presented in this work, is applicable to Tri-gate and gate-all-around device architectures and should also be the focus of future work.

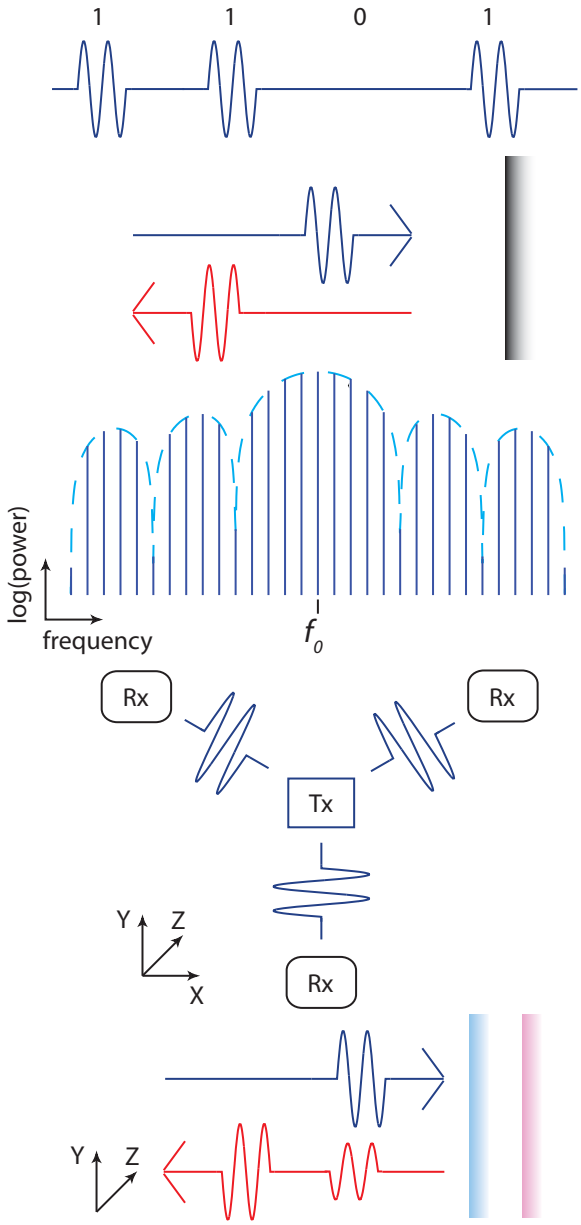

Figure 44: Illustration of wavelets in communication, radar, spectroscopy, localization, and imaging applications.

Appendix A

Calculation of Current Density Through the DBH

This appendix outlines the calculation of the transmission probability that was presented in Section 2.1. The 1-D time-independent Schrödinger equation, describing the transmission through the DBH discussed in Section 2.1, is given by (63).

$$-\frac{\hbar^2}{2}\nabla\left(\frac{1}{m^*(z)}\nabla\right)\Psi(z)+V(z)\Psi(z)=E_z\Psi(z) \tag{63}$$

Here, $V(z)$ is the confining potential of the DBH. The transmission probability is obtained by looking at the relation between the amplitude of the wavefunction at the emitter and collector side.

A simple approach is to use the transfer matrix theory described in [32, 33]. The idea is to approximate the potential of the DBH by a series of small steps, and to calculate the scattering parameters for each of these steps, before multiplying them together to give the total transfer matrix $\boldsymbol{T}$ of the DBH. The division of the DBH into segments, used in calculating the current in Fig. 9 is shown in Fig. 45, each segment is 0.1 nm wide. The wavefunction in each of these segments may be expressed in plane-wave form, according to (64).

$$\psi_i = A_i e^{ik_i z} + B_i e^{-ik_i z} \tag{64}$$

Here, the index i refers to which of the segments is considered, A_i and B_i are the amplitude of the part of the wavefunction traveling in positive and negative z-direction. The wavenumber k_i is given by the parabolic effective mass approximation when energies above the conduction band are considered. However, this approach is not adequate when considering tunneling through the band gap of semiconductors, instead the theory of complex band structure has been employed in the calculations [91].

As the particle flux through the DBH is conserved, the following conditions applies at all boundaries between the segments (65,66).

$$\Psi_i = \Psi_{i+1} \tag{65}$$

$$\frac{1}{m_i^*}\frac{\partial\Psi_i}{\partial z} = \frac{1}{m_{i+1}^*}\frac{\partial\Psi_{i+1}}{\partial z} \tag{66}$$

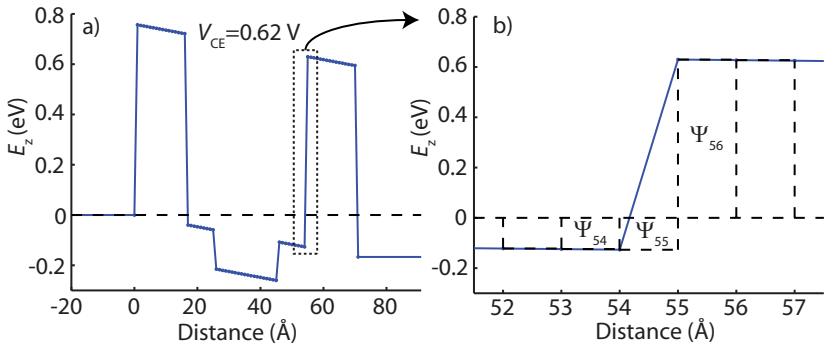

Figure 45: (a) Shows the DBH under bias and (b) illustrates the division into segments and the corresponding wavefunctions and potentials.

The relation between the amplitude of the wavefunctions on the emitter and collector side of the DBH is then given by (67), where each segment contributes to the overall transfer matrix.

$$\begin{bmatrix} A_C \\ B_C \end{bmatrix} = \boldsymbol{T} \begin{bmatrix} A_E \\ B_E \end{bmatrix} \tag{67}$$

The ingoing amplitude on the emitter side, A_E, is thus related to the outgoing amplitude on the collector side, A_C, by T_{11}. Using T_{11} as the transmission probability in (7) gives current density through the DBH, as a function of applied bias, reported in Fig. 9(d).

References

[1] D. Bodanis, *Elektricitet*. Stockholm: Norstedts förlag, 2005.

[2] B. Razavi, "Gadgets gab at 60 ghz," *Spectrum, IEEE*, vol. 45, no. 2, pp. 46–58, Feb. 2008.

[3] F. W. DC. (2002, feb) Fcc first report and order: In the matter of revision of part 15 of the commission's rules regarding ultra-wideband transmission systems, fcc 02-48. [Online]. Available: http://hraunfoss.fcc.gov/edocs_public/attachmatch/FCC-02-48A1.pdf

[4] W. Alliance. (2012, March) Wimedia phy specification 1.5. [Online]. Available: www.wimedia.org/en/specs.asp?id=specs

[5] R. Daniels and R. Heath, "60 ghz wireless communications: emerging requirements and design recommendations," *Vehicular Technology Magazine, IEEE*, vol. 2, no. 3, pp. 41–50, Sept. 2007.

[6] E. Grass, I. Siaud, S. Glisic, M. Ehrig, Y. Sun, J. Lehmann, M. Hamon, A. Ulmer-Moll, P. Pagani, R. Kraemer, and C. Scheytt, "Asymmetric dual-band uwb / 60 ghz demonstrator," pp. 1–6, Sept. 2008.

[7] N. Guo, R. C. Qiu, S. Mo, and K. Takahashi, "60-ghz millimeter-wave radio: Principle, technology, and new results," *EURASIP Journal on Wireless Communications and Networking*, Sep. 2007.

[8] M.-G. D. Benedetto and G. Giancola, *Understanding Ultra-wideband radio fundamentals*. New Jersey: Prentice Hall, 2004.

[9] M. Win and R. Scholtz, "Ultra-wide bandwidth time-hopping spread-spectrum impulse radio for wireless multiple-access communications," *Communications, IEEE Transactions on*, vol. 48, no. 4, pp. 679–689, Apr 2000.

[10] M. Win, R. Scholtz, and M. Barnes, "Ultra-wide bandwidth signal propagation for indoor wireless communications," vol. 1, pp. 56–60 vol.1, Jun 1997.

[11] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, N. Kinayman, N. Jain, R. Anderson, F. Kolak, R. Wohlert, S. Bawell, J. Bennett, and J.-P. Lanteri, "Ultra-wideband radar sensors for short-range vehicular applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 9, pp. 2105 – 2122, sept. 2004.

[12] D. Van Der Weide, F. Keilmann, V. Agrawal, and J. Murakowski, "Gas absorption spectroscopy with electronic terahertz techniques," in *Terahertz Electronics Proceedings, 1998. THz Ninety Eight. 1998 IEEE Sixth International Conference on*, sep 1998, pp. 117 –119.

[13] M. Segura, V. Mut, and H. Patino, "Mobile robot self-localization system using ir-uwb sensor in indoor environments," in *Robotic and Sensors Environments, 2009. ROSE 2009. IEEE International Workshop on*, nov. 2009, pp. 29 –34.

[14] A. Arbabian, S. Callender, S. Kang, B. Afshar, J.-C. Chien, and A. Niknejad, "A 90 ghz hybrid switching pulsed-transmitter for medical imaging," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 12, pp. 2667 –2681, dec. 2010.

[15] K. K. Lee, M. Dooghabadi, H. Hjortland, O. Naess, and T. Lande, "A 5.2 pj/pulse impulse radio pulse generator in 90 nm cmos," in *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, may 2011, pp. 1299 –1302.

[16] C. Hu and P. Chiang, "All-digital 3-50 ghz ultra-wideband pulse generator for short-range wireless interconnect in 40nm cmos," in *Custom Integrated Circuits Conference (CICC), 2011 IEEE*, sept. 2011, pp. 1 –4.

[17] B. Badalawa and M. Fujishima, "60 ghz cmos pulse generator," *Electronics Letters*, vol. 43, no. 2, pp. 100–102, 18 2007.

[18] D. Wentzloff and A. Chandrakasan, "Gaussian pulse generators for subbanded ultra-wideband transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 4, pp. 1647–1655, June 2006.

[19] Y. Nakasha, Y. Kawano, T. Suzuki, T. Ohki, T. Takahashi, K. Makiyama, T. Hirose, and N. Hara, "A w-band wavelet generator using 0.13-μm inp hemts for multi-gigabit communications based on ultra-wideband impulse radio," in *Microwave Symposium Digest, 2008 IEEE MTT-S International*, june 2008, pp. 109 –112.

[20] D. Wentzloff, F. Lee, D. Daly, M. Bhardwaj, P. Mercier, and A. Chandrakasan, "Energy efficient pulsed-uwb cmos circuits and systems," Sept. 2007, pp. 282–287.

[21] N. Kamegai, S. Kishimoto, K. Maezawa, T. Mizutani, H. Andoh, K. Akamatsu, and H. Nakata, "Ultrashort pulse generators using resonant tunneling diodes and their integration with antennas on ceramic substrates," *Japanese Journal of Applied Physics*, vol. 47, no. 4, pp. 2833–2837, 2008.

[22] M. Devulder, N. Deparis, I. Telliez, S. Pruvost, N. Rolland, F. Danneville, and P. Rolland, "60 ghz uwb transmitter for use in wlan communication," *Signals, Systems and Electronics, 2007. ISSSE '07. International Symposium on*, pp. 371–374, 30 2007-Aug. 2 2007.

[23] A. Siligaris, N. Deparis, R. Pilard, D. Gloria, C. Loyez, N. Rolland, L. Dussopt, J. Lanteri, R. Beck, and P. Vincent, "A 60 ghz uwb impulse radio transmitter with integrated antenna in cmos65nm soi technology," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2011 IEEE 11th Topical Meeting on*, jan. 2011, pp. 153 –156.

[24] T.-A. Phan, J. Lee, V. Krizhanovskii, S.-K. Han, and S.-G. Lee, "A 18-pj/pulse ook cmos transmitter for multiband uwb impulse radio," *Microwave and Wireless Components Letters, IEEE*, vol. 17, no. 9, pp. 688–690, Sept. 2007.

[25] D. Barras, F. Ellinger, H. Jackel, and W. Hirt, "Low-power ultra-wideband wavelets generator with fast start-up circuit," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 5, pp. 2138–2145, May 2006.

[26] N. Deparis, A. Siligarisy, P. Vincent, and N. Rolland, "A 2 pj/bit pulsed ilo uwb transmitter at 60 ghz in 65-nm cmos-soi," in *Ultra-Wideband, 2009. ICUWB 2009. IEEE International Conference on*, sept. 2009, pp. 113 –117.

[27] M. Reddy, S. Martin, A. Molnar, R. Muller, R. Smith, P. Siegel, M. Mondry, M. Rodwell, H. Kroemer, and J. Allen, S.J., "Monolithic schottky-collector resonant tunnel diode oscillator arrays to 650 ghz," *Electron Device Letters, IEEE*, vol. 18, no. 5, pp. 218–221, May 1997.

[28] A. Seabaugh, X. Deng, T. Blake, B. Brar, T. Broekaert, R. Lake, F. Morris, and G. Frazier, "Transistors and tunnel diodes for analog/mixed-signal circuits and embedded memory," in *Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International*, Dec 1998, pp. 429–432.

[29] T. Broekaert, B. Brar, J. van der Wagt, A. Seabaugh, F. Morris, T. Moise, E. Beam, and G. Frazier, "A monolithic 4-bit 2-gsps resonant tunneling analog-to-digital converter," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 9, pp. 1342–1349, Sep 1998.

[30] H. De Los Santos, K. Chui, D. Chow, and H. Dunlap, "An efficient hbt/rtd oscillator for wireless applications," *Microwave and Wireless Components Letters, IEEE*, vol. 11, no. 5, pp. 193–195, May 2001.

[31] U. Auer, W. Prost, G. Janssen, M. Agethen, R. Reuter, and F. Tegude, "A novel 3-d integrated hfet/rtd frequency multiplier," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 2, no. 3, pp. 650–654, Sep 1996.

[32] J. H. Davies, *The physics of low-dimensional semiconductors*. Cambridge: Cambride university press, 1998.

[33] H. Mizuta and T. Tanoue, *The physics and applications of resonant tunnelling diodes*. Cambridge: Cambride university press, 1995.

[34] E. Lind, *Tunneling based electronic devices*. Lund: Doctoral Thesis, 2004.

[35] E. Lind, L.-E. Wernersson, I. Pietzonka, and W. Seifert, "Realization of a resonant tunneling permeable base transistor with optimized overgrown gaas interfaces," *Electron Devices, IEEE Transactions on*, vol. 49, no. 6, pp. 1066–1069, Jun 2002.

[36] Q. Liu, A. Seabaugh, P. Chahal, and F. Morris, "Unified ac model for the resonant tunneling diode," *Electron Devices, IEEE Transactions on*, vol. 51, no. 5, pp. 653 – 657, may 2004.

[37] K. Maezawa and T. Mizutani, "A new resonant tunneling logic gate employing monostable-bistable transition," *Japanese Journal of Applied Physics*, vol. 32, no. Part 2, No. 1A/B, pp. L42–L44, 1993.

[38] J. Stock, J. Malindretos, K. Indlekofer, M. Pottgens, A. Forster, and H. Luth, "A vertical resonant tunneling transistor for application in digital logic circuits," *Electron Devices, IEEE Transactions on*, vol. 48, no. 6, pp. 1028 –1032, jun 2001.

[39] M. Feiginov, C. Sydlo, O. Cojocari, and P. Meissner, "Resonant-tunnelling-diode oscillators operating at frequencies above 1.1 thz," *Applied Physics Letters*, vol. 99, no. 23, p. 233506, 2011.

[40] E. R. Brown, J. R. Soderstrom, C. D. Parker, L. J. Mahoney, K. M. Molvar, and T. C. McGill, "Oscillations up to 712 ghz in inas/alsb resonant-tunneling diodes," *Applied Physics Letters*, vol. 58, no. 20, pp. 2291–2293, 1991.

[41] International technology roadmap for semiconductors. [Online]. Available: http://public.itrs.net

[42] M. Chu, Y. Sun, U. Aghoram, and S. E. Thompson, "Strain: A solution for higher carrier mobility in nanoscale mosfets," *Annual Review of Materials Research*, vol. 39, no. 1, pp. 203–229, 2009.

[43] M. Frank, "High-k / metal gate innovations enabling continued cmos scaling," in *Solid-State Device Research Conference (ESSDERC), 2011 Proceedings of the European*, sept. 2011, pp. 25 –33.

[44] T. J. K. Liu and L. Chang, *Into the nano era, transistor scaling to the limit*. Berlin: Springer, 2009.

[45] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, dec. 2011, pp. 1.1.1 –1.1.6.

[46] K. Kuhn, M. Liu, and H. Kennel, "Technology options for 22nm and beyond," in *Junction Technology (IWJT), 2010 International Workshop on*, may 2010, pp. 1 –6.

[47] M. Rodwell, U. Singisetti, M. Wistey, G. Burek, A. Carter, A. Baraskar, J. Law, B. Thibeault, E. J. Kim, B. Shin, Y. ju Lee, S. Steiger, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, E. Chagarov, A. Gossard, W. Frensley, A. Kummel, C. Palmstrom, P. McIntyre, T. Boykin, G. Klimek, and P. Asbeck, "Iii-v mosfets: Scaling

laws, scaling limits, fabrication processes," in *Indium Phosphide Related Materials (IPRM), 2010 International Conference on*, 31 2010-june 4 2010, pp. 1 –6.

[48] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon cmos devices beyond scaling," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 339 –361, july 2006.

[49] A. J. del Alamo, "Nanometre-scale electronics with iii-v compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, nov. 2011.

[50] B. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted tri-gate cmos transistors," *Electron Device Letters, IEEE*, vol. 24, no. 4, pp. 263 – 265, april 2003.

[51] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, "Electrostatics improvement in 3-d tri-gate over ultra-thin body planar ingaas quantum well field effect transistors with high-k gate dielectric and scaled gate-to-drain/gate-to-source separation," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, dec. 2011, pp. 33.1.1 –33.1.4.

[52] S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller, L. Gignac, S. Mittal, J. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. Frank, and J. Sleight, "High performance and highly uniform gate-all-around silicon nanowire mosfets with wire size dependent scaling," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, dec. 2009, pp. 1 –4.

[53] M. Passlack, "off-state current limits of narrow bandgap mosfets," *Electron Devices, IEEE Transactions on*, vol. 53, no. 11, pp. 2773 –2778, nov. 2006.

[54] T.-W. Kim, D.-H. Kim, and J. del Alamo, "60 nm self-aligned-gate ingaas hemts with record high-frequency characteristics," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, dec. 2010, pp. 30.7.1 –30.7.4.

[55] G. Doornbos and M. Passlack, "Benchmarking of iii-v n-mosfet maturity and feasibility for future cmos," *Electron Device Letters, IEEE*, vol. 31, no. 10, pp. 1110 –1112, oct. 2010.

[56] A. Khakifirooz and D. Antoniadis, "Mosfet performance scaling;part ii: Future directions," *Electron Devices, IEEE Transactions on*, vol. 55, no. 6, pp. 1401 –1408, june 2008.

[57] J. J. Gu, Y. Q. Wu, and P. D. Ye, "Effects of gate-last and gate-first process on deep submicron inversion-mode ingaas n-channel metal-oxide-semiconductor field effect transistors," *Journal of Applied Physics*, vol. 109, no. 5, p. 053709, 2011.

[58] A. Alian, G. Brammertz, N. Waldron, C. Merckling, G. Hellings, H. Lin, W. Wang, M. Meuris, E. Simoen, K. D. Meyer, and M. Heyns, "Silicon and selenium implantation and activation in in0.53ga0.47as under low thermal budget conditions," *Microelectronic Engineering*, vol. 88, no. 2, pp. 155 – 158, 2011.

[59] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. Hudait, J. Fastenau, J. Kavalieros, W. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-k gate dielectric for high-performance short-channel in0.7ga0.3as quantum well field effect transistors on silicon substrate for low power logic applications," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, dec. 2009, pp. 1 –4.

[60] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, "Border traps in al_2o_3/$in_{0.53}ga_{0.47}as$ (100) gate stacks and their passivation by hydrogen anneals," *Applied Physics Letters*, vol. 96, no. 1, p. 012906, 2010.

[61] N. Waldron, D.-H. Kim, and J. del Alamo, "A self-aligned ingaas hemt architecture for logic applications," *Electron Devices, IEEE Transactions on*, vol. 57, no. 1, pp. 297 –304, jan. 2010.

[62] A. Baraskar, V. Jain, M. Wistey, U. Singisetti, Y. J. Lee, B. Thibeault, A. Gossard, and M. Rodwell, "High doping effects on in-situ ohmic contacts to n-inas," in *Indium Phosphide Related Materials (IPRM), 2010 International Conference on*, 31 2010-june 4 2010, pp. 1 –4.

[63] J. K. W. Yang and K. K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," vol. 25, no. 6. AVS, 2007, pp. 2025–2029.

[64] R. Matz, H. Heinecke, B. Baur, R. Primig, and C. Cremer, "Facet growth in selective area epitaxy of inp by mombe," *Journal of Crystal Growth*, vol. 127, no. 1-4, pp. 230 – 236, 1993.

[65] D.-H. Kim and J. del Alamo, "30 nm e-mode inas phemts for thz and future logic applications," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, dec. 2008, pp. 1 –4.

[66] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, H. S. Plis, E. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature*, vol. 468, no. 7321, pp. 286–289, nov. 2010.

[67] Y. Wu, R. Wang, T. Shen, J. Gu, and P. Ye, "First experimental demonstration of 100 nm inversion-mode ingaas finfet through damage-free sidewall etching," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, dec. 2009, pp. 1 –4.

[68] C. Thelander, L. Froberg, C. Rehnstedt, L. Samuelson, and L.-E. Wernersson, "Vertical enhancement-mode inas nanowire field-effect transistor with 50-nm wrap gate," *Electron Device Letters, IEEE*, vol. 29, no. 3, pp. 206 –208, march 2008.

[69] R. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W. Loh, J. Oh, C. Smith, P. Kirsch, P. Majhi, and R. Jammy, "Self-aligned iii-v mosfets heterointegrated on a 200 mm si substrate using an industry standard process flow," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, dec. 2010, pp. 6.2.1 –6.2.4.

[70] U. Singisetti, M. Wistey, G. Burek, A. Baraskar, B. Thibeault, A. Gossard, M. Rodwell, B. Shin, E. Kim, P. McIntyre, B. Yu, Y. Yuan, D. Wang, Y. Taur, P. Asbeck, and Y.-J. Lee, "Channel mosfets with self-aligned inas source/drain formed by mee regrowth," *Electron Device Letters, IEEE*, vol. 30, no. 11, pp. 1128 –1130, nov. 2009.

[71] L.-E. Wernersson, C. Thelander, E. Lind, and L. Samuelson, "Iii-v nanowires-extending a narrowing road," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2047 –2060, dec. 2010.

[72] E. Lind and L.-E. Wernersson, "Design of rf properties for vertical nanowire mosfets," *Nanotechnology, IEEE Transactions on*, vol. 10, no. 4, pp. 668 –673, july 2011.

[73] I. Kwon, M. Je, K. Lee, and H. Shin, "A simple and analytical parameter-extraction method of a microwave mosfet," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, no. 6, pp. 1503 –1509, jun 2002.

[74] M. Isler and K. Schunemann, "Impact-ionization effects on the high-frequency behavior of hfets," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 3, pp. 858 – 863, march 2004.

[75] F. Heiman and G. Warfield, "The effects of oxide traps on the mos capacitance," *Electron Devices, IEEE Transactions on*, vol. 12, no. 4, pp. 167 – 178, apr 1965.

[76] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. McIntyre, P. Asbeck, M. Rodwell, and Y. Taur, "A distributed model for border traps in mos devices," *Electron Device Letters, IEEE*, vol. 32, no. 4, pp. 485 –487, april 2011.

[77] X. Sun, S. Cui, A. Alian, G. Brammertz, C. Merckling, D. Lin, and T. P. Ma, "Ac transconductance dispersion: A method to profile oxide traps in mosfets without body contact," *Electron Device Letters, IEEE*, vol. PP, no. 99, pp. 1 –3, 2012.

[78] A. Teranishi, K. Shizuno, S. Suzuki, M. Asada, H. Sugiyama, and H. Yokoyama, "Fundamental oscillation up to 1.08 thz in resonant tunneling diodes with high indium composition transit layers," in *Compound Semiconductor Week (CSW/IPRM), 2011 and 23rd International Conference on Indium Phosphide and Related Materials*, may 2011, pp. 1 –4.

[79] R. Tsu and L. Esaki, "Tunneling in a finite superlattice," *Applied Physics Letters*, vol. 22, no. 11, pp. 562–564, 1973.

[80] C. L. Chen, R. H. Mathews, L. J. Mahoney, S. D. Calawa, J. P. Sage, K. M. Molvar, C. D. Parker, P. A. Maki, and T. C. L. G. Sollner, "Resonant-tunneling-diode relaxation oscillator," *Solid-State Electronics*, vol. 44, no. 10, pp. 1853 – 1856, 2000.

[81] E. R. Brown, C. D. Parker, S. Verghese, M. W. Geis, and J. F. Harvey, "Resonant-tunneling transmission-line relaxation oscillator," *Applied Physics Letters*, vol. 70, no. 21, pp. 2787–2789, 1997.

[82] H. De Los Santos, K. Chui, D. Chow, and H. Dunlap, "An efficient hbt/rtd oscillator for wireless applications," *Microwave and Wireless Components Letters, IEEE*, vol. 11, no. 5, pp. 193–195, May 2001.

[83] N. Nguyen and R. Meyer, "Start-up and frequency stability in high-frequency oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 27, no. 5, pp. 810–820, May 1992.

[84] A. Seabaugh, Y.-C. Kao, and H.-T. Yuan, "Nine-state resonant tunneling diode memory," *Electron Device Letters, IEEE*, vol. 13, no. 9, pp. 479–481, Sep 1992.

[85] C. Kidner, I. Mehdi, J. East, and G. Haddad, "Power and stability limitations of resonant tunneling diodes," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 38, no. 7, pp. 864–872, Jul 1990.

[86] W. F. Chow, *Principles of tunnel diode circuits*. New York: Wiley, 1964.

[87] F. Verhulst, *Nonlinear differential equations and dynamical systems*. Berlin: Springer Verlag, 2000.

[88] S. M. Sze, *Physics of semiconductor devices*. New York: Wiley, 1969.

[89] T. Yoshida, T. Deguchi, K. Kawaguchi, and A. Nakagawa, "Ka-band planar gunn oscillators using flip-chip gaas gunn diodes fabricated by boron ion implantation," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2000. 22nd Annual*, 2000, pp. 165 –168.

[90] N. Deparis, C. Loyez, N. Rolland, and P.-A. Rolland, "Uwb in millimeter wave band with pulsed ilo," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 4, pp. 339–343, April 2008.

[91] J. N. Schulman and T. C. McGill, "Complex band structure and superlattice electronic states," *Phys. Rev. B*, vol. 23, no. 8, pp. 4149–4155, Apr 1981.