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Receiver Front-Ends in CMOS with Ultra-Low Power Consumption

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LUND UNIVERSITY

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Abstract

Historically, research on radio communication has focused on improving range and data rate. In the last decade, however, there has been an increasing demand for low power and low cost radios that can provide connectivity with small devices around us. They should be able to offer basic connectivity with a power consumption low enough to function extended periods of time on a single battery charge, or even energy scavenged from the surroundings. This work is focused on the design of ultra-low power receiver front-ends intended for a receiver operating in the 2.4 GHz ISM band, having an active power consumption of 1 mW and chip area of 1 mm². Low power consumption and small size make it hard to achieve good sensitivity and tolerance to interference. This thesis starts with an introduction to the overall receiver specifications, low power radio and radio standards, front-end and LO generation architectures and building blocks, followed by the four included papers.

Paper I demonstrates an inductorless front-end operating at 915 MHz, including a frequency divider for quadrature LO generation. An LO generator operating at 2.14 GHz is shown in Paper II, enabling a front-end operating above 2 GHz. Papers III and IV contain circuits with combined front-end and LO generator operating at or above the full 2.45 GHz target frequency. They use VCO and frequency divider topologies that offer efficient operation and low quadrature error. An efficient passive-mixer design with improved suppression of interference, enables an LNA-less design in Paper IV capable of operating without a SAW-filter.

Populärvetenskaplig sammanfattning

I avhandlingen presenteras delar till radiomottagare med extremt låg effektförbrukning. Detta behövs då dagens samhälle blir allt mer och mer uppkopplat, och detta gäller inte bara persondatorer och mobiltelefoner. Med den snabba teknikutvecklingen inom radiokommunikation, driven av små och smarta mobiltelefoner, går det nu även att få prylar av alla de slag att tala med varandra. I förlängningen strävas det efter att i princip allting i ens omgivning ska kunna kommunicera trådlöst. Bland annat ska små givare kunna sättas lite överallt för insamling av data i så kallade sensornätverk. Till exempel kan de användas i smarta hus för att hålla reda på luftkvalitet och temperatur, och för att styra belysning och liknande. Sensornätverk kan också användas för att hålla reda på belastningar i en struktur vid t.ex. byggnadsarbeten. De kan även komma till användning på och även i kroppen. Det kan då handla om medicinska sensorer, som håller koll på din hälsa, och kontinuerligt vidarebefordrar informationen till en mobiltelefon eller kanske även till sjukvården. Redan idag har vi enkla trådlösa sensorer för att hålla reda på hjärtrytm och stegfrekvens vid sportutövning. Utvecklingen av effektsnåla trådlösa sensorer är dock ännu i sin linda. Några steg har redan tagits, med sport-sensorer och nya trådlösa standarder som Bluetooth Smart och ANT, men vi kommer nog att se vilken potential de har först när tekniken är bättre utvecklad.

Sensorerna behöver klara sig länge på en batteriladdning, vilket i vissa fall som med trådlösa möss och tangentbord, kan lösas med hjälp av relativt stora batterier. För att verkligen kunna sprida sensorer överallt måste de dock kunna göras mycket små och trots det ha en lång batteritid; i många fall kan det handla om flera år. För att klara av detta behövs nya radiokretsar och kommunikationsstandarder som är mycket bättre optimerade för låg effektförbrukning än dagens lösningar.

Avhandlingens syfte var att ta fram de analoga byggblocken i en extremt effektsnål radio. Delarna det handlar om sitter direkt vid antennen (front-end) och har som funktion att ta emot radiosignalen, förstärka den, och flytta ner den till en mycket lägre frekvens som kan hanteras av resten av radion. Den här delen av radion måste alltså hantera de högfrekventa radiosignalerna, och kretsarna måste därför vara snabba nog. Eftersom strömförbrukningen i en krets är i stort sett proportionell mot hastigheten är det svårt att bygga radiokretsar med mycket låg effektförbrukning, och i små trådlösa sensorer är det de analoga radiokretsarna som kräver mest ström. Därför är det mycket viktigt att de använder strömmen så effektivt som möjligt. Ytterligare ett problem vid konstruktionen av kretsar med låg strömförbrukning är att de har svårare att hantera stora signalstyrkor med låg distorsion (olinjäritet). Det innebär är att radion får svårare att klara av starka störsignaler. Mottagaren är tänkt att fungera i det licensfria 2.4GHz-bandet, som dessutom används av bland annat trådlösa hemnätverk (WiFi), Bluetooth-enheter och mikrovågsugnar. Alla dessa riskerar att störa ut en mottagare utan tillräcklig linjäritet.

Arbetet har utförts som en (i stort sett oberoende) del av ett större projekt med målet att utveckla alla delarna (analoga och digitala) av en radiomottagare med låg effekt. Målet har varit att kunna ta emot en signal i det öppna 2.4GHz-bandet med datahastighet på 250kbit/s, med en total strömförbrukning av 1mW, vilket är ett rätt så aggressivt mål. Ytterligare ett mål har varit att få in hela mottagarkedjan på ett $1 \times 1 \text{mm}^2$ chip. För att t.ex. kunna hantera kommunikation mellan två hörapparater eller andra enheter på olika delar av kroppen bör mottagaren dessutom ha god känslighet.

Avhandlingen har undersökt flera varianter av "front-end"-kretsar. Den första är konstruerad helt utan induktanser på chip för att den ska vara så fysiskt liten som möjligt (induktanser/spolar kan inte göras lika små på chip som andra komponenttyper). Den har en effektförbrukning på $280 \mu\text{W}$ och arbetar vid 915MHz. Nästa front-end klarar att arbeta vid 2.4GHz tack vare en ovanligt kompakt spole, och är dessutom mer komplett då den även innehåller en källa som genererar referenssignalen som behövs

för att stämma av mottagaren till en viss frekvens. Den sista front-end-kretsen lyckas kraftigt förbättra undertryckningen av störningar utan att nämnvärt höja effektförbrukningen. Undertryckningen av störningar är i nivå med mottagare som normalt brukar kräva minst tio gånger mer effekt.

Contents

Contents	vii
Preface	xi
Acknowledgments	xiii
List of Acronyms	xv
List of Symbols	xix
Introduction	1
1 Motivation	3
2 Ultra Portable Devices	5
2.1 UPD Sub-projects	5
2.2 UPD System Overview	7
2.2.1 Receiver Architecture	8
2.2.2 Modulation	9
2.2.3 Link Budget	10
2.2.4 MAC protocol	12
2.2.5 Handling of Interference	13
3 Low Power Radio	17
3.1 Network configurations	18

3.2	Low power radio standards	19
3.2.1	Bluetooth	19
3.2.2	Zigbee	19
3.2.3	Ant	20
4	Receiver Front-end	21
4.1	Architecture	21
4.1.1	Hetrodyne	21
4.1.2	Homodyne/Direct conversion	22
4.2	LO Generation	23
4.2.1	Quadrature generator	23
4.2.2	PLL	25
4.3	Building Blocks and Components	26
4.3.1	LNA	26
4.3.2	MIXER	33
4.3.3	Oscillator	36
4.3.4	Frequency divider	39
4.3.5	Inductors	40
4.4	Low Power Front-end Design	44
4.4.1	Survey of Low Power Front-ends	44
4.4.2	Summary, Paper I	45
4.4.3	Summary, Paper II	46
4.4.4	Summary, Paper III	47
4.4.5	Summary, Paper IV	48
4.4.6	Performance summary	50
	Bibliography	53

I A 65nm CMOS 282μW 915MHz Direct Conversion Receiver Front-end	59
II A 65-nm CMOS 250uW Quadrature LO Generation Circuit	67
III A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS	75
IV A 0.55mW SAW-less Receiver Front-end for Bluetooth Low Energy Applications	83

Preface

The first part of this thesis consists of an introduction and gives a general overview of the field of study. The main scientific contribution is in the papers attached at the end, and consists of:

- [1] C. Bryant and H. Sjöland, "A 65nm CMOS 282 μ W 915MHz Direct Conversion Receiver Front-end," *Proceedings of the European Solid State Circuits Conference (ESSCIRC), 2011*, pp. 547–550, 2011.
- [2] C. Bryant and H. Sjöland, "A 65-nm CMOS 250uW Quadrature LO Generation Circuit," *International Microwave Symposium Digest (MTT), 2012 IEEE MTT-S, 2012 IEEE, 2012*.
- [3] C. Bryant and H. Sjöland, "A 2.45GHz Ultra-low Power Quadrature Frontend in 65nm CMOS," *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE, pp. 247–250, 2012*.
- [4] C. Bryant and H. Sjöland., "A 0.55mW SAW-Less Receiver Front-end for Bluetooth Low Energy Applications," *IEEE J. Solid-State Circuits [Submitted]*.

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In addition to the papers included as part of the dissertation, I have authored or co-authored the following works:

- [5] K.-K. Lee, C. Bryant, M. Törmänen, and H. Sjöland, "A 65-nm CMOS Ultralow-power LC Quadrature VCO," *NORCHIP, 2009*, pp. 1–4, 2009.
- [6] H. Sjöland, C. Bryant, V. Bassoo, and M. Faulkner, "Switched mode transmitter architectures," in *Analog Circuit Design*, pp. 325–342, Springer, 2010.
- [7] C. Bryant and H. Sjöland, "A 175 μ W 100MHz-2GHz Inductorless Receiver Frontend in 65nm CMOS," in *NORCHIP, 2010*, pp. 1–4, Nov. 2010.
- [8] K. K. Lee, C. Bryant, M. Törmänen, and H. Sjöland, "Design and Analysis of an Ultra-low-power LC Quadrature VCO," *Analog Integrated Circuits and Signal Processing*, vol. 67, no. 1, pp. 49–60, 2011.
- [9] J. Lindstrand, C. Bryant, M. Törmänen, and H. Sjöland, "A 1.6-2.6GHz 29dBm Injection-locked Power Amplifier with 64% peak PAE in 65nm CMOS," in *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pp. 299–302, 2011.
- [10] H. Sjöland, J. B. Anderson, C. Bryant, R. Chandra, O. Edfors, A. J. Johansson, N. S. Mazloum, R. Meraji, P. Nilsson, D. Radjen, et al., "A Receiver Architecture for Devices in Wireless Body Area Networks," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 2, no. 1, pp. 82–95, 2012.
- [11] C. Bryant, J. Lindstrand, H. Sjöland, and M. Törmänen, "A 70 and 210 GHz LO Generator in 65nm CMOS," in *Radio-Frequency Integration Technology (RFIT), 2012 IEEE International Symposium on*, pp. 195–197, 2012.

Patents & patent applications

- [12] C. Bryant, "Pulse-width modulator methods and apparatus," July 2010. US Patent 7,760,041.
- [13] C. Bryant, "Pulse-elimination pulse-width modulation," Jan. 2011. US Patent 7,863,956.
- [14] C. Bryant, "Quadrature pulse-width modulation methods and apparatus," May 2012. US Patent 8,179,957
- [15] J. Lindstrand, C. Bryant, and H. Sjöland, "High efficiency power amplifier," Feb. 2013, US Patent application 2013/0033,321.

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Lastly, I would like to thank my mother and father who are always there.

It is very hard to acknowledge everyone who have been important to me in my time here, so perhaps I should try a different approach:

To whom it may concern:

Thanks!

List of Acronyms

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BAN	Body Area Network
BB	Baseband
BER	Bit Error Rate
BFSK	Binary Frequency Shift Keying
BLE	Bluetooth Low Energy
BT	Bluetooth
BW	Bandwidth
CG	Common Gate
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
$\Delta\Sigma$	Delta Sigma
ESD	Electro-Static Discharge
F	Noise Factor

FET	Field Effect Transistor
FOM	Figure of Merit
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GPS	Global Positioning System
IC	Integrated Circuit
ICP _{1dB}	Input referred 1dB Compression Point
IF	Intermediate Frequency
IIP ₂	Input referred Second-Order Intercept Point
IIP ₃	Input referred Third-Order Intercept Point
IL	Insertion Loss
IM	Intermodulation
IM ₂	Second order intermodulation
IRR	Image Rejection Ratio
ISM	Industrial Scientific Medical
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LO	Local Oscillator
MAC	Media Access Control
MOS	Metal Oxide Semiconductor
NF	Noise Figure
NMOS	N-channel Metal Oxide Semiconductor
NR	Noise Ratio
OFDM	Orthogonal Frequency-Division Multiplexing
OOK	On-Off Keying
P2P	Point-to-Point
PAR	Peak-to-Average Ratio
PCB	Printed Circuit Board
PhD	Doctor of Philosophy
PLL	Phase Locked Loop
PMOS	P-channel Metal Oxide Semiconductor

PN	Phase Noise
PVT	Process, Voltage, Temperature
SAW	Surface Acoustic Wave
SNR	Signal to Noise Ratio
SRF	Self Resonance Frequency
Q	Quality factor
QAM	Quadrature Amplitude Modulation
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
VCO	Voltage Controlled Oscillator
V_{DD}	Supply Voltage
WUR	Wake-up Receiver
WSN	Wireless Sensor Network
XO	Crystal Oscillator

List of Symbols

C_{gs}	Gate to source parasitic capacitance
$\Delta\omega$	Offset angular frequency
E_b	Energy per bit
F_{min}	Minimum achievable noise factor
NF_{min}	Minimum achievable noise figure
f_{LO}	Local oscillator frequency
f_{RF}	Radio frequency
f_T	Transition frequency
g_m	Transconductance
i_n	Noise current
k	Boltzmann's constant
$\mathcal{L}(\Delta\omega)$	Phase noise at certain offset frequency
N_0	Noise power density
P_{int}	Power of interferer
PN_{1MHz}	Relative phase noise at 1 MHz offset
R_S	Source resistance
T	Temperature
Z_{in}	Input impedance
ω_0	Resonance angular frequency

Introduction

1

Motivation

With the advent of widespread computer networks, both wired and wireless, the world is becoming ever more connected. It is now possible to access services and information from pretty much anywhere in the world using a smartphone small enough to be held in one hand. The next step in the wireless revolution, the connection of all the things around us to the wider world, popularly referred to as the Internet of Things, has only just taken its first tentative steps. Currently we have low power wireless connectivity with a few select items, such as Bluetooth headsets, keyboards, game controllers, heart rate monitors, etc. While not really a true internet of things, the radios in such devices need to solve the same basic problem of providing basic connectivity at all times, while consuming hardly any power at all. My home keyboard, for example, is rated to last three years on a couple of AA batteries. This is all well and good, but in order to put wireless connectivity just about everywhere, we need devices that can operate at least that time on a single button cell battery, or even energy scavenged from the surroundings.

To achieve this level of portability we need transceivers capable of operating with minimal power consumption. One of, if not the main power consumer in such a device, is the RF front-end. Having to operate at high frequencies compared to the baseband circuits, the RF circuits need to draw a comparatively high current just to function properly. Thus, we need efficient circuit designs that use every drop of current exactly where it is needed, and where as few parts as possible operate at radio frequencies. To enable placement of such devices all around us, they should be as cheap as possible. For this purpose it is advantageous to produce such a device in a CMOS process. CMOS technology is used primarily for digital circuits such as processors, but since the unit cost is low when manufactured on a large scale, its use for analog circuits has also become common. Although initially too slow to make it particularly

suitable for the implementation of radio circuits, CMOS technology has undergone a remarkable scaling over the past decades. With Moore's "Law" predicting a doubling of transistors in integrated circuits approximately every two years, the devices are now so small that more than a billion of them can be fitted into a high performance CPU. As the feature sizes have shrunk, the intrinsic speed has increased to the point where CMOS is suitable for high performance RF circuits. With the advanced processes available today, CMOS has become so fast that we can afford to trade away some of that speed for increased efficiency, and in turn open up the opportunity to operate RF circuits at very low power.

This thesis focuses on the design of receiver front-ends with ultra-low power consumption, implemented in CMOS. Different circuits have been designed exploring different performance metrics, as well as incrementally advancing overall performance. The first front-end presented in this thesis explores a fully inductorless implementation at a lower operating frequency. It was early determined that LO generation circuits had to be included to give a fair representation of the overall performance under realistic circumstances, so the next circuit is a basic LO-generation circuit, demonstrating low power operation at above 2 GHz. The next circuit is a front-end operating at the full 2.45 GHz target frequency, together with an integrated LO-generation circuit. It departs slightly from the previous inductorless approach, demonstrating improved performance with a highly compact inductor. This circuit essentially fulfills the initial design targets. The front-end after that demonstrates operation without the LNA, and greatly improves tolerance to interference for slight increases in size and power consumption.

This work is not intended as a text book on the design of low power front-ends. To put the work into perspective, however, the following chapters provide an introduction to the project as well as some background information on receiver front-ends, the necessary building blocks, and issues faced in their design.

2

Ultra Portable Devices

This research has been conducted within the wider project “Wireless Communication for Ultra Portable Devices”, UPD in short, funded by SSF — Swedish Foundation for Strategic Research. The goal of this project is to build a radio receiver for operation in ultra-low power devices, such as sensor nodes or medical devices or similar. Some project targets are shown in Table 2.1. Apart from a small chip area, the receiver should have as few external components as possible to further aid portability.

Table 2.1: Project targets

Active power consumption	1 mW
Data rate	250kbps
Operating frequency	2.45 GHz
Chip area	1 mm ²

The project is divided into six sub-projects with one PhD student in each. Although each person has primarily been responsible for one part, there has been common work to study overall receiver and system functionality, such as finding more detailed specifications. An overview of the proposed system can be found in a joint journal paper from 2012 [10].

2.1 UPD SUB-PROJECTS

Antenna design/Channel modeling, Rohit Chandra

Small, compact antennas have been investigated combined with channel modeling of primarily on-body communication, such as ear-to-ear communication between hearing aids. The information obtained has

been taken into account in the overall system design specifications, so that it will function even in some of the tougher use cases of on-body communication.

Front-end, Carl Bryant

The sub-project described in this dissertation. The basic function of the front-end is to receive a weak RF signal from the antenna, amplify it and shift it to a much lower frequency range where it can be more easily processed. It is in the front-end and associated local oscillator (LO) signal generation we encounter the highest frequency circuits, since they have to operate at the full frequency of the incoming radio signal. Fast circuits generally have high power consumption, and so the majority of our power budget will be needed by the RF circuits. As the first active part of the receiver chain the performance of the front-end is what ultimately limits the overall sensitivity and tolerance to interference. Thus we need carefully optimized circuits that makes use of every bit of power it draws, and without too large sacrifices in performance.

Analog to digital converters, Dejan Radjen

The goal is to design an analog to digital converter (ADC) with sufficient dynamic range so that the receiver may operate without automatic gain control, while still maintaining small size and low power consumption. Continuous time Delta Sigma ($\Delta\Sigma$) converters are considered to be a suitable architecture. The advantage of $\Delta\Sigma$ converters is that it can use a low resolution quantizer, trading speed for resolution, advantageous with the high inherent speed of advanced CMOS processes available also at low power. The main advantage of the continuous time $\Delta\Sigma$ is that the loop filter, implemented in the analog domain, also functions as an anti-aliasing filter, relaxing the filtering requirements before the ADC.

Digital baseband, Yasser Sherazi

The digital baseband includes decimation and sharp channel filtering, as well as synchronization and demodulation. While coarse filtering is performed in the analog domain early in the signal chain, digital filters allow a much sharper cutoff. This subproject is concerned with finding optimized structures and efficient implementations. One of the fundamental trade-offs in digital circuitry implemented in an advanced CMOS node is speed versus leakage current. Techniques that trade these include series versus parallel logic, use of multiple thresholds, bulk biasing, etc.

Analog Decoder, Reza Meraji

In situations with poor signal transfer, error correcting codes can trade data rate for fidelity by adding redundancy to the data. Traditionally the decoding of such signals is performed in the digital domain. The decoder circuits can be fairly complex and it is believed that performing the computations in the analog domain may actually be faster and more power efficient, possibly by orders of magnitude [16]. An example of an operation that may be more efficient in the analog domain is multiplication. In the digital domain it is costly, while in the analog domain a multiplication can be performed using only a handful of devices. The main issues with analog computations are the susceptibility to noise and particularly device mismatch. Although both can be mitigated by making the devices large enough, this will make the circuits slower and also a large physical size may be an issue when used in a device meant to be compact and very cheap to manufacture. Methods of mitigating the effect of mismatch other than increasing the device size should therefore be sought. To test the viability of analog decoders, they should be compared to equivalent digital implementations. The results to date are very promising with an analog decoder substantially outperforming its digital counterpart in simulations, both in terms of power consumption and size [17].

System Control, Nafiseh Mazloun

The system control concerns the proper and efficient operation of the receiver in different situations. In practice this to a large extent involves the study and design of the media access control (MAC) protocol for a low power sensor network. The MAC describes the fundamental operations performed to establish a link and transfer data. How this is performed can be just as important to achieving low power operation as the circuits themselves. We expect the data requirements for the target applications to be small and infrequent. If the radio circuits can be powered down when there is no data the average power consumption can then be reduced substantially, but this has to be performed without incurring an unacceptable latency. The work done in this area has shown the potential power savings that can be achieved by introducing a separate ultra-low power wake-up receiver. This is discussed further in section 2.2.4.

2.2 UPD SYSTEM OVERVIEW

To get a better understanding of how the front-end is intended to function together with its surroundings, we should look at the system as a whole,

i.e. the front-end together with the rest of the receiver chain. In a paper from 2012 the intended architecture of the Ultra Portable Devices receiver is presented together with an analysis of some of the basic specifications [10]. In this case we have assumed an application of communication between two hearing aids. When using hearing aids for both ears simultaneously, they need to keep synchronized for best performance. This is one of the tougher examples of on-body communication since radio energy is quickly absorbed by the body and the radio waves thus have to propagate around the head.

The receiver is intended to operate in the 2.4 GHz ISM (Industrial, Scientific, Medical) band (2400-2483 MHz). Lower frequencies require larger antennas for efficient radiation, while losses tend to increase with higher frequencies. The 2.4 GHz band is deemed to offer a fair trade-off, but more importantly the ISM-band provides 80 MHz of unlicensed bandwidth. Additionally it is adjacent to a band recently approved for medical body area networks at 2360-2400 MHz, of which the top 10 MHz requires no registration or coordination [18].

2.2.1 RECEIVER ARCHITECTURE

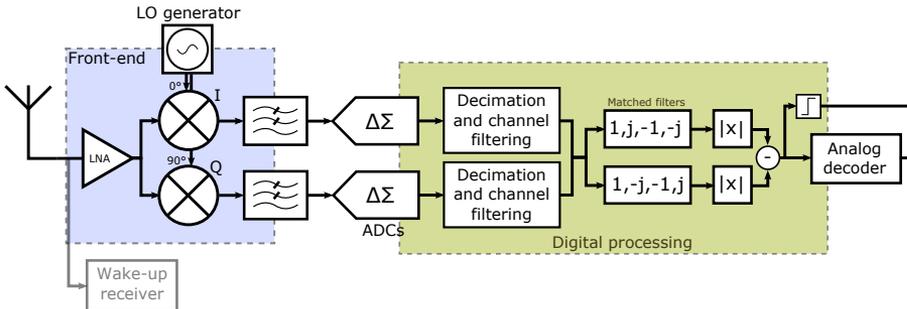


Figure 2.1: Proposed receiver structure

The proposed receiver architecture is shown in figure 2.1. It consists of a direct conversion front-end, ADCs and a digital demodulator. Coding may be used when the signal to noise ratio (SNR) is low. In this case an analog decoder is used since it is reckoned to be power efficient (See section 2.1). Although the analog decoder requires digital to analog converters (DAC) the resolution needed is low enough that they shouldn't require much power. At 100 μ W each it is reckoned that the ADCs can achieve more than 50 dB SNDR [10] which should give the receiver sufficient dynamic range (DR) to minimize the need for automatic gain control (AGC).

The 1 mW power budget is designated as follows: The synthesizer and

front-end should together draw $650\ \mu\text{W}$. The ADCs are each allocated $100\ \mu\text{W}$, the digital baseband $100\ \mu\text{W}$ and decoder $50\ \mu\text{W}$. The work on digital baseband and analog decoders indicates that the power required will be considerably less than this, so there is likely room to reallocate some of that power.

2.2.2 MODULATION

The system is intended to use wideband frequency shift keying (FSK) as it has several properties especially well suited for a low power transceiver. The modulation index is chosen such that the frequency deviation and data rates match ($250\ \text{kbit/s}$, $\pm 250\ \text{kHz}$). This results in a full 360° change of phase each symbol. The data is encoded in the direction of rotation, with an advancing phase encoding a "1" and a retreating phase a "0". Fig. 2.2 shows this phase rotation in the I/Q-plane. We see that as the signal spends an equal time at all phase positions, the I and Q signals contain no DC component. This is advantageous for a direct conversion receiver architecture, that can have problems with low frequency noise and DC-offsets. The signal also has a constant envelope (amplitude), i.e. a unity peak to average ratio (PAR). The transmitter thus doesn't need any additional headroom when transmitting at a certain power level. It is also suitable for use with a non-linear (often more efficient) power amplifier.

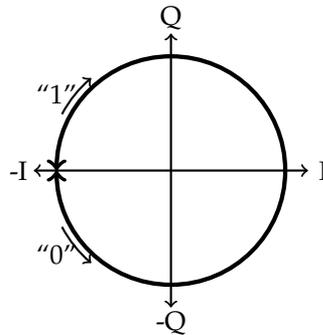


Figure 2.2: Path taken in I/Q diagram during transmission of one symbol. The direction of rotation determines the encoded bit.

The resulting power spectrum of a binary FSK (BFSK) signal with data rate of $250\ \text{kbit/s}$ and matching deviation of $\pm 250\ \text{kHz}$ is shown in figure 2.3. The notch in the centre is due to the absence of DC in the modulation.

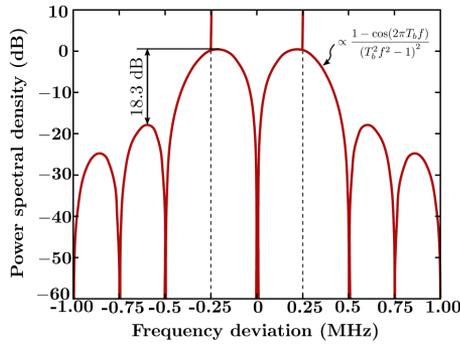


Figure 2.3: Ideal spectrum of wideband BFSK modulation with 250kbit/s and ± 250 kHz deviation.

This type of modulation is also easy to demodulate with a simple detector, a major advantage for a system like this, since simplicity usually translates to low power consumption. In this case the detection is performed by multiplying the complex input vector with a pair of matched filters. One filter uses the sequence “1, j, -1, -j” and the other “1, -j, -1, j”, representing a clockwise and counter-clockwise rotation in the complex plane. By comparing the output magnitudes of the filters we can determine if the data is most probably a “1” or “0”. Just as the modulation lacks DC, this detector will reject any DC content.

2.2.3 LINK BUDGET

As previously mentioned we have assumed hearing aid to hearing aid communication as a representative example of low power communication. Since there is no line of sight between the two nodes and they are separated by a highly lossy medium, we can get an idea of the worst case conditions that we should handle for a body area network (BAN) application.

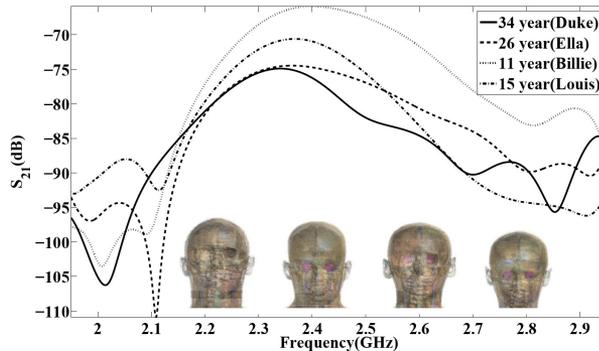


Figure 2.4: Ear-to-Ear Link Loss for different head phantoms

Simulations using four heterogeneous head phantoms based on real people [19], show that the worst case link loss in the 2.4 GHz band with in-the-ear antennas is -79 dB, as seen in Fig. 2.4 [20] [10].

The transmitter should also consume below 1 mW, and assuming it has an overall efficiency of 20%, it should be able to transmit 0.2 mW or -7 dBm. Assuming a SAW-filter with 3 dB (worst case) loss this becomes -10 dBm. This indicates that the receiver needs a sensitivity of $-10 - 79 = -89$ dBm. Uncoded the data rate is 250 kbps and we require a E_b/N_0 of 12 dB for 0.001 bit error rate (BER). To meet the required sensitivity we need an overall receiver noise figure of $-89 - 12 + 174 - 10 \cdot \log_{10}(250k) = 19$ dB. With the SAW-filter loss and assuming the front-end and ADC contribute equally to the noise figure, we achieve this with a front-end noise figure of 13 dB. If we can achieve a lower noise figure we will have a bit of margin. A front-end NF of 10 dB for instance gives a sensitivity of -92 dBm. There may still be situations when even more sensitivity is required to guarantee a viable connection, however, and with coding data rate can be sacrificed for sensitivity. With half the data rate the sensitivity can be increased by 5 dB. The filter is used to protect the receiver from interference, and to prevent the transmitter from emitting interference in other bands. Since linearity, and with it sensitivity to interference, is intimately connected to power consumption, it is one of the main trade-offs when designing a low power receiver. If, despite this, we can construct a receiver with sufficient robustness to not warrant a SAW-filter, the link budget is improved by 3 dB. If we can build such a receiver, it is probably not too hard to build a transmitter that doesn't require an external filter either, improving the situation by another 3 dB. The transmitted power is low, and so it does not need very high spectral purity to meet regulations on spurious emissions.

2.2.4 MAC PROTOCOL

Building a transceiver with very low power consumption is only part of the solution to providing radio connectivity with extremely low power consumption. For this we also need to make sure that the radio circuits are powered down as much as possible when there is no data to be transferred. In sensor networks and similar we expect the data to be rare and sporadic. This means that the receiver is effectively unused most of the time. The problem is that we do not know when another node has data to send, and thus the receiver needs to keep listening to its surroundings. The transceiver should thus be paired with an efficient protocol that can establish a link even while requiring the radio circuits to be turned on as little as possible. The main way of achieving this is to duty cycle the receiver, so that it wakes up at regular intervals to check for a signal. This moves some of the burden to the transmitter instead, as it has to provide a preamble/beacon alerting the receiver of the impending message, and this has to be long enough to ensure that the receiver will wake up at least once in this time period. Increasing the listening interval reduces the average receiver power consumption, but increases the time it takes until we can establish a connection with any certainty. Thus there is a trade-off between power consumption and latency. One of the more advanced MAC-protocols built on this principle is XMAC [21] [22]. In this protocol short pauses are inserted in the preamble, where the receiver has an opportunity to send an acknowledgment (ACK) once it has detected the preamble.

An alternative method to reduce power consumption is to use a secondary receiver that is used only for the purposes of waking up the main receiver. This secondary receiver would be of a simple construction and have even lower power consumption. A wake-up signal could for instance be modulated with on-off-keying (OOK), which could be detected with an envelope detector, a diode rectifier in its simplest implementation. A wake-up receiver is not without its problems, however. Firstly the sensitivity is generally quite poor. The best to date having a -72 dBm sensitivity at a raw data rate of 100kbps and power consumption of $52 \mu\text{W}$ while operating at 2 GHz [23]. Secondly this kind of circuit has poor frequency selectivity, making it sensitive to interference over a large bandwidth. Both of these could potentially be mitigated by transmitting long, known, coded wake-up messages. By correlating the received signal to the expected message, the chances of picking up the wake-up signal improves. Although we are trading data rate, the wake-up message should carry hardly any data, a recipient address at most.

The wake-up receiver holds on its own little advantage to the previously discussed receiver duty cycling, since there is a limit to how much less power the wake-up receiver can consume compared to the main receiver and still be functional. The wake-up receiver itself can, however, also be duty cycled [24].

2.2.5 HANDLING OF INTERFERENCE

DYNAMIC RANGE

Assuming a front-end NF of 10 dB we have a sensitivity of -92 dBm. With an E_b/N_0 of 12 dB, a data rate of 250 kbps and RF bandwidth of 1 MHz, the effective signal to noise ratio (SNR) before the ADCs is about 6 dB. If the ADCs have a full scale (differential) input amplitude of 200 mV it reaches an SNDR of 6 dB at approximately 1.3 mV, assuming a dynamic range of 50 dB. With -92 dBm equating to $7.94 \mu\text{V}$ over 50Ω , at least 44 dB voltage gain is required before the ADCs while at maximum sensitivity. In practice it looks like the ADCs will achieve more than 50 dB dynamic range, and so the gain required will likely be lower than this.

At 44 dB front-end gain and 50 dB dynamic range the ADCs saturate at an RF input power of $-92 + (50 - 6) = -48$ dBm in-channel. With a supply voltage of 0.8-0.9V the front-end baseband amplifiers can probably handle higher output signal amplitudes. Assuming they can handle a peak-to-peak amplitude 50% of a 0.8V supply, equating to a differential amplitude of 400 mV, the front-end saturates at an input power of -42 dBm in-channel. This equates to an IIP_3 of around -32 dBm assuming the well known 10 dB relation when compression is dominated by third order effects. Though there are ways of increasing this somewhat, including rail-to-rail amplifiers, it is ultimately constrained by our sensitivity specification and the dynamic range that can be achieved by an ADC in our power budget.

Outside the receive and neighboring channels the linearity is improved as the signal reaching the ADCs is attenuated by filtering in the front-end and anti-aliasing filters.

SECOND ORDER DISTORTION

The second order intermodulation distortion is a concern particularly for direct conversion receivers, as a single amplitude modulated signal anywhere in the band will cause low frequency IM_2 products at the mixer output. Operating in the 2.4 GHz band a common source of interference is from wireless local area networks (WLAN). The low bandwidth of our system compared to WLAN is beneficial in this case, as most distortion falls outside the receiver bandwidth. We have assumed a WiFi interferer with a power of P_{int} and a channel bandwidth of 20 MHz. The RF bandwidth is in this case 16 MHz. The resulting input referred IM_2 product can be estimated as (2.1) where $IL_{band-select}$ is the worst-case insertion loss of the band-select (SAW) filter.

$$IM_2 = 2 \cdot (P_{int} - IL_{band-select}) - IIP_2 \quad (2.1)$$

This energy will be distributed as follows; DC (50%), twice the carrier frequency (25%), and baseband (25%) [25]. The energy at baseband will be distributed from DC to the RF bandwidth of the signal, which in this case is 16 MHz. Since the energy at DC is rejected by the matched filters and the baseband has a bandwidth of 0.5 MHz, compared to the interfering signal bandwidth of 16 MHz, we can estimate the total IM_2 energy entering the receiver as (2.2), where -6 dB corresponds to the 25% energy at baseband, and -15 dB to the bandwidth ratio. With a data rate of 250kbit/s (no coding) an Eb/No of 12 dB is required. With an intermodulation power density of $P_{int-BB} - 10 \cdot \log(500k)$ the largest WiFi interferer with 3 dB loss of sensitivity can be estimated as (2.3), where +3 dB is an increase in effective Eb , since the energy comes from both sidebands.

$$P_{int-BB} = 2 \cdot (P_{int} - IL_{band-select}) - IIP_2 - 6dB - 15dB \quad (2.2)$$

$$P_{int} = IL_{band-select} + \frac{P_{sens} + IIP_2 + 21 - Eb/No + 3 + 10 \cdot \log(500k) - 10 \cdot \log(250k)}{2} \quad (2.3)$$

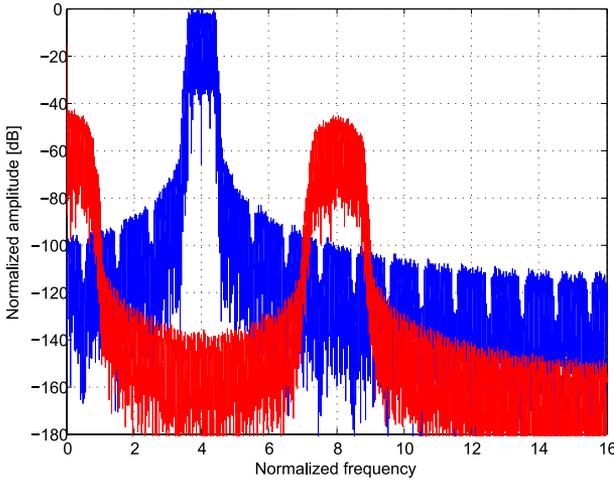


Figure 2.5: Simulated interfering WiFi signal and its IM_2 .

With a base sensitivity (P_{sens}) of -92 dBm and an IIP_2 of 0 dBm the maximum tolerable interferer is estimated to -35.5 dBm. However, it should be noted that the power spectral density of the intermodulation is not flat, and the intermodulation is strongest at low baseband frequencies. The above calculations are thus a bit optimistic. A more accurate estimate can be had from

a Matlab simulation. A 64QAM OFDM WiFi signal was generated and sent through a 2^{nd} order nonlinearity, and the resulting spectrum can be seen in figure 2.5. The signal is in blue and the IM_2 in red. Note that since the carrier frequency is not important it is reduced for improved visibility. The result is that we can tolerate a -37.5 dBm interferer, a degradation of 2 dB compared to the calculation.

SELECTIVITY

With sharp digital filters the selectivity performance in the adjacent channels is dominated by the phase noise superimposed on an interferer due to reciprocal mixing. The phase noise introduced through an interferer in an adjacent channel can be estimated by integrating the noise that spills over into the receiver channel. Assuming the phase noise power falls off at a $1/(\Delta f)^2$ slope (see section 4.3.3) the integrated phase noise can be estimated as (2.4), from the phase noise at 1 MHz offset. BW_{rcv} is the receiver bandwidth, in our case 1 MHz, within which the phase noise is approximated as flat.

$$P_{PN,rcv} = P_{int} \cdot PN_{1MHz} \cdot \left(\frac{1M}{\Delta f} \right)^2 \cdot BW_{rcv} \quad (2.4)$$

This is a fair approximation in most cases. For the adjacent channel, however, the receiver bandwidth is large compared to the distance to the interferer, and so assuming the phase noise to be flat in the receive channel is inaccurate. To find out how much difference it makes, we can integrate the phase noise (assuming a $1/(\Delta f)^2$ falloff), equation (2.5). We know the phase noise at 1 MHz which we can use to find N_0 by equation 2.6.

$$P_{PN_{1/f_2},rcv} = \int_{f_1}^{f_2} N_0 \frac{1}{f^2} df = N_0 \left(\frac{1}{f_1} - \frac{1}{f_2} \right) \quad (2.5)$$

$$N_0 \cdot \frac{1}{(1M)^2} = P_{int} \cdot PN_{1MHz} \quad (2.6)$$

$$\frac{P_{PN_{1/f_2},rcv}}{P_{PN,rcv}} = \frac{N_0 \left(\frac{1}{f_1} - \frac{1}{f_2} \right)}{N_0 \cdot \frac{1}{(1M)^2} (f_2 - f_1)} = \frac{(1M)^2}{f_1 \cdot f_2} \quad (2.7)$$

With $f_1=0.5$ MHz and $f_2=1.5$ MHz we find the flat noise approximation underestimates the integrated noise by 1.25 dB (2.7). For most estimates this is actually quite acceptable.

The oscillators built within this project have all had better than -106 dBc/Hz phase noise at 1 MHz offset. The receiver requires an effective SNR of 6 dB and has a base sensitivity of -92 dBm. From these numbers we estimate that for

a sensitivity degradation of 3 dB the receiver can tolerate an adjacent channel interferer about 35.5 dB stronger than the desired signal, and 42.5 dB in the second adjacent channel. This assumes an unmodulated interferer in the center of the channel, and may therefore in practice be slightly worse.

At larger offsets the tolerance to interference is instead dominated by other effects such as saturation of the ADC and compression of the front-end. In the absence of a SAW-filter the phase noise may also affect the tolerance to out-of-band interference, as the LO generator phase noise is white at large frequency offsets.

3

Low Power Radio

In the past a lot of research has gone into providing radio communication with increasing data rates, especially since the introduction of the smartphone. Lately, however, interest is increasing for providing connectivity with portable devices and sensors, that can be all around us. Such connectivity is sometimes referred to as the internet of things (IoT) [26]. Here, the challenge is, instead, to provide basic connectivity at very low power consumption. An example of the application of ultra-low power radio communication is wireless sensor networks (WSN). A wireless sensor network consists of small sensors combined with a radio transmitter/transceiver. They are used for monitoring, possibly over a wide area, usually reporting data back to a central controller. They could, for example, monitor temperature and air quality, or structural loading during construction work. Each node should be small and cheap, and should function extended periods of time on a battery charge. With low enough power consumption the energy used may be harvested from the surroundings, from sources such as heat, motion, radio interference, blood glucose, etc. Ideally the sensors should be cheap enough for one time use.

Similar to the WSN, a body area network (BAN) consists of devices worn on the body, or perhaps even implanted. A BAN may be used for health monitoring, perhaps detecting medical conditions early, or to help diagnose a condition that requires long term monitoring. Currently an early form of BAN exists in the form of sports sensors that connect to your phone or sports watch, and are used to monitor things like heart rate and activity. Some of these devices can also connect to stationary sports equipment such as a treadmill. Low power wireless devices may also, for example, be used in smart houses to, apart from monitoring purposes, control lights and other equipment. The full potential of low power radio will materialize as the technology matures.

3.1 NETWORK CONFIGURATIONS

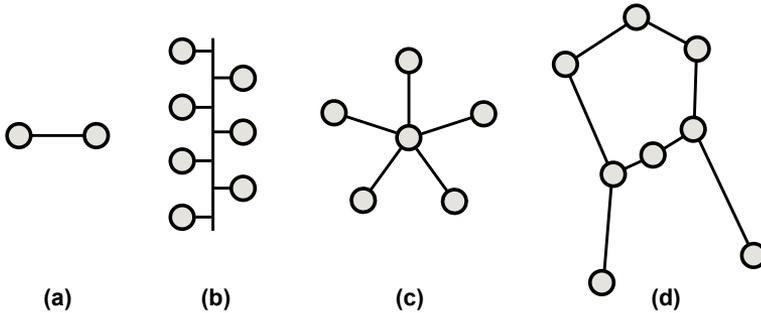


Figure 3.1: Network topologies (a) Point to point (b) Bus (c) Star (d) Mesh

A wireless network may be organized in a number of different ways. Figure 3.1 shows some of the basic network topologies. The simplest configuration is point-to-point (P2P) which is just a link set up between two devices.

In a bus topology all nodes have equal access to the rest of the network on the same frequency with no particular priority. Steps must be taken to avoid collisions when two nodes have data to communicate simultaneously, such as carrier sensing, where a node will only attempt to transmit if it detects that the channel is free.

In a star network, all devices are connected to a central node (hub), which handles all traffic on the network. Any data passed from one peripheral node to another has to be repeated by the hub. This configuration makes sense in a network combining low power sensor nodes with a single higher powered device. An example is peripheral devices such as a wireless headset or sports monitors connected to a mobile phone. The phone has a large battery compared to the connected devices and it is possible to let it provide the main part of the energy required to communicate. The hub, for instance, can keep the network synchronized by transmitting a beacon at regular intervals. It may also contain a more sensitive radio, allowing the other devices to transmit with less power.

Another network topology is the mesh. In a mesh messages may be relayed through several nodes, and there may be more than one path available. With the nodes collaborating, the network may cover larger distances and improve connectivity with nodes otherwise obscured by large objects.

3.2 LOW POWER RADIO STANDARDS

3.2.1 BLUETOOTH

Created by Ericsson in the late nineties, and now maintained by the Bluetooth special interest group (SIG), Bluetooth (BT) is a wireless standard intended for providing a short range connection to devices such as computers, phones, headsets, etc. Operating in the 2.4 GHz ISM band it is designed to be simple and cost effective. The original BT standard has a data rate of 1 MBit/s in a 1 MHz channel, using Gaussian frequency shift keying (GFSK) modulation. To reduce susceptibility to interference, BT employs frequency hopping, and will also actively avoid crowded channels [27].

Later revisions of the BT standard have added optional support for increased data rates by enabling more advanced modulation schemes, or by transferring large data payloads via a 802.11 (WiFi) link. Enhanced data rate (EDR) and high speed (HS) options increase the maximum data rate to 3 and 24 MBit/s, respectively.

With the recent introduction of BT v4.0 [28] support for a new low power communication protocol has been added, called Bluetooth Low Energy (BLE). It is not directly compatible with classic bluetooth, and a BT v4.0 device may implement either classic BT, BT low energy, or both. Support for BLE is also referred to as Bluetooth SMART, indicating a BLE only device, or Bluetooth SMART ready for a device implementing both protocols. Recently a number of smartphones have been released that are Bluetooth SMART ready.

Bluetooth low energy has a data rate of 1 Mbit/s with an average throughput of 270 kbit/s. It uses frequency hopping and GFSK modulation, similar to classic BT, but at a higher modulation index (0.5 instead of 0.35), which is easier to demodulate, but results in a larger signal bandwidth. It is configured in a star-bus hybrid network topology.

3.2.2 ZIGBEE

Zigbee is a standard from 2003, based on the 802.15.4 standard. It can operate in the 868 MHz (Europe), 915 MHz (North America) and 2.4 GHz ISM bands, and it supports a mesh network topology with up to 65536 nodes. The data rate varies from 20kbit/s in the 868 MHz band to 250 kbit/s in the 2.4 GHz band. Binary phase shift keying (BPSK) is used for lower data rates, and offset quadrature phase shift keying (OQPSK) for the highest data rate. To improve resistance to interference the signal is spread over a 5 MHz wide channel using direct sequence spread spectrum (DSSS) [29].

3.2.3 ANT

Launched in 2003, ANT is a proprietary protocol for communication with ultra low power devices, and optimized for communication with small payloads. The 2.4 GHz ISM band is used, divided into 1 MHz channels. It can be configured into a wide range of network topologies, including P2P, Star, Bus, Mesh, Broadcast, and hybrid solutions [30]. While communicating one node is designated as the master. The master node will transmit short eight bit payloads at regular intervals, which the slave nodes use to synchronize to the master. A slave may also transmit data to the master. One frequency channel may be divided up into several time-interleaved channels, and devices on different networks will adjust their timing to avoid collisions. The data rate is 1 Mbit/s with GFSK and the average throughput is 20 kbit/s.

4

Receiver Front-end

This chapter briefly describes the function of a receiver front-end as well as the components that it is constructed from, including some of the considerations required in the design of a low power receiver front-end. A short summary of the circuits described in the included papers is also given, together with a table comparing their performance.

4.1 ARCHITECTURE

4.1.1 HETRODYNE

The traditional way of building a receiver front-end is with the superhetrodyne structure, Fig. 4.1, invented by E. H. Armstrong in 1918. After coarse filtering, the RF signal is amplified by a first amplifier to strengthen the signal before further processing. At the heart of the hetrodyne receiver is a mixer, basically a multiplier, which is used to bring the signal down to a much lower intermediate frequency (f_{IF}). To do so the RF signal is multiplied with a reference signal from the local oscillator (LO), placed such that its frequency $f_{LO} = f_{RF} \pm f_{IF}$. Products of the multiplication will appear at various frequencies, among them the difference frequency f_{IF} . Two different input frequencies, $f_{RF} = f_{LO} \pm f_{IF}$, will yield the same output frequency. Since we are only interested in receiving one frequency at the time, anything at the other frequency (the image frequency) is attenuated by image rejection filtering prior to mixing. The bandwidth of a filter is generally proportional to the center frequency, and the sharp filtering for selectivity is thus performed at the IF frequency where it is much easier to build a narrow filter, allowing us to separate out just one channel.

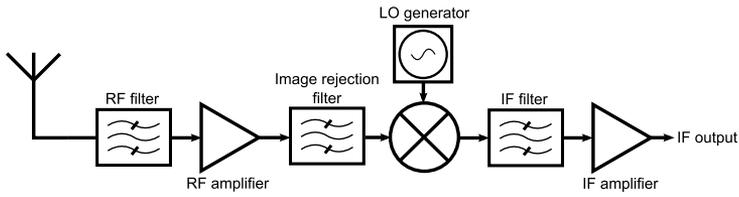


Figure 4.1: Superhetrodyne receiver

The super heterodyne architecture is effective and it has been used widely for a long time. The extensive filtering required is, however, a drawback when implementing it on-chip. On-chip components have considerable component variation and, especially inductors, generally have low quality (Q) values, rarely exceeding 20. This limits the filtering properties of the RF filters, and especially the image reject filter will be too poor, as the frequencies of the wanted signal and the image are very close to each other at RF. The IF filter is also an issue since the inductors required to build a passive filter at low frequency will be so large that they may not even fit on the chip. Though there are other ways of implementing an IF filter more suitable on chip, including active filters, it is not an ideal situation.

4.1.2 HOMODYNE/DIRECT CONVERSION

The direct conversion architecture is an attractive solution. The concept is fundamentally very similar to the heterodyne receiver, with the main difference that the IF frequency is zero (it is also referred to as a "zero IF" receiver). This is attractive for a couple of reasons. Firstly the image frequency does not pose any problem, since it coincides with the frequency of the wanted signal. This also means that twice as much of the wanted signal power enters the mixer, improving the SNR by 3 dB, effectively reducing the mixer noise figure. Secondly, the output signal is now at baseband. This means that the circuits after the mixer are operating at the lowest possible frequency, and can be implemented in a power efficient manner. Also the channel (IF) filter is now of a low-pass characteristic, and much easier to implement on-chip. The direct conversion receiver does require some additional circuitry to function properly, however. Since both the upper and lower sidebands of the RF signal are converted to the same output frequencies, we need additional measures to keep the information apart. This is achieved with a quadrature mixer, which is basically two separate mixers operated with LO signals 90° apart. This effectively treats the RF signal as two separate amplitude modulated carriers, sine and cosine, which according to Fourier theory are orthogonal to each other.

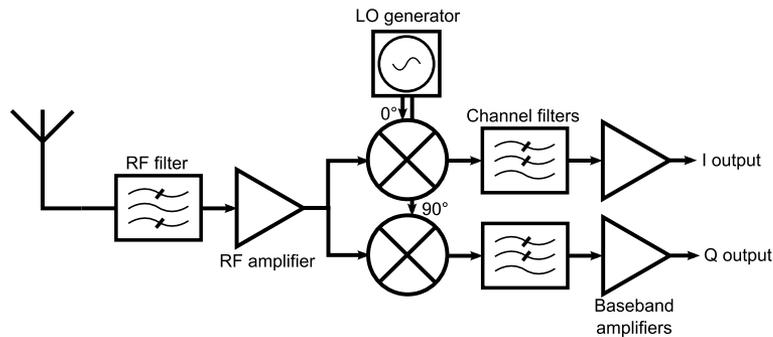


Figure 4.2: Direct conversion receiver

There are, however, some issues that have prevented the direct conversion architecture from being widely used until the last decade. Noise tends to increase at very low frequencies. As current passes through an electric component, such as a transistor, it will emit a type of noise dubbed “flicker noise”. A property of this noise is that most of its energy is concentrated to low frequencies. In fact its spectral content is inversely proportional to the frequency as $1/f$, and it is often known as $1/f$ noise. Since the receiver output signals appear at baseband, they are sensitive to low frequency noise, and the flicker noise must thus be kept to a minimum to not impair the receiver sensitivity. There are also other issues. The LO frequency is the same as that of the RF signal, and if the mixers are not perfectly symmetrical energy from the LO will leak into the signal path. Apart from leading to unwanted emission through the antenna, some of the power may be reflected back into the mixers, and will produce a DC offset at the outputs. Though these problems can be reduced by different means they will always be present. As mentioned in section 2.2.2 we have proposed a modulation scheme which contains no information close to DC. Additionally, the direct conversion architecture is sensitive to second order intermodulation distortion. Second order distortion will cause intermodulation products from an amplitude modulated interfering signal to appear at baseband (and at twice the signal frequency), potentially desensitizing the receiver. The low frequency IM_2 products from a signal with constant amplitude will appear at DC.

4.2 LO GENERATION

4.2.1 QUADRATURE GENERATOR

Operating a direct conversion receiver requires quadrature LO signals. Typically two differential signals are required, resulting in four signals spaced 90°

apart (0° 90° 180° 270°). There are different ways of generating such signals, including quadrature coupled oscillators or a single voltage controlled oscillator (VCO) together with a frequency divider or a polyphase filter [31]. Since the polyphase filter attenuates the signal, especially if implemented with multiple stages, it is less suitable for low power implementations where we have to conserve as much power as possible. This section briefly introduces the first two options.

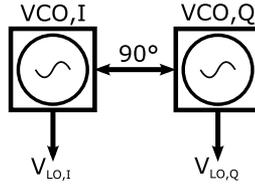


Figure 4.3: Quadrature coupled VCO

The quadrature VCO (QVCO, Fig. 4.3) consists of two VCO cores that are coupled together in a way that forces them to oscillate with a phase difference of 90° . With all high frequency nodes in resonance, the QVCO can potentially operate with lower power consumption than the frequency divider approach. The QVCO is, however, sensitive to interference injected from the RF signal path. To address this LO buffers should be used to isolate it, and these may offset the power saved by the use of a QVCO. A second issue with the QVCO is that since both cores require an inductor each, it occupies a fairly large area on chip.

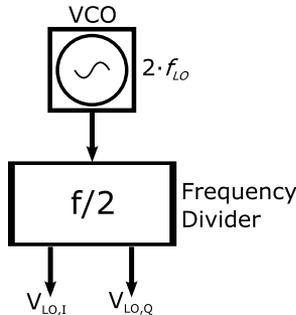


Figure 4.4: VCO and frequency divider

The main alternative to a QVCO is the combination of a VCO operating at a harmonic frequency of the LO, and a frequency divider (Fig. 4.4). Since the VCO is operating at a higher frequency each oscillation period takes less time, resulting in sufficient time resolution to define signals with multiple phase

positions at a lower frequency. A differential VCO produces two signals 180° apart. Generating enough phases for a quadrature front-end the number of phases thus needs to be doubled, from two to four, which can be achieved by halving the frequency.

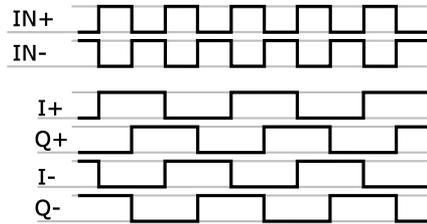


Figure 4.5: Frequency divider $f/2$ operation

To illustrate how a frequency divider can be used to produce quadrature signals, consider figure 4.5. At the top of the figure are the input signals, in this case assumed to be square waves for purposes of clarity. Below are the four phases produced by a digital $f/2$ frequency divider. The digital dividers will act on the flanks of the input signals, so that each flank in the outputs corresponds to a flank in the input signal.

A high frequency digital divider requires large power consumption to handle the fast transitions required. It does, however, help isolate the VCO from the mixers, and if it has enough drive strength it avoids the need for separate LO buffers. The divider can potentially achieve better quadrature accuracy than the QVCO thanks to its sharp transitions that are well defined in time. Furthermore, this approach requires only one VCO inductor and this can be made smaller as the oscillator operates at higher frequencies, meaning it is likely to require considerably less chip area.

4.2.2 PLL

An LO generator based on just an LC VCO cannot achieve the frequency accuracy and signal purity required by the receiver. A VCO tuned by a varactor is sensitive to variations in component values from manufacturing tolerances as well as changes induced by varying operating temperature. Free running, the frequency is not accurate and stable enough for use in a narrow-band receiver. With practical Q factors below 20, the VCO also has enough integrated noise for the jitter to interfere with demodulation. Compare this with a crystal resonator which typically has a Q above 10000. A crystal, however, resonates at low frequencies, typically below 30 MHz, and is effectively not tunable. The phase locked loop (PLL) [32] allows the RF VCO to be locked to a frequency multiple of a crystal oscillator (XO). This allows an LO signal

to be produced with a frequency accuracy approaching that of the XO, but which can be tuned in frequency by changing the multiplication factor.

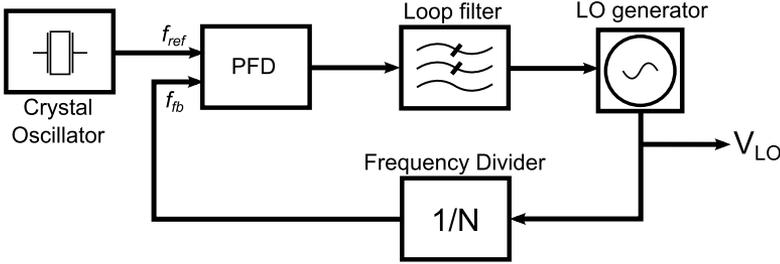


Figure 4.6: PLL

Figure 4.6 shows the basic structure of a PLL. A frequency divider produces a feedback signal at frequency $f_{fb} = f_{LO}/N$. It can be implemented as a counter that produces one pulse for every N input pulses. A phase frequency detector (PFD) compares this signal with the reference generated by the XO, and a signal proportional to the time difference is passed to the LO generator through a loop filter that suppresses ripple at the reference frequency, and that shapes the frequency response of the PLL. When f_{fb} and f_{ref} are close enough the difference in phase corresponds to (4.1).

$$(\theta_{fb} - \theta_{ref}) = \int (f_{fb} - f_{ref}) \quad (4.1)$$

The PLL strives to minimize the phase difference $\theta_{fb} - \theta_{ref}$ through continuous adjustments to the VCO frequency, until eventually f_{fb} and f_{ref} are equal, and the output is locked to $f_{LO} = f_{fb} \cdot N = f_{ref} \cdot N$. By letting the divider ratio change slightly each reference period it is possible to achieve an effective non-integer division ratio, allowing finer frequency steps.

4.3 BUILDING BLOCKS AND COMPONENTS

4.3.1 LNA

COMMON SOURCE

The inductively degenerated Common Source (CS) LNA, shown in figure 4.7, is a popular LNA topology as it is capable of achieving high noise performance. The input impedance is given by (4.2), assuming ideal inductors. Inductor L_s and the gate-source capacitance C_{gs} form a feedback path from the transistor drain current to the input current, which results in a resistive part of the input impedance equal to $L_s \frac{g_m}{C_{gs}} = L_s \omega_T$.

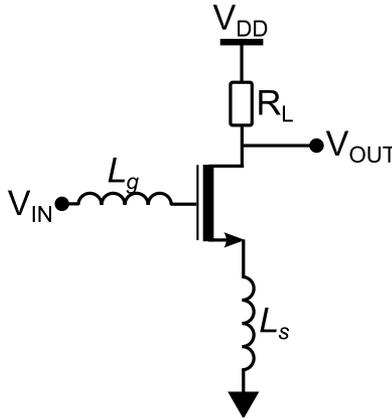


Figure 4.7: Common source topology with inductive degeneration

$$Z_{in} = L_s \frac{g_m}{C_{gs}} + \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) \quad (4.2)$$

L_s is chosen to provide a desired input resistance, typically 50Ω . For a fast transistor $\frac{g_m}{C_{gs}}$ will be high, and L_s may thus be very small, perhaps below 1 nH, making it difficult to implement, especially in a single ended design, where it will be sensitive to any inductance in the ground path. L_g is chosen such that it resonates with C_{gs} and L_s (4.3), making the input impedance completely resistive at the operating frequency. With practical device sizes, C_{gs} is fairly small, leading to a large value of L_g , requiring large area to implement.

$$\omega_0(L_g + L_s) = \frac{1}{\omega_0 C_{gs}} \quad (4.3)$$

These problems may be mitigated by placing a capacitor in parallel with C_{gs} . This increases the effective value of C_{gs} , without the increased Q of the input circuit increasing the gate induced noise [33].

COMMON GATE

The common gate (CG) LNA (Fig 4.8) provides a resistive input while being both simple and inductorless. The input impedance Z_{in} is equal to $1/(g_m + g_{mb})$, neglecting source terminal capacitance and drain-source conductance. If the device, and hence C_{gs} , is small, the input impedance may be predominantly resistive over a very wide frequency range, making the CG topology particularly well suited for ultra-wideband (UWB) applications.

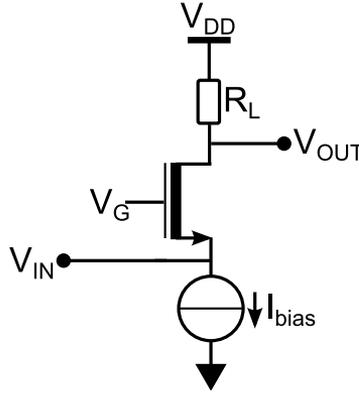


Figure 4.8: Common gate topology

Since the input impedance is almost entirely dependent on g_m , and it should be matched to the RF source ($Z_{in} = R_S$), we have very little freedom in the design parameters. One way this manifests itself is the noise performance that is limited to (4.4), where γ is ideally $2/3$ for a long channel device (and significantly larger for short channel devices), and α is equal to g_m/g_{ds0} . For long channel devices α is ideally one, while it is smaller for short channel devices. If, for example, a short channel device has $\frac{\gamma}{\alpha} = 2$ this means that the lowest noise figure we can achieve with that device is 4.8 dB.

$$F_{min,CG} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s} = 1 + \frac{\gamma}{\alpha} \quad (4.4)$$

More important when designing for low power consumption is that the current consumption is set by the need to provide a certain input impedance. Although g_m/I_d can be improved somewhat by biasing the transistor in weak inversion (at the expense of bandwidth), it is not enough for truly low power designs.

A differential CG LNA design may improve the noise performance through capacitive cross-coupling, where the gates are driven by the opposite polarity input. This halves the required g_m , and reduces the minimum noise factor (4.5) [34].

$$F_{min,cross-coupled CG} = 1 + \frac{\gamma}{\alpha \cdot 2} \quad (4.5)$$

SHUNT FEEDBACK

Just like the CG and CS amplifiers, the shunt feedback LNA (Fig. 4.9) provides a resistive input impedance through a feedback path, with an input

impedance given by (4.6). Compared to the CG topology, g_m may be larger than $1/R_S$, and thus it can achieve better noise performance.

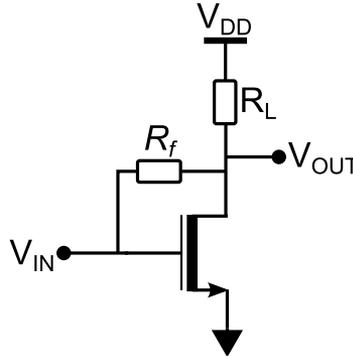


Figure 4.9: Shunt feedback topology

$$Z_{in} \approx \frac{R_f + R_L}{1 + g_m R_L} \quad (4.6)$$

All the input current still has to be provided by the transistor, and so g_m still has a lower limit of $1/R_S$ (which we get when $R_L \gg R_f$). This approach is thus unlikely to be any better for ultra-low power designs than the CG stage.

RESISTIVE TERMINATION

By far the simplest method of matching is to simply terminate the input with a resistor to ground (Fig. 4.10). Independent of the amplifier it is quite attractive at first glance. The problem with this solution is that we are attenuating the RF signal. In other words we are just dumping RF power without making proper use of it, and so it is hard to achieve an acceptable noise figure with this topology [35].

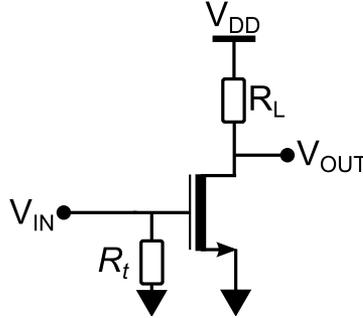


Figure 4.10: Resistive termination

$$F_{RT} \approx 2 + \frac{4\gamma}{\alpha g_m R_S} \tag{4.7}$$

Ignoring the noise of R_L the noise factor is given by (4.7). We can see that $NF_{min} > 3$ dB. This may not seem so bad, but to get close to this g_m must be much larger than $1/R_S$, which results in a very large power consumption. If, for the sake of comparison, we assume the same power consumption as in the CG topology ($g_m = 1/R_S$) and the same $\gamma/\alpha = 2$ we get a noise figure of 10 dB, compared to 4.8 dB for the CG. Lowering the power consumption further, the noise figure will quickly become unacceptable.

NOISE CANCELLATION

Noise cancellation is a method where the noise contribution from the channel of one device can be suppressed at the output [36]. An example of this is shown in figure 4.11. The noise i_n from the transistor channel is injected into the signal path at two different points with opposite polarity. The wanted signal has the same polarity in these two points, and if the gain to the output from both points is matched, for instance with a second gain stage, the noise will be canceled while the wanted signal is amplified. This is precisely the operation of [37].

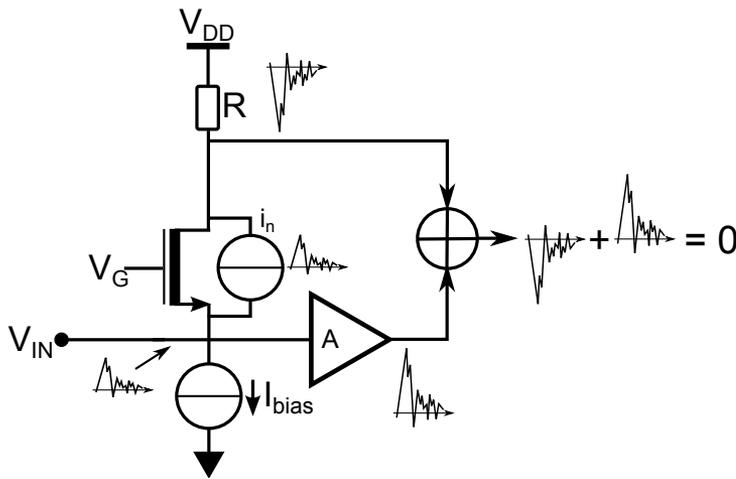


Figure 4.11: Example of noise cancellation

With the noise from one device being canceled other sources will dominate, for instance the amplifier used to match the gain of both signal paths. Noise canceling can be particularly useful when employed to combine the properties of different amplifier stages. For instance, a common gate and a common source stage may be combined in one LNA. Together they act as a balun, while the total noise figure is close to that of the common source stage, which can reach lower noise figures than the common gate [38].

LC-RESONATOR

Most RF circuits are designed for use in a 50Ω (or in some cases 75Ω) environment, but that does not mean that it is an absolute requirement. A transceiver could operate with other impedances, as long as the antenna, interconnects, and filters are designed with this in mind. The impedance (or characteristic impedance) indicates the ratio of voltage to current. Moving to a higher impedance thus results in a larger voltage swing for a given power. As shown in (4.8) a move from an impedance of 50Ω to Z_Z gives a voltage increase $V_Z/V_{50\Omega}$ equal to the square root of the relative change in impedance. By increasing the operating impedance we can lower the circuit power consumption (while trading linearity), since the circuits can operate with lower g_m .

$$P_Z = P_{50\Omega} \implies \frac{V_Z^2}{Z_Z} = \frac{V_{50\Omega}^2}{Z_{50\Omega}} \implies \frac{V_Z}{V_{50\Omega}} = \sqrt{\frac{Z_Z}{Z_{50\Omega}}} \quad (4.8)$$

Increasing the operating impedance is, however, not without drawbacks. Firstly, all components in the RF path need to be fully customized. The an-

tenna should most likely be a custom design in any case, but it is hard to acquire SAW-filters for non-standard impedances. There is, however, a chance that a standard filter component may still function well enough, although its frequency response will be affected. Secondly, there are limits to the characteristic impedance that can be practically achieved with a PCB transmission line. An extremely narrow 0.1 mm non-grounded coplanar waveguide even on a thin substrate with low ϵ_r is unlikely to exceed a characteristic impedance of 200Ω by far.

The problems of non-standard components and difficulty of verifying a non 50Ω device makes an on-chip impedance transformation attractive. The chip can then be used in a standard 50Ω environment, while the LNA can have a higher input impedance resulting in less power consumption. An LC filter (Fig. 4.12) may provide the impedance transformation with a single on-chip inductor. Ignoring the parasitic capacitance of the pad and ESD-diodes as well as the finite Q of the reactive components, the basic design equations are given in (4.9)-(4.11). The mentioned non-idealities will degrade the performance by introducing losses and by reducing the effective transformation ratio.

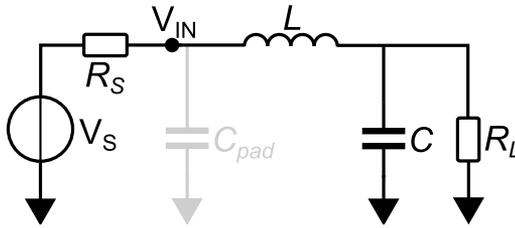


Figure 4.12: LC matching network

$$Q = \sqrt{\frac{R_L}{R_S} - 1} \quad (4.9)$$

$$\frac{1}{\omega_0 C} = R_L / Q \quad (4.10)$$

$$\omega_0 L = R_S \cdot Q \quad (4.11)$$

Ideally the components should have high Q, but that means the inductor will require large chip area. It is, however possible to make quite a compact inductor if a low Q can be tolerated. Returning to the matching technique with resistive termination, a possibility is to let the parasitic resistance of the inductor form the termination resistance.

4.3.2 MIXER

The mixer acts to convert a signal from one frequency to another. In a receiver front-end it converts the RF signal to a much lower frequency where it can be more easily amplified and processed. The mixing is essentially a multiplication of the signal with a tone at some other frequency. Although this can be performed with pretty much any non-linear device, due to its high performance the most used method is to use transistors as switches, rapidly switching the polarity of the signal as it passes from input to output.

A mixer may be implemented with just a single device, but suffers from a lack of isolation between the RF and LO signals. The single balanced mixer provides this isolation, and with a differential output, it is much better suited to conveying IF signals close to DC. There is still some leakage from the LO to IF ports, but in a direct conversion receiver the frequency difference is high enough that it can be easily attenuated with a filter. Placing two single balanced mixers side by side, operating with opposite phase RF and LO signals and combining the outputs, we get a double balanced mixer, where all ports are differential, and where also RF to IF leakage is attenuated. Triple balanced mixers do exist, but are rarely necessary. In low power design a single ended RF port is generally preferred since it usually requires less power for the same noise performance, and we avoid some extra circuit complexity, especially since most antennas do not provide balanced signals. In this section single balanced active and passive mixers are briefly treated.

ACTIVE MIXER

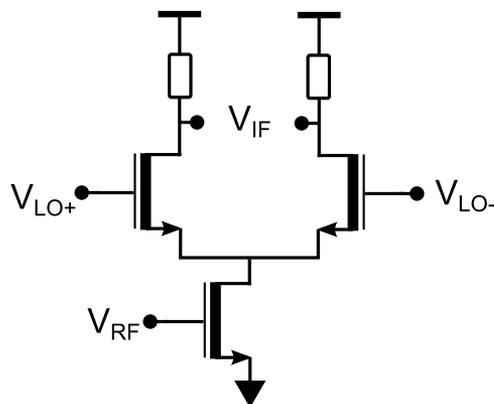


Figure 4.13: Single balanced active mixer

Being powered, the active mixer (Fig. 4.13) can provide power gain. The input device also provides additional isolation from LO to RF ports. The main drawback of the active mixer, apart from the power consumption, is the noise generated, particularly low frequency $1/f$ noise. $1/f$ noise is especially harmful to direct conversion receivers since the output signals are at baseband. The mixer noise is mainly injected during the switch period, where both devices are conducting at the same time [39], [40]. At other times the switch devices are saturated, acting as cascodes, and so their noise will have little effect on the current passing through.

PASSIVE MIXER

The passive mixer, like its name suggests, does not consume any power, and at the RF node the DC current is zero. The main advantage of passive mixers is the lack of $1/f$ noise, making them particularly suited for direct conversion receivers. The passive mixer in Fig. 4.14 is operating in voltage mode. They can also operate in current mode, but this requires low impedances, and thus large devices, and it is thus less suitable for low power applications and more for situations when very high linearity is required. One way of viewing a voltage mode passive mixer driven by square waves is as a sample and hold operation performed directly on the RF signal, and they are sometimes referred to as sampling mixers.

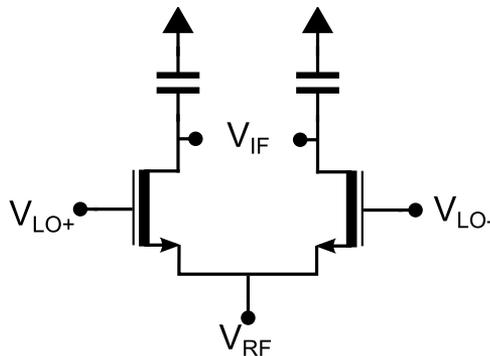


Figure 4.14: Single balanced passive mixer

The gain and linearity of especially a passive mixer are dependent on the LO waveforms. A transistor requires a certain voltage between gate and source to conduct well. As the amplitude of the RF or IF signal gets large enough, the voltage may force the transistors to turn off when they should not. In a similar way it could also cause the transistors to turn on when they should be off. The larger the LO amplitude, the larger the other signals

may be before this happens, improving linearity. The attenuation of a passive mixer is dependent on the shape of the LO waveform. In the case of a mixer such as the one shown in Fig 4.14, when driven by symmetrical square waves the voltage conversion gain is ideally $2/\pi$. Decreasing the duty cycle of the square wave will make the mixer more closely resemble an ideal sampling operation, and the attenuation will be reduced [41]. With the devices conducting in shorter periods, the average resistance increases, reducing the mixer bandwidth. An additional problem that arises from the use of a square wave LO signal, especially with a low duty cycle, is the harmonic content. Harmonics of the LO risk mixing with noise or unwanted signals, worsening the mixer noise performance and making it susceptible to interference (although interference at the harmonic frequencies can be attenuated quite well with an RF filter).

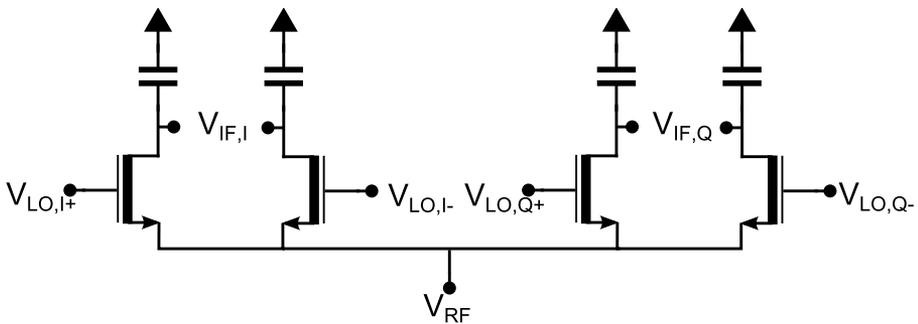


Figure 4.15: Single balanced quadrature passive mixer

Figure 4.15 shows a quadrature passive mixer. With the active mixer there is no problem connecting two mixers side by side, operating in quadrature. In that case the input device provides reverse isolation to the RF port. In the case of passive quadrature mixers, however, this is not as straightforward. If switches in both mixers at any point conduct at the same time, it will allow current to pass between the different IF outputs, discharging the output capacitors and attenuating the output signals. To remedy this, the LO signals should have no overlap, ensuring that only one device at a time can conduct. Typically this is achieved by providing LO signals with 25% or less duty cycle. Another method of avoiding conduction overlap is by placing two switches in series in each branch, effectively incorporating a logical AND function [42]. By operating these switches on different phases of the LO, the conduction period of each branch can be made non-overlapping, even with symmetrical (50% duty cycle) LO waveforms.

4.3.3 OSCILLATOR

An oscillator is a circuit that produces a periodic signal at a certain frequency. Oscillators are used to produce clock signals for timekeeping, and also as a source of RF energy, such as the LO signal. The frequency of the oscillator(s) determines the operating frequency of the receiver. RF oscillators are generally tunable with an input signal, such as the voltage controlled oscillator (VCO) which is tuned by a voltage.

Oscillators may be (close to) linear or nonlinear. A linear (harmonic) produces a (largely) sinusoidal output, and is tuned to a well defined frequency by a reactive load or feedback network. Linear oscillators include negative resistance, Colpitts, Clapp, Heartly, Wien Bridge and Pierce oscillators. A nonlinear (relaxation) oscillator may produce other waveforms such as triangle or square waves. A typical relaxation oscillator is the ring oscillator, which consists of an odd number of inverting gain stages connected in a ring. The period of the oscillating signal is equal to two times the sum of the delays of the inverters of the ring. Another form of relaxation oscillator is formed with a latch, or other switching circuit with hysteresis, and an energy storing component, typically a capacitor, which is charged and discharged each period. Relaxation oscillators generally have inferior phase noise performance since they have poor (low Q) filtering and they cannot store as much energy from one oscillation period to the next as an LC oscillator can.

DIFFERENTIAL LC OSCILLATOR

The most common high frequency oscillator to be implemented on chip is the differential LC negative resistance oscillator, such as depicted in figure 4.16. The negative resistance is provided by two cross-coupled transistors (4.12). If $R_{diff-pair}$ is lower than the effective parallel resistance of the LC tank, the differential pair will add more energy to the LC tank than is lost each period, counteracting the damping. For the oscillation to start up the initial loop gain (4.13) has to be greater than unity. Eventually, as the oscillation grows, the differential pair will saturate, reducing the effective g_m , and the oscillation will stay at a constant amplitude, given by(4.14).

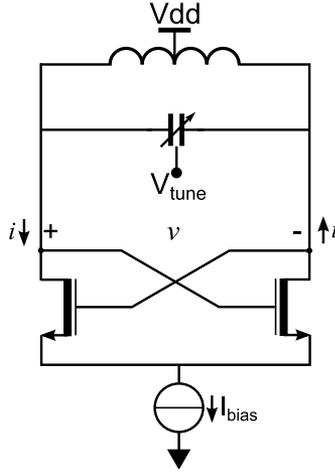


Figure 4.16: Differential voltage controlled LC oscillator

$$R_{diff-pair} = \mathbb{R}\left(\frac{v}{i}\right) = -\frac{2}{g_m} \quad (4.12)$$

$$A_{start-up} = g_m \cdot R' = g_m \cdot \omega_0 \cdot LQ > 1 \quad (4.13)$$

$$|\hat{v}| = i \cdot R' = \frac{4}{\pi} \cdot I_{bias} \cdot \omega_0 \cdot LQ \quad (4.14)$$

A general model of oscillator phase noise is found in [43]. According to this it can be modelled as (4.15) for different frequency offsets $\Delta\omega$ from the oscillation frequency ω_0 . $\frac{2FkT}{P_{sig}}$ is the relative power density of the thermal noise originating from the oscillator circuit, where F is the oscillator noise factor and P_{sig} is the power entering the resonance tank. Within $\Delta\omega = \frac{\omega_0}{2Q}$ the oscillator noise is amplified by the loop gain with a second order dependency on $\Delta\omega$, giving it a $(1/f^2)$ slope. At the lowest offset frequencies $1/f$ noise from the oscillator dominates ($\Delta\omega < \Delta\omega_{1/f^3}$), increasing the phase noise slope to $1/f^3$. The phase noise behavior is illustrated in Figure 4.17.

$$\mathcal{L}(\Delta\omega) = 10 \log \left[\frac{2FkT}{P_{sig}} \left\{ 1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right\} \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right] \text{ dBc/Hz} \quad (4.15)$$

From (4.13)–(4.15) it is apparent that the choice of inductor is important concerning the oscillator performance. A resonance tank with high Q improves the filtering properties of the oscillator, improving the phase noise

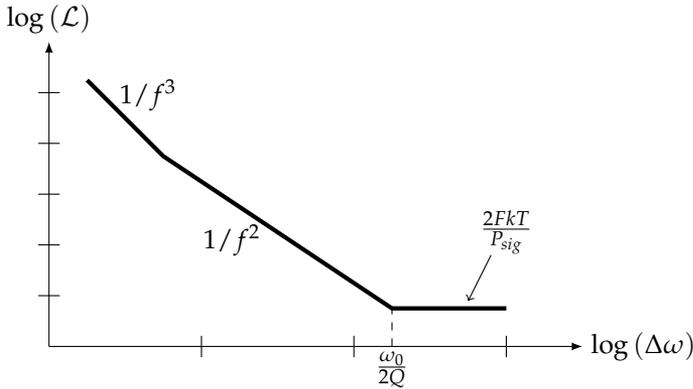


Figure 4.17: Oscillator phase noise vs. offset frequency

performance (all else being equal). For low power design a high LQ product is especially important, since it determines the minimum current required for start-up, as well as the output amplitude achievable with a certain current consumption.

With a low current consumption and thus low output amplitude, it is advantageous to minimize the supply voltage to remove unneeded voltage headroom and improve efficiency. An alternative to a reduced voltage is current reuse, where two or more parts of the same circuit are placed in series, operating from the same DC-current. Examples of such oscillators are the push-pull topology (Figure 4.18a), and the technique in [44], where the switch pair is formed by one NMOS and one PMOS device sharing the same current (Figure 4.18b).

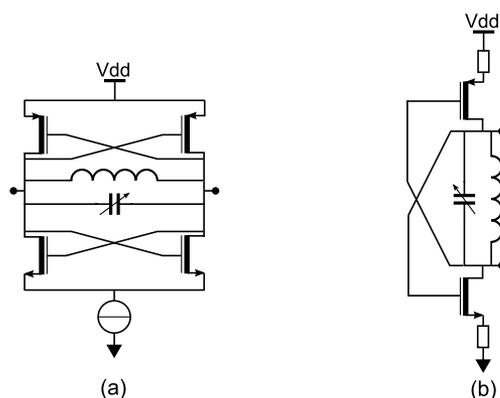


Figure 4.18: Complementary LC oscillators. (a) Push-Pull (b) Current reuse by stacking

QUADRATURE OSCILLATOR

A quadrature oscillator consists of two regular oscillators coupled in such a way that they are forced to oscillate 90° apart. The coupling is achieved through injection locking. A signal is then entered into the oscillator, and if the injected signal has a frequency close to the oscillation frequency, and a large enough amplitude, it will force the oscillator to match the frequency of the injected signal [45], [46]. The most common way of coupling a quadrature oscillator is shown in Figure 4.19. Here two differential oscillators are coupled to each other in a feedback loop, where the delay in each section amounts to a phase difference of 90° . The accuracy of the quadrature signal depends on the matching of the two oscillators and the coupling paths.

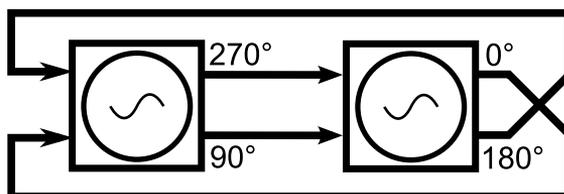


Figure 4.19: Quadrature oscillator coupling

4.3.4 FREQUENCY DIVIDER

The basic function of a frequency divider is to produce a signal with a frequency that is lower than the input signal frequency by a fixed ratio (N). A frequency divider is usually implemented with an injection locked oscillator tuned to the output frequency [47], [48], or with digital circuits that basically

count the pulses of the input signal, outputting one pulse for every N at the input [49]. A divider, such as the one used in a PLL, may have a fairly high division ratio, and it may even be a fractional number. A second use for a frequency divider is to provide multiple signals with different phases, for instance when generating a quadrature LO signal. By providing pulses at alternating outputs, a divider may produce N output signals with different phases from one N times higher frequency input signal.

With a differential input, a quadrature LO signal may be generated with a divide-by-2 circuit. It may use a locking mechanism similar to the quadrature oscillator topology of Figure 4.19, except in a digital implementation the oscillator cores are replaced by flip-flops clocked by the input signal, in a master-slave configuration [50].

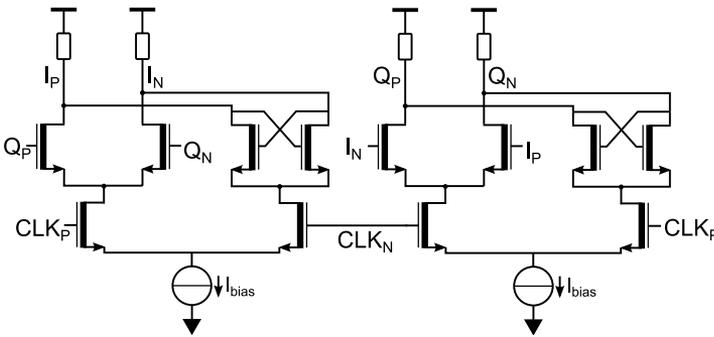


Figure 4.20: Typical implementation of Master-slave frequency divider for quadrature generation

A typical high frequency master-slave divider is implemented with current mode logic (CML), such as the one shown in Figure 4.20. CML supports high speed operation, but a drawback is that in the pull-down state it draws a constant current, making it inefficient for slower operation. This type of divider may have both a maximum and minimum frequency of operation, typically when operating with input signals that do not switch from rail to rail. In this case the range of operation is mainly dependent on the amplitude of the input signal, and there will be a frequency around which the divider is most sensitive [51].

4.3.5 INDUCTORS

A limiting factor when implementing RF integrated circuits, especially oscillators, is the inductors that can be implemented on chip. On-chip inductors are physically large and rarely achieve Q -values above 20. With space at a premium it is imperative that any inductor is carefully optimized. A large num-

ber of design variables together with the high computing load required for a full 3D field simulation, limits the possibility of accurate computer optimization. Simplifications may be required when modeling the process substrate and metal/dielectrics stack, or they may not be fully known, depending on the level of detail provided by available documentation. Altogether this means inductor design is an iterative process, which may contain considerable uncertainty, especially when designing for an unfamiliar process.

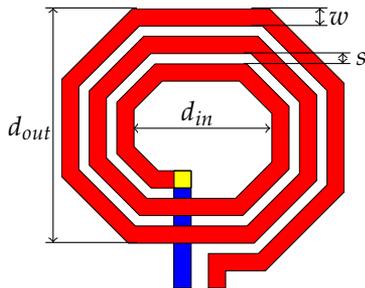


Figure 4.21: Spiral inductor

An on-chip inductor is implemented as a spiral in of one or more layers of metal, as illustrated in Figure 4.21. The inductance primarily depends on the diameter and number of turns. Estimating the inductance with the analytical model given by [52] we get (4.16), where μ_0 is the permeability of free space and n is the number of turns. d_{avg} and ρ_{fill} are the average diameter (4.17) and a fill ratio (4.18), respectively. c_{1-4} are layout dependent constants (depending on a choice of circular, rectangular, octagonal or other geometry).

$$L_s = \frac{\mu_0 n^2 d_{avg} c_1}{2} \left[\ln\left(\frac{c_2}{\rho_{fill}}\right) + c_3 \rho_{fill} + c_4 \rho_{fill}^2 \right] \quad (4.16)$$

$$d_{avg} = \frac{d_{out} - d_{in}}{2} \quad (4.17)$$

$$\rho_{fill} = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (4.18)$$

Modeling an inductor as accurately as possible requires simulation with a field solver such as Momentum or similar, stored as a two port representation with as many frequency points as possible. Such a representation may not be ideal when used in circuit simulations, however, as it adds complexity, requires more computations and may not work with all types of simulation. We may thus wish to use a simplified lumped model such as the single- π shown in Figure 4.22. It is accurate for frequencies close to where it is computed,

and is thus particularly suitable for narrow-band circuits, such as oscillators. This model is also more intuitive and helps to understand the behavior of a particular inductor.

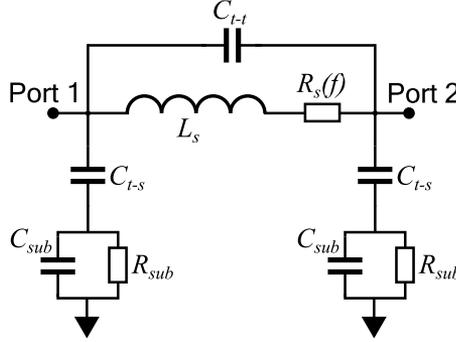


Figure 4.22: Single- π lumped model

R_s is the effective series resistance of the inductor at its operating frequency, and is the primary source of loss in an LC resonator ($Q \approx \frac{\omega L_s}{R_s}$). C_{t-s} and C_{sub} are the capacitive coupling to the substrate, and substrate capacitance, respectively. R_{sub} models resistive losses in the substrate due to capacitive coupling, and may be decoupled using a patterned ground shield above the substrate to provide a low impedance path to ground. C_{t-t} models the turn-to-turn capacitance. The inductor also couples inductively to the substrate, causing eddy currents in the substrate. Losses due to eddy currents may be incorporated into R_s .

R_s comes primarily from the metal resistance in the coil, and so to increase Q the conductor cross-section should be increased. An increase in width (w) may not lower the resistance proportionally, however, due to current crowding effects. A high frequency current passing through a conductor will tend to stay close to the surface. As the current does not effectively use the full cross section of the conductor, the resulting resistance will be higher than the DC resistance. The effective depth of the current is called the skin depth, given by (4.19), where μ and σ are the material permeability and conductivity, respectively.

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \quad (4.19)$$

With a skin depth of $1.3 \mu\text{m}$ for copper at 2.45 GHz the skin effect is limited for compact inductors where w may only be a few μm . In a multi turn inductor there is, however, an additional current crowding effect called the proximity

effect [53] where neighboring turns influence each other. The frequency where the proximity effect begins to become significant is given in (4.20), where R_{\square} is the conductor sheet resistance. With values of $w = 4\mu\text{m}$ and $s = 3\mu\text{m}$ and $R_{\square} = 0.012$, for instance, ω_{crit} is around 2 GHz.

$$\omega_{crit} = \frac{3.1}{\mu} \left(\frac{w+s}{w^2} \right) R_{\square} \quad (4.20)$$

It is clear that increasing the conductor width is unlikely to improve Q much, particularly due to the proximity effect. Generally it is more advantageous to increase the thickness by connecting several metal layers in parallel, especially since most metal layers are less than $1\mu\text{m}$ thick.

An inductor is physically large compared to other components, and maximizing inductance and Q requires a large amount of metal (relatively speaking). A large coil will have large parasitic capacitances, limiting the frequency where it can be practically used. As a rule of thumb an inductor should have a self resonance frequency (SRF) at least twice the operating frequency. Trying to operate the inductor close to its SRF means much of the total capacitance is in the coil. This means the circuit cannot contain much capacitance, limiting design parameters such as tuning range, and it becomes very sensitive to uncertainty of the inductor parasitics.

In a spiral inductor the dominant source of capacitance is normally to the substrate (C_{t-s}). In a differential coil (Fig. 4.23), however, there may be parasitic coupling across conductors several turns apart, making the turn-to-turn (C_{t-t}) capacitance much more noticeable. Since a differential inductor is generally used with balanced signals, the effect of C_{t-t} is further enhanced by the Miller effect [54]. Thus, the price paid for a symmetric coil is a reduced SRF.

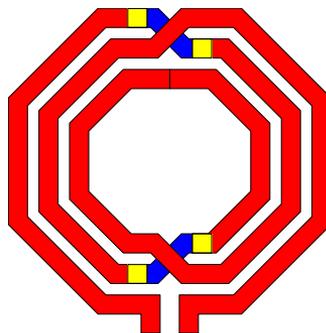


Figure 4.23: Differential inductor

4.4 LOW POWER FRONT-END DESIGN

4.4.1 SURVEY OF LOW POWER FRONT-ENDS

Like pretty much all electronics, RF circuits have been constantly improving since the birth of radio. Lately it has been driven partly by the rapid improvement in integrated circuit technology. There is a drive to increase data rates, coverage and cost effectiveness, as more and more data is used by phones and tablets. As RF electronics have become more compact there has also been an increasing interest of late in sensor networks and similar low power short range communication systems. Included here are some receiver front-ends that achieve good performance with low power consumption. It is, however, by no means an exhaustive list.

In [55] a front-end intended for GPS reception is presented. Operating at 1.575 GHz it has a power consumption of 352 μ W including a QVCO and is thus one of the lowest power receiver circuits published in this frequency range. It achieves this low power by operating on a very low supply voltage down to 250 mV. To function at this low voltage, the circuit requires extensive use of inductors, giving it a rather large chip area of about 1.7 mm². The QVCO achieves a good figure of merit (FOM) of 187.4 dB but requires two inductors per core. Also, the oscillator is connected to the mixers with little isolation to the RF signal. The circuit achieves much of its gain at RF, through the use of positive feedback. The positive feedback may be varied to change the gain, but close to maximum gain there is concern that stability may be compromised, especially in combination with a non-50 Ω antenna impedance. It is designed for low IF operation, but the IF filters are not implemented.

Reference [56], from the 2013 ISSCC conference, presents a receiver circuit with 2.7 mW power consumption (1.6 mW excluding VCO). It is based on a Blixer structure, which is basically a combination of LNA and mixer on top of each other, using the same current. The LNA part has a single-ended input and differential output through matched common source and common gate stages. The advantage is that the mixer is double balanced, improving isolation between ports. Additionally a biquad and an active inductor improve filtering, and the mixer outputs are combined in an image reject structure with complex impedance loads. It is one of the smaller solutions with an active area of 0.26 mm². The Blixer structure is operated off a 1.2 V supply, which is probably necessary with several components stacked on top of each other.

Paper [57] describes a low IF receiver front-end and VCO operating on a low 300 mV supply with a power consumption of 1.6 mW. It has a folded cascode (common gate) LNA incorporating a transformer based balun and a single mixer. Switched capacitor filters provide sharp IF-filtering. With a

single mixer it has no apparent image rejection. Including the mixer it has an IIP_3 of -21.5 dBm which should, in combination with the sharp IF filters, dominate the out of channel linearity. This is fairly low, especially considering the gain of 20.7 dB at this point. It does, however, achieve a good NF of 6.1 dB. With several transformers the active area is about 0.85 mm².

A 2.4 GHz transceiver operating on a supply below 600 mV is presented in [58]. It consumes $0.8 - 1.45$ mW with quadrature reception. It can optionally be scaled down in power, including turning off one VCO core. The most significant feature of this circuit is passive mixers combined with a lack of LNA. This makes it harder to achieve low NF, but can greatly improve out-of-band linearity, and the receiver achieves an out-of-band IIP_3 of about -7.5 dBm. The RF input is differential, and an LC matching network provides some voltage gain. The QVCO is coupled directly to the passive mixers, risking poor isolation between RF and LO signals. The bias current is set entirely by varying the power supply voltage, making the circuit sensitive to PVT variations, and should give a low power supply rejection ratio (PSRR). The active area is about 0.7 mm².

All the above receivers are designed for low IF operation. Although this should lower their sensitivity to second order intermodulation distortion, it does not remove the problem. It is thus interesting to note that none of them have characterized their second order intercept point.

4.4.2 SUMMARY, PAPER I

In Paper I a quadrature front-end is presented that explores a completely inductorless implementation. It consists of an LNA and active mixers, and the quadrature LO is generated by a frequency divider from an external source. Operating at a frequency of 915 MHz the total power consumption is about 280 μ W.

The LNA (Fig. 4.24a) consists of a noise canceling structure as found in [59], combined with a gain boosting inverter amplifier (M1 & M2). Apart from increasing the effective g_m of the input, capacitance in the feedback loop is translated to the input as an inductance, helping to make the input impedance resistive. Since the input impedance is proportional to g_m , itself proportional to the current consumption, the circuit was designed for a 200Ω input impedance, which was deemed to be about the highest practically usable off chip. The input impedance at 915 MHz is actually closer to 150Ω . With this input impedance an acceptable match -10 dB may be achieved with a source impedance as low as 80Ω , at reduced noise performance.

The front-end uses complementary active mixers (Fig. 4.24b) with a resistor bleeding current past the switch devices. Current reuse is achieved by placing complementary mixers head to head. The NMOS and PMOS halves together

act as a pseudo-balanced mixer, providing additional isolation from the LO signals. Able to provide high output impedance a higher voltage gain can be achieved than with resistive loads. The current bleeding reduces the mixer $1/f$ noise [60] [61] by reducing the bias current through the switch devices.

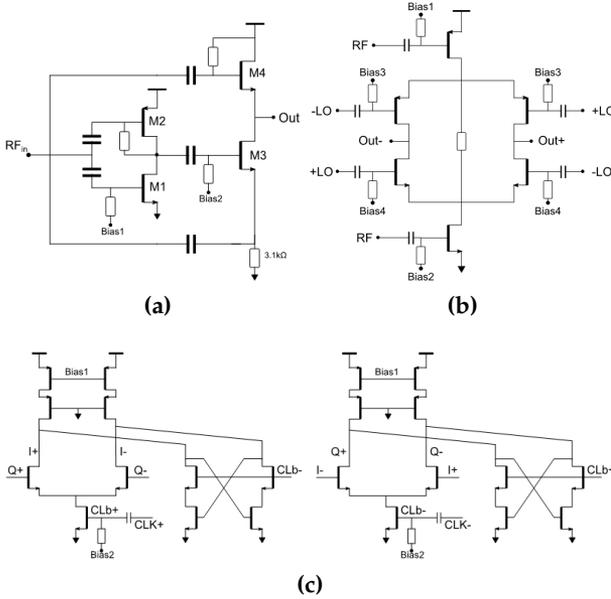


Figure 4.24: Schematics of front-end (a) LNA (b) Mixer (c) Frequency divider

The frequency divider (Fig. 4.24c) uses a master-slave topology implemented in current mode logic, with a couple of modifications. Firstly, it replaces the resistive loads with high impedance current sources to improve efficiency. Secondly, the latches have been rearranged to improve the voltage headroom, which is otherwise limited with the entire circuit implemented with standard threshold devices.

4.4.3 SUMMARY, PAPER II

The frequency divider topology in paper I turned out to be too sensitive to parasitics for efficient operation at a higher frequency of 2.45 GHz. The primary purpose of the new design was therefore as a demonstration of a low power LO generator including frequency divider operating above 2 GHz.

The circuit uses a push-pull type oscillator, operated together with the divider from a 0.65 V supply voltage. Instead of using a resistive load or the

current sources used in paper I, the latches have been implemented with PMOS devices and moved up above the gain stages. This way the passive loads can be removed, and the resulting flip-flops only draw current during state transitions [62].

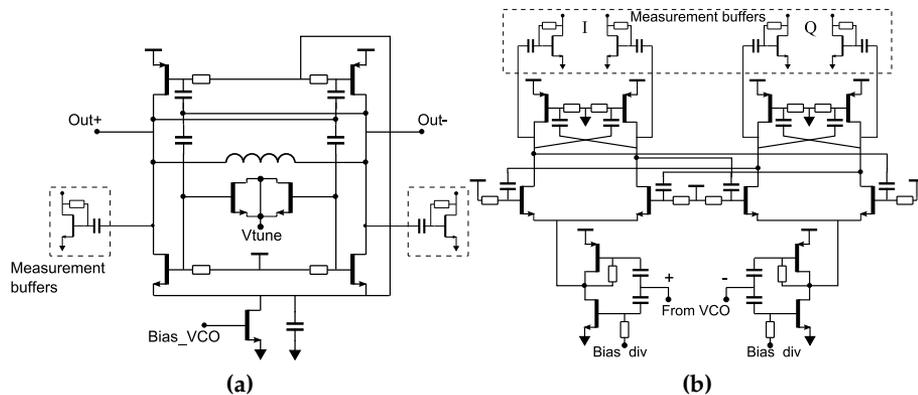


Figure 4.25: (a) VCO schematic (b) divider schematic

4.4.4 SUMMARY, PAPER III

Paper III details a combined front-end and LO generator operating at 2.45 GHz (Fig. 4.26). It achieves a 50Ω input impedance through resistive termination and an on-chip LC-matching network. As discussed in section 4.3.1 the noise performance of an LNA with resistive termination improves with increasing source resistance. Essentially the LC-match is providing voltage gain before the LNA. Although the front-end is not inductorless it uses a very compact multi-layered coil with a diameter of only $80\mu m$, with the internal resistance forming the LNA input match (like [63], but much more compact).

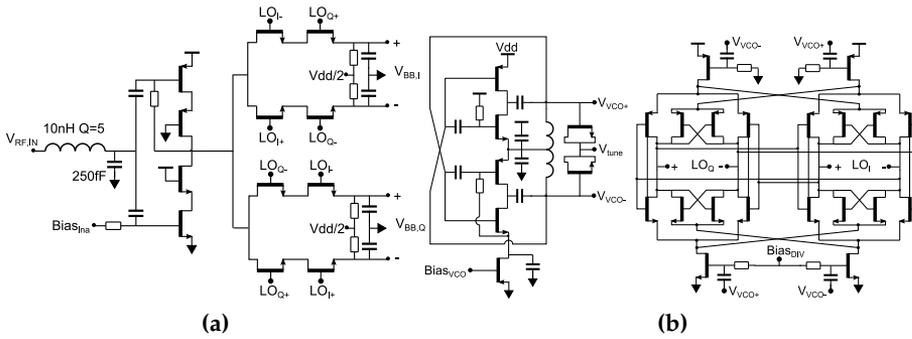


Figure 4.26: (a) Front-end schematic (b) VCO & divider schematic

Passive sampling (voltage mode) mixers are used to achieve good low frequency noise performance. AND-function mixers [64] ensures there is no conduction overlap despite overlapping LO signals, something which may otherwise reduce the performance of a passive quadrature mixer.

The LO generator has been designed to operate on the same 0.8 V power supply as the front-end. It achieves this with extensive current-reuse with complementary devices. The VCO, for instance, has all devices stacked in a single current path. Despite this it is relatively symmetrical, with identical NMOS and PMOS devices connected to both outputs. Just like in paper II the divider avoids the need for static current sources and a constant current draw through complementary design. In this case, however, the PMOS side is a mirror image of the NMOS side. Apart from the efficiency improvement, this additionally evens out the effect of VCO imbalance on the quadrature accuracy, since all phases are affected roughly equally by the positive and negative oscillator outputs. This is particularly useful when the oscillator is not perfectly symmetrical, like in this design.

4.4.5 SUMMARY, PAPER IV

This paper details the design of an LNA-less front-end together with an LO generator (Fig. 4.27). The front-end contains passive mixers connected to the input, with no LNA other than a passive matching network. This topology promises significantly improved suppression of interference, but the lack of LNA makes it harder to maintain an acceptable noise figure. With greatly improved out-of-band linearity, the front-end can function without an external SAW-filter, saving both space/cost and improving the overall sensitivity (see subsection 2.2.3).

The improved suppression of interference comes from the fact that it is much easier to perform sharp filtering at baseband than at RF, and the advantage of not having an LNA is that the received signal is transferred to

baseband already in the first stage, before it has been amplified. Any interference outside the channel will then be suppressed already by the capacitors at the mixer output. An LNA can not achieve the same narrow filtering, and so it will amplify any interference that is not separated by a very large difference in frequency, and in amplifying the interference it will generate intermodulation distortion.

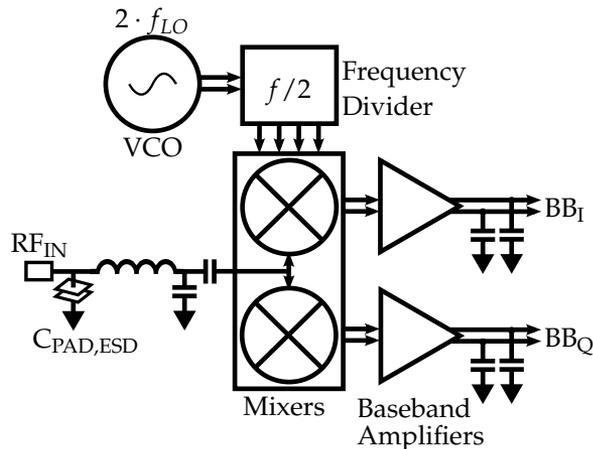


Figure 4.27: Receiver Front-end and LO generator

The mixers (Fig. 4.28a) perform an AND function like those in paper III, but with an improved topology that use the transistors more effectively. The out-of-band filtering has also been improved with the introduction of capacitors between the first and second stages of the mixers. These capacitors additionally suppress mixing with the LO second harmonic, something usually only achieved with double balanced mixers.

The baseband amplifiers (Fig. 4.28b) are single stage, but can provide over 26 dB voltage gain thanks to using $3 \mu\text{m}$ long devices. The large devices additionally keep $1/f$ noise at a minimum and aid device matching. The LO-generator (Fig. 4.28c) is largely the same as in paper III, except that it has been scaled up to reliably drive the larger passive mixers, and it uses a VCO inductor with lower inductance and higher Q-value.

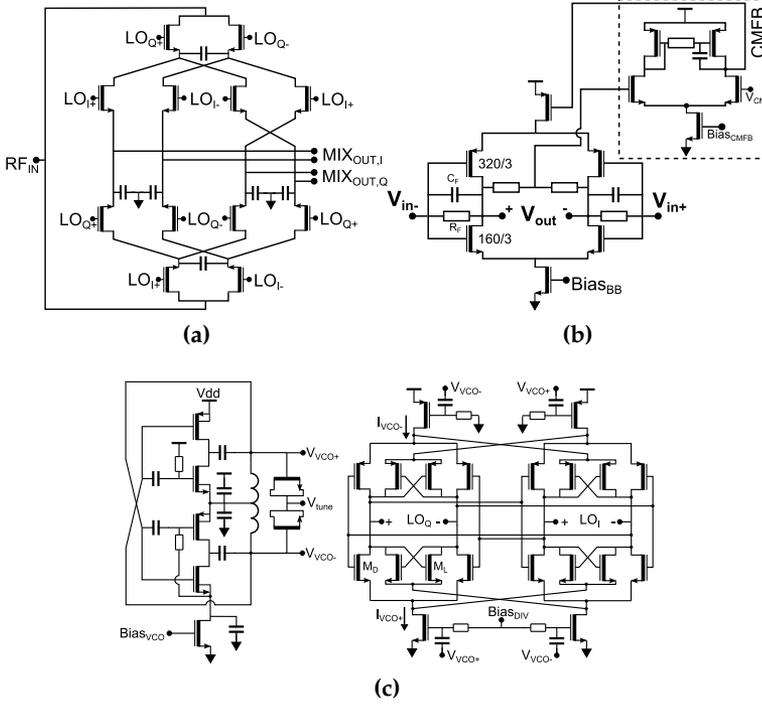


Figure 4.28: (a) Mixer schematic (b) Baseband amplifier schematic (c) VCO & divider schematic

The front-end achieves excellent suppression of out-of-band interference and has a low quadrature error, while achieving a noise figure below 10 dB. It has a $1/f$ noise corner of about 30 kHz.

4.4.6 PERFORMANCE SUMMARY

Table 4.1 contains a side by side comparison of the performance achieved by the circuits described in the included papers.

Table 4.1: Performance comparison of included works

Paper	I	III	IV
f (MHz)	915	2450	2600
Supply (V)	0.9	0.8	0.85
Power (mW)	0.28*	0.4	0.55
Noise figure (dB)	<9	9	9.6
Conversion gain (dB)	30/36**	27.5	41
IIP ₃ (dBm)	-28	-24.5	-30
IIP _{3-OOB} (dBm)	-	-21	-3
IIP ₂ (dBm)	>-5	2	0
IIP _{2-OOB} (dBm)	-	>6	29.5
LO-RF leakage (dBm)	-95	-81	-69
Quadrature phase error (°)	<3	<2	<0.6
Active area (mm ²)	0.016	0.08	0.15

*No VCO **w/ external 50Ω match

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Paper I

Paper I

A 65nm CMOS 282 μ W 915MHz Direct Conversion Receiver Front-end

C. Bryant and H. Sjöland, "A 65nm CMOS 282 μ W 915MHz Direct Conversion Receiver Front-end," © 2011 IEEE. Reprinted from *IEEE Proc. European Solid State Circuits Conference, ESSCIRC 2011*, pp. 547-550, Sep. 12 - 16, 2011, Helsinki, Finland.

A 65nm CMOS 282 μ W 915MHz Direct Conversion Receiver Front-end

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Abstract—This paper presents an inductorless ultra-low power radio receiver front-end intended for applications such as sensor networks and medical implants. It consists of low noise amplifier, quadrature mixer, and a frequency divider for the generation of quadrature local oscillator signals. The power consumption is just 282 μ W from a 0.9V supply when it operates in the 915 MHz ISM band. It achieves a total gain of 30dB and a noise figure below 9dB. Manufactured in 65nm CMOS, the active area is 0.016mm². In a 200 Ω environment it achieves a -17dB S11 without any external matching network.

I. INTRODUCTION

In applications like wireless sensor networks and medical implants, highly compact wireless nodes must be able to operate for years from a small battery or other power source. Such devices require circuits that are small and consume minimal power. Though they only need to communicate over small distances and thus require limited performance, pushing the power consumption to below one milliwatt is still a challenge. In this project we aim to build a compact receiver with a total active power consumption including the digital baseband below 1mW, and thus the front-end should consume only part of that.

We can use the high inherent speed of modern CMOS processes to our advantage. By biasing the transistors in the weak to medium inversion regions, we can achieve more gain for the same current consumption [1]. Though speed is sacrificed, it is something we can afford to trade.

To minimize external components the receiver must be able to provide acceptable matching on chip. Though an inductorless design is the most compact, providing a resistive impedance without excessive noise or power consumption is a challenge.

II. RECEIVER OVERVIEW

A direct conversion receiver architecture is used, which requires a quadrature mixer, and quadrature local oscillator (LO) signals. To minimize the chip area the quadrature LO signals are generated by a frequency divider, clocked by a differential signal at twice the operating frequency (fig. 1).

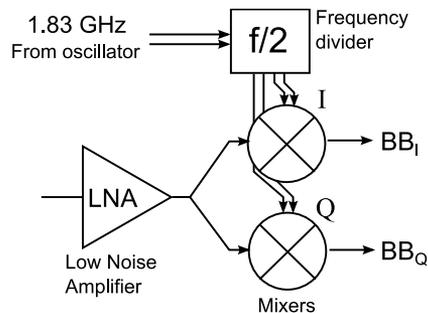


Figure 1. Receiver structure

This removes the need for a large quadrature oscillator. It is estimated that this method will require more power than a quadrature oscillator, but that the cost is small compared to the area saved.

III. LOW NOISE AMPLIFIER

The low noise amplifier (LNA) schematic is shown in fig. 2a. It is designed to provide a 200 Ω resistive input impedance at the pad. To provide a real input impedance with an inductorless circuit the LNA can either be resistively terminated (resistor shunted to ground), or provide some form of current feedback [2,3]. Resistive termination, though requiring no additional current, results in a high noise figure. Current feedback is better in terms of noise but the resulting input impedance is directly related to the effective transconductance of the loop. With the available power budget there is simply not enough current to achieve a 50 Ω input match this way. We are not, however, forced to operate with a 50 Ω source. Designing for a higher impedance can keep the power consumption down, at the expense of greater sensitivity to parasitic capacitance from the pad and ESD protection. The proposed circuit attempts to achieve as low an impedance as possible with the available current, while also minimizing the effect of parasitic capacitance by presenting an input impedance with an inductive component.

A gain stage (M1, M2) is used to boost the effective transconductance of the common gate input stage. It also forms part of an active inductance circuit (fig 2b), where the capacitance of the intermediate node is gyrated to form an inductance at the input [4]. All resistors are used for biasing purposes.

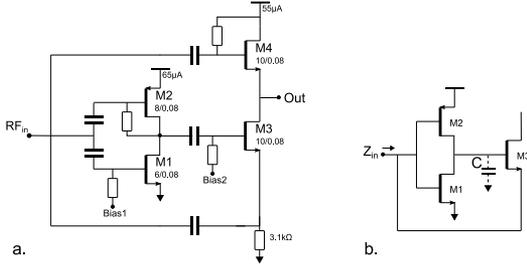


Figure 2. a. LNA schematic b. Active inductor loop

The transconductance increase is equal to the voltage gain of the boosting stage, which means that the input impedance can be made significantly lower than if all current had instead been used in the common gate stage.

A device at the output configured as in [5] provides a broadband load with better noise performance than if using a simple resistor. The LNA power consumption is $109\mu\text{W}$.

IV. FREQUENCY DIVIDER

The frequency divider (fig. 3) is based on a common architecture using current mode logic [6]. With a reference signal at twice the output frequency having steep signal edges, the internal nodes must provide high speed despite the low current consumption, and thus the divider is highly sensitive to load and parasitic capacitances. High impedance current sources provide low internal loading, allowing most of the signal current to be used to drive the mixers. To improve the voltage headroom at the output, the latch stage tail source/switch has been split and placed above the cross coupled pair. The voltage headroom is otherwise limited by the threshold of the standard low power (LP) devices, which is fairly high, especially at short gate lengths. Simulations indicate that it can exceed 0.5V. The power consumption of the divider is $100\mu\text{W}$.

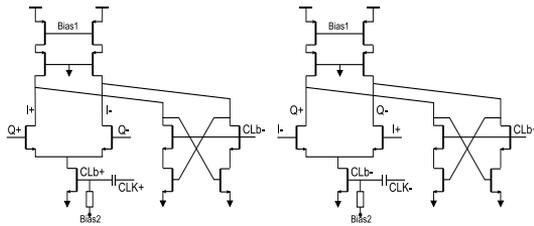


Figure 3. Frequency divider schematic

V. MIXER

Complementary stages allow the mixers (fig. 4) to use the current efficiently. Additionally, the combination of NMOS and PMOS single-balanced mixers will work as a single pseudo double-balanced mixer, giving some cancellation of the LO signal feedthrough to the outputs. The switching devices operate like cascodes when on, and with the complementary design the total output impedance thus becomes quite high. In the absence of a resistive load the voltage conversion gain can therefore be high. The complementary configuration can also improve the IP2 performance somewhat thanks to its symmetrical properties [7]. To slightly reduce the flicker noise some of the bias current bypasses the switching stages [8] through a resistor. The total power consumption of both (I and Q) mixers is $73\mu\text{W}$.

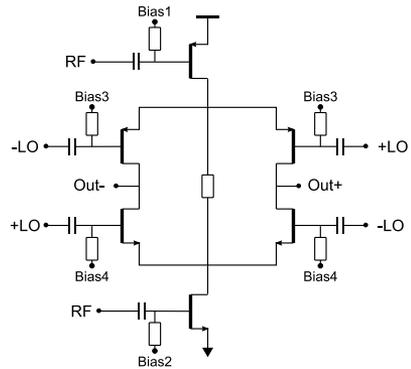


Figure 4. Mixer schematic

VI. MEASUREMENT RESULTS

The circuits, manufactured in 65nm CMOS, were wirebonded to a printed circuit board (PCB). An LC network on the PCB was used to match the 200Ω LNA input impedance to the 50Ω of the measurement equipment for gain, noise and linearity measurements. Though designed for 915MHz the centre frequency of the LC network was slightly lower. External opamps were used at the mixer outputs to drive the 50Ω equipment.

As can be seen in fig. 5 the noise figure is better than 9dB at the operating frequency. The total voltage conversion gain is about 36dB, where 6dB is attributed to the matching network (50Ω - 200Ω). Measurements of a standalone LNA fabricated on the same chip yields a gain of 12dB, and thus the mixer conversion gain is about 18dB. The measured $1/f$ noise corner is close to 100kHz.

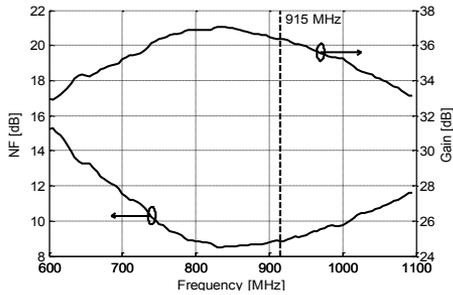


Figure 5. Measured noise figure and gain

To measure the input impedance a TRL (Through-Reflect-Line) calibration kit was manufactured that duplicates the input PCB conductor, allowing calibration to the input bond wire. Fig. 6 shows how the gyrated inductance of the feedback loop helps provide an input impedance with minimal reactance. The measured data includes the capacitive load from pad and ESD protection. The grey ring around the centre marks the boundary where S_{11} is better than -10 dB. The square marks 915MHz.

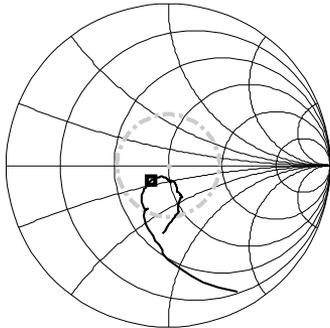


Figure 6. Input impedance, $Z_0 = 200\Omega$

At 915MHz the input matching (fig. 7) is better than -17 dB with a 200Ω source. Sacrificing some noise performance we could also achieve a good match at a slightly lower impedance.

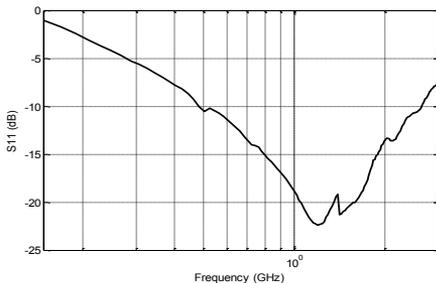


Figure 7. Input matching, $Z_0 = 200\Omega$

The measured quadrature error was 1.3° averaged over three different circuits. The 1.83GHz frequency reference was generated off-chip, and combined with the frequency divider's sensitivity to differential input signal imbalance, there seems to be a measurement uncertainty of a few degrees. In any case the quadrature accuracy is good enough for a low power, short range receiver, both for direct conversion and low IF configurations.

The 1dB compression point (input referred) was measured to -37 dBm and the third order intercept point (IIP3) to -28 dBm, as can be seen in fig. 8. The second order intercept point (IIP2), measured at a 4MHz IF, is better than -5 dBm at a fixed bias point for the different circuits. With calibration to find the bias point of best linearity, another 10dB could be achieved.

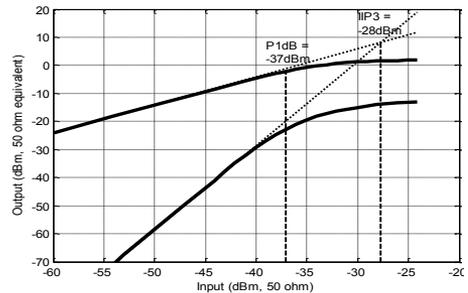


Figure 8. Compression and third order intercept point

To put this into perspective we can look at the specifications for Zigbee/802.15.4. As can be seen from [9] the requirements are quite relaxed. With blockers at ± 10 MHz and ± 20 MHz, the third order intercept point, IIP3, should be better than -32 dBm, and IIP2 better than 10.5 dBm, including 10dB margins. This receiver is more sensitive to blockers, but it is also designed for even lower power and range. Due to the high conversion gain the overall linearity is limited by the mixer output. Gain can thus be traded for improved linearity by resistively loading the output. As long as sufficient gain remains, the effect on noise performance will be limited.

LO leakage at the RF port was better than -95 dBm for all three samples measured. The total power consumption for the entire receiver is $282\mu\text{W}$, and the active circuit area, marked in Fig. 8 is 0.016mm^2 .

Figure 9 shows the die photo of the manufactured circuit. The total area including pads is $0.78 \times 0.43\text{mm}$. The active area is to the right and marked by dashed lines. Further left is a standalone copy of the LNA with a buffered output. The four tightly placed pads to the far left are not part of the circuit.

In table I the performance is compared to other published ultra-low power receiver front-ends. The active areas have been estimated from chip photographs. Where possible the LO generation has been excluded from the comparison. An additional column shows how the performance of this work is affected by the inclusion of an external 50Ω matching net. Only the voltage gain will change.

TABLE I. SUMMARY OF RESULTS

	This Work ($Z_{in}=200\Omega$)	w/ 50 Ω match	[10] JSSC 11	[11] ISSCC 10	[12] JSSC 08	[13] ISCAS 08	[14] JSSC 07
Technology	65 nm CMOS		130 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Frequency (MHz)	915		1575	1575	2500	2500	2200
Single ended	Yes		Yes	No	No	Yes	Yes
Power (μ W)	282 (182 ¹)		200	1000	1400	1060	500
Gain (dB)	30	36	41.8	42.5	43	24	30.5
NF (dB)	< 9		7.2	6.5	5	8.4	9.2
CP _{1dB} (dBm)	-37		-48	-40		-30.5	-31
IIP3 (dBm)	-28		-35.8	-30	-37	-21	
IIP2 (dBm)	> -5					-5	
LO-RF leakage (dBm)	-95		-81.75	-75		-79	
Area (mm ²)	0.016		0.9	0.5	0.8	0.85	0.55

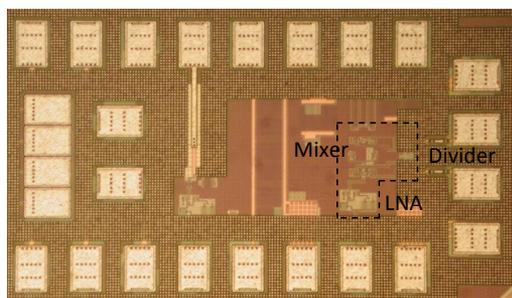
¹Excluding frequency divider

Figure 9. Die photo

VII. CONCLUSIONS

A 915MHz direct conversion front-end with an ultra low power consumption of 282 μ W has been demonstrated in a 65nm CMOS technology. A current feedback structure gives the low noise amplifier an actively matched 200 Ω input. Complementary mixers provide high voltage conversion gain, as well as some cancellation of the LO feedthrough. Quadrature LO signals are generated by a frequency divider. The design is completely inductorless, resulting in an active area of just 0.016mm².

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Paper II

Paper II

A 65-nm CMOS 250uW Quadrature LO Generation Circuit

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A 65-nm CMOS 250 μ W Quadrature LO Generation Circuit

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Abstract — This paper presents a quadrature LO generation circuit with ultra-low power consumption. Apart from applications such as sensor networks and medical implants, we show that it could even be used as part of a secondary WCDMA receiver, since most of the time the signal conditions are significantly relaxed compared to the worst case scenario. Consisting of an oscillator and frequency divider, the circuit, manufactured in 65nm CMOS, consumes less than 250 μ W from a 0.65V supply while operating in the 2.14GHz band.

Index Terms — CMOS, frequency dividers, receivers, voltage-controlled oscillators, WCDMA.

I. INTRODUCTION

For cellular applications the radio front-end will usually have stringent performance requirements. When far away from the base station the receiver is operating close to its sensitivity level, while the phone is at the same time transmitting a strong signal. Phase noise and intermodulation will cause a fraction of the transmitted power to leak into the receiver, where it will behave as noise. This means that unless the front-end circuits have excellent phase noise and linearity, the receiver will lose sensitivity, to the point where it may not be able to receive the signal. To achieve such performance the circuit power consumption will tend to be quite high.

Much of the time the channel conditions are, however, significantly better than the worst case scenario. Fig. 1 shows the expected probability, as defined in the TS.09 (DG.09) specification [1], that the transmitted power is below a certain level.

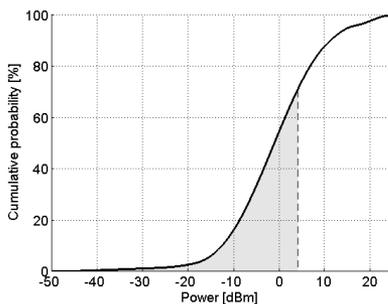


Fig. 1. WCDMA output power probability (class 3)

We can see that typically a WCDMA transmitter is expected to operate more than half the time backed off by more than 20dB from the maximum output power, as indicated by the

shaded area of Fig. 1. Assuming that the same applies to the received power level, the overall performance requirements are considerably relaxed. This implies that much of the time we can use circuits that have one or two orders of magnitude lower power consumption than in the worst case scenario. This could be exploited by implementing a secondary receiver with low power consumption that is turned on in conditions with good reception. If it is made as compact as possible, the extra cost should be minimal. In this paper we implement a band 1 quadrature LO generation circuit for such a receiver, which explores the extremes of such a low power solution. Naturally such a circuit could, with minor modifications, find uses in other types of applications, such as sensor networks, body area networks or medical implants to name but a few.

II. REQUIREMENTS

Although we are not implementing a full receiver chain in this paper, the limited driving strength of the circuit means that the corresponding receiver, and thus its performance must be scaled accordingly. We should thus apart from investigating the phase noise requirements, explore what happens to some of the linearity requirements to ensure that they can be met by such a receiver.

Assuming that the sensitivity level can be increased by the same amount (in dB) as the transmitter power is backed off, the receiver can tolerate 20dB more noise and leakage products due to nonlinearity than the main receiver. The phase noise from blockers can be increased by the same amount. Based on the worst case requirement calculated in [2] the LO phase noise is in this case reduced from -129dBc/Hz at an 8MHz offset to -109dBc/Hz. The required IIP2 due to blocker nonlinearity (not dependent on Tx power) will scale by the same amount and the corresponding IIP3 by 10dB [2]-[3]. The reduced transmitter power means that noise and nonlinearity dependent on the Tx level will reduce even further. The phase noise at the duplex distance can thus be relaxed an additional 20dB, in total 40dB, while the required IIP2 due to direct Tx leakage will in total be reduced by 60dB since the second order intermodulation depends on the square of the signal power. The phase noise requirement at the duplex distance that is usually a stringent -160dBc/Hz can now be relaxed to -120dBc/Hz. It is clear that under conditions with good reception the receiver requirements are relaxed considerably, making it likely that a small low power receiver will suffice.

IV. CIRCUIT DESIGN

To keep the required space at a minimum we have chosen to generate quadrature signals with a frequency divider. This means that only a single oscillator is required, and this uses only a single inductor. Since the VCO operates at twice the LO frequency this inductor will also be more area efficient than the inductors required for a quadrature VCO solution.

The VCO is a complementary type as shown in Fig. 2. When designing for minimal current consumption it is hard to achieve sufficient loop gain for the oscillator to start, as well as sufficient voltage swing to drive the frequency divider. The complementary solution is advantageous in that it can achieve higher voltage swing and more transconductance for the same current. It has been shown in [4] that the second switch pair does not incur any penalty to the noise figure. We can further increase the startup loop gain by biasing the devices in weak inversion, thus trading some of the high speed inherent to a modern CMOS process.

The standard V_t low power devices used here have a fairly high threshold voltage of about half a volt, but with the gates biased independently from the drains the voltage and thus power consumption can be minimized. Without independent bias the supply voltage would have to be increased from 0.65V to about 1.1V.

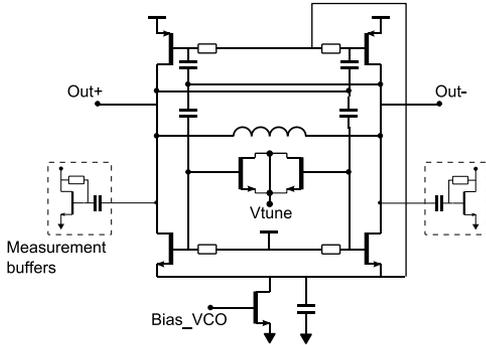


Fig. 2. Oscillator schematic

The frequency divider (Fig. 3) is designed to operate from the same low supply voltage as the VCO (0.65V). Like [5] it uses two Dynamic Single-Transistor-Clocking (DSTC) latches, that operate alternatively, based on a clock at twice the output frequency. The gates are biased through resistors to allow for enough speed while operating with the low supply voltage. While a solution based on current mode logic (CML) may be faster, it also draws a continuous current [6]. The DSTC solution only draws current during transitions, improving efficiency. The switches used to inject the VCO signal have been complemented with a pair of small PMOS devices that help turn off the gain stages, increasing robustness for large loads.

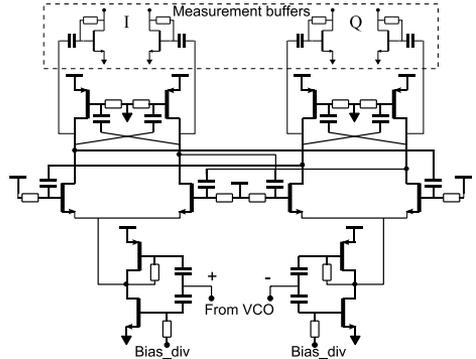


Fig. 3. Frequency divider schematic

VI. MEASUREMENTS

The circuit was manufactured in a 65nm CMOS process. The measurements were performed with the chip directly bonded to PCB. Fig. 4 shows the tuning characteristic for four measured samples. The tuning range is greater than five percent in all cases. Although some samples do not fully cover the 2110-2170MHz Band 1 downlink, in a redesign it should be easy to increase the size of the varactors. One should also remember that there are currently measurement buffers connected directly to the VCO. Removing these will make it possible to improve the tuning range. As a reference, turning the buffers on drops the VCO frequency by 25MHz.

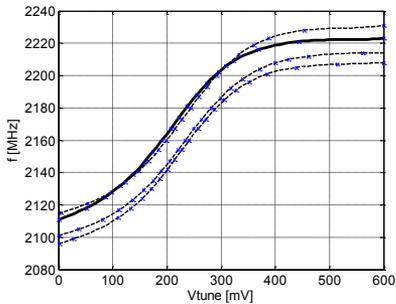


Fig. 4. Tuning characteristic

The phase noise was measured using a Europtest PN9000 phase noise measurement system. The phase noise performance is at its lowest in the middle of the tuning range, where all samples measured better than -106dBc/Hz at a 1MHz offset, and best towards the edges of the tuning range where it could reach to below -110dBc/Hz . In Fig. 5 the phase noise versus offset frequency is shown for one of the samples while in the middle of the tuning range, and while at the lowest part. The dark flat lines indicate the required phase noise for a WCDMA receiver 20dB from its worst case sensitivity. The phase noise at the duplex distance of 190MHz

was measured using a spectrum analyzer and a SAW filter to avoid reciprocal mixing inside the instrument. It was found to be below $-140\text{dBc}/\text{Hz}$, which as indicated in section II is good enough at these levels.

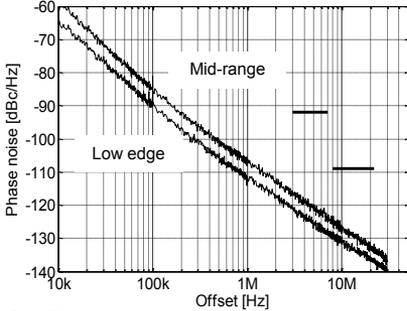


Fig. 5. Phase noise

The total power consumption can be seen in Fig. 6. The VCO consumes just under $90\mu\text{W}$ over the entire range. Note that the divider is biased 15% above its minimum operating current to ensure robustness.

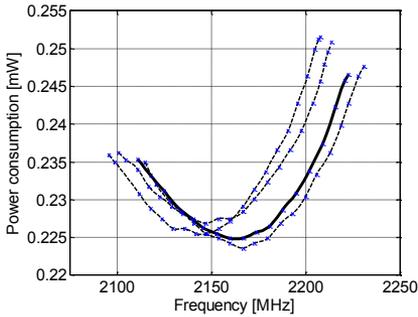


Fig. 6. Power consumption

The resulting figure of merit for the LO generator is between 179.5dB and 184dB , as shown in Fig. 7.

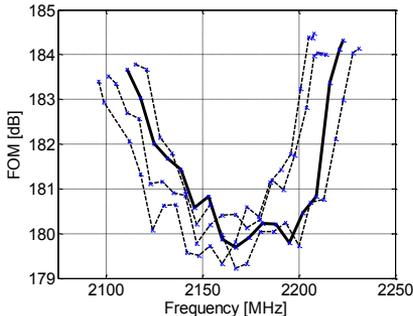


Fig. 7. FOM, LO generator

Since the VCO consumes less than half of the total power, its corresponding figure of merit should be more than 4dB

higher than the FOM for the circuit as a whole. The VCO figure of merit was found to vary between 183.5dB and 189dB .

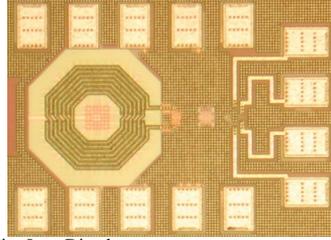


Fig. 8. Die photo

Fig. 8 shows the die photo of the manufactured circuit. The total area including pads is $0.53\times 0.38\text{mm}$.

VII. CONCLUSION

An quadrature LO generation circuit with an ultra-low power consumption of below $250\mu\text{W}$ has been demonstrated in a 65nm CMOS technology. Its application as part of a compact and low power secondary WCDMA receiver has been explored. The secondary receiver can be used to minimize power consumption of mobile equipment in common use cases.

ACKNOWLEDGEMENT

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Paper III

Paper III

A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS

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A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS

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Abstract — This paper presents a 2.45GHz ultra-low power direct conversion receiver front-end, intended for applications such as medical implants and body area networks. It consists of low noise amplifier, passive quadrature mixers, voltage controlled oscillator and frequency divider. Manufactured in 65nm CMOS it achieves 27dB gain, 9dB noise figure and S_{11} better than -14dB, while consuming below 400 μ W from a 0.8V supply. It has an in band and out of channel IIP₃ of -24.5 and -21dBm, respectively. Requiring only two inductors it occupies an area of less than 0.1 mm² excluding pads.

Index Terms — CMOS, frequency dividers, low-noise amplifiers, mixers, receivers, voltage-controlled oscillators.

I. INTRODUCTION

As we strive to integrate wireless technology as widely as possible, there are applications such as sensor networks that must be able to operate extended periods of time on a small battery, and where the physical size is of critical importance such as in medical implants and body area networks. Even though they don't need to communicate over large distances or with high data rates, it is still a challenge to implement circuits with minimal size and power consumption while still offering acceptable performance. This receiver front-end is intended to be part of a receiver that including digital baseband consumes below 1mW while occupying less than 1mm². The front-end can thus only consume part of this.

Since inductors are generally large and scale poorly with process node, we aim for a design that uses as few as possible, something that adds to the difficulty of high frequency low power design. To minimize the size of the full implementation, external components should be avoided as far as possible. This implies that the circuit should be able to provide input matching completely on chip, and that all analog parts of the receiver (including baseband components such as the ADCs) should operate off a single supply voltage.

II. FRONT-END

The front-end consists of a Low Noise Amplifier (LNA) and quadrature passive mixers. The quadrature local oscillator is generated by a frequency divider driven by a differential voltage controlled oscillator at twice the operating frequency. Generating the signal this way means that we only need a single inductor for the VCO, thus

saving space. Operating at a higher frequency the size of this inductor is further reduced. The front-end has a single-ended input to simplify the RF interface.

A. Low Noise Amplifier

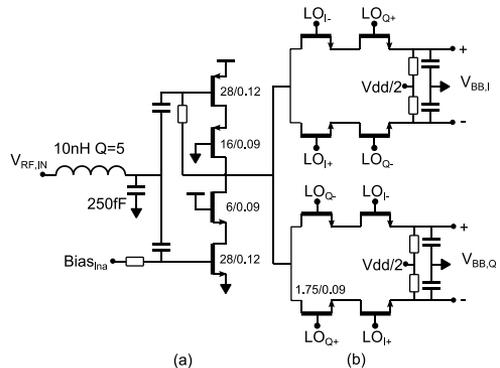


Fig. 1 (a) LNA schematic (b) Mixer schematic

There exist a few different methods that can be used to provide an LNA with resistive input impedance. To minimize area it is attractive to use inductorless techniques. The simplest technique is to simply terminate the input to ground with a 50 Ω resistor, but this solution tends to be excessively noisy [1]. Shunt feedback and common gate solutions instead provide an active current feedback path to set the voltage to current ratio at the input, and they will normally offer a better noise figure. The problem here is that the input impedance is dependent on the transconductance of the feedback path, and with a minimal supply current, we cannot achieve an input of 50 Ω . It appears that we will not be able to avoid the use of at least one inductor. Instead of an inductively degenerated amplifier a compromise is suggested in [2], where the input impedance is provided by the parasitic resistance of a single low quality inductor. The inductor provides voltage gain proportional to its Q value. This voltage gain increases the effective transconductance of the LNA, which improves the noise figure over a completely resistive termination. The advantage of using a low quality inductor is that it can be made unusually compact. In our circuit it consists of four layers with three windings in each of the top three layers, and a single winding below

that, achieving a 10nH inductance and Q of 5 while occupying an area of 0.0142mm². The input inductor is used with complementary common source stages with cascodes as seen in Fig. 1a. The current reuse that the complementary design provides means that more transconductance can be achieved for the same bias current.

B. Mixer

When designing for ultra-low power consumption a tradeoff with linearity is unavoidable. To minimize the risk for excessive sensitivity to interference, passive mixers is an attractive choice. Using such mixers the load capacitance is frequency translated to the input to form an impedance with a band pass characteristic [3]. Though the switch resistance sets a lower limit to this impedance, just reducing the amplitude of interferers by a few dB can be very valuable. An additional advantage of passive mixers is that they have little or no 1/f noise, which is especially advantageous in a direct conversion receiver. Quadrature sampling mixers can achieve very low insertion loss, but only as long as there is no overlap in the conduction period of each path [4]. This can be solved by providing LO signals with 25% duty cycle or by putting two switches in series to form an AND function between two phases of the reference [5]. The quadrature mixers are shown in Fig. 1b. The LO signals have been biased to Vdd through high pass RC filters.

C. Voltage Controlled Oscillator

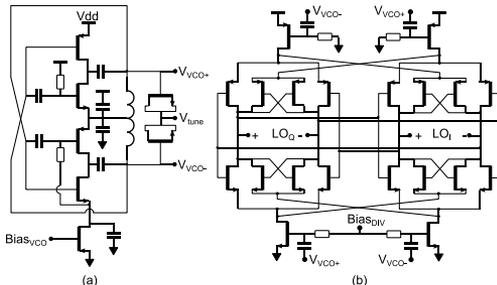


Fig. 2 (a) VCO schematic (b) Frequency divider schematic

The start-up performance of an oscillator is directly proportional to the transconductance of the devices. Since the transconductance is dependent on the bias current flowing through those devices it is easy to see that designing a VCO with ultra-low power consumption is a challenge. One strategy is to minimize the power supply while maintaining a relatively high supply current. To avoid the requirement for an additional supply voltage we would prefer to match the oscillator to the other

components of the receiver. To trade current for voltage we can employ current reuse techniques, such as a complementary push-pull configuration [6] or the technique in [7] where a single current path flows through the devices on both sides of the inductor.

We propose a solution (Fig. 2a) that combines both these techniques to achieve an additional level of current reuse, resulting in the same current flowing through all devices. This configuration has more advantages. Firstly the low current means that the energy lost in the tail current source is minimized, since the required drain source voltage is unchanged. Secondly, especially in combination with a triple-well process, good matching can be achieved, since identical NMOS and PMOS devices are used on both sides of the inductor. The VCO uses accumulation mode varactors.

D. Frequency Divider

When limiting the power consumption to this degree, even in an advanced process node the devices slow down significantly, and so we need a fast and efficient divider structure. Current mode logic (CML) structures [8] are commonly used where speed is of the essence. They do, however, waste a significant amount of energy by drawing a constant current, and from the voltage drop over their resistive loads.

We propose a fully complementary structure, as seen in Fig. 2b. In this solution the main switches only draw current during transitions, while the complementary device is turned off, meaning that nearly all current is flowing to or from the load. Furthermore, since the divider is fully complementary, each section of the divider is driven by both the positive and negative signals from the VCO. This leads to a reduced sensitivity to mismatch of the differential VCO outputs. The quadrature accuracy is now dominated by mismatch in the divider itself and the divider load. An additional benefit is that a complementary design can achieve a large output voltage swing, with simulations indicating that it can reach to within 100mV of each rail. A large swing is important to maximize the performance of the passive mixers.

III. MEASUREMENTS

The circuit was manufactured in a 65nm CMOS process from STMicroelectronics. For verification it was wirebonded directly to PCB. The mixer outputs were buffered using Analog Devices AD830 differential to single ended video amplifiers. To date only a single sample has been measured.

The power consumption of all parts of the front-end are shown in Table I. The frequency divider consumes 15μW

less at the lower end of the tuning range. For robustness, it has more than 16% margin over its minimum operating current over the entire tuning range. The VCO has a start-up power consumption above $36\mu\text{W}$ and it can drive the divider from $47\mu\text{W}$.

TABLE I
POWER CONSUMPTION

LNA	VCO	Divider	Total
100 μW	65 μW	230 μW	395 μW

As can be seen from the frequency tuning characteristic in Fig. 3, the circuit is capable of operating over the full 2.45GHz ISM band.

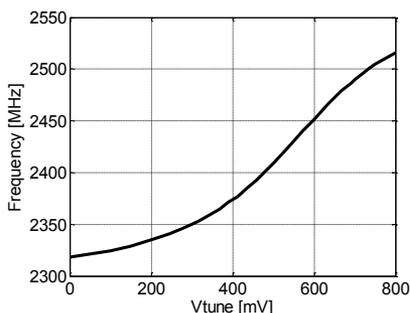


Fig. 3 Frequency tuning characteristic

The phase noise was measured on a downconverted tone using a spectrum analyzer. It was found to be better than $-106\text{dBc}/\text{Hz}$ at a 1MHz offset, over the entire tuning range, indicating the FOM for the LO generator is better than 179dB. As the VCO operates at twice the frequency we can assume its phase noise is better than $-100\text{dBc}/\text{Hz}$, indicating a VCO FOM greater than 186dB.

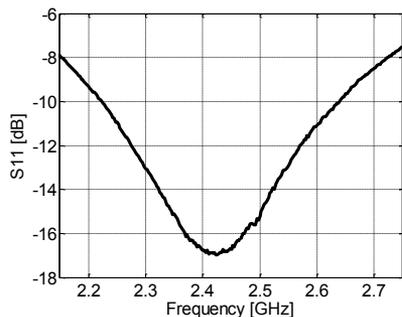


Fig. 4 Input matching

The input matching, S_{11} , is better than -15dB over the entire 2.45GHz ISM band, and equal to or better than -14dB over the full circuit tuning range (Fig. 4).

Fig. 5 shows the noise figure and gain of the front-end when operating mid-band. It achieves a gain of 27.5dB and noise figure below 9dB up to an IF of 1.8MHz.

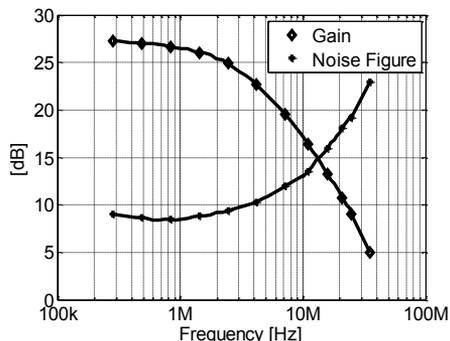


Fig. 5 Front-end conversion gain and noise figure

The input referred compression point was measured to -34dBm . The in band IIP3 was measured to better than -24.5dBm with tones at 1 and 1.2MHz offset. The in band IIP2 was measured to better than 0dBm with tones at 900kHz and 1.3MHz offset. The out of channel IIP3 and IIP2 were measured to better than -21dBm and 5dBm, respectively.

The quadrature phase error (Fig. 6) was measured to below 2 degrees and the quadrature gain error to below 1.1% over the entire tuning range.

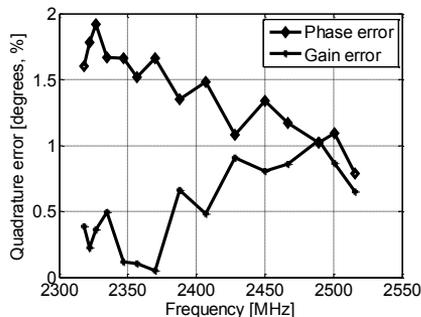


Fig. 6 Quadrature error

In Table II the performance is compared to recently published ultra-low power front-ends with integrated LO generation. The active areas have been estimated from chip photographs. As can be seen the area of the circuit is

clearly state-of-the art, and also the combination of noise figure, linearity and power consumption is highly competitive.

TABLE II
PERFORMANCE COMPARISON

	This work	[9]	[10]	[11]
CMOS process [nm]	65	130	90	130
Frequency [GHz]	2.45	1.6	2.2	1.6
Supply voltage [V]	0.8	0.25	1	1
Power [μ W]	400	352	1300	2000
Gain [dB]	27.5	41.8	27	42.5
NF [dB]	9	7.2	13	6.5
IIP3 [dBm]	> -24.5/-21	-35.8	-14.1 ^a	-30
IIP2 [dBm]	> 0/5	-	-	-
Active area [mm ²]	0.08	1.7	0.24 ^b	0.57

^a Estimated from CP_{1dB}

^b External inductor

Fig. 7 shows the die photo of the manufactured circuit. The total area including pads is 0.61x0.39mm. To the left and top right are banks of decoupling capacitors filling otherwise empty space.

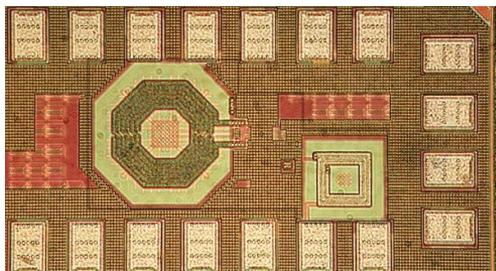


Fig. 7 Die photo

IV. CONCLUSION

A direct conversion receiver front-end with ultra-low power consumption, intended for operation in the 2.45GHz ISM band has been demonstrated in 65nm CMOS. Employing complementary current reuse techniques it achieves a power consumption below 400 μ W from a 0.8V supply. Using only two inductors, the active area is just 0.08mm². It shows competitive performance to recently published works, while occupying significantly less area.

ACKNOWLEDGEMENT

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Paper IV

Paper IV

A 0.55mW SAW-less Receiver Front-end for Bluetooth Low Energy Applications

C. Bryant and H. Sjöland, "A 0.55mW SAW-less Receiver Front-end for Bluetooth Low Energy Applications," *IEEE J. Solid-State Circuits* [Submitted]

A 0.55mW SAW-less Receiver Front-end for Bluetooth Low Energy Applications

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ABSTRACT

This paper presents an ultra-low power direct conversion receiver front-end operating at 2.6 GHz with high out-of-band linearity and low quadrature error. This is achieved through the use of efficient mixers with improved out-of-band suppression, and an LO generator achieving current reuse and rejection of VCO signal imbalance through the use of complementary devices. Manufactured in 65 nm CMOS and with a power consumption below 550 μ W from a 0.85 V supply, the front-end achieves a conversion gain of 41 dB and a noise figure of 9.6 dB. It has an out-of-band IIP₃ and IIP₂ of -3 dBm and 29.5 dBm, respectively. The quadrature phase error is below 0.6°. Requiring only two inductors it occupies an area of just 0.15 mm² excluding pads.

I. INTRODUCTION

As wireless technology becomes ever more ubiquitous there is increasing focus on portability, extending beyond purely cellular applications. With small and low cost radio circuits we enable communication with small devices around us or even on us. In many cases these devices should for maximum usability be able to operate extended periods, weeks, months or perhaps even years on a single battery charge, despite being small enough to fit virtually anywhere. An example of the current trend to portability is Bluetooth Low Energy (BLE), described in version 4.0 of the Bluetooth (BT) core specifications [1], which enables communication at significantly lower power consumption than classic BT. Many coming and recently released smartphones and tablets have support for Bluetooth version 4.0, and are thus prepared for communication with BLE (also known as Bluetooth SMART) devices. To enable connectivity with as many different devices as possible we need low cost circuits with very low power consumption. The radio transceiver is a major source of energy consumption in such a device, and

keeping it to a minimum is a considerable challenge. To further reduce the size and cost of the device, we want to minimize the external components required, including the SAW-filter at the antenna port. Operating without a SAW-filter in an electrically noisy environment puts high requirements on the receiver out of band linearity. In this work we demonstrate an LNA-less receiver front-end with a power consumption below 550 μ W achieving a noise figure of 9.6 dB and an out of band 1 dB compression point better than -15 dBm while operating on a 0.85V supply.

The paper is organized as follows. Section II presents the design specifications. Section III describes the architecture, design considerations and circuit implementations for the front-end and its building blocks. Section IV describes the LO generator. Experimental results are discussed in Section V, and a conclusion is given in Section VI.

II. SPECIFICATIONS

To understand the requirements of a Bluetooth Low Energy receiver, we should study the specifications given in [1]. BLE operates in the 2.4GHz ISM band, with channels spaced 2MHz apart. The specification defines a reference sensitivity level of -70 dBm with a bit error rate (BER) of 0.1%. The interference performance is specified for a wanted signal 3dB above this reference sensitivity. BLE uses Gaussian frequency shift keying (GFSK) modulation and a raw data rate of 1Mbps, similar to regular Bluetooth, except for a higher modulation index of 0.5 compared to 0.35 for Bluetooth (BT). Correct reception should be possible with an E_b/N_0 of 18dB for regular Bluetooth [2][3]. BLE is more robust due to its higher modulation index, resulting in a lower E_b/N_0 requirement. In [4] an SNR of 14dB is specified over a 1.25MHz bandwidth, which translates to an E_b/N_0 of 15dB. The maximum noise figure to meet the reference sensitivity can then

be calculated according to (1) where P_{SENS} is the reference sensitivity (in dBm), and BR is the bit rate. Section IV presents the design of the LO generator. Experimental results are discussed in Section V and the conclusion is given in Section VI

$$NF \leq P_{SENS} - \frac{E_b}{N_0} - 10 \cdot \log_{10}(BR) - 10 \cdot \log_{10}(kT) \quad (1)$$

$$= -70 - 15 - 60 - (-174) = 29dB$$

Interference can desensitize the receiver through different mechanisms. Intermodulation products from receiver non-linearity can appear in channel, large blockers can cause receiver gain compression, and phase noise from the LO generator can appear in-band through reciprocal mixing with an interferer. The maximum allowed NF is quite high, and so we will assume that the sensitivity is dominated by interference. If the thermal noise is at least 6 dB below the level of the interference induced noise, it will cause a less than 1 dB increase of the of total noise.

A. In-Band interference

Bluetooth modulated adjacent channel interferers are specified at 1, 2 & ≥ 3 MHz offset at power levels of -82 , -50 & -40 dBm, respectively. Apart from requiring a sufficient compression point, such interferers impose phase noise requirements on the LO-generator. Assuming a rectangular phase noise distribution over the receiver channel, the required phase noise at 1, 2 & 3 MHz offset is below -61 , -93 & -103 dBc/Hz, respectively. According to the intermodulation specification, the receiver should also tolerate two interferers each with -50 dBm power level, with the wanted signal 6 dB above the reference sensitivity. Including a 1 dB margin to account for the addition of thermal noise, this translates to an IIP_3 of -32 dBm.

B. Out-Of-Band interference

The Out-Of-Band (OOB) interference tolerance is specified for a desired signal in the centre of the band (2440MHz). The receiver should tolerate a single continuous wave (CW) tone with a strength as shown in table I.

A strong OOB blocker may desensitize the receiver front-end either from forcing it into compression or from reciprocal mixing with the LO phase noise at large frequency offsets. Additionally

TABLE I: Out-of-band blocker strength

f_{INT}	P_{INT}
30-2000 MHz	-30 dBm
2003-2399 MHz	-35 dBm
2484-2997 MHz	-35 dBm
3000-12750 MHz	-30 dBm

some of the blocker power may be rectified due to even order distortion, leading to a DC offset. As the specification assumes a CW blocker, the even order distortion will appear purely as DC, and strictly speaking it would be possible to meet the specification by simply removing it, for instance with a digital filter, or by employing the front-end in a low-IF architecture. In practice, however, most interference is in some way modulated, and the distortion products will be spread across a range of frequencies. If we make a rough worst case approximation and assume that the low frequency IM_2 energy is spread evenly across the entire channel we get an approximate IIP_2 requirement of 23 dBm for a -30 dBm interferer level. Since only one OOB blocker is specified, it doesn't impose any direct limit on IIP_3 . If a second blocker is allowed, a worst case scenario may be obtained with two -30 dBm tones. In this case the required IIP_3 is -3.5 dBm.

III. RECEIVER FRONT-END

When implementing a receiver without external SAW-filter, interference over a large bandwidth can enter the receiver with little attenuation. To handle this the receiver must have considerably better out-of-band linearity than otherwise. Since we have a strict power budget, we must use an architecture that limits the signal swing caused by interference. To achieve this as much of the filtering as possible should occur early in the receiver chain, before applying much gain. An attractive receiver architecture that can achieve good rejection of out-of-band interference is to do away with the LNA and instead to place a direct conversion passive mixer directly at the antenna port. The advantage is that the RF signal is converted to baseband almost immediately, before any gain is applied. At baseband it is considerably easier to provide narrow band filtering, and even the first order low-pass function provided by a direct sampling mixer can provide significant attenuation of out-of-band interference. While this configuration

generally has too poor noise figure for cellular applications, a short range radio standard such as Bluetooth requires significantly less sensitivity.

When demonstrating an ultra-low power receiver front-end, LO generation circuits including the VCO should be co-integrated to obtain a fair comparison, since a strong external LO could otherwise hide a major source of power consumption. Fig. 1 shows the structure of the implemented receiver front-end. It consists of quadrature passive sampling mixers for zero IF conversion, and baseband amplifiers to provide voltage gain. The mixer input impedance is matched to 50Ω through a matching network, which also provides about 9 dB voltage gain. The inductor of the matching network is a tightly wound coil with ten turns, using one thin and two thicker metals connected in parallel. The conductor is $2.4\mu\text{m}$ wide, with a spacing of $0.6\mu\text{m}$. The top aluminium layer is not used since it requires a considerably larger spacing and would not allow for such a compact coil. A metal ground shield in metals 1 & 2 is used below the coil. FastHenry simulation indicates an inductance of 10.6 nH , a self resonance frequency of 6.36 GHz , and a Q of 10.7 at 2.5 GHz . The LO generation circuit consists of a VCO operating at twice the LO frequency and a frequency divider to provide the quadrature LO signals. The LO signals are biased to V_{DD} through high pass filters before being fed to the mixers.

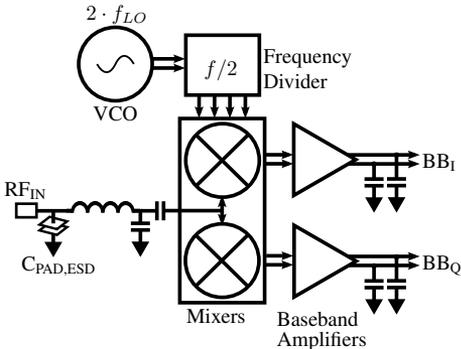


Fig. 1: Receiver Front-end and LO generator

An advantageous property of the direct sampling mixer is that since it lacks reverse isolation, the input will be affected by the load impedance. A capacitive load at baseband will thus appear at the input as an impedance with band-pass character around the LO frequency (Fig. 2). This effect can

help suppress interference outside the channel of interest already at the mixer input. The filtering properties of this type of mixer has been derived in [5], [6].

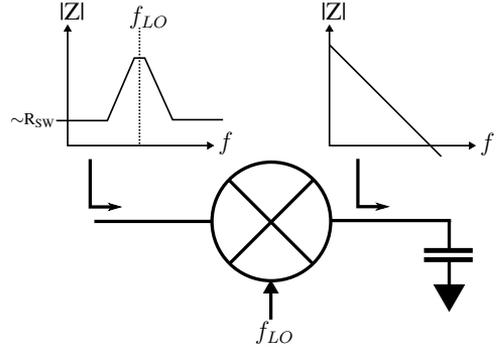


Fig. 2: Mixer input impedance due to frequency translation

Since no gain is provided until after the mixer, the out-of-band interference tolerance will be determined almost entirely by the nonlinearity and filtering properties of the passive mixer. In other words, to minimize sensitivity to out-of-band interference, we should ensure the maximum possible impedance ratio at the mixer input between the in-channel and out-of-band frequencies. The limiting factor here is the resistance of the switches in the conductive state (on-resistance), providing a lower bound to the input impedance (Fig. 2).

A. Mixer

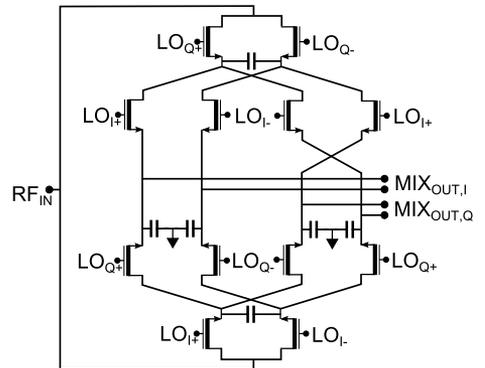


Fig. 3: Mixer schematic

A problem of quadrature passive mixers is that if there is overlap in the periods when switches in the I (In phase) and Q (Quadrature phase) branches conduct, a current can pass between the output capacitors of the different outputs, discharging some of the stored charge, increasing the mixer attenuation and noise figure [7]. This is usually solved by providing rectangle wave clock pulses with 25% duty cycle to the switch devices [8]. With four phases there is no instance when the clock pulses overlap. Providing clock pulses with 25% duty cycle requires, however, a more complex LO generation. Either we have to supply a frequency divider capable of delivering the required clock pulses directly, or we need clock buffers with AND gates or similar.

A different approach to providing non-overlapping conductive periods is to put two switch devices in series in each branch (Fig. 4a), driven by different phases of the LO, thus incorporating an AND-function in the mixer [9]. Each path conducts in the period when both devices are on, as illustrated in figure 4b. All four LO phases are illustrated, together with a line through the center representing the switch threshold. The filled black areas mark the period when both switches conduct.

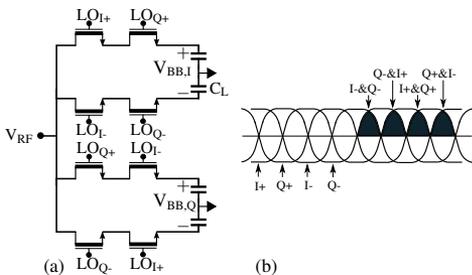


Fig. 4: Single balanced and-function sampling mixer

The advantage of this type of mixer is that it can be driven by overlapping LO signals, such as square waves (50% duty cycle) or sine waves. In other words, it can be driven directly from almost any type of quadrature LO source. This is particularly useful when designing a receiver (transceiver) for operation with very low power consumption. Firstly it is easier to produce a symmetric waveform, since it contains less high frequency components. Producing the 25% duty cycle wave for use with a regular mixer requires a circuit with fast time constants

to handle the short pulse period. Secondly, with a severely restricted power budget it is advantageous to concentrate the supply current to as few blocks as possible. This way each block can be as large as possible, minimizing the effects of mismatch, and have as large signals as possible, providing reliable and low noise operation. Parasitic capacitance comprises a significant part of the total load that each block has to drive (including its own), and using more blocks than necessary will create more paths with parasitic capacitance. This could lead to reduced reliability due to unintended coupling paths and/or increased power consumption.

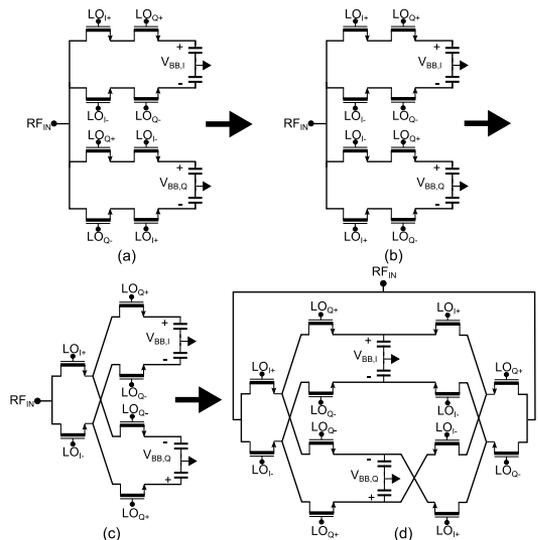


Fig. 5: Optimizing and-function mixer

The disadvantage of the mixer in fig. 4 is that since there are two devices in series it has relatively high series resistance, increasing the minimum noise figure as well as degrading the input filtering properties. If we are to manage without an LNA with this type of mixer, we should find ways to reduce the series resistance. The original AND-type mixer shown in fig. 5a is organized so that the LO signals in each path occur in the same order, to ensure symmetry. If we for a moment ignore symmetry and change the order of the LO-signals on one side (fig. 5b), we see that there are now two pairs of devices closest to the RF port that are clocked by the same phases of the LO. By merging these (fig. 5c) the switch resistance has been reduced by 25% without any change in the

total size of the mixer. The problem is that the mixer is now asymmetrical. This is especially detrimental in a zero-IF architecture, where asymmetry will lead to I/Q imbalance, DC-offsets and increased LO leakage through the RF port. To solve this we split the mixer into two halves clocked in opposite orders (fig. 5d). For example there is a path on one side clocked from input to output with LO_{I+} to LO_{Q+} . In the other mixer half there is a corresponding path clocked in the reverse order (LO_{Q+} to LO_{I+}). Both paths conduct simultaneously, and now all paths are fully symmetrical.

A second technique we propose to improve the operation of the AND-type mixer involves placing capacitors (C_P) across the intermediate nodes of the mixer (Fig. 6d). These capacitors are small compared to C_L , since the mixer is sensitive to parasitic capacitance to ground at these nodes. Since they are small they mainly effect the mixers at higher IF frequencies, such as out of band.

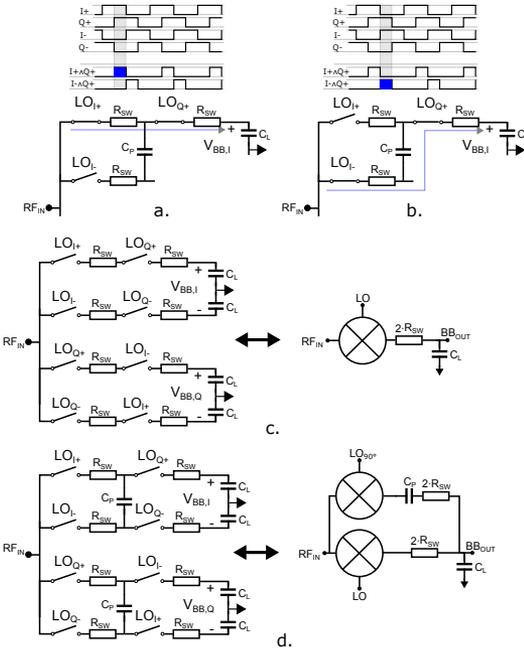


Fig. 6: Modeling and-mixer with extra capacitors

To understand the effect of the capacitors, consider fig 6a,b, which show part of the mixer coupling to one of the outputs. In fig. 6a we see the time instant when the mixer is conducting through the

normal path (LO_{I+} & LO_{Q+}), and in fig. 6b we see the next time instant when the LO_{I+} switch has opened, and where instead we have a path to the load through LO_{I-} , LO_{Q+} and the capacitor C_P . These operations occur 90° apart relative to the LO, and it is observed that their charge contributions to C_L are largely independent. In fig. 6c a simple model of the mixer is shown, including the effect of switch resistances (R_{SW}). In fig. 6d the capacitors C_P are included in the schematic, and as their effect is largely independent from the usual mixer operation, they are modeled by a separate path with a mixer driven by an LO signal shifted by 90° . We can see that C_P has little or no effect close to the LO frequency. Out-of-band, however, the second path substantially halves the effective switch resistances, improving the suppression of interference at the mixer input by up to 6dB.

The extra capacitors have the additional advantage of suppressing second harmonic downconversion. Signals at twice the LO frequency will in a regular single balanced mixer be converted to a common-mode signal at the output. This could create unwanted intermodulation products, or leak directly into the signal path through finite common-mode suppression in the baseband amplifiers. To understand how the second harmonic signal is suppressed, consider Fig. 7. For each period of the LO the RF port is exited with two periods. We will be looking at the four mixer states that occur for each LO period. For illustration we have assumed here that the second harmonic starts by going high during the first state. We see that a charge is then pushed into one of the load capacitors (C_L). In state two a path conducts across C_P while the RF port is low, discharging C_L . In state three the other load capacitor is charged. In state four it is discharged through C_P . This will also remove the charge stored in C_P during state two, since the current through the capacitor is in the opposite direction. From this it is clear that C_P will prevent charging of C_L , and no voltage will then build up at the main output.

Fig. 8 shows the input impedance of a mixer with $R_S = 1k\Omega$, $C_L = 25pF$ and R_{SW} of 100Ω with and without the capacitors C_P . We see that without C_P the input impedance is high around the second harmonic, since the energy is not dissipated. When adding C_P , we can observe that not only is the input impedance halved for frequencies far from f_{LO} , but the peak at $2 \cdot f_{LO}$ is now gone.

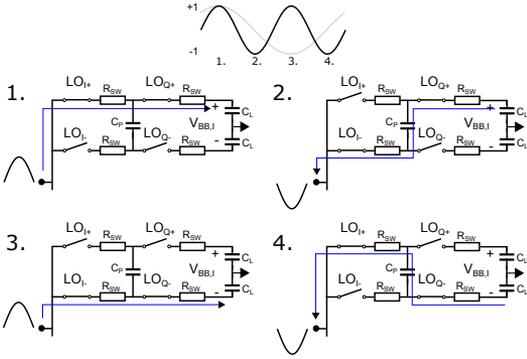


Fig. 7: Suppression of second harmonic down-conversion

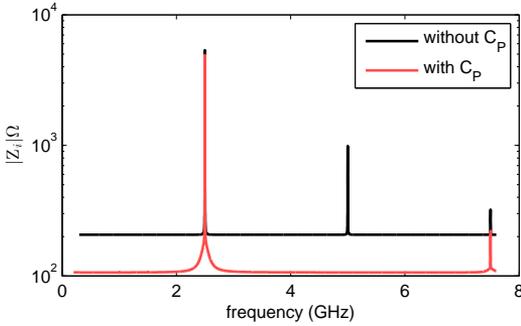


Fig. 8: Simulated mixer input impedance vs. frequency with & without C_p

Combining both these techniques we arrive at the implemented mixer structure shown in Fig. 3.

B. Baseband Amplifiers

With no LNA at RF, the main noise contributors are the mixers and baseband amplifiers. To keep the noise figure as low as possible the baseband amplifier (Fig. 9) input devices should have as high transconductance as possible, which is achieved with a single stage design. By making the devices $3\ \mu\text{m}$ long the complementary devices achieve high output impedance, resulting in a voltage gain of over 26 dB. Large area devices also keep the flicker noise low, and ensures good matching. The feedback resistors R_F are primarily for biasing purposes, and are made large enough to have only a minor effect on the amplifier gain. The common mode feedback (CMFB) has 36 dB loop gain at DC, and for stability

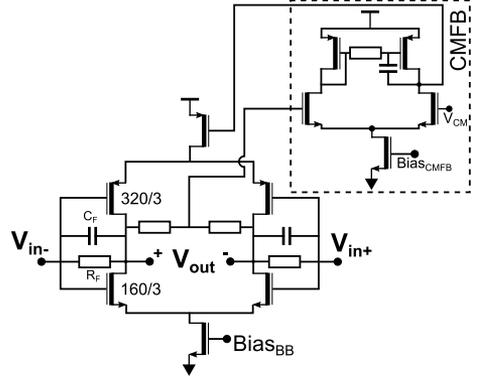


Fig. 9: Schematic of the baseband amplifier

it is compensated with a resistor and capacitor placed in the current mirror.

IV. LO GENERATION

The LO signal generation is the dominant source of power consumption in this circuit, having to drive the relatively large passive mixers. A low quadrature error and good LO symmetry is advantageous to ensure maximum performance. This is difficult to achieve in low power design, since the devices used are small, making them susceptible to mismatch as well as parasitic capacitances that risk forming unintended coupling paths.

There exist a couple of different approaches to generating a quadrature LO signal. The most common methods are by means of a quadrature oscillator, or with a frequency divider operating from a single VCO at twice the frequency. Initially the quadrature VCO approach seems most attractive. All output nodes are connected to a resonance circuit, which is generally more power efficient, since energy is kept in storage and not immediately dissipated. The resonant loads additionally mean that the LO generation can be operated on a very low supply voltage. There are two problems with this approach, however, which favor the alternative solution with a frequency divider. Firstly we are striving for a cheap and thus small design. This effectively means that we try to avoid the use of inductors as far as possible, since they scale poorly with advancing technology nodes. A quadrature VCO requires two VCO cores with at least one inductor each. The divider based solution only

requires a single VCO core, and this operates at twice the frequency, further reducing the required area. Secondly isolation should be provided between VCO and RF circuits, especially in the case of a direct conversion receiver. Without sufficient isolation to the RF path the VCO is potentially susceptible to injection locking from strong interferers. As it turns out, simulations indicate that providing the isolation by inductorless LO buffers strong enough to drive the passive mixers in the receiver, require a similar amount of power as a frequency divider with the same driving strength.

For reasons of simplicity and minimizing the number of external components, we wish to use a single supply voltage for the entire circuit. A largely inductorless low power circuit will make extensive use of complementary devices (NMOS & PMOS). To make the RF parts operate well at the frequencies used in this design we require a supply voltage of at least 0.8V. A higher supply voltage has the advantage that we can handle larger voltage swing, thus making it easier to provide good linearity. The performance can be further helped by the inherent symmetry of a complementary design. The LO generator, consisting of oscillator and divider is shown in fig. 10. It uses an architecture presented in [10].

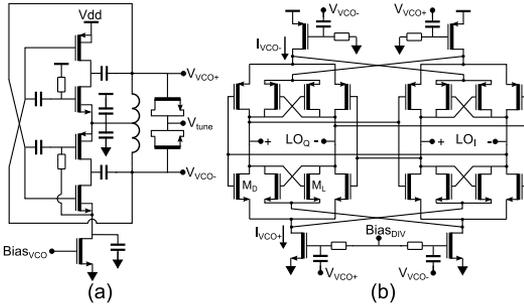


Fig. 10: LO generator circuit. (a) VCO (b) Divider

A. VCO

The lower limit for the power consumption of the VCO is determined by the point where the oscillator loop gain drops below unity, and where oscillation cannot be maintained. The loop gain, as we see from (2)

$$A_{start-up} = g_m \cdot R' = g_m \cdot \omega_0 \cdot LQ > 1 \quad (2)$$

is given by the transconductance of the devices in the VCO core, as well as the load impedance presented by the resonant tank. Additionally, the output swing is determined by the bias current and load impedance, and it has to be sufficient to reliably drive the frequency divider. We see that in order to minimize the power consumption we need an inductor with a high LQ product. It should also preferably have a high Q value to minimize the phase noise.

The inductor is a custom designed differential coil with five turns in one thin metal, two thick metals, and the top aluminium metal layer connected in parallel. The conductor has a width of 4 μm and the spacing between turns is 3 μm . It has a ground shield in interleaved strips of metals 1 & 2, patterned according to the simple ground shield of [11]. Due to an initial modeling error of the VCO inductor, the operating frequency is slightly higher than intended. Since then the inductor has been remodeled with a more accurate representation, verified by simulations in FastHenry and Momentum. The new model also corresponds well with measured receiver performance. It has an estimated inductance of 3.7 nH, a Q value of 17.9 at 5 GHz, and a self resonance frequency of 10.5 GHz.

A possible strategy for maximizing the VCO performance with a low power consumption is to lower the supply and increase the current draw. This will not only improve the transconductance, but also increase the output swing to supply voltage ratio, resulting in improved efficiency. We, however, prefer operating the front-end on a single supply voltage. To achieve this and still maintain the same low power consumption we need to employ some sort of current reuse technique to maximize the transconductance for a given supply current, and to improve the efficiency. Existing techniques include the complementary push-pull configuration [12] and the technique in [13], where a single current flows through the devices on both sides of the inductor. We have chosen a combination of both these techniques, to achieve an additional level of current reuse (Fig. 1b). In this solution the same supply current passes through all devices of the VCO, giving high loop gain for minimal current consumption. The effective supply voltage for each NMOS, PMOS inverter is less than half of the total supply voltage, allowing high efficiency at reduced output swing. An additional advantage is that since

both n-type and p-type devices are connected to both sides of the resonant tank, it can achieve a higher degree of symmetry than the single stacked solution. The symmetry is improved further with a triple-well implementation, isolating the bulk of the NMOS devices from the substrate.

Another way of arriving at the proposed solution is to start with a simple push-pull oscillator (fig. 11a). We then separate the supplies for each side, so that one pair is fed from V_{dd} to $V_{dd}/2$, while the other side is fed from $V_{dd}/2$ to ground (fig. 11b). In essence we have placed both pairs in series with $V_{dd}/2$ as an intermediate node. By now decoupling the intermediate node and removing some unnecessary components, we arrive at the final solution (fig. 11c). The VCO uses accumulation mode varactors as they have suitable tuning characteristics with one terminal connected to $V_{DD}/2$, with V_{SG} in the range $\pm V_{DD}/2$ [14].

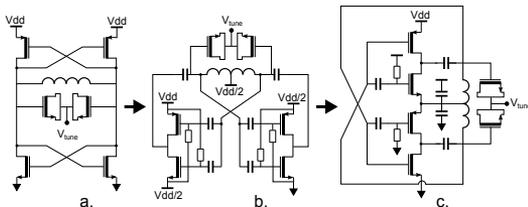


Fig. 11: Deriving the VCO structure

B. Divider

there are many different frequency divider topologies, usually based on either injection locked oscillators [15] or static dividers using digital logic [16]. The digital approach is natural when aiming for the smallest possible area, since no inductors are required. Since a digital frequency divider has to handle quickly toggling signals they are often implemented with current mode logic (CML) which can achieve high speed. This is, however, not the most power efficient, since CML draws a constant current and uses resistive loads. Our divider is based on a common approach with a master-slave topology. This is typically implemented in CML, but we have instead made it fully complementary (Fig. 10b), making it behave more like regular CMOS logic. It thus only draws current during transitions, and nearly all current flows to and from the load. With the complementary devices working in tandem, we

also get more transconductance for a given current consumption. Additionally, with devices that both push upwards and pull downwards, we can achieve high output swing with a limited supply voltage. In fact, simulations indicate that in our case the output can reach to within 100 mV of each rail in normal operation.

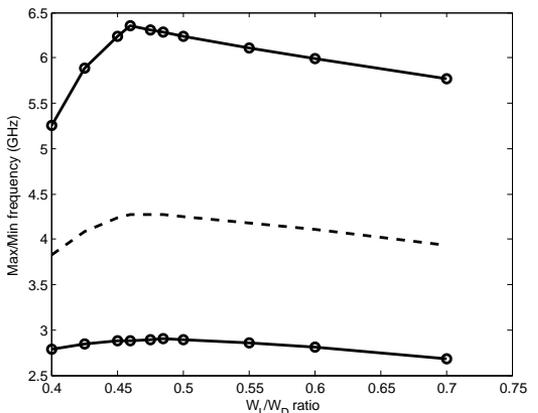


Fig. 12: Simulated maximum & minimum divider input frequency vs. W_L/W_D ratio for a VCO amplitude of 190 mV (one side). The dashed line indicates the geometric mean.

A divider of this type is most sensitive to the input signal at a certain frequency, depending on design and bias points. An important design choice is the ratio between the devices that couple between the two halves of the divider (M_D) and the latches (M_L). If the latches are made too small they will not store enough energy, while if they are made too large, too much energy is required to set the state of the latches. It has been found in similar CML-based dividers that there is an optimum W_L/W_D device ratio close to 0.5, where the divider is sensitive to the broadest possible range of input frequencies [17]. Fig 12 shows simulated maximum and minimum frequencies where the divider can operate for an input amplitude of 190 mV, with varying ratio device width ratios (W_L/W_D). The dashed center line shows the geometric mean of maximum and minimum frequencies. It can be seen that the largest frequency range is achieved with a W_L/W_D ratio of 0.46, but a ratio of 0.5 was chosen to simplify the layout, and to provide some margin to the sharp roll-off that occurs for smaller than optimum devices.

A fully complementary implementation has a further and not immediately obvious advantage. Since each section of the divider is driven roughly equally by both the positive and negative signals from the VCO, asymmetry in the VCO signal is suppressed. This feature is especially useful in this design, since the VCO used will never be completely symmetric. To better understand how input signal asymmetry can be suppressed we should consider how the VCO signal is injected into the divider. As the NMOS devices pull current, the PMOS devices push, resulting in a signal injected with the opposite sign. In Fig. 10b we see that V_{VCO-} and V_{VCO+} work in tandem ($V_{VCO+} = -V_{VCO-} \rightarrow I_{VCO+} \approx I_{VCO-}$), driving the same parts of the divider. Basically the PMOS devices are supplying an inverted copy of the currents injected by the NMOS devices. If the inverted currents are equal, any difference in V_{VCO-} compared to V_{VCO+} will affect both sides of the divider the same, and will thus not contribute any quadrature error.

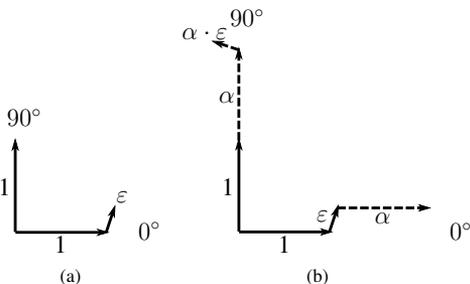


Fig. 13: Illustration of VCO imbalance propagation through a complementary divider. The solid lines indicate the contribution to I and Q LO-signals through NMOS devices, and the dashed lines contributions through the PMOS devices

We have seen that if the injection paths are perfectly matched they can completely remove the imbalance coming from the VCO. The remaining error will thus be due to imbalance between the NMOS and PMOS paths. In an NMOS only divider V_{VCO+} will contribute mainly to two of the output phases, while V_{VCO-} contributes to the remaining two. In fig. 13a output signals are represented by two vectors with amplitude 1. One vector is the in-phase output, controlled primarily by one of the input signals, the other is the quadrature phase output, controlled primarily by the other input signal. Let

us assume that there is a VCO imbalance resulting in a quadrature error in phase and amplitude that we represent with the vector ϵ placed on one of the quadrature outputs. Now let us assume that the VCO signals also contribute to the outputs through the PMOS paths (dashed lines) by a factor α (Fig. 13b). Since the quadrature error emanates from one of the input signals, it will now be present on both the outputs, scaled by α . In the case $\alpha = 1$ the paths are perfectly matched and we expect the error, ϵ , to be fully suppressed, since it contributes exactly equally to both I and Q outputs. Investigating the difference in the residual quadrature error $\Delta\epsilon_{90^\circ} = \epsilon \cdot (1 - \alpha)$. The injected signals will be increased due to the extra injection paths by a factor $1 + \alpha$, and so the relative quadrature error will be $\epsilon \frac{(1-\alpha)}{(1+\alpha)}$ compared to the NMOS only case where the error is ϵ .

The error coupling $\left| \frac{(1-\alpha)}{(1+\alpha)} \right|$ as a function of α is shown in Fig. 14. We can see that when the PMOS device paths are matched to within $\pm 50\%$, the VCO imbalance is suppressed by more than 66%. With high suppression the quadrature error will probably be dominated by mismatch in the divider itself. When $\alpha = 0$ or goes to infinity, there is no suppression of VCO error. This is expected, since $\alpha = 0$ indicates that there is no PMOS path, and when $\alpha = \infty$ there is no NMOS.

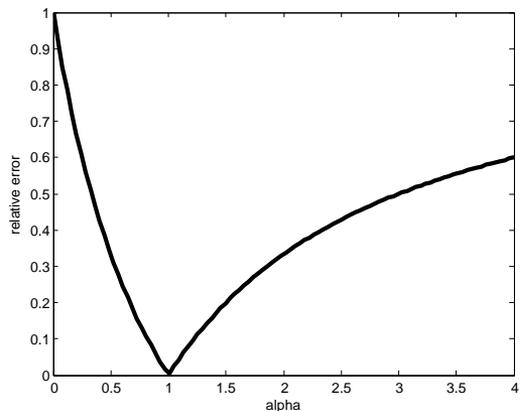


Fig. 14: Suppression of VCO imbalance vs. PMOS/NMOS injection ratio

V. MEASUREMENT RESULTS

The receiver front-end was manufactured in a standard 65 nm CMOS process with eight metal layers, MIM capacitors and triple-well. All pins are attached to ESD protection diodes. Fig. 15 shows the die photo of the receiver, which occupies an area of $0.73\text{mm} \times 0.4\text{mm}$ including pads. The active area (dashed) is just below 0.15mm^2 including on-chip decoupling. The circuit was wire bonded directly to a two-layer PCB. The baseband outputs were buffered by AD812 operational amplifiers configured as voltage followers, and then converted to a single ended output with AD830 video difference amplifiers. The input matching is achieved entirely on chip, i.e. no matching components were used on the PCB. Most measurements were performed on three samples.

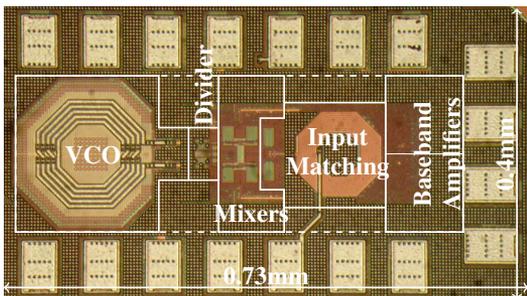


Fig. 15: Die Photo of the front-end with a visible area of $0.73 \times 0.4\text{mm}$

The VCO, divider and baseband amplifiers consume below $95\ \mu\text{W}$, $355\ \mu\text{W}$ and $100\ \mu\text{W}$, respectively, resulting in a total power consumption less than $550\ \mu\text{W}$.

Fig. 16 shows the tuning characteristic for all three samples, measured using a signal generator to produce an input signal and a spectrum analyzer to study the resulting output. As previously explained the circuit is tuned high, and operates above the 2.4 GHz ISM-band. It should, however, be easy to lower the VCO frequency in an updated design. Lowering the operating frequency should also reduce the power requirements of the frequency divider. The circuit currently operates from below 2.5 GHz to about 2.7 GHz.

The input reflection coefficient was measured with an R&S ZVC vector network analyzer. Fig. 17a shows the behavior of S_{11} for different varactor

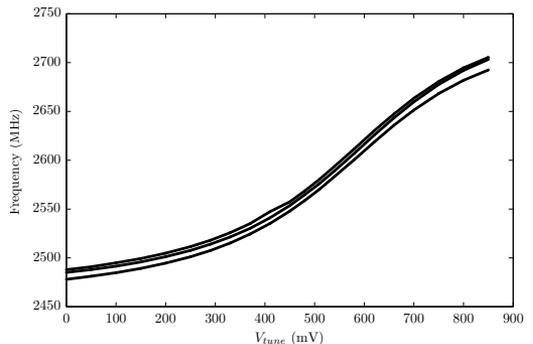
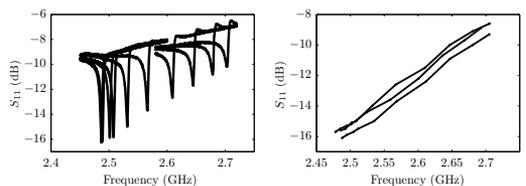


Fig. 16: Operating frequency vs. tuning voltage



(a) S_{11} for different tuning frequencies (b) In-channel input reflection coefficient vs. frequency

Fig. 17: Input matching measurements

tuning voltages of one sample. In Fig. 17b only the in-channel (close to the LO frequency) reflection coefficient has been plotted versus operating frequency. This indicates how well matched the receiver is for wanted signals. We can see that the receiver front-end is well matched in the lower frequency range close to the intended 2.4 GHz ISM-band. Even though the circuit is operating at higher frequency than intended, S_{11} is still better than $-10\ \text{dB}$ over most of the tuning range.

The noise figure and gain were measured using an R&S FSEB spectrum analyzer. Measurements of all three samples operating in the middle of their tuning range ($V_{tune} = 580\text{mV}$) are shown in Fig. 18. The conversion gain reaches about 41 dB with a $-3\ \text{dB}$ bandwidth of 1.15 MHz, while the noise figure is below 9.6 dB at its best. The noise figure is below 10 dB between 150 kHz and 1.5 MHz, and at 30 kHz it has increased by 3 dB. Simulations indicate that the low frequency noise mainly comes from amplitude noise of the frequency divider. The dashed lines show the gain and noise figure predicted by simulations.

The linearity measurements were taken with the

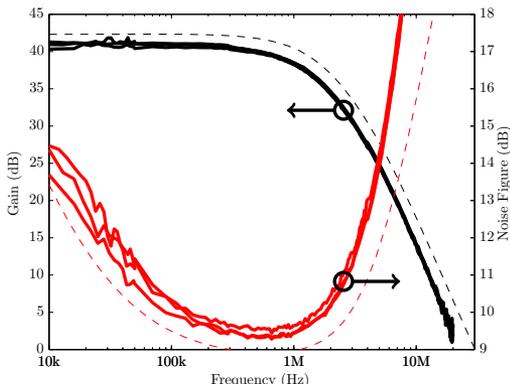


Fig. 18: Noise figure and gain vs. output frequency measurements (solid) and simulations (dashed).

receiver front-end operating in the middle of the tuning range, while sweeping the frequency of the interfering signals. The compression and two-tone measurements were performed with a spectrum analyzer and one or two signal generators, all automated through GPIB commands issued from a Matlab script. A first impression of the large signal handling is provided by the compression point. A single tone was thus applied to the RF input at increasing offset frequencies, and at each frequency the power was swept. The resulting 1 dB compression point for all three samples is shown in Fig. 19. All curves are for the upper sideband, but the lower sideband behaves in a near identical way. We can see that the input referred 1 dB compression point is about -41 dBm in-channel and increases with offset frequency. At 3 MHz offset it is better than -31 dBm, and at 10 MHz it saturates at about -15 dBm. When the gain is high the compression point is limited by the voltage swing at the output. The dotted line shows the response predicted by the front-end conversion gain. Eventually, as the conversion gain drops, it is instead limited by the mixer, causing the curve to saturate.

The third order intercept measurements were performed by applying two tones at the RF port with frequencies such that a third order intermodulation product appears at a set frequency in-channel. In this case the frequency of the down converted intermodulation product f_{IF} was kept constant at 250 kHz, while the two interfering tones were placed such that $f_{LO} + f_{IF} = 2 \cdot f_{inner} - f_{outer}$ while varying f_{inner}

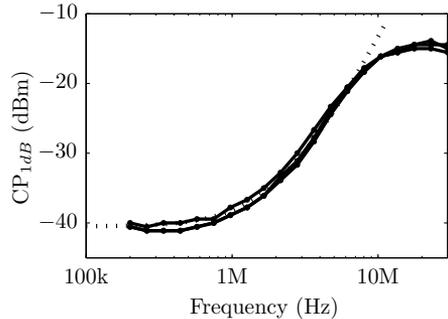


Fig. 19: 1dB compression point vs. offset frequency

& f_{outer} relative to f_{LO} . At each point the input power was swept, and the measurements closest to forming a third order slope extrapolated. The extrapolation was compared to the gain in-channel to get a measurement of the effective intercept point. Fig. 20 shows the effective input referred IP_3 for all samples versus the frequency of the outer tone, f_{outer} . Though the tones are attenuated by different amounts at the output of the front-end, the behavior is very similar to that of the compression point. We can observe that IIP_3 is about -30 dBm in channel, and increases while moving further from the operating frequency, until it saturates at 10 MHz at about -3 dBm. The difference between the 1 dB compression point and IIP_3 is close to the often observed 10 dB.

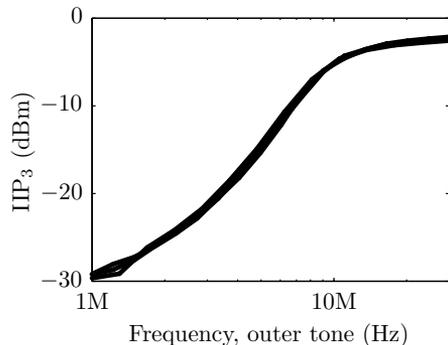


Fig. 20: IIP_3 vs. offset frequency

The quadrature error was measured by applying a tone at the RF port at a small offset compared to the LO, resulting in an IF frequency of 200 kHz. The I and Q baseband outputs were recorded with a Tektronix TDS 7404 digital oscilloscope, and FFT's

of the signals were then compared to each other in Matlab[®]. The resulting quadrature phase error (Fig. 21a) is below 0.6° for all three samples over the entire tuning range, while the amplitude error (Fig. 21b) stays below 3%. This corresponds to an image rejection ratio better than 36 dB.

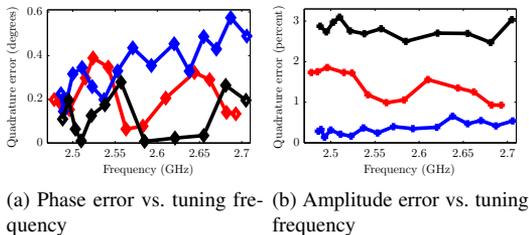


Fig. 21: Quadrature error measurements

Like IIP_3 the second order intercept point was measured at varying offsets from the carrier frequency. The two tones were placed at 100 kHz above and below the reported offset frequency, placing the measured IM_2 product at an IF frequency of 200 kHz. A power sweep was made for each offset frequency, and the region close to a second order slope was isolated. Fig. 22 shows the second order intercept point for all three samples for varying offset frequency. Close to the carrier frequency IIP_2 is better than 0 dBm, improving rapidly until saturating at about 5 MHz offset with all measurements better than 29.5 dBm.

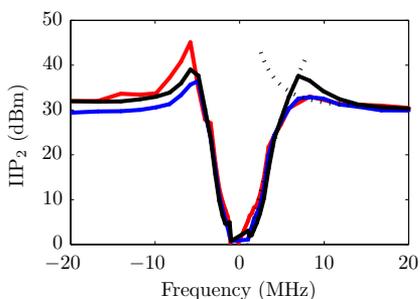


Fig. 22: IIP_2 vs. offset frequency. Dotted lines show response predicted from amplifier gain & (5)

Close to the LO frequency the gain is high and the second order distortion is dominated by the base-band amplifiers. Further out, where the conversion gain is low, it is instead dominated by the mixers, and at high offsets the mixer linearity levels out.

To understand why this happens consider the output of the mixer for large offset frequencies as a low pass RC filter with a non-linear resistance. If we excite the filter with a voltage V_S , a current I_S will flow through R and C according to (3). At low output frequencies the current flowing will be very small, as the capacitors dominate the impedance. As the frequency increases the current will saturate to a value set by the resistance. Second order non linearity in the resistance will create a voltage V_D proportional to I_S squared (Eq. 4). Since the IM_2 product of interest appears in-channel at fixed frequency, the RC filter will have little further influence. Thus, the out of band IIP_2 due to the mixer output will act approximately as (5), starting high and tapering off to a constant value. The mixer IIP_2 will also depend on matching, since in a mixer free from mismatch the IM_2 generated at the output will be a pure common mode signal.

$$I_S = V_S \cdot \frac{j\omega_{IF}C}{1 + j\omega_{IF}RC} \quad (3)$$

$$V_D \propto I_S^2 \quad (4)$$

$$IIP_{2,OOB} \propto \left| \frac{1 + j\omega_{IF}RC}{j\omega_{IF}C} \right|^4 \quad (5)$$

Apart from the effects described above there are complex interactions between different distortion products. Since the sign of the second order product is set by mismatch and hence random, there may be points where IM_2 products from the mixer and amplifier happen to cancel, creating random peaks in the IIP_2 response.

To judge the tolerance to the strongest out of band blockers, noise figure measurements were made while applying a tone 400 MHz below the operating frequency of 2.58 GHz. To make sure that wideband phase noise from the signal generator wouldn't dominate the measurement, it was filtered through a custom made filter, providing 26 dB and 9.5 dB suppression at the LO frequency and the third harmonic of the LO, respectively. The noise figure was measured at an IF frequency of 300 kHz with a resolution bandwidth of 30 kHz. With a narrow measurement bandwidth and a DC-blocker to protect the spectrum analyzer the result is not influenced by DC signals, but does tell us how the receiver is influenced by gain compression and wideband phase noise. Fig. 23 shows the resulting noise figure for

TABLE II: Comparison to other published works

Ref.	Tech.	f (GHz)	Supply (V)	Power (mW)	CG(dB)	NF(dB)	IIP ₃ (dBm)	IIP ₂ (dBm)	Area (mm ²)	Comments
This work	65 nm	2.6	0.85	0.55	41	9.6	-30/-3	0/29.5	0.15	channel/OOB
[18] 2011	130 nm	1.6	0.25	0.35	41.8	7.2	-35.8/	-	1.7	NF @ 10 MHz
[19] 2013	65 nm	2.45	0.6&1.2	2.7	55	9	-6	-	0.26	OOB linearity
[20] 2013	65 nm	2.45	0.3	1.5	20.7	5.1	-21.5/	-	0.85	IF amp. excluded
[21] 2012	180 nm	2.45	1	0.7	36	18.2	-4	-	0.8	External Ref. OOB
[22] 2011	90 nm	2.45	1.2	4.7	30	7.5	-16.2/	14.4/-	0.74	External Ref.
[5] 2006	130 nm	2.38	0.6	0.75	-	5.1	-7.5/	-	0.7	

varying blocker strength. The receiver is desensitized by less than 1 dB at -23.5 dBm input signal power, and does not reach the maximum tolerable noise figure even at the highest measured blocker level of -6 dBm, significantly greater than the -30 dBm requirement. With a blocker of -10 dBm the noise figure is below 18 dB, which satisfies the largest out of band blocker requirements of even the regular Bluetooth specifications.

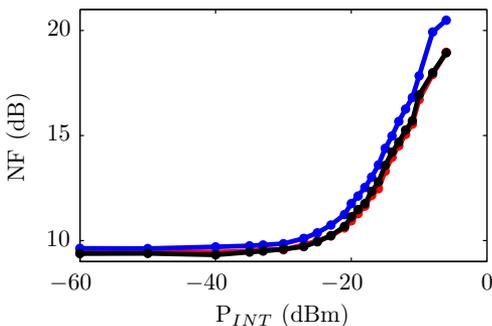


Fig. 23: Measured noise figure with out of band CW blocker at 400MHz below operating frequency

The phase noise was measured on a downconverted tone using a spectrum analyzer. At 1 MHz offset it was found to be below -105.7 dBc/Hz when tuned to 2.6 GHz, and better than -107.3 dBc/Hz at the edges of the tuning range. The measured LO leakage to the RF port was below -69 dBm for all samples.

VI. CONCLUSIONS

An ultra-low power receiver front-end and LO generator has been demonstrated in 65 nm CMOS. Operating at 2.6 GHz from a 0.85 V supply it consumes below $550 \mu\text{W}$. Using an LNA-less architecture and an efficient passive mixer structure it achieves good rejection of out-of-band interference

while also rejecting interference at the even harmonic of the LO, despite using a single-ended input. A complementary divider structure offers an LO with low quadrature error despite an asymmetric oscillator structure. Using only two inductors, the circuit occupies an area of just 0.15 mm^2 excluding pads. Retuned to operate in the 2.4 GHz ISM band, it has sufficient performance for a Bluetooth Low Energy receiver even without a SAW-filter. The front-end performance is summarized and compared to some recently published works in Table II. Works with integrated LO-generation have been primarily selected, and the active areas estimated from chip photos. The circuit performs favorably on primarily linearity, active area and power consumption.

ACKNOWLEDGEMENT

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