A 24-GHz Automotive Radar Transmitter with Digital Beam Steering in 130-nm CMOS

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A 24-GHz Automotive Radar Transmitter with Digital Beam Steering in 130-nm CMOS

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***Abstract*— In this paper simulations of a 130-nm CMOS 24-GHz automotive radar transmitter with digital beam steering is presented. The beam steering is performed by multiple PAs connected to separate antenna elements. The output phases of the PAs are individually controllable through 360° by binary weighting of quadrature phases. The circuit contains 18 PAs, each delivering 0 dBm to the antenna, resulting in a combined output power of 13 dBm. The 18 element antenna array will at 24 GHz be 11 cm, and have a directivity of 12 dB and a half power beam width of 5 degrees.**

I. Introduction

The car industry and the legislators are very interested in an automotive radar system. The injuries from car collisions cost the society a lot both in medical bills and in human tragedies. In the United States (US) alone motor vehicle crashes accounted for 42,000 deaths, more than 5.3 million injuries, and over $231 billion in economic losses in 2000 [1]. Already today there is a system called Adaptive Cruise Control (ACC), or sometimes AICC, where I stands for Intelligent. The ACC system measures the distance to the closest vehicle ahead, either by radar or laser [2]–[4]. If the distance becomes too short the car closes its throttle, or if necessary the system will apply the brakes. If the vehicle ahead changes lane or accelerates, the ACC system will open the throttle and accelerate up to the speed preset by the cruise control. This system adds about $1,500 - $3,000 to the cost of the car [2]. The price of radar solutions has to go down if they are going to be available in all cars. This is the main reason for choosing standard CMOS technology. The cost of the system can then also be further reduced by integrating much of the digital functionality on the same chip.

The European Telecommunications Standards Institute (ETSI) has a temporary standard [5] for Short Range Radar (SRR) operating in the frequency band from 24.05 GHz to 24.25 GHz. The maximum Effective Isotropic Radiated Power (EIRP) is 20 dBm, limiting the maximum allowed output power. Furthermore, both ETSI and the Federal Communications Commission (FCC) have a license free UWB frequency band in this range[1], which also can be used for automotive radar applications. A permanent frequency band in Europe and US is opened at 76-77 GHz with a maximum EIRP of 40 dBm and 48 dBm respectively [6], [7]. In Europe there is also a permanent location for anti-collision SRR at 79 GHz with an EIRP of 50 dBm [8]. With today's CMOS technologies 24 GHz operating frequency is possible, enabling low-cost implementation of 24 GHz SRR systems. In the coming years, CMOS technology feature sizes are predicted to decrease making also low-cost implementations of 77 GHz systems possible. According to the International Technology Roadmap for Semiconductors (ITRS) [9] the 45 nm node and beyond will have f_T:s higher than 200 GHz making them possible for 77 GHz implementation.

A typical specification for a 77 GHz radar front end can be seen in Table I, [3], [10]–[12]. Since our aim is to find a transmitter architecture that can be migrated to 77 GHz when sufficiently fast CMOS technology becomes available, we use this specification for our design, although the EIRP is a bit high.

TABLE I
Specification for a 77 GHz front end

Transmitter	
Frequency	76-77 GHz
Modulation	FM-CW
Tx Phase Noise	<-80 dBc/Hz @ 100 kHz offset
Sweep Width	300 MHz
Range	2 → 150 m
Linearity	<0.5%
Transmit Power	10-15 dBm
Reciever	
Beam Width	3°
Field Of View	8°-20°
Beam Overlap	0.5°
Relative Speed	-200 → +100 km/h
Calculation Frequency	10 Hz
Range (for 1 m^2 target)	1-100 m

II. Air Interface

The antenna has to have a high directivity and a small Half Power Beam Width (HPBW) to be able to ful-

[1]In the US the band is 22 GHz-29 GHz and in Europe 22.65 GHz-25.65 GHz.

fill the specification. In addition to that it should be steerable and mechanically stable. A linear array needs to be at least $10\lambda_0$ to achieve the required HPBW. This corresponds to 4 cm at 77 GHz and 13 cm at 24 GHz. A linear array of $\lambda/2$ dipole patches has been assumed, fed in the center by the differential signal from the PAs, see Fig. 1. The supply voltage to the PAs is inserted at the signal ground at end of the antenna patches. The physical size of the dipole antenna is $\lambda_{sub}/2$, where λ_{sub} is the wavelength in the patches on the substrate.

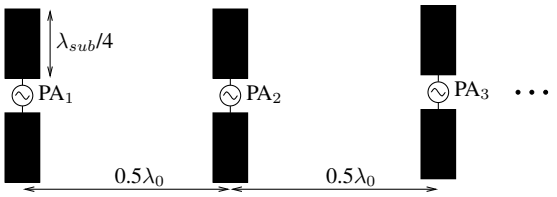

Fig. 1. The dipole patch antenna array with the PA feeding indicated

In Fig. 2 the radiation pattern is plotted when the beam is swept over Field Of View (FOV). To achieve a FOV of $\pm 13^\circ$ up to $\pm 40^\circ$ phase difference of adjacent antenna elements is required. The PAs are not restricted to this FOV, however, since they can deliver any phase difference between the antenna elements.

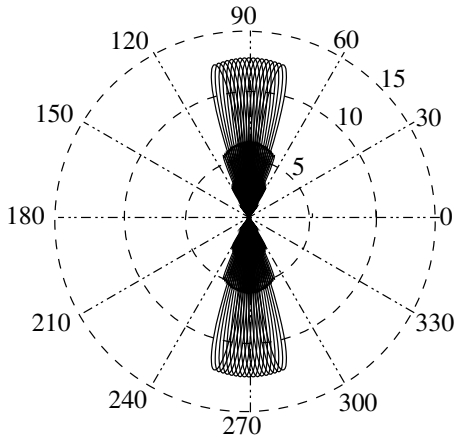

Fig. 2. Radiation patterns for $\lambda/2$ spacings of the antenna elements

The HPBW and directivity have been simulated, see Fig. 3. The phase between different elements was swept from 40° to -40° giving $\pm 13^\circ$ beam steering. As can be seen, the directivity is larger than 12 dB over the complete range and the HPBW is below 4.3 degrees. To achieve a HPBW of 3 degree or better over the full range the size of the antenna array would have to be increased. An increased antenna element spacing of $0.65\lambda_0$ would give 3 degree HPBW with 18 antenna elements.

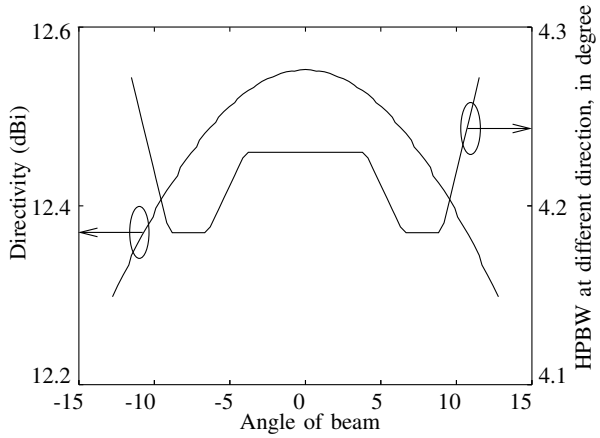

Fig. 3. HPBW and directivity with 18 antennas in a linear patch array and $0.5\lambda_0$ spacing

III. Design and Simulation

With today's CMOS processes, such as the 130 nm used in this paper, 77 GHz is a very high frequency. The aim is therefore set on the 24 GHz frequency band for car radar applications. The specifications in Table I are used for this band as well.

A block diagram of the beam steering multiple PA circuit can be seen in Fig. 4. Distributing the quadrature signal to the 18 PAs therefore requires long interconnect lines which has to be considered during simulation.

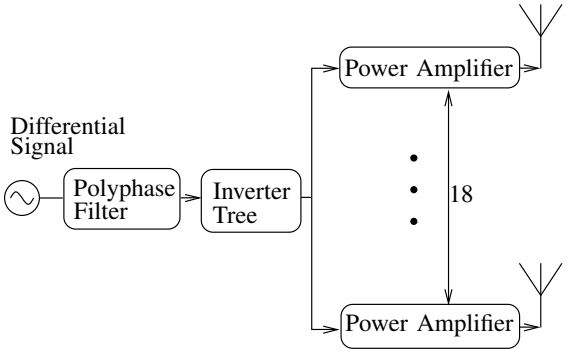

Fig. 4. Block diagram the car radar transmitter

In the following sections the different parts of the circuit are described from left to right in Fig. 4.

A. Polyphase Filter

To convert the externally applied differential input signal to a quadrature signal, a passive polyphase filter [13] is used, see Fig 5. The filter has two links, tuned to a lower and a higher frequency. The filter is thereby rather broadband. For a $\pm 2^\circ$ quadrature phase error the band is from 18 GHz to 29 GHz, and the voltage loss of the filter within that band is less than 11 dB, when loaded by the inverter tree.

To reach the high operating frequencies, the resistances of the filter must be low, 45 Ω and 60 Ω in the two stages.

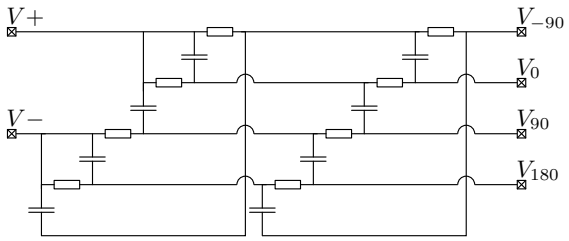

Fig. 5. The passive two stage polyphase filter

This results in an input impedance of about 10-j14 Ω. To get a 50 Ω input impedance of the circuit, better suited for the measurement equipment, an on-chip L-match network is used in-front of the polyphase filter.

B. Inverter Tree Driver

Since the loading of 18 PAs is high (6.4 pF) a tree structure has been chosen for the driver circuit. The driver consists of five stages of inverters, see Fig. 6. Each inverter symbol in

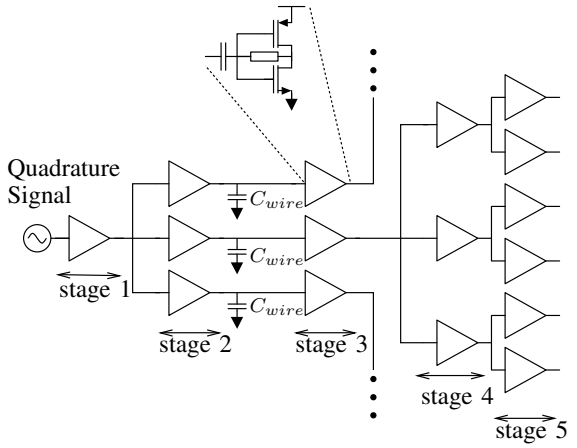

Fig. 6. Structure of the driver circuit for the PAs

Fig. 6 has four inverters, one for each phase of the quadrature signal. To stabilize the inverter output DC voltage at $V_{dd}/2$, a high ohmic resistive feedback is applied locally, and a DC-block capacitor is connected in series with the input to isolate the stages.

The purpose of the first stage in the inverter tree is to reduce the loading of the polyphase filter and to drive the three following inverters. The routing from the first to the third stage is long, thus an second stage is inserted to drive the interconnect wire and the inverters of the third stage. The capacitance of one of the interconnect wires is roughly 18 fF, and the series resistance in the same wire is below 1 Ω. From the third to the fifth stage the routing is local and thus the tree starts to grow, ending in 18 output branches.

The ratio of the output current and input current of the inverter tree, when placed in the transmitter circuit, is 3.3 times, achieving an amplitude of 112 mV at the PA input.

C. Power Amplifier

A 360° phase steering PA fed by a quadrature signal has been designed, see Fig. 7. The binary weighted transistor banks gives the possibility to weight the phases differently by changing the control voltages, V_{x_y}. Then the transmitted signal from each PA can have an arbitrary phase[2].

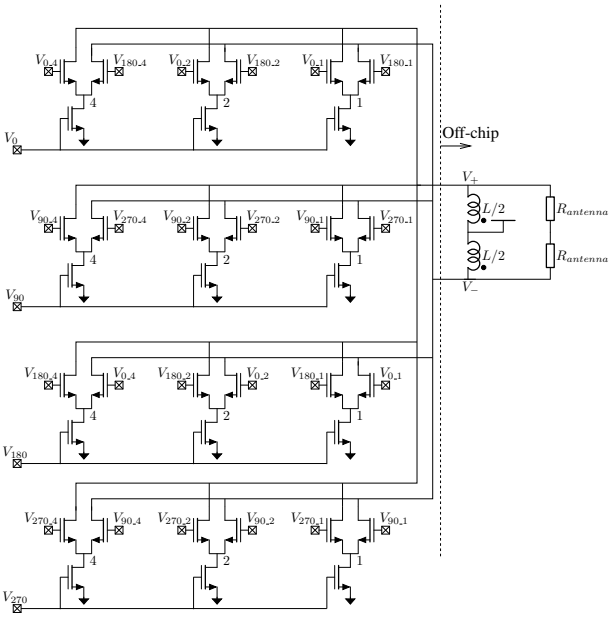

Fig. 7. Schematic of the power amplifier with three binary weighted transistors per bank

The power delivered to the antenna array should be 10 dBm, distributed among the 18 PAs. Each PA should then deliver at least -3 dBm, and is therefore designed to output 0 dBm into a 60 Ω load, giving a 3 dB margin for losses in antenna feeding networks. The 60 Ω patch resistance is obtained by tuning the feeding point, x, of the patch antenna according to (1a). $R_{in}(x = 0)$ is made high by making the patch width, W, small (1b) [14].

$$R_{in}(x) = R_{in}(x = 0)\cos^2\left(\frac{\pi}{L}x\right) \tag{1a}$$

$$R_{in}(x = 0) = \frac{1}{2G} = 45\left(\frac{\lambda_0}{W}\right)^2 \qquad W \ll \lambda_0 \tag{1b}$$

Thus the patch can be made small and matched to the PA at the same time.

It should be stressed that the inductors in Fig. 7 are on the antenna substrate and not on-chip, they are to be realized as stubs.

The phasor of one of the PAs has been swept over a quadrant and the result is plotted in Fig. 8 together with the ideal points. The other PA, which loads the same inverter one stage back, is set to 45° during the sweep.

[2]This is true if the discretization depth is large ($\Rightarrow \infty$). In this case there are 40 different output phases with an output power within ±11%.

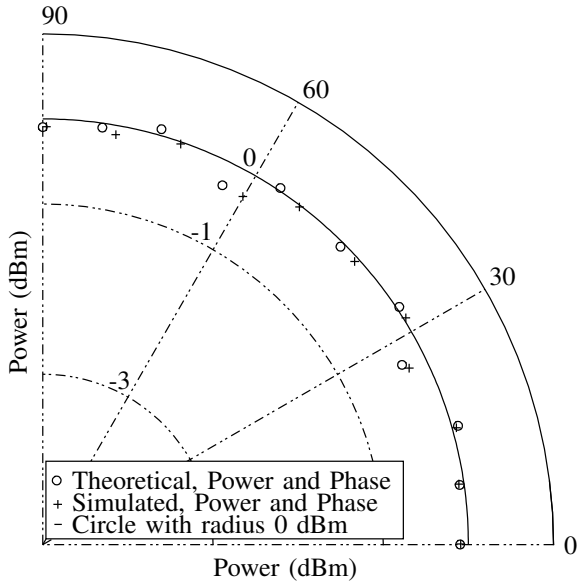

Fig. 8. The output phasors of a PA in one quadrant

D. Shift Register

To change the phase setting of the 18 PAs a shift register has been designed to serially clock in the digital phase control word that gives the new position of the beam. The total time for each beam position is about 10 ms, see Table I[3]. In this time slot a new phase setting must be clocked in, the circuit has to stabilize, and a new measurement be performed. To clock in the 216 (12×18) control signals does not take more than a couple of microseconds with a 100 MHz clock, which is not considered high in modern digital CMOS processes. The shift register is built with the cell shown in Fig. 9.

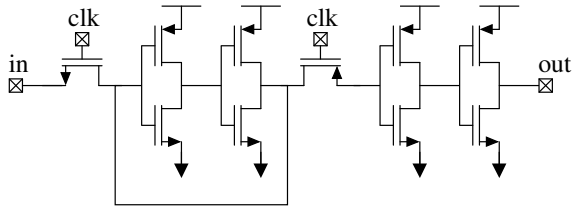

Fig. 9. Schematic of the shift register cell

The last inverter in the stage is larger than the preceding one. It is necessary to have a large driving capability of the last inverter to force a change in the next stage. In this case the last inverters are made 4/3 times larger.

IV. Conclusion

The results of the simulations support the idea that a low cost automotive radar system in CMOS can be built, enabling increased safety on the roads.

It has been shown that the transmit power needed to get sufficient distance coverage is possible to deliver with 130 nm CMOS technology at 24 GHz, by use of multiple PAs. The multiple PAs deliver 13 dBm in total. They also support digital beam steering with good accuracy. Electrical beam steering makes the radar design more robust and less expensive than mechanical solutions.

[3]To sweep the FOV approximately 10 phase settings is required. This should be performed 10 times per second, thus giving 10 ms per phase setting.

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