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1998

Link to publication

Citation for published version (APA):
Olsson, T., Jönsson, C.-M., Öwall, V., & Nilsson, P. (1998). *Interference cancellation detectors in a hardware implementation perspective*. Paper presented at NORCHIP Conference, 1998, Lund, Sweden.

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Interference Cancellation Detectors in a Hardware Implementation Perspective

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ABSTRACT: *To combat interference between users in a DS/CDMA system, several multi-user detection schemes have been proposed. This paper presents a prestudy for a custom DSP implementation of a multi-user detector scheme based on non-decision directed interference cancellation. Two architectural implementation methods for asynchronous detection are suggested and mutually compared. Each of the architectures is shown to have its particular advantages and therefore, a design combining the methods described in this paper is worth future studies.*

1. INTRODUCTION

In a DS/CDMA system, Multiple Access Interference (MAI) is likely to severely degrade the channel. To combat the MAI, multi-user detection can be used. The objective of multi-user detection is to jointly detect all user data sent simultaneously by several transmitters, sharing a multiple-access communication channel. Since multi-user detection requires knowledge of all signature waveforms (chip sequences) used in the system, its main application will be for up-link reception in the base station. In 1986 Verdu analyzed an optimum multi-user detector, the maximum-likelihood sequence detector [1]. However, if there are K users transmitting γ chips/bit, the resulting optimum detector has a complexity proportional to $2^{K\gamma}$. The maximum likelihood detector is too complex to implement in practical DS/CDMA systems for reasonable values of K and γ. Research within this area has therefore mainly been focused on finding sub-optimum detectors. One such detector is the subtractive interference cancellation detector, where the MAI, contributed by each user is estimated in order to subtract it. This group of sub-optimal detectors can operate non-linearly and use different approaches, e.g. feed-back detectors such as Parallel Interference Cancellation (PIC) and Successive Interference Cancellation (SIC) [2,3]. The PIC detector estimates and subtracts in parallel the MAI as seen by each user, while the SIC detector takes a serial approach to cancelling interference. In this paper, a SIC detector, the Non-Decision Directed Interference Canceller (NDDIC) [4], will be used. The NDDIC detector uses the soft outputs from each detected user for cancelling of the MAI. The NDDIC detector has a relatively low complexity, and is shown to offer substantially better performance than the conventional single-user matched filter detector [4].

In an actual system, the received signals arrive to the base station with different delays. Therefore, the detection problem must be framed over the whole message for optimum detection [5]. Since framing over the whole message will lead to a complex architecture, other methods, using a smaller window of bits will be analyzed in this paper.

2. ALGORITHM

In this chapter, a brief description of the NDDIC algorithm is given. In the following text, the received signal is treated as a vector of samples after a chip-matched filter. For each user, the

NDDIC detector makes a soft decision detection by despreading the received vector, using the given chip sequence. The user is cancelled from the received signal in order to reduce the MAI experienced by the remaining users. This process can be repeated in a multistage structure, where in the proceeding stages, all bit estimates are regenerated for new estimation and cancellation. The sequential outline of the NDDIC units in a two stage cancellation scheme is illustrated in Figure 1. The best bit decision is from the strongest signal, and therefore it is very important to cancel the strongest signal first and continue in order of decreasing received signal power. An estimate of the signal strength can, for instance, be made using conventional matched filter detection, or by using the signal strength of preceding bits.

The benefit of using interference cancellation is illustrated in Figure 2, where a one and a two stage NDDIC detector are compared to a conventional single-user matched filter detector and to the single-user bound.

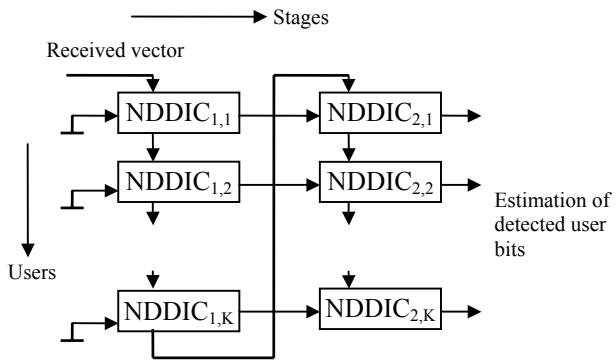

Figure 1. General two-stage interference cancellation structure used in this study.

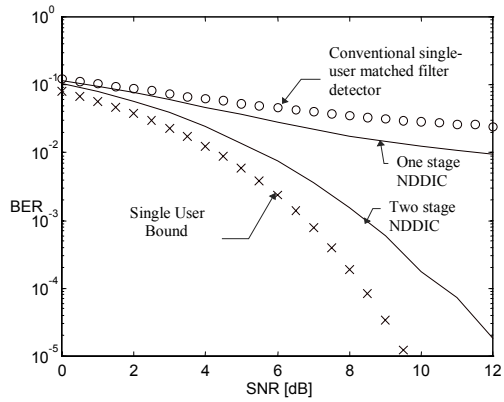

Figure 2. One and two stage NDDIC detection compared to a conventional detector.

The simulation (MATLAB) is made using an AWGN channel, 128 chips/bit, 30 users in the system, and a signal to noise ratio (SNR) of 0 to 12 dB. The simulation parameters compared to the implemented parameters, which are given in section 3, are chosen to decrease the simulation time.

A general NDDIC detector is shown in Figure 3, handling the input signal vector of user k at stage i. For the case of changes in received signal powers, ranking of users is forwarded into the NDDIC detector. For the first user in the first stage, the input signal vector equals the received signal vector, denoted $\bar{r}$,

$$\bar{r}_{1,1} = \bar{r} . \qquad (1)$$

The NDDIC detector regenerates the signal contribution from the users and passes it on for cancellation. The regenerated signal for the NDDIC detector of user k at stage i, is denoted $f(\bar{r}_{i-1,k})$ and the decomposition of the input signal vector in the NDDIC detector is

$$\bar{r}_{i,k} = f(\bar{r}_{i-1,k}) + \bar{r}'_{i,k} , \quad (2)$$

where $\bar{r}'_{i,k}$ is the remaining part of the received vector. In the first stage, no regenerated input signal is present, i.e.

$$f(\bar{r}_{0,k}) = \bar{0}, \qquad (3)$$

where $\bar{r}_{0,k}$ is defined as $\bar{0}$. In the first stage, the signal vector $\bar{r}'_{1,k+1}$ contains the signal from the remaining K-k users not yet cancelled plus the non-cancelled MAI from the k-1 users already subtracted from the received signal vector. Better estimates are provided in the multi-stage case, resulting in less non-cancelled MAI in the error signal vector [4]. The soft estimates of the detected users are

$$y_{i,k} = \bar{s}_k^{\,T} \bar{r}_{i,k}, \qquad (4)$$

where $\bar{s}_k$ is the spreading sequence and correspondingly, the regeneration of the signal cancellation contribution is

$$f(\bar{r}_{i,k}) = \bar{s}_k y_{i,k}. \qquad (5)$$

As users are subtracted from the received signal vector, the MAI experienced in the detection of the remaining users will be less significant. The distinction in lower bit-error rate (BER) can be seen in Figure 2, for the two-stage scheme compared to the single stage. It has been shown, for instance in [4], that additional stages (more than two) do not increase the performance substantially. An increase in the number of stages will inherently increase the time delay in the DSP, which is one of the most critical parameters for the realization.

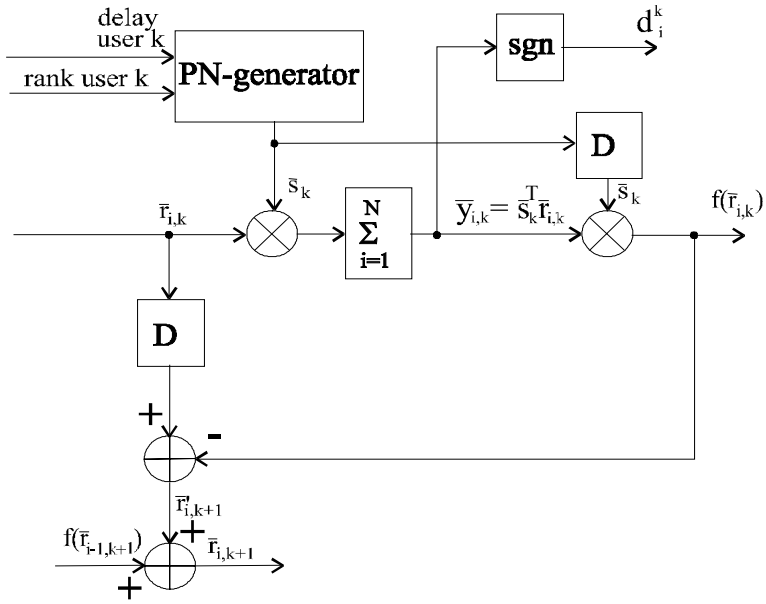

Figure 3. General NDDIC detector.

3. Assumptions for realization

When designing the custom DSP, the following assumptions were made:

- An SNR of 7 dB and a maximum uncoded BER of 1%.
- A two stage NDDIC detector structure.
- A bit rate of 15 kbit/s.
- Spreading sequence of 256 chips/bit, leading to a chip rate of 3.84 Mchip/s.
- Eight bits representation of the chip values.
- Six bits representation of the bit estimates of each user.
- The delay of one bit should be less than 10 ms.

The assumptions of 15 kbit/s and 256 chips/bit are corresponding to a suggested parameter set in FMA2 [6] for UMTS. In the simulations, the comparison between the different detectors is the main issue. For simplicity, we therefore use an AWGN channel instead of a fading mobile channel. Simulations (MATLAB) show that an SNR of 7 dB and a BER of 1% allows approximately 80 users in the system. A delay of 30 ms is acceptable for voice communication, consequently, the delay of 10 ms is leaving room for additional delay from other blocks such as decoding units etc.

In order to get a set of spreading sequences, two carefully chosen maximum length shift registers are connected by an XOR gate (see figure 4). Different spreading sequences can be obtained by loading the registers with unique start values for each user.

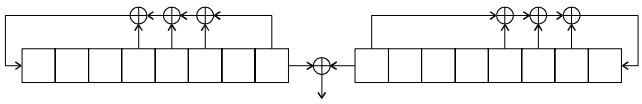

Figure 4. Shift registers.

4. DESIGN USING PARALLEL FOLDED ARCHITECTURE

In the parallel folded architecture, a set of parallel NDDIC processors are used (see Figure 5). Two extra units for interfacing is also needed; one for administrating incoming bits, and one for sending calculated soft decisions. One NDDIC processor in Figure 5 consists of an NDDIC detector as seen in Figure 3. This processor is used repeatedly for detection of the users in both stages. The datapath of the NDDIC processors are used chip by chip in a series of loop sequences. The reason for using the parallel processor structure is to match both the demand of a delay less than 10 ms and the 15 kbit/s throughput demand. Without considering any additional clock cycles for loop computation the number of clock cycles elapsed are lower bounded to about 200 kcycles in each of the parallel NDDIC processors for a two stage detection. Since the maximum delay for a bit is 10 ms, a clock rate of 20 MHz is needed. Given a clock rate of 20 MHz and a bit rate of 15 kbit/s, the number of parallel NDDIC processors must be at least 150. Since the throughput of one NDDIC processor (100 bit/s using a clock rate of 20 MHz) is much lower than the bit rate (15 kbit/s), detection of subsequent bits have to be made independently. Therefore, a method of implementing the NDDIC detector scheme using a received vector representing three bit lengths is introduced. The advantage of this method is its ability to handle asynchronous reception without great loss in performance.

The received vector can be seen as a window of chips, representing three bit lengths (768 chips). In such a vector, there are always at least two entire bits of each user. A right and a left bit estimate is made on the entire bits for each user as seen in *A* of Figure 6. The two bit estimates are cancelled and added according to the NDDIC algorithm. Since this approach will result in good cancellations in the middle 256 chips of the received vector, the output estimates from the last stage are based on the parts of the left and right bits covered by those chips as *B* in Figure 6. The left bit estimate of the preceding bit is saved during one bit period and added to the present right estimate for the same bit. Thus, no information is lost in the process. Figure 7, shows a BER simulation of this method. For comparison, a simulation of the bit synchronous case, using random generated spreading sequences is shown. The simulation shows an almost equivalent BER for the asynchronous case and the synchronous case using random generated spreading sequences. The deviation for the SNR of 12 dB is due

to a limited number of iterations. Obviously the method using three bit lengths is good for taking care of asynchronous reception.

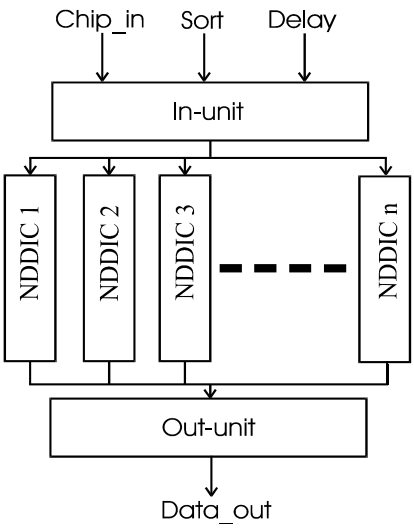

Figure 5. Parallel NDDIC architecture.

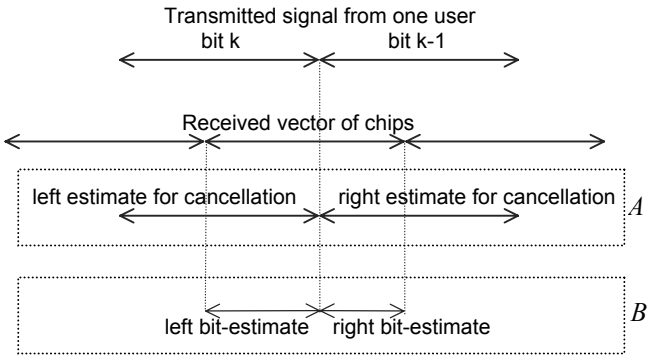

Figure 6. Three bits windowing method.

In Figure 5, chip frames, delay estimates, and amplitude sorting order of the users are received by the "In-unit". The "In-unit", works in a cyclic manner and sends chips representing three bit lengths at a time to an NDDIC processor, (see Figure 6). There must always be at least one free NDDIC processor in order to maintain throughput in the system. The "Out-unit" receives and adds the left and right bit estimates from each user.
The datapath of the NDDIC processors used for asynchronous reception can be seen in Figure 8. Instead of describing the function of each of the blocks of the datapath, a simplified signal flow is described; The incoming chips are received through the block "IO_interface" and stored in the RAM "received".

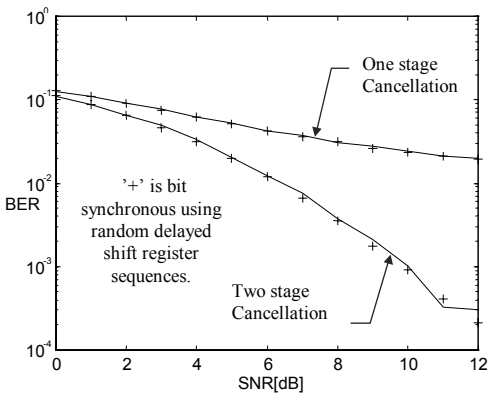

Figure 7. Three bits windowing method compared to the bit synchronous case.

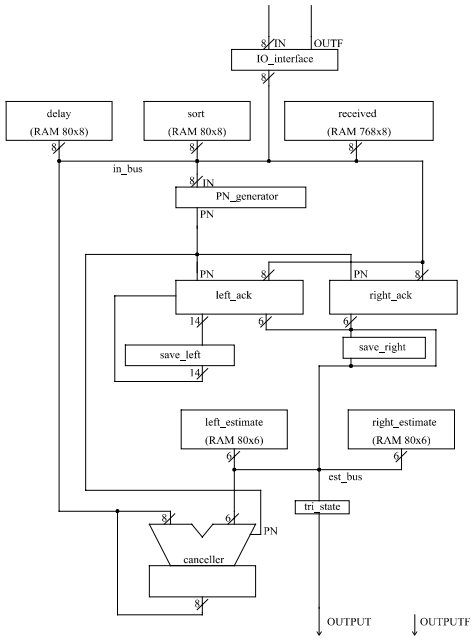

Figure 8. Datapath of one NDDIC processor in the parallel architecture.

Despreding of the chips according to *A* in Figure 6 is performed in the blocks “left_ack” and “right_ack”. The cancellation and addition of the despreaded bits is performed in the block “canceller”. The block “PN_generator”, containing the shift registers of Figure 4, generates the spreading sequence needed for spreading and despreading. Since the output of each block in the NDDIC unit is equipped with tri-state gates, all blocks can be connected directly to the buses.

5. DESIGN USING HARDWARE MAPPED ARCHITECTURE

The hardware mapped architecture presented in this section is quite different from the parallel folded architecture. In the architecture using parallel NDDIC processors, the chips representing information bits are stored in RAMs. The RAM structure is, however, restricted to one read and/or write operation per clock cycle. Instead of using a RAM, the same data is stored in a register bank, making read or write operations possible on all chips simultaneously. The registers are to be connected cyclically, to enable a number of shift operations determined by the delay of each user. If the chips are stored in a register bank of 512 chips, corresponding to two bit lengths, the register bank will contain at least one entire bit per user. This architecture is designed to have a throughput equal to the bit rate. Therefore, cancellation of previous bits can be used. Estimation and cancellation of all users must be performed during one bit period, this prompts faster methods of despreading the chips. For despreading, an adder tree [7] of width 256, using 8 levels, calculates the sum of 256 chips in one clock cycle. However, to be able to perform the complete 8 level addition, intermediate storage registers in the adder tree, increasing the number of clock cycles for despreading, may be necessary.

New chips representing one bit length are shifted into the register bank each bit period. The former leftmost 256 chips now become the rightmost 256 chips, which are cancelled of interference from the preceding bits of each user. The register bank is for each user clocked a number of steps, matched to the delay of that user. Using the adder tree, it is now for that user, possible to make a bit estimate.

In order to use all chips of the spreading sequence simultaneously, the spreading sequence of each user is extracted from the PN generator and stored in a $K \times 256$ bit RAM, where K is the maximum number of users in the system. It is assumed that the set of spreading sequences does not change for subsequent bits. Figure 9 illustrates the adder tree connected to the register banks. In Figure 9, the value of each chip passes through a conversion block (“con”), converting the chip value to its two’s complement depending on the corresponding chip in the spreading sequence. The two’s complement conversion is done by inverting the chip and then adding one LSB. The total estimated value of the despreaded bit is stored in a register “est_reg”. Cancellation and addition can be performed in one clock cycle. This is done by connecting an adder/subtractor to each chip, adding or subtracting the value of “est_reg” depending on the corresponding chip of the spreading sequence. When estimations, additions and cancellations of all users are made for one bit, 256 new chips are shifted into the register bank and a new information bit can be processed. The suggested method of shifting the register values has the drawback of requiring a fast on-chip clock speed.

One way to speed up this implementation is to use an address unit for pointing out the right delay instantaneously instead of shifting cyclically in order to adapt to the delay of each user. The drawback of this method may be the additional complexity required for addressing. A compromise between complexity and speed is to enable shifts of larger steps than one chip at a time in the register bank. The considerably lower number of clock cycles for complete

detection is an advantage of the hardware mapped architecture. Another advantage is the possibility to use the detector for quickly finding the delay of each user. This is done by correlating the received chip vector to the spreading sequence in a sliding manner. One drawback using the hardware mapped architecture, will be a higher BER for a given SNR, since cancellation is only performed on present and preceding bits. This is to be compared with the method used in the parallel folded architecture where cancellation is performed on two bits at a time. Simulations for an SNR of 7 dB, 256 chips/bit and 80 users give a BER of 1.6% for the hardware mapped architecture and a BER of 0.7% using the parallel folded architecture.

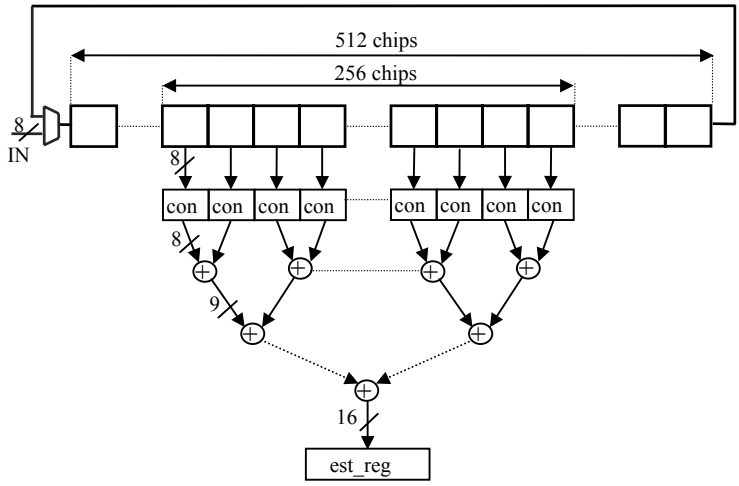

Figure 9. Adder tree arithmetic, connected to a cyclic register bank

6. RESULTS

An evaluation of the proposed design methods is presented in Table 1. The number of clock cycles for a two stage detection of one bit is given together with the maximum delay and the required clock frequency. To evaluate the complexity of the different architectures, an estimation of the number of memory cells, register cells and adders are calculated. An estimate of the complexity of the controller is also performed. For all the architectures, a system of 80 users, 256 chips/bit and a bit rate of 15 kbit/s is considered. As an example of the suggestion of enabling shift operations larger than one chip at a time, an architecture enabling shifts of eight chips at a time is evaluated. It is notable that higher on-chip clock speeds in the parallel folded design will lead to a decrease in size. This is due to fewer parallel NDDIC processors. For instance, if the on-chip clock speed is increased to 100 MHz, the number of parallel NDDIC processors will be 30 instead of 150. The hardware mapped design on the other hand will be unaffected in size by higher clock speeds. In the case of fewer users in the system, some of the NDDIC processors in the parallel design will be idle. If shutting of the power of NDDIC processors is possible, this will cause reduced power consumption.

7. CONCLUSIONS

We have shown that a multi-user detector using serial interference cancellation can be built and different approaches of this problem are presented requiring different levels of complexity. The hardware mapped design have the advantage of a lower number of clock cycles elapsed for complete detection, although the parallel folded design can not be ignored since it has a better BER for a given SNR. A design, which combines the methods described in this paper, is worth future studies. For instance, pieces of the hardware mapped architecture

can be used in the parallel folded architecture. Other topics for future developments will be to use oversampling, i.e. more than one sample value per chip and to investigate the possibility of implementing sorting and delay tracking of the users.

Table 1 Evaluation of design methods.

Design method	Elapsed cycles	Max Delay [ms]	Clock [MHz]	Memory #	Register #	Adder #	Controller
Sequential arithmetic (150 parallel units).	200000	10	20	$12.5 * 10^6$	10000	5000	Complex[i]
Hardware mapped design using shift operations.	41500	0.067	620	20500	4100	4300	Simple
Hardware mapped design using addressing unit.	800	0.067	12	20500	4100	4300	Complex[ii]
Hardware-mapped design able to use shift of 8.	6500	0.067	100	20500	4100	4300	Medium[iii]

[i] A complex control unit will be required to handle the loop structure of this realization.
[ii] For simplification of the area calculations, the address unit, having an area hard to define, is in this table incorporated in the controller.
[iii] For the same reason as above, the additional multiplexers needed to enable shifts of 8 steps in the register bank, is incorporated in the controller.

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