Charge transport in III-V narrow bandgap semiconductor nanowires

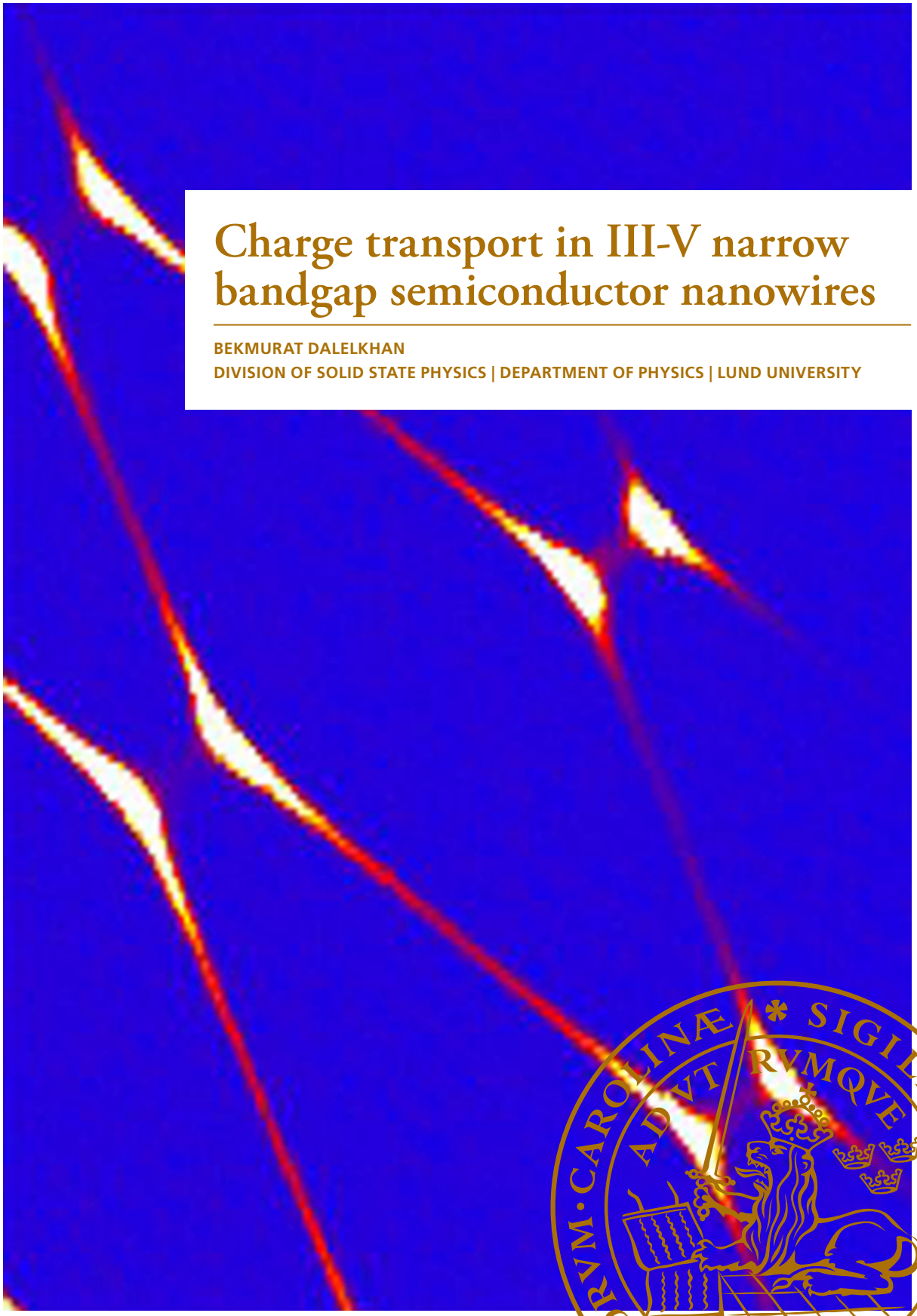
Dalelkhan, Bekmurat

2019

Document Version:
Publisher's PDF, also known as Version of record

Charge transport in III-V narrow bandgap semiconductor nanowires

BEKMURAT DALELKHAN
DIVISION OF SOLID STATE PHYSICS | DEPARTMENT OF PHYSICS | LUND UNIVERSITY



Printed by Media-Tryck, Lund 2019 NORDIC SWAN ECOLABEL 3041 0903

Faculty of Engineering
Division of Solid State Physics
Department of Physics

ISBN 978-91-7895-099-7

Charge transport in III-V narrow bandgap semiconductor nanowires

Charge transport in III-V narrow bandgap semiconductor nanowires

Bekmurat Dalelkhan

LUND
UNIVERSITY

Division of Solid State Physics

Department of Physics

Lund University

DOCTORAL DISSERTATION

by due permission of the Faculty of Engineering, at Lund University, Sweden. To be publicly defended on Friday, the 17th of May, 2019, at 13:15 in the Rydberg Lecture Hall at the Department of Physics, Sölvegatan 14, Lund.

Faculty opponent

Dr. Stefan Ludwig

Paul-Drude-Institut, Germany

Organization:
LUND UNIVERSITY
Division of Solid State Physics
Department of Physics
P. O. Box 118, SE-221 00 Lund, Sweden

Document name
Doctoral Dissertation

Date of issue

Author: Bekmurat Dalelkhan

Sponsoring organization

Title: Charge transport in III-V narrow bandgap semiconductor nanowires

Abstract

This thesis describes charge transport in III-V narrow bandgap semiconductor nanowires. We are particularly interested in quantum transport in InSb, InAs and InP-InAs core-shell nanowires. According to the type of transport mechanism dominating in the devices, this thesis can be divided into four parts.

In the first part of this thesis, we investigated the temperature dependent transport properties of InSb nanowires using field effect transistors made of InSb nanowires grown by chemical vapor deposition. Ambipolar transport is observed in measurements in a wide range of temperatures up to 300 K. A bandgap of 220 meV is extracted from the temperature dependent measurements. Hole and electron field effect mobility are determined and their temperature dependence studied. The off state current shows a strong dependence on the temperature and the channel lengths of the transistors.

In the second part of this thesis, spin relaxation and quantum interference in InSb nanowires are explored. Low-field magneto-conductance measurements are performed and a crossover from weak antilocalization to weak localization is observed. The experimental results are well explained with quasi one dimensional weak localization theory. Spin relaxation length and phase coherence length are defined. A strong spin-orbit strength of $\alpha_R = 0.4$ eVÅ-0.87 eVÅ is extracted.

In the third part of this thesis, electron transport in a single quantum dot is studied in the weak and strong dot coupling regimes. The single quantum dots are formed in InSb nanowires by side gates. Various transport features such as sequential tunneling, excited states, and cotunnelings are investigated. Low temperature transport properties of InP-InAs core-shell nanowires are also explored and the coulomb blockade effect is revealed from a quantum structure extending over the entire core-shell nanowire.

In the last part of this thesis, we report on electron transport through double quantum dots in InSb and InAs nanowires defined by side gates. From the measurements in the weak inter dot coupling regime, Pauli spin blockade is observed. The evolutions of states in the Pauli spin-blockade region with magnetic field is also studied.

Key words: InAs, InSb, InP-InAs, narrowband gap, spin-orbit interaction, quantum dots, Nanowire

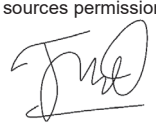
Classification system and/or index terms (if any)

Supplementary bibliographical information | Language: English

ISSN and key title | ISBN: 978-91-7895-099-7

Recipient's notes | Number of pages: 118 | Price

Security classification

Signature 

Date 2019-04-05

Charge transport in III-V narrow bandgap semiconductor nanowires

Bekmurat Dalelkhan

LUND
UNIVERSITY

Division of Solid State Physics
Department of Physics
Lund University
Sweden, 2019

Front cover: Current is shown as a function of plunger gate voltages in a charge stability diagram of a double quantum dot at low bias.

Faculty of Engineering
Department of Physics

ISBN 978-91-7895-099-7 (print)

ISBN 978-91-7895-100-0 (pdf)

Printed in Sweden by Media-Tryck, Lund University
Lund 2019

This thesis is dedicated with love to my parents, my wife Bizat and my son Beibars.

Contents

Abstract

This thesis describes charge transport in III-V narrow bandgap semiconductor nanowires. We are particularly interested in quantum transport in InSb, InAs and InP-InAs core-shell nanowires. According to the type of transport mechanism dominating in the devices, this thesis can be divided into four parts.

In the first part of this thesis, we investigated the temperature dependent transport properties of InSb nanowires using field effect transistors made of InSb nanowires grown by chemical vapor deposition. Ambipolar transport is observed from the measurements in a wide range of temperatures up to 300 K. A bandgap of 220 meV is extracted from the temperature dependent measurements. Hole and electron field effect mobility are determined and their temperature dependence studied. The off state current shows a strong dependence on the temperature and the channel lengths of the transistors.

In the second part of this thesis, spin relaxation and quantum interference in InSb nanowires are explored. Low-field magnetoconductance measurements are performed and a crossover from weak antilocalization to weak localization is observed. The experimental results are well explained with quasi one dimensional weak localization theory. Spin relaxation length and phase coherence length are defined. A strong Rashba spin-orbit strength of α_R = 0.4 eVÅ-0.87 eVÅ is extracted.

In the third part of this thesis, electron transport in a single quantum dot is studied in the weak and strong dot coupling regimes. The single quantum dots are formed in InSb nanowires by side gates. Various transport features such as sequential tunneling, excited states, and cotunnelings are investigated. Low temperature transport properties of InP-InAs core-shell nanowires are also explored and the coulomb blockade effect is revealed from a quantum structure extending over the entire core-shell nanowire.

In the last part of this thesis, we report on electron transport through double quantum dots in InSb and InAs nanowires defined by side gates. From the measurements in the weak inter dot coupling regime, Pauli spin blockade is observed. The evolutions of states in the Pauli spin-blockade region with magnetic field is also studied.

Popular Scientific Summary

The silicon-based semiconductor industry has experienced a rapid development since the first transistor was invented in 1947 by J. Bardeen, W. Brattain, and W. Shockley at Bell Labs. Transistors work as switches or amplifiers for both digital logics and analog applications and they are therefore the heart of modern electronic devices. Obviously, the development has had a large impact on our daily life, from computers, smart phones to control systems found in automobiles. The development is achieved by a reduction in the size of transistors to improve transistor density, performance and power density. However, as the size of a transistor is approaching the scale of only a few atoms, it is revealed that further miniaturization will not work anymore partially due to quantum effects. In fact, it is a fundamental limit since an electron cannot be treated as a point like particle, instead it possesses a duality of a particle and a wave. At the atomic scale, quantum mechanical effects such as tunneling, interference, and confinement take place and the transport in a transistor is governed by these quantum effects, leading to degradation of device performance. This brings a need to search for new materials and novel devices, or techniques, which address the problems facing modern electronic devices.

When we look at the world in atomic scales, things start to behave in unusual ways. One particle can be co-exists in servals states at the same time. This is known as the superposition principle in the quantum world. Taking advantages of quantum physics to build a computer leads us to the era of quantum computing where the law of classical physics will not be applicable anymore. A quantum computer uses a qubit instead of a bit which is used in the conventional computer. To imagine the power of quantum computer, let's consider a sphere as storage of information. A bit can be at one of the poles of the sphere while a qubit can exist at any points on the sphere. It means that, the quantum computer can store enormous amount of information with less energy than the conventional computer does. The quantum computer also can be used for quantum simulations to design new materials which is practically impossible to tackle with conventional computers. The quantum computer has more other advantages over the conventional computer. However, building a quantum computer is incredible complex. It is therefore of fundamental importance to understand physics in atomic scales and properties of materials to realize quantum computers.

Nanowires are small structures with typical diameters of 10-100 nm and lengths of several micrometres. Nanowires provide an excellent platform to study interesting quantum phenomena in nanostructures. Combinations with wide range of martials in growth can be achievable due to relaxed strains in the nanowires. Nanowires can also be grown in complex structures. For example, radially grown 'core-shell' nanowires can be achieved by first growing a core nanowire, then changing the growth conditions to deposit a homogenous shell around it. Many other advantages that nanowires have, make them attractive for various applications, including building quantum computers by using devices made of nanowires.

The focus of this thesis is to investigate low temperature charge transport properties of III-V narrow bandgap semiconductor nanowires. Various fascinating physics of mesoscopic systems are studied with devices which are made of III-V narrow bandgap semiconductor nanowires.

List of papers

This thesis based on the following papers:

I. Ambipolar and temperature dependent transport properties of InSb nanowires grown by chemical vapor deposition

B. Dalelkhan, V. F. Maisi, D. Göransson, C. Thelander, K. Li, Y. J. Xing, and H. Q. Xu

Manuscript

I took part in project planning and device designing. I fabricated the devices, performed the measurements, I did data analysis and wrote the manuscript with the help of the listed authors.

II. Strong spin-orbit interaction and spin relaxation in InSb nanowires revealed by magnetotransport measurements

B. Dalelkhan, D. Göransson, A. M. Burke, V. F. Maisi, K. Li, Y. J. Xing and H. Q. Xu

Manuscript

I took part in project planning and device designing. I fabricated the devices, performed the measurements, I did data analysis and wrote the manuscript with help from the listed authors.

III. Quantum dots realized in InSb nanowires using side finger gates by employing a single step lithography technique

B. Dalelkhan, D. Göransson, V. F. Maisi, A. M. Burke, P. Caroff, and H. Q. Xu

Manuscript

I took part in project planning and device designing. I fabricated the devices, performed the measurements, I did data analysis and wrote the manuscript with help from the listed authors.

IV. Side-gated, enhancement mode, InAs nanowire double quantum dot devices-towards controlling transverse electric fields in spin-transport measurements

Dorsch, S., **Dalelkhan, B**., Fahlvik, S., and Burke, A. M

Nanotechnology 30, 14, 144002, 2019.

I contributed to the development of the side gate techniques and the writing of the paper.

V. Coulomb blockade from the shell of an InP-InAs core-shell nanowire with a triangular cross section

Göransson, D. J. O., Herulin, M., **Dalelkhan, B**., Abay, S., Messing, M. E., Maisi, V. F., Borgström, M. T., Xu, H. Q

Applied Physics Letter. 114, 5, 053108, 2019.

I contributed to the part of the measurements, discussions and data analyses. I gave comments on the manuscript.

The following paper is not included in the thesis:

VI. Proximity Induced Superconductivity in Triangular InP-InAs Core-Shell Nanowires

David J. O. Göransson, **B. Dalelkhan**, V. F. Maisi, M. E. Messing, M. T. Borgström, and H. Q. Xu.

Abbreviations

InAs	Indium arsenide
InSb	Indium antimonide
QD	Quantum dot
NW	Nanowire
DQD	Double quantum dot
PSB	Pauli spin blockade
SOI	Spin-orbit interaction
FET	Field effect transistor
WL	Weak localization
WAL	Weak antilocalization
EBL	Electron beam lithography
SEM	Scanning electron microscopy
MF	Majorana fermions
QC	Quantum computer
TQC	Topological quantum computer

Chapter1
Introduction

1.1 Semiconductors and Nanoelectronics

Quantum theory gives a deep insight into interactions between the crystal structure of materials and electrons. The interactions generate a concept of the band structure in a solid, which describes the available states of electrons in the material. In a bulk material, relatively continuous bands separated by bandgaps are formed by these states. The occupation of electrons in these states are determined by the Fermi-Dirac distribution which describes the number of occupied states as a function of energy, E, above the fermi level, E_F:

$$f(E) = \frac{1}{e^{\frac{E-E_F}{KT}}+1} \tag{1.1}$$

In a metal, the Fermi level is located within one of the bands where many unoccupied states are available (conduction band) that make the electrons or charge carriers free to move, therefore metals are highly electrically conductive. In contrast to a metal, the Fermi level is located within a bandgap in an insulator. As a result, an insulator does not conduct any current. Since the Fermi level is located within the bandgap for a semiconductor, under normal conditions, the electrical conductivity of a semiconductor is very low. However, compared with insulators, semiconductors have a smaller bandgap that makes it possible to tune and control the conductivity of semiconductors by supplying an energy from external sources, like heating or irradiating with light. In electronics, the conductivity of a semiconductor can be tuned by either introducing doping atoms to control the number of charge carriers in the semiconductor or by using an electric field to shape the band structure.

The outstanding properties of semiconductors, such as their flexibility and tunability of the conductivity have brought rapid developments in the semiconductor industry. It began with the invention of the transistors in 1947 by J. Bardeen, W. Brattain, and W. Shockley at Bell Labs. The transistor has become a building block for performing logic functions in most electronic devices. Therefore, its inventors were awarded the Nobel Prize in Physics [1]. The next breakthrough in electronics was

the invention of the integrated circuit by Jack Kilby and Robert Noyce in 1958. Since then, modern electronics which is based on Si Metal-Oxide-Semiconductor (CMOS) has experienced an exponential development in integration density and performance during the last 50 years. The development of CMOS circuits was driven by the miniaturization of the transistor size according to Dennard's classical scaling principle [2]. Dennard's scaling rule allows improvement in performance and power efficiency by geometry scaling. Therefore, the traditional scaling has been the main focus of the industry to achieve developments in performance. For example, one of the processors, introduced by Intel in 2007, has 820 million transistors with a minimum feature size of 45 nm [3], today the transistor size is about 22 nm.

However, as the size of transistors are reduced to a length scale of only a few atoms, it is revealed that the miniaturization is faced with a number of problems and obstacles. For example, reduced gate response, a high off state current introduced by short channel effects and a poor subthreshold slope [4]. Moreover, as the size of a transistor becomes comparable to the electron wavelength, quantum mechanical effects like tunneling, interferences, confinement happen. The transport in a transistor is governed by these quantum effects, which cause degradation of device performances. It will therefore be unlikely to keep shrinking the transistor size in future transistor designs. This challenge brings a need for researchers to develop new materials, novel gate geometries and new devices which rely on the advantages of utilizing quantum effects [5-7].

1.2 Quantum computers

A long term, but revolutionary solution to increase the functionality of computation is building a quantum computer (QC). A QC is a machine which is made using bizarre concepts of the quantum world. For example, superposition, allowing a particle in multiple states at the same time; quantum measurements, where the outcome of a measurement is uncertain, depending on how it is detected; and entanglement - 'spooky action at a distance'. These quantum properties enables a quantum computer to perform calculations, which would be impossible to tackle by its counterpart classical computer. As examples, quantum algorithms are predicted to solve certain problems, among these are, factoring large numbers or searching unstructured databases faster than classical algorithms. The QC is also expected to help us design new materials more efficiently, for instance room temperature superconductors or catalyst for reduction of greenhouse gases. The QC would also allow us to decode cryptic codes and simulation of quantum systems, which may be a key to the development of new medicines and new materials [8].

The elementary component of a quantum computer is the quantum bit or qubit, which can, unlike a classical bit, be in a superposition of binary states, 0 and 1.

Qubits made from several quantum systems, which have their own advantages and challenges, are being investigated. For example, single atoms in ion traps [9], NV defect centres in diamond [10], superconducting circuits [11], semiconductor qubits [12], and topological qubits [13]. In order to carry out quantum computing by qubits, the quantum states of the qubits have to be initialized, read out and manipulated [14]. In contrast to classical bits, quantum states are sensitive to interactions with the environment and measurement systems. Consequently, the main technological challenge emerging for quantum computation is losing coherence of the quantum states. The loss of coherence limits the time for using qubits to computation. Concerning the materials we have studied in this thesis, we will give a very brief review of spin qubits and topological qubits.

1.3 Spin qubits

The concept of a semiconductor spin qubit is based on the use of the spin degree of freedom. A long spin dephasing time (approaching microseconds) [15-17], ultrafast coherent spin manipulation [18], phase coherent spin transport over a distance of up to 100 μm [15-17] have been experimentally revealed in semiconductors. Indeed, it makes the spins in a semiconductor promising for the implementation of spin qubits. Electrons in semiconductors can be controlled by confining them into a 'tiny box' referred to as quantum dots. In a quantum dot, the motion of electrons is restricted in all three dimensions giving rise to quantization of the energy spectrum resembling that of an atom. In fact, semiconductor quantum dots provide great flat form to manipulate and control spin states. The combination of these two fields, using spin of electrons in quantum dots as spin qubits was proposed by Loss and Di Vincenzo [14]. This proposal uses two qubit quantum gates based on the exchange interaction of coupled quantum dots, and relies on spin-to-charge conversion for efficient read-out schemes. Unfortunately, this spin-charge coupling was found to make the qubits sensitive to electrical noise, particularly to low-frequency noise [19]. Spin-orbit interaction (SOI) is one source of decoherence, because it mixes spin and charge [20]. However, it has been proposed to use SOI to manipulate coherent interaction of qubits [21, 22]. Unlike the exchange interaction, SOI generates states of spin and charge where the mixing happens at a high frequency, which makes the qubits tolerant to low frequency noise [23]. A recent theoretical study of InSb NW demonstrates that SOI can be tuned and controlled by using different gate configurations to modify the symmetry and charge distribution in the nanowire [24]. Therefore, quantum dots made of semiconductor materials with strong SOI are of current interest for the implementation of spin based quantum information technologies.

1.4 Topological qubits

An alternative approach to address the problems that appeared in QC is to use the topology state of a matter. Topological quantum computation relies on exotic quasi particles, called anyons, for storing and manipulating quantum information [25]. The exotic statistical behavior of anyons, which in neither like bosons nor fermions [25], the presence of a non-trivial quantum evolution described by topology, makes them insensitive to local geometrical details. Therefore, when anyons are used to encode quantum information, this topological behavior provides much desired tolerance of local perturbations and control errors [25]. In other words, anyons create a degenerate coherence sub-space that can only be discharged when the anyons are moved adiabatically around each other. Let us assume that we have topological qubits where part of the quantum state is in point M, while the other part is far away from M, in point N. Disturbances that occur at M and N would not change the state of the qubits, unless there is a transfer of the qubit from one state to the other state, such as N→M, or M→N. This 'topological protection' makes the topological qubits promising for realizing quantum computation. Anynons are also expected to have applications in quantum errors and quantum error corrections [25].

Naturally, the question arises about which systems could anyons be created in? Several topological states that support anyons have been predicted. For example, fractional quantum hall states that occur by interaction of cold electrons at very strong magnetic fields, spin liquids generated by collective states of strongly interacting spins, and topological superconductors (p-wave superconductors) in heterostructures [25]. While natural p-wave superconductors are yet to be found, topological superconductors can be engineered under certain conditions. For example, when a spin-orbit coupled semiconductor [26], a topological insulator, [27, 28] or a chain of a magnetic atoms [29, 30] is placed in the proximity of a regular s-wave superconductor. According to a proposal made by Kitav [31], wires made of the above materials in combination with s-wave superconductors can host a pair of anyons, referred to as Majorana fermions at the ends of the wire which can be probed by tunneling measurements.'Majorana fermions' are a consequence of a real solution to the Dirac equation [25]. The following ingredients have been put forward for creating Majorana fermions in a nanowire based device [31-33]: (1) a one-dimensional electronic system, ensures that only two Majorana fermions are created at the ends of the wire (2) spin orbit interaction, mixes the spin up and down (3) superconductivity, supply electrons with opposite spins. (4) Magnetic fields, lifts the spin degeneracy. It is worth to point out that in order to achieve the realization of Majorana modes, it is essential to choose suitable materials which ensure to fulfil the above ingredients.

1.5 Narrow bandgap III-V semiconductor nanowires

Semiconductor nanowires are a perfect platform for studying various interesting quantum and topological phenomena [34-37]. Due to their low density of defects and relaxed strain, growth of materials in a wide range of combinations and complex structures can be achieved [38]. The quasi one-dimensional geometry of nanowires allows for the creation of quantum dot systems by confining electrons via gate electrodes [35]. On the other hand, core-shell nanowires have been gaining attentions for studies related to quantum interference and quantum topology [39, 40].

Among other III-V compound semiconductor nanowires, a great deal of attentions is paid to narrow bandgap nanowires like InSb and InAs because of their unique transport properties, such as high electron mobility [41], large Lande g-factors [42, 43] and strong spin-orbit interactions [43]. The first InAs NW based spin qubits were realized in 2010 by Nadj-Perge et al. [34] and subsequently with InSb NWs in 2013 by Van den Berg et al. [44]. Helical spin states were reported from measurements with InSb NW devices [45], which is essential for quantum information processing. Beside their ability to realize spin qubits, the combination of strong spin-orbit interaction and the superconducting proximity effect, make these nanowires promising materials to explore Majorana fermions and ultimately topological qubits. So far, great efforts have been made to create Majorana fermions with quantum devices made from InSb and InAs nanowires [36, 37, 46, 47].

1.6 Aim and content of this thesis

In this thesis, we aim at investigating charge transport in III-V narrow bandgap semiconductor nanowires, especially we are interested in InSb, InAs and InP-InAs core-shell nanowires.

To investigate charge transport properties of InSb nanowires grown by chemical vapor deposition (CVD), we made field effect transistors with these nanowires and performed electrical measurements for various temperature ranges in paper I. We further extended our measurements with CVD grown InSb nanowires to magnetoconductance measurements in quantum diffusive regime to explore spin relaxation and spin-orbit interaction strength in paper II. A side gate technique is developed and used to form both single and double quantum dots to study electron transports in InSb nanowires quantum dots in paper III and InAs nanowire double quantum dots in paper IV. Low temperature electron transport properties of InP-InAs core-shell nanowires are investigated in paper V.

This thesis is organized as follows:

Chapter 2 describes material growth methods, device fabrication techniques and measurement set up.

Chapter 3 describes charge transport in InSb NW field effect transistors. The temperature dependent transport properties of InSb NW grown by chemical vapor deposition are investigated. Field effect mobility for holes and electrons are extracted and their dependence on temperature are explored. The bandgap of the material is extracted. Dependence of off state current on channel lengths and temperatures are studied.

Chapter 4 describes quantum diffusive transport in InSb nanowires. Magneto-conductance measurements under low magnetic fields are performed. The experimental results are interpreted using weak localization quasi 1D theory. Spin relaxation length, phase coherence length, and spin-orbit strength are extracted.

Chapter 5 describes electron transport in single quantum dots. InSb nanowire single quantum dots are defined by side gates. Various transport features from sequential tunneling to higher order cotunnelings are investigated. Low temperature transport properties of InP-InAs core-shell nanowires are also studied and Coulomb blockade effect is observed from a quantum structure formed in core-shell nanowires.

Chapter 6 describes electron transport through a double quantum dot. A double quantum dot is formed in InSb and InAs nanowires by side gates. Electron transport in weakly coupled double quantum dots are studied. Pauli-spin blockade is observed. Evolution of quantum states in Pauli spin blockade region with external magnetic fields are investigated.

Chapter 2
Materials and device fabrication

To make nanoscale devices, advanced nanofabrication techniques are essential. For the devices studied in this thesis, we rely on sophisticated nanowire growth techniques and art clean room facilities to make our nanowire devices. In section 2.1, we will briefly describe material properties and nanowire growth techniques. A description of nanofabrication techniques used to make single nanowire devices are included in section 2.2. In section 2.3, we will introduce the measurement set-up used for low temperature electrical measurements on the fabricated devices.

2.1 Materials and growth techniques

Semiconductor nanowires are a perfect platform for optoelectronics and nano-electronics due to their following advantages: First of all, carrier motion is limited to the axial direction. Strong confinement in the radial direction of the nanowires makes them attractive for studying quantum dot systems where dots can be formed easily with various methods, such as electrical gating [35], and using different crystal phase structures [48]. Secondly, the one-dimensional geometry of the nanowire allows for combining complex device fabrication for making devices with novel designs and gates. As examples, local bottom gates, top gates, and all-around gate geometries. Thirdly, enhanced surface effects due to the small scale lead to the formation of crystal structures which usually do not exist in their counterpart bulk materials [49]. Finally, because of their small diameter, strain can be relaxed giving access to combinations of materials in broader ranges in the growth process [38]. This applies to both axial growth of heterostructure nanowires and radial growth to achieve core-shell nanowires [50-53].

Nanowires can be epitaxial grown by using several different growth techniques for instance, metal organic vapor phase epitaxy (MOVPE), molecular beam epitaxy (MBE), chemical vapor deposition (CVD) and chemical beam epitaxy (CBE). The underlying mechanism for nanowire growth is the vapor-liquid-solid (VLS) mechanism proposed by Wagner and Ellis in the mid-1960 [54]. The VLS mechanism is based on the assistance of a metal catalyst in the growth process. In

this mechanism, at high temperatures, a liquid alloy is formed by the metal catalyst that absorbs vapor components. For some reason, the alloy gets supersaturated and becomes a solution with higher actual concentration of the component than the equilibrium concentration. This leads to precipitation of the component and it is driven to the liquid-solid interface to achieve the minimum free energy of the alloy system. Consequently, nanowires start to grow and continue their growth as long as the vapor components are being supplied. Since, vapour (carriers of solid components), liquid (catalyst alloy) and solid phases participate in the growth process, it is called the VLS mechanism. A schematic illustration of the VLS mechanism is shown in figure 2.1. The diameter of the nanowires is determined by the size of the metal catalyst particles. In the following, we will describe some growth techniques in which VLS is applicable and used to grow the nanowires studied in this thesis.

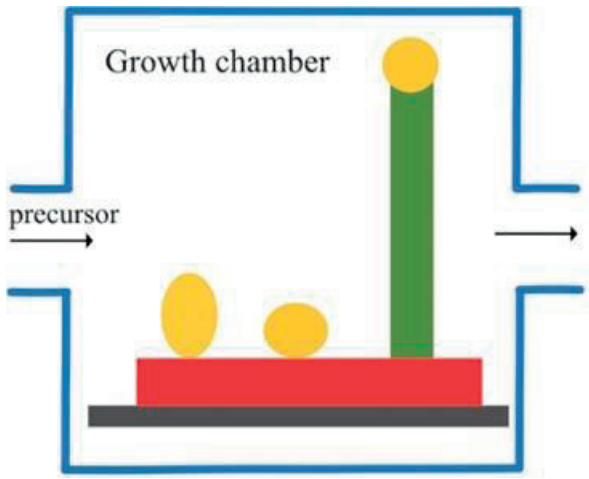


Figure2.1: A schematic illustration of VLS mechanism for nanowire growth.

Chemical Vapor Deposition (CVD) The CVD contains a gas delivery system to supply the precursors. Usually, either pure hydrogen H_2 or pure nitrogen N_2 is used as a carrier gas. The precursors are placed individually in the mixing chambers. In the chamber, the precursors are first evaporated at high temperatures, then with assistance of the carrier gas enter into the cell to be deposited on the heated substrate by the chemical reactions occurring on or in the vicinity of the substrate. The CVD enables epitaxial synthesis of InSb NWs. The growth rate can be varied with the molar fraction of the III/V ratio which in turn depends on the type of precursors and growth temperatures. CVD offers the possibility of synthesis of InSb NWs with dimeters varying from below 10 nm up to tens of micrometres in lengths. For the work in papers I and II we used CVD grown InSb nanowires to make the devices. For more detailed descriptions of InSb nanowire growth with CVD we refer

reference [55]. A SEM image of InSb nanowires grown by CVD is given in figure 2.2a.

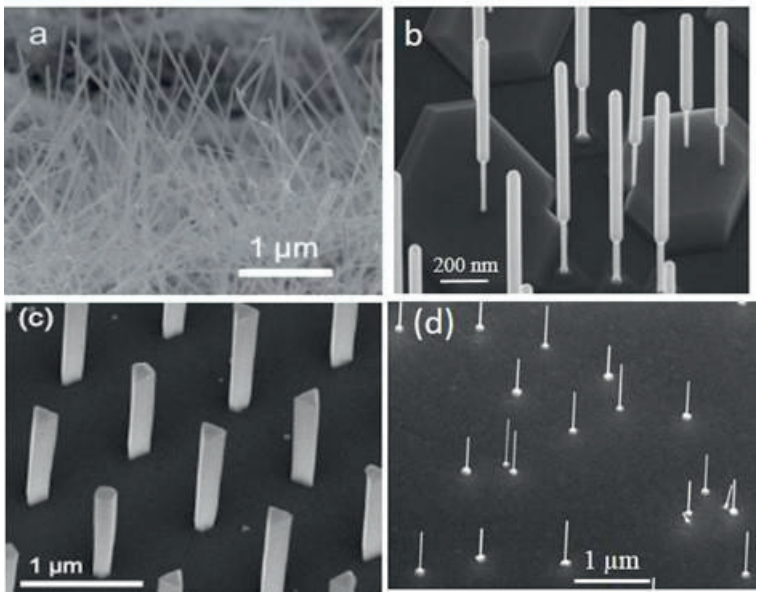


Figure 2.2: (a) SEM image of InSb NWs grown by CVD, 80° tilted view. (b) SEM image of InAs/InSb NWs grown by MOVPE, 30° tilted view. (c) SEM image of the InP-InAs core-shell NWs grown by MOVPE. (d) SEM image of InAs NWs grown by CBE, tilted 30°.

Metal organic vapor phase epitaxy (MOVPE) it is the most versatile epitaxial growth technique and can be used for large-scale systems. Similar to CVD, carrier gases such as hydrogen are used in MOVPE systems. The precursors used in a MOVPE system are generally an alkyl and a hydride for the III and V sources respectively. The sources are usually kept in 'bubblers' at constant temperatures and their flow rate can be controlled by the rate of hydrogen flow through the bubblers. Before starting the growth, these precursors are mixed then introduced into the reaction chamber by the carrier gas and directed onto the hot substrate where chemical reactions occur. The growth process is controlled by the molar fraction of the reactants and temperature. The InSb nanowires used for the work in paper III are grown by MOVPE on an InAs substrates. At first, InAs nanowires were grown to form a stem, then changing the As source to Sb, the growth of InSb NWs is achieved. The full descriptions of the InAs/InSb nanowire growth are given in ref. [56]. In figure 2.2b, a SEM image of the InAs/InSb nanowires grown by MOVPE are presented. The InP-InAs core-shell nanowires (figure 2.2c) investigated in paper V was also grown by MOVPE using a selective area growth method.

Chemical beam epitaxy (CBE) Nanowires grown by CBE differ in many aspects from the nanowires grown by other methods. CBE can be considered as combinations of MOVPE and MBE. In contrast to MOVPE, the growth temperature window is significantly broader [57] and no carrier gas is needed for a CBE system [57]. In CBE, the metal-organic precursors can be directly introduced into the growth chamber without a carrier gas. The nanowires grown by CBE can have the following advantages: A high growth rate is expected due to ballistic mass transport to substrate at low pressure. As a result, pure nanowires without any contamination can be obtained. The ingredients for growth of the nanowires can be adjusted by a digital mass controller. The InAs nanowires (in figure 2.2d) used for the studies in paper IV were grown by CBE. Detailed discussions of InAs NW growth by CBE can be found in ref [58].

Among III-V compound semiconductors, InSb NWs and InAs NWs are of great interest to use in nanoelectronics and quantum information processing technologies because of their unique transport properties. For examples, narrow bandgap, high electron mobility, large g-factors and strong SOI. The strong SOI in these nanowires, has drawn a lot of attention for using them in combination with superconductors to create Majorana fermions [36, 46]. These nanowires also differ from each other in some aspects, leading to separate considerations when they are used to make devices and their transport features are investigated. InSb nanowires have zinc blende (ZB) crystal structure [55], which is a face centred cubic (fcc) structure with two different atoms, In and Sb, at each basis point. The crystal structure of InAs nanowires can be either ZB or wurtzite depending on growth conditions and nanowire diameters [59-60]. These two different crystal structures, result in InAs nanowires having different band structures and bandgap energies. Theoretical and experimental studies show that the bandgap of InAs NWs with WZ structure have from tens of to hundreds of meV larger than that of InAs nanowires with ZB structure. It was confirmed that, the InAs nanowires we studied in this thesis exhibit the Wurtzite crystal structure.

2.2 Device fabrication

2.2.1 Preparation of device substrates

In order to fabricate nanowire devices, the nanowires will be transferred from the growth substrate to a suitable device substrate which consists of bit markers and metal electrode pads. The markers are required to define the nanowire coordinates and to align the of electron beam lithography (EBL) processing. The metal electrode pads are used to connect the fabricated devices to the measurement set-up via a chip

carrier and aluminium bonding wires. A highly doped Si substrate covered with 100-200 nm SiO_2 is used for the device substrate, which can serve as a global back gate in combination with thin metal layers. In this subsection, we will describe how to prepare a device substrate.

We used highly n-doped Si substrates covered with thermally grown 100-200 nm thick SiO_2 to make device substrates. First, we begin to prepare the global back gate. The front side of the wafer is covered with UV resist to avoid etching of SiO_2 while the back side is being cleaned from the native oxide using HF, followed by a deposition of Ti/Au (10nm/90nm) layers in the chamber of a thermal evaporator. Next, electrode pads are defined via a UV lithography method. After development, the sample is transferred to the thermal evaporator to deposit Ti/Au (10 nm/100 nm) layers followed by the standard lift-off process. Finally, a set of grid and markers are patterned with the following sequential steps of: EBL exposure, development, oxygen plasma etching, deposition of Ti/Au, and lift-off. The images of a fabricated device substrate (chip) is given figure 2.3.

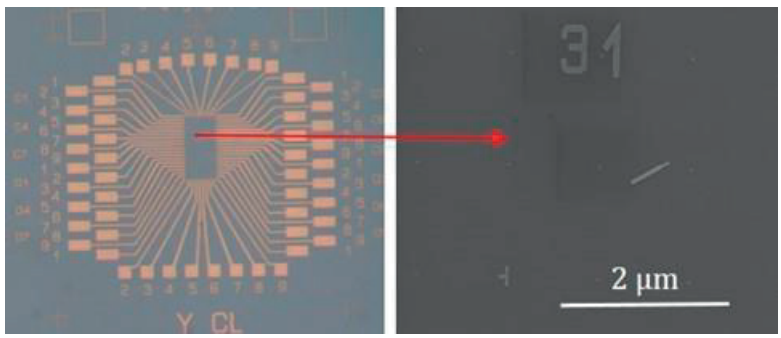


Figure 2.3: Optical microscopy image of a device substrate (the left figure), SEM image of the coordinate system (the right figure).

2.2.2 Fabrication of nanowire devices

Nanowire transfer

After having prepared the device substrates, the nanowires need to be transferred to a device substrate (chip) to make devices. The nanowire transfer is done by using a tissue, gently wiping it over the growth substrate and then over the device substrate, where the nanowires will be deposited randomly on the chip. Sometimes for special purposes, the nanowires are required to be transferred deterministically onto the chip. This can be achieved with a wire deposition set up. This set up consists of an optical microscope and an indium tip. A single nanowire on the growth substrate is

identified by an optical microscope and removed from the substrate using the indium tip. The nanowire can then be deposited at the targeted place on the chip. After that, the nanowires are imaged using an optical microscope or scanning electron microscopy to locate their coordinates for EBL exposures.

Preparation of contacts

Contacts to the nanowires can be made via a lift-off process as demonstrated in figure 2.4. First the sample is spin coated with a positive resist, followed by baking on a hot plate. The baking time and temperature are determined by the properties of the resist. Next, the contact patterns are defined using EBL. Development is required to dissolve the areas of the resist which were exposed by the electron beams. Further, the samples are ashed by oxygen plasma ashing to remove the residual resist. Nanowires have a thin native oxide layer on the surface, which prevents a direct contact to achieve desirable contacts. Prior to deposition of metal electrodes, therefore, the native oxide has to be removed. Concerning the nanowires we investigated in this thesis, this can be achieved with two different methods, sulphur passivation and dry etching. For the sulphur passivation method, the nanowires are etched using a diluted ammonium polysulfide $(NH_4)_2S_x$ solution. The method is more controllable, consequently the damage to the nanowires during the etching can be reduced or avoided. The dry etching relies on bombarding the nanowires using high energy ions, for example with argon [61]. An advantage of the argon etching is that the metal electrodes can be deposited in the same chamber right after the etching, avoiding the re-oxidation of the nanowires. The drawback is, the crystal structure of the nanowires can be damaged during the etching. We used the sulphur passivation method for all our devices studied in this thesis. An SEM image of an InSb nanowire after the etching is given in figure 2.5a. After the etching the nanowire, metal electrodes are deposited by using a thermal evaporator. Followed by a lift-off process, the contacts to the nanowire devices are completed. One of our global back gate devices with Ti/Al contacts to an InGaSb nanowire is shown in figure 2.5b.

Preparation of gates

To locally control the electrical potential in the nanowires, either side, bottom, or top gates can be used. The advantage of the side gates is that it can be done with single lithographic step, together with forming of the contacts. However, due to the poor dielectric permittivity of vacuum, the side gates have to be as close as possible to the nanowire to achieve stronger gate coupling to the wires. We found better side gate performance at less than 50 nm distance between the side gates and nanowires. That demands precise EBL alignment and controls over the fabrication processing

to prevent short circuiting between the side gates and nanowires. Making top gates and bottom gates require use of dielectric materials. Aluminium oxide (Al2O3) and

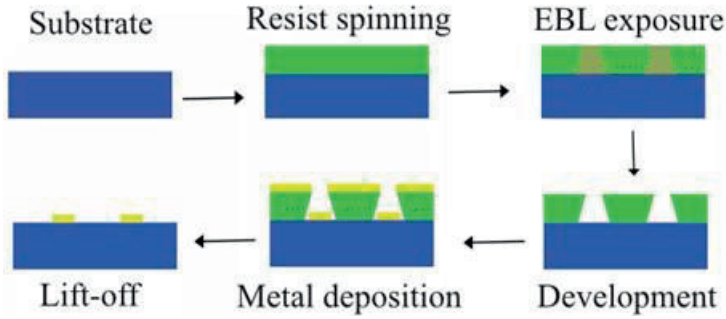


Figure 2.4: Schematic illustration of lift off process using electron beam lithography.

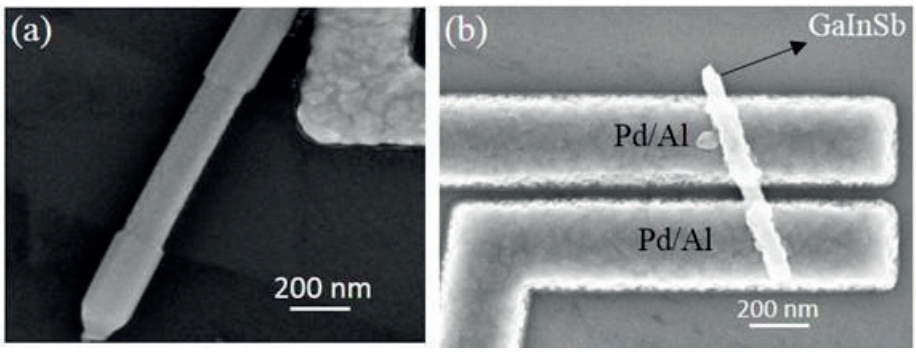


Figure 2.5: (a) SEM image of etched InSb nanowires by wet etching method described in the text. (b) SEM image of InSb nanowire devices connected two Pd/Al contacts.

hafnium oxide (HfO_2) are often used due to their high k values, which enable strong coupling of the gates to the nanowires. The dielectrics can be deposited using atomic layer deposition (ALD). Our fabrication procedure for top and bottom gates as follows, after defining the gate patterns with EBL, a 10 nm thick HfO_2 layer grown by ALD at 90 °C for either top gates or bottom gates. Due to step coverage of this process, the lift-off becomes hard. To do the lift-off after the ALD deposition, the sample is left in acetone overnight, followed by ultra sound at low power. Top and bottom gates can also be done with a mask etching method, in which process the entire chip is covered with oxide, then an etch mask is defined with EBL followed by etching using hydrofluoric acid (HF) or dry etching with Argon ions to access contact and bonding pads [62]. The top gates provide stronger coupling than the other gate techniques. However, the drawback is the presence of pronounced charge

trap states at the nanowire-dielectric interfaces. Choosing suitable dielectric materials and reliable recipes are therefore, essential to have higher quality top gates. Moreover, bottom gates can also be fabricated with a suspended nanowire design. In that case, there is no need for dielectric materials. Thin metal stripes are created with different heights using EBL and a metal evaporator. Transferred nanowires onto the stripes are expected to be suspended, the patterns underneath the wire can be used as gates. Figure 2.6 displays our fabricated devices with different gate designs.

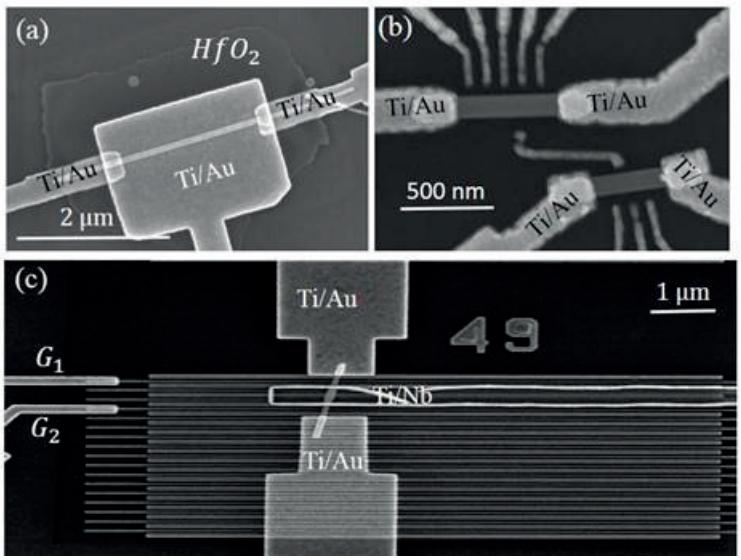


Figure 2.6: SEM images of InSb nanowire devices in different gate designs. (a) A top gate device, 10 nm hafnium oxide was deposietd on the nanowire by ALD. (b) Two nanowire devices with side gates coupled via a metal stripe. (c) InSb nanowire suspended device with two Ti/Au and one Ti/Nb contact. The wide and thin metal stripes have different heights to suspend nanowire onto the wide metals while the thin stripes underneath the nanowire serve as bottom gates.

Post-processing

After making the devices, in next step the chip is glued on a chip carrier using silver paint. Connections between the devices and the chip carrier are done by using ultrasonic wire bonding with an aluminium wire. For the devices with a global back gate, care must be taken to avoid damage of the SiO_2 during the bonding to prevent leakage currents from appearing between the contacts and the back gate. One of bonded chips is shown in figure 2.7a.

2.3 Measurement set-ups

Observations of quantum mechanical effects require low temperatures which can be achieved in a dilution refrigerator. Most of the measurements described in this thesis are performed in a dilution refrigerator with electron temperatures below 100 mK. Figure 2.7b presents the dilution refrigerator used for the measurements discussed in this thesis. Some components are required to connect the device inside the dilution refrigerator to room-temperature measurement electronics. The bonded chip on a chip carrier is loaded to the dilution fridge by using a sample holder of the dilution fridge, figure 2.7c. Signal filters such as low-temperature RC-filters, room temperature π-filters are required to be installed inside the fridge to suppress noise and accurately measure the small signals. As shown in figure 2.7d, for DC measurements or low-frequency (50-100 Hz) AC measurements Yokawa, Keithley voltage meters or a lock-in amplifier are used. The measurement set-ups communicate with a computer via a GBIB interface. We used labview programs developed by Cleas Thelender to run the computers for measurements.

Figure 2.7: (a) The device chip is glued on a chip carrier and bonded with Al wires to electrically connect the device to measurements pads. (b) The picture of dilution fridge used for the most of the measurements described in this thesis. (c) The sample holder of the dilution fridge used to load the devices into the fridge. (d) Electronic set ups used for the measurements.

Chapter 3
InSb nanowire field effect transistors

3.1 Introduction

It has been challenging to grow thin and long InSb nanowires with the most common growth techniques, like molecular beam epitaxy, chemical beam epitaxy and metal organic vapor phase epitaxy. Because InSb has a low surface energy which leads to InSb tends to float on top of the substrate. However, CVD can overcome these challenges, resulting in the growth of InSb nanowires with a diameter of down to 5-10 nm, and lengths of up to tens of micrometer [38]. The dimensions can play a critical role for transport in mesoscopic systems. It determines what kind of transport takes place in the system and therefore, the underlying physics could be different. Quantum confinement in the transverse direction of a nanowire increases as its diameter decreases. This leads to significant changes in their transport properties like mobility, effective mass, bandgap and spin orbit coupling strength. A comprehensive study of transport properties of InSb nanowires grown by CVD has so far been missing.

In this chapter, transport properties of InSb nanowires grown by chemical vapor deposition are explored by employing top gate field effect transistors. This chapter begin with introducing physics of nanowire field effect transistors, followed by discussions about experimental results.

3.2 Physics of nanowire field effect transistors

A nanowire FET consists of three terminals as presented in figure (3.1a): a gate terminal that is electrically isolated from the nanowire by a thin insulating layer; source and drain reservoirs connected to the nanowire. The nanowire length L between the source and drain determines the transistor size and the ultimate speed of the transistor. The conductance of the nanowire channel is controlled by the gate. The operation principle of MOSFETs can be well explained by the height of an

energy barrier in the channel, as illustrated in figure (3.1b). The voltage applied to the gate modulates the barrier height by either raising or lowering it. In the case of non-equilibrium, where there is a potential energy difference between the chemical potentials of source and drain, when negative voltages are applied to the gate of n-MOSFETs, the barrier height is high, and electrons are blocked from flowing between source and drain in results the transistor is off. If positive voltage is applied to the gate, the barrier is lowered, and electrons start to flow from source to drain, the transistor will be in the on state. The drain current I_D of a MOSFET can be

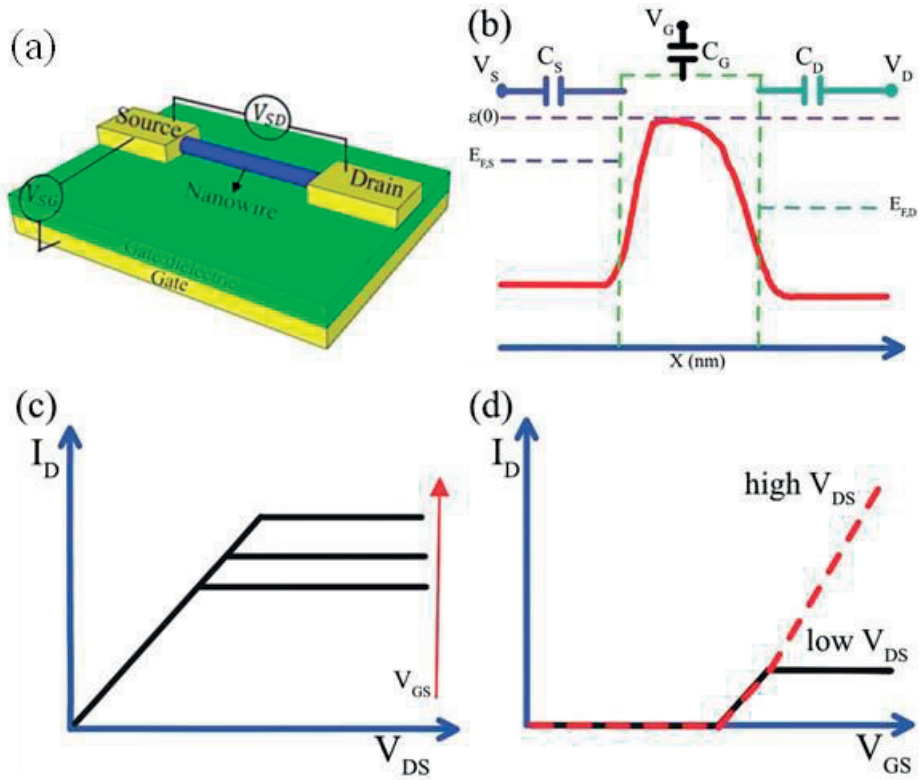


Figure 3.1: (a) Schematic illustration of a NWFET. (b) Top of the barrier model for a conduction band of a MOSFET. The transistor consists of three capacitances to modulate the channel charge. (c) Output characteristics of the MOSFETs (d) Transfer characteristics of the MOSFETs.

illustrated by two different two-dimensional graphs as shown in figure (3.1c-d): in the output characteristic, I_D is measured as a function of V_{SD} at fixed V_{GS} and for the transfer characteristic, I_D is measured as a function of V_{GS} at fixed V_{SD}.

As can be seen in fig. (3.1c), at low source-drain voltages V_{DS}, the current I_D increases linearly with V_{SD}, then gets saturated at high source-drain voltages V_{SD}. In this region, the current I_D increases as the gate voltage V_{GS} is increased. For the

linear region, the device operates like a gate voltage dependent resistor. The on-state resistance can be determined by the inverse slope dV_{DS}/dI_D. The independence of current I_D for high gate voltage V_{GS} in low source-drain bais can been seen from the transfer characteristics in figure 3.1d. Depending on the length scales of the mean free path of the material l and channel length of the transistor L, a device operates in two different regimes. When $l \gg$ L the device in the ballistic regime, where no scattering events take place during the electron traveling from source to drain. In contrast, if L $\gg l$ the device is in the diffusive regime where scattering events are involved in the transport.

Characteristic features of 1-D ballistic transport in nanowire MOSFETs was theoretically investigated for T= 0 K by Raseong Kim et al. [63]. Using that reference, we will give a brief explanation of the I-V characteristics of a nanowire field effect transistor in the ballistic regime for T= 0 K. We assume that one sub band contributes to the transport. If positive bias V_{DS} is applied to drain, while the source is kept grounded, the fermi level on the source side is F_S, and on the drain side is $F_D = F_S - qV_{DS}$. Two currents in opposite directions are expected, which given by:

$$I^{+} = \frac{2q^2}{h}\frac{F_S - \varepsilon(o)}{q}\Theta\big(F_s - \varepsilon(0)\big), \tag{3.1a}$$

$$I^{-} = \frac{2q^2}{h}\frac{F_S - \varepsilon(o) - qV_{DS}}{q}\Theta(F_s - \varepsilon(0) - qV_{DS}), \tag{3.1b}$$

The step function Θ is introduced to indicate occupation of +k and –k states depending on the position of the source and drain fermi levels, with respect to the top of the barrier. The potential energy $\varepsilon(0)$ on top of the barrier plays a critical role for current flowing through the transistor. According to the top of the barrier model [64], $\varepsilon(0)$ can be determined as:

$$\varepsilon\,(0) = \frac{C_G}{C_\Sigma}(-qV_G) + \frac{C_D}{C_\Sigma}(-qV_D) + \frac{C_S}{C_\Sigma}(-qV_S) + \frac{q^2}{C_\Sigma}(n_L - n_0), \tag{3.2}$$

where C_G, C_D, C_S denote the gate, drain, and source capacitance, C_Σ is the sum of the capacitances, and n_0 is the carrier density at zero bias.

Assuming an ideal gate control, $\frac{C_G}{C_\Sigma} = 1, and\ \frac{C_S}{C_\Sigma} = 0, \frac{C_D}{C_\Sigma} = 0$ and setting V_S as reference ($n_0 = 0$) equation (3.2) can be reduced to:

$$\varepsilon\,(0) = -qV_{GS} + \frac{q^2 n_L}{C_{OX}}, \tag{3.3}$$

where $C_G = C_{OX}$ for MOSFETs and $n_L = n_L^+ + n_L^-$ is the 1-D carrier density. n_L^+ and n_L^- can be determined from the ballistic transport model as:

$$n_L^+ = \frac{\sqrt{2m^*(E_F - \varepsilon(0))}}{\pi\hbar}\Theta\big(E_F - \varepsilon(0)\big), \tag{3.4a}$$

$$n_L^- = \frac{\sqrt{2m^*(E_F - \varepsilon(0) - qV_{DS})}}{\pi\hbar}\Theta(E_F - \varepsilon(0) - qV_{DS}), \tag{3.4b}$$

where $m^*$is the effective mass and $\hbar$ is the reduced Planck's constant. The current I_D for output and transfer characteristic can be calculated by solving equations (3.3) and (3.4) self-consistently. However, a simple analytic expression for I_D can be obtained by considering the (3.3) and (3.4) in the following three regions:

I) When $\varepsilon(0) > F_S$, there are no available states, therefore $I_D = 0$, $n_L = 0$. According to (3.3) $\varepsilon\,(0) = -qV_{GS}$, and $\varepsilon\,(0)$ decreases with increasing positive gate voltages. As $V_{GS} > V_{Th} = -\frac{F_S}{q}$ current starts to flow, where V_{Th} is the threshold voltage.

II) When $F_S - \mathrm{q}V_{DS} < \varepsilon(0) \leq F_S$, $\varepsilon(0)$ is below F_S but above F_D, the current I_D flows only in one direction $I_D = I^+, n_L = n_L^+$, from equations (3.1a), (3.3) and (3.4a) the I_D current becomes:

$$I_D = \frac{2q}{h}\left[-\frac{\sqrt{2m^*}q^2}{hC_{OX}} + \sqrt{\frac{2m^*q^4}{h^2C_{OX}^2} + q(V_{GS} - V_{Th})}\right]^2. \tag{3.5}$$

III) When $\varepsilon\,(0) \leq F_S - qV_{DS}$, currents can flow in both directions and the net current I_D is equal to:

$$I_D = I^+ - I^- = \frac{2q^2}{h}V_{DS}\,, \tag{3.6}$$

The I-V characteristics in figure (3.1c, d) can be interpreted using the above analytical expressions for I_D. In the I_D-V_{DS} curve (figure 3.1c), as V_{DS} is smaller than saturation drain voltage V_{st}, the current I_D does not depend on V_{GS} as shown in (3.6). When V_{DS} becomes larger than V_{st}, $V_{DS} > V_{st}$ the current I_D shows independent of V_{DS} and increases with increasing V_{GS} as given in (3.5). Using the relation, $\varepsilon(0) = E_F - qV_{st}$, the V_{st} can be described as:

$$qV_{st} = \left[-\frac{\sqrt{2m^*}q^2}{hC_{OX}} + \sqrt{\frac{2m^*q^4}{h^2C_{OX}^2} + q(V_{GS} - V_{th})}\right]^2, \tag{3.7}$$

and V_{st} increases with V_{GS} as seen in figure 3.1c.

Figure 3.1d shows the $I_D - V_{GS}$ characteristics for a 1D-MOSFET at low and high bias V_{DS}. Following equation (3.5) at low a value of V_{DS}, $the\ I_D$ first increases with V_{GS}, then gets saturated, finally becoming independent of V_{GS} as seen in (3.6). This is due to the constant energy range. For smaller V_{DS} the transfer curves appear to be an abrupt step function. As V_{DS} become high, the current I_D keeps increasing with V_{GS} as predicted in (3.5). The physics behind this can be interpreted as increased energy ranges with increasing V_{GS}. When multiple sub bands contribute to the transport, at low bias the current increases in steps with the gate voltage V_{GS} and the conductance changes in discrete values, leading to quantization of the conductance. We will discuss this further in chapter 4.

3.2 Transistor metrics

Transconductance

An important transistor metrics is defined as the partial derivative of I_D with respect to V_{GS}

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3.8}$$

It can be understood as the number of amperes delivered per volt of the gate voltage above the threshold. In an RF-circuit, it is desirable to have a high g_m since it allows for a high low-frequency gain.

Threshold voltage

The threshold voltage V_T refers to the gate voltage at which there is transition from the off state to the on state. Its extraction is somewhat arbitrary. However, one of the most common ways to determine the threshold voltage is a linear extrapolation of the current I_D in the linear region of the transfer curve.

Sub-threshold swing

The sub-threshold swing is one of important metrics that determines how effective the MOSFETs are as switcher. In other words, the sub-threshold swing tells how much gate voltage V_{GS} is needed to change the I_D by a factor of 10. It is given by:

$$SS = \frac{K_B T}{q}\left[\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right] \tag{3.9}$$

The smaller the SS, the lower the gate voltage to turn the transistor from off to on. At room temperature, the theoretically limit of SS for MOSFETs is $SS \geq 60\,\frac{mV}{decade}$.

On state current I_{ON} and off state current I_{OFF}

The I_{ON} is the maximum drain current at the bias point defined as $V_{DS} = V_{DD}$, $V_{GS} = V_{OFF} + V_{DD}$, where V_{DD} is power supply voltage and V_{OFF} the gate voltage in which the drain current is equal to I_{OFF}. The off state current I_{OFF} is the minimum drain current of the transistor. The propagation delay of the CMOS inverter t_p is given by:

$$t_p = \frac{C_L V_{DD}}{2I_{ON}} \tag{3.10}$$

C_L is the capacitance of the load. As shown in (3.10) in order to have a small propagation delay, a large I_{ON} is desirable. A logic operation at higher clock frequencies needs to have a smaller propagation delay [65].

3.3 Experimental results and discussions

3.3.1 Temperature dependent transfer characteristics

In order to study transport properties of InSb nanowires grown by chemical vapor deposition, we fabricated top gate InSb nanowire field effect transistors. Devices were made with different channel lengths, particularly channel lengths of 1 μm and 260 nm. SEM images of one of the devices is shown in figure 3.2a. The device has a channel length of 1 μm and a nanowire diameter of 50 nm. A 10 nm thick HfO_2 was used as the top gate dielectric material. In addition to the nanowire, the top gate partially covers the source-drain contacts to obtain efficient gating of the nanowire over the full channel length. As illustrated in figure 3.2b, the wrap gate geometry of the device enables gating efficiently to tune the Fermi level from deep in the

conduction band to deep into the valence band, as a result achieving ambipolar transport.

To electrical characterise the fabricated devices, electrical measurements were performed in a temperature ranging from 4.2 K to 300 K. The measurement circuit

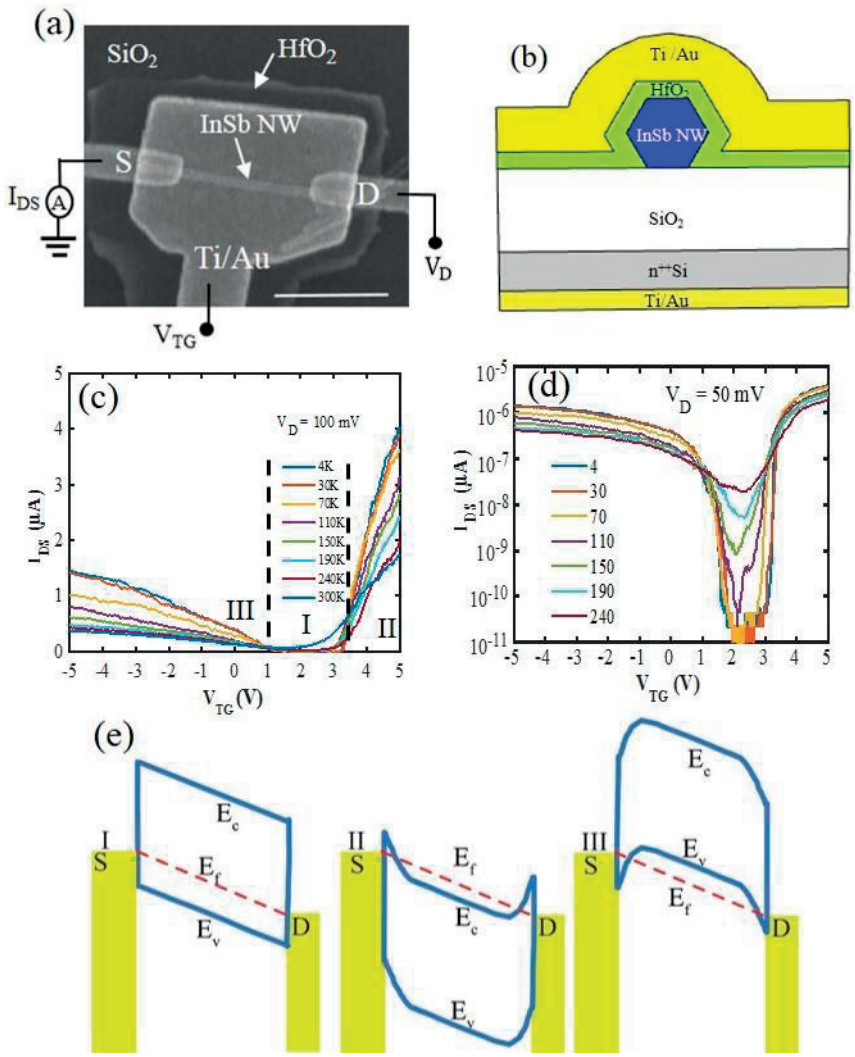


Figure 3.2: (a) SEM image of a top gate nanowire field effect transistor. (b) Cross section schematics of the device. (c) Transfer characteristics of the device in various temperatures at a source-drain bias of V_D = 100 mV. (d) Transfer characteristics in logscale plot for various temperatures at V_D = 50 mV. (e) Band diagrams illustrating Fermi level positions corresponding to the regions I, II, III in figure (c).

diagram is shown in figure 3.1a. We applied a fixed DC bias voltage V_D to the drain and measured the current I_{DS} from the source contact as a function of top gate voltage V_{TG}. The back gate was grounded throughout the measurements. The measured drain current I_D as a function of top gate voltage V_{TG} at various temperatures and at a fixed source-drain voltage V_D of 100 mV is shown in figure 3.2c. The transfer curves reveal clear ambipolar transport with three distinguished transport regions: In region I: 1.4 V $\leq V_{TG} \leq$ 3.2 V, the current I_{DS} is suppressed, since the Fermi level E_f resides within the bandgap of the material as shown in the middle diagram of figure 3.1e. In region II, where V_{TG} > 3.4 V and in the region III where V_{TG} < 1.4 V, the current I_{DS} increases with applied gate voltage V_{TG}, since in these two regions the Fermi level E_f enters into the conduction band or the valence band respectively. The corresponding band diagrams are given in figure 3.1e. The normalized maximum on currents are $I_{ON}/\pi d$=26 μA/μm for electrons and 10 μA/μm for holes at 4 K, where d is the diameter of the nanowire. The ambipolar transport has not been observed at low bias in previous reports for InSb NW FETs [66-69]. The lowest current in the bandgap known as the off current, I_{OFF} is smaller than the previously reported values [66, 67] and decreased from 65 nA at 300 K to below noise level of 2-3pA at 4 K.

Figure 3.2d depicts the transfer curves with logscale for various temperatures at a fixed V_D = 50 mV. It is obvious that in region I, the current I_D increases exponentially as the temperature increases. In this region, the transport is dominated by thermally excited currents through the bandgap of the material. In region II and III, the drain current I_D decreases as the temperature increases. The temperature dependence of the on state resistance in region II and III are given in figure 3.3a. The resistance decreases as the temperature decreases for both electron and hole transport sides. Similar temperature dependence behavior of the resistance has been observed for InAs nanowire field effect transistors [70] and InSb field effect transistors [71]. This was explained by a suppression of phonon scattering at low temperatures. From figure 3.2d we extracted sub-threshold slopes of 75 mV/dec and 100 mV/dec for electron and hole transport sides respectively, at 4 K. The larger SS of holes compared with electrons may be due to the much smaller mobility of holes than electrons.

Now we extend transport measurements for a short channel device with L= 260 nm, and nanowire diameter of 65 nm. Figure 3.3b shows transfer characteristics at various temperatures at a drain bias V_D = 50 mV. The device shows fairly symmetric ambipolar transport, the hole and electron side currents are of almost equal magnitude in contrast to the 1 um long device. Both electron and hole currents are more than a factor of two higher than the first device under the same applied bias, likely due to reduced scattering in the nanowire channel. We obtained a normalized hole current of 12 μA/um at V_D = 50 mV. To our knowledge, the hole current from this device is the highest value which has been reported so far for InSb NWFETs.

We also observed increased excess off currents at higher temperatures compared with the long channel device. We will discuss this in more detail in subsection 3.3.3.

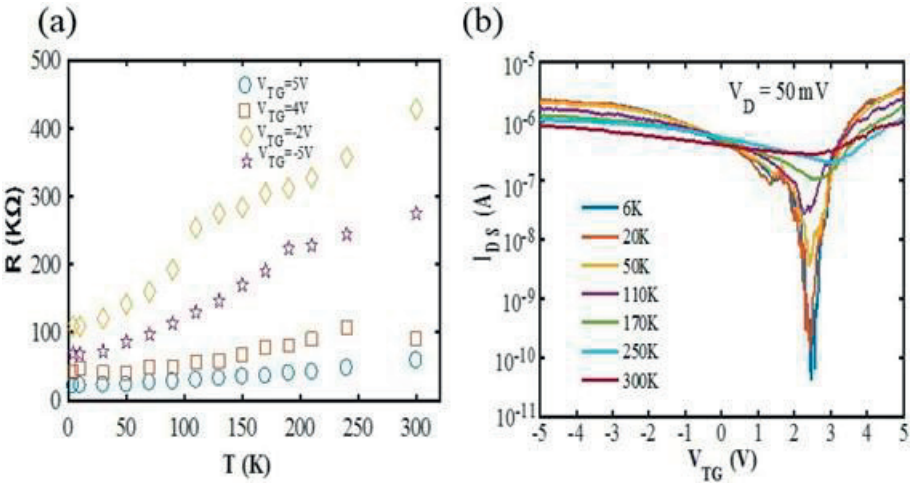


Figure 3.3: (a) Temperature dependence of the on-state resistances at different top gate voltage for regions II and III in fig. 3.2c. (b) Temperature dependent transfer characteristics for the short channel device, with channel length L= 260 nm.

3.3.2 Extracting the bandgap energy

The bandgap of the material can be extracted by using data from temperature dependent measurements. In this section, we describe the extraction of the bandgap energy by using two methods.

The first method is extracting the activation energy, using the Arrhenius plots converted from T-dependent transfer curves in Figure 3.2c. Transport in region I is dominated by thermally excited electrons through the bandgap of the material. The thermal emission current, for $V_{SD} \gg \frac{K_B T}{e}$, is given by:

$$I_{DS} = AA^{*}T^{2} \exp\left(\frac{-e\Phi_B}{K_B T}\right). \tag{3.11}$$

where A is the effective contact area and A^{*} is the Richardson constant [72]. Based on the equation (3.11), Arrhenius plots are presented in figure 3.4a for different top gate voltages in high temperature ranges. Figure 3.4b shows activation energy Φ_B, which are extracted from the slope of the Arrhenius plots in figure 3.4a, as a function of V_{TG} at fixed V_D = 100 mV and 200 mV. The maximum activation energy shown

by the blue star in figure 3.4b corresponds to half of the bandgap. At this value of gate voltage V_{TG} = 2.2 V, the Fermi level in the nanowire resides in the middle of the bandgap and the I_D current has a minimum value, called the I_{OFF} current. From that, the obtained bandgap energy is $E_g = 2\Phi_{B,MAX}$ = 190 meV. Further increasing gate voltage V_{TG} to more positive (negative) shifts the Fermi level towards the conduction (valence) band and the activation energy decreases. Eventually, the activation energy Φ_B gets zero as the Fermi level in the wire enters the top of the valence band or bottom of the conduction band. Deeper in the conduction and valence bands, we obtain negative activation energies which is due to the fact that thermionic emission does not apply in this regime. The band diagrams and Fermi level locations in the nanowire corresponding to regions I, II, III are given in figure 3.2e.

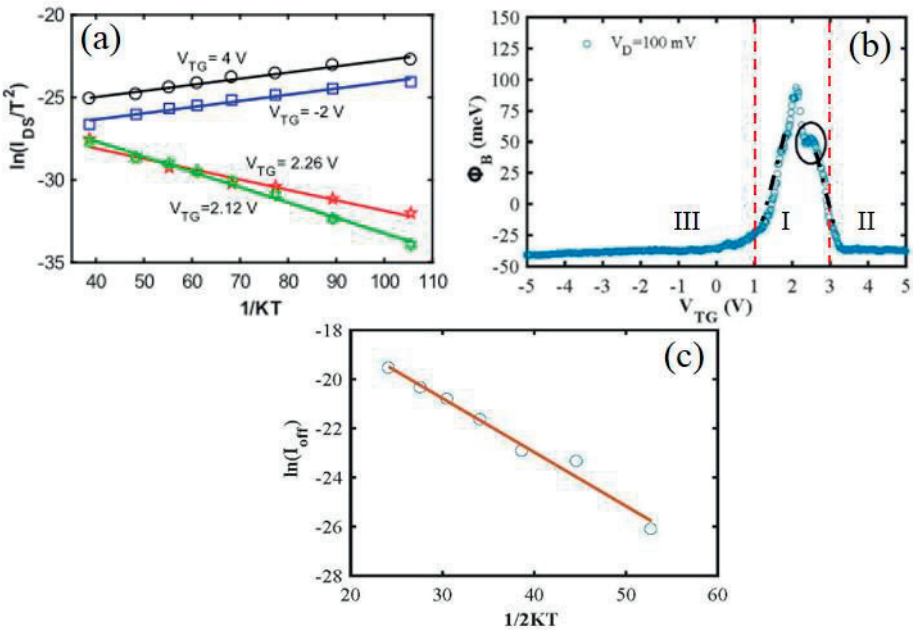


Figure 3.4: (a) Arrhenius plots converted from figure 3.2c for various gate voltages at V_D = 100 mV. (b) Activation energy Φ_B as a function of top gate voltage V_{TG}. (c) Off state current given in natural logarithm scales as a function of temperatures.

We estimated the gate conversion factor α from the slope of the activation energy (shown by the black dashed lines) as 0.13 and 0.097 for holes and electrons, respectively. A shoulder on the electron side of the activation energy peak, which is indicated by a black circle, can be seen in figure 3.4b. A similar behaviour was observed in ref. [73] and explained by charge trap states located within the band

gap. The origin of the charge trap states in the bandgap could be due to imperfect nanowire- oxide interfaces as studied in ref. [74].

The second method we used for extracting the bandgap energy is based on the relationship between the off current I_{OFF} and the bandgap of the material E_g. For ambipolar transport the current I_D has the minimum values when the Fermi level in the material is located in the middle of the bandgap, and the current I_{OFF} is given by [75]:

$$I_{off} \sim e^{-\frac{E_g}{2KT}} \tag{3.12}$$

The equation (3.12) can be related to the relationship between the intrinsic conductivity and the bandgap energy. The figure 3.4c depicts the off current I_{OFF} as a function of temperature in a semi-logarithmic scale at V_D = 10 mV. The linear fit (red solid line) to the data yields a bandgap energy of E_g = 220 meV. The extracted 220 meV bandgap energy is slightly higher than the bulk value of 170 -180 meV due to the quantum confinement effect. The smaller bandgap energy extracted from the first method can be explained with enhanced band to band tunnelling due to applied large bias to the drain.

3.3.3 Dependence of I_{OFF} on channel lengths and temperature

When $L_g < 4.6\lambda$ where λ is the characteristic length of the transistor, and L_g is the gate length, the well-known short channel effect takes place resulting in an undesired increase in the off state current. This becomes even more of issues for a transistor made of narrow bandgap materials. Contributions of band to band tunnelling and thermally excited carriers through the bandgap of materials at higher temperatures give higher off state currents for a FET, even if it has a much longer channel length than the characteristic length of the device.

The dependence of the off current I_{OFF} on temperature is given with the log scale plot in figure 3.5 for devices with channel lengths of L= 1000 nm and 260 nm. For both devices, I_{OFF} shows an exponential increase as the temperature increases. However, the device with the channel length 1 um has a factor of one thousand smaller I_{OFF} than the device with channel length 260 nm at the same temperatures. For a top gate or all-around gate geometry the characterization length λ is given by:

$$\lambda = \sqrt{\frac{2\varepsilon_{InSb} d_{wire}^2 ln\left(1+\frac{2t_{ox}}{d_{wire}}\right)+\varepsilon_{ox} d_{wire}^2}{16\varepsilon_{ox}}}, \tag{3.13}$$

where ε_{InSb}= 16.8, is the dielectric constant of InSb, ε_{ox} = 16, is the dielectric constant of HfO_2, t_{ox} is the thickness of the gate oxide and d_{wire} is the nanowire diameter. A characteristic length of λ = 16.3 nm is obtained, which is much smaller than the channel length of the short channel device. Therefore, the excess off current of the short channel device may not be due to short channel effects. There must be other mechanisms contributing to the excess off current.

The origin of excess off currents for short channel FET have been widely studied [76-79], and it has been found that the excess off current contains two components, diffusive current and band to band tunneling current (BTBT). The diffusive current depends on the gate voltage and when the gate voltage fully depletes the channel, its contribution to the off current becomes negligible [80]. Since gate fully covered the channel in our device, we could neglect the contribution of the diffusive current to the off current.

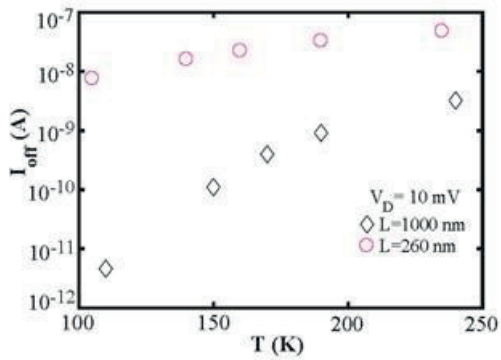


Figure 3.5: Temperature dependence of current I_{Off} for the two devices with channel lengths of L= 1µm and 260 nm.

Applied voltages to the gate and drain induce drain gate electric fields, which leads to energy bending near the drain end of the channel. Due to the small bandgap of InSb, electrons from the valence band tunnel in to the conduction band, in results band to band tunneling currents contribute to the off current. It is also found that the stronger the gate response, the larger the BTBT current is due to a larger band bending near the drain [80]. For long channel devices, the gate drain voltages drop across a longer distance and make the gate drain electric field weaker. As a consequence, the BTBT current decreases leading to smaller off currents. However, the BTBT current can be reduced for a short channel device by employing a partially covered gate design, as studied in ref. [80].

3.3.4 Electron and hole field effect mobility

For the fields of high speed and ballistic devices, it is of fundamental importance to use materials which possess high carrier mobility. Using InSb nanowires for Majorana devices and quantum devices are not beyond the requirements of high carrier mobility. Bulk InSb has the highest electron mobility of 77000 cm^2/Vs. However, for InSb nanowires a much lower electron mobility than the bulk value has been reported. Previous studies have proposed several reasons which may contribute to the reduced mobility [41]. There is still a lack of comprehensive studies of carrier mobility, particularly its T-dependence, for InSb nanowires grown by CVD. In this subsection, electron and hole field effect mobilities are determined from the long channel device of L = 1μm and their dependence on temperature is explored.

According to the Drude model, the carrier mobility is defined as the proportionality factor between an applied electric field E and the drift velocity of the carriers, v_d

$$v_d = \mu E. \tag{3.14}$$

Mobility also can be described by the scattering time τ, as follows:

$$\mu = \frac{e\tau}{m^*} \tag{3.15}$$

where m^* is the electron effective mass, and e is the electron charge. Mechanisms such as impurity scattering, phonon scattering and surface roughness scattering effect the mobility. According to the Mathiessen rule [81], the net mobility μ can be determined as:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots, \tag{3.16}$$

and the mechanism with the lowest mobility contribution determines the net mobility.

The mobility can be extracted from transport measurements with MOSFETs. In this method, classical, diffusive transport is assumed. This implies that $L \gg l_e, l_\varphi$, where, L is the channel length, l_e is the mean free path and l_φ is the phase coherence length. The mobility depends on both transverse and longitudinal electric fields in the nanowire, as well as, both applied gate and drain bias. At a low source-drain bias V_D, the drift velocity v_d increases linearly with applied gate voltage V_g, so the mobility is assumed to be constant and can be obtained from the linear regime of the I-V characteristics. The conductance G, of a FET in the linear regime is given by [76]:

$$G(V_g) = \frac{\mu C}{L^2}(V_g - V_{th}), \tag{3.17}$$

C is gate capacitance, L is channel length of the FET, V_{th} is the threshold voltage. The field effect mobility can be obtained using equation (3.17) via the transconductance:

$$g_m = \frac{dG}{dV_g}. \tag{3.18}$$

This equation neglects the effect of the gate voltage on the mobility and assumes mobility to be constant, and is often evaluated from the peak transconductance. This method may underestimate the mobility since it does not consider the enhanced surface roughness scattering with increased gate voltage.

It is worth pointing out that, in order to extract the field effect mobility more accurately, several issues should be taken into account for an InSb nanowire FET. Unlike InAs nanowires, InSb nanowires lack a surface accumulation layer, which gives an interface resistance of a few kΩs at the nanowire and the metal contacts [41]. This interface resistance from the contacts reduce the trans-conductance peak, leading to an underestimation of the intrinsic mobility [62]. Because of a longer phase coherence lengths from $l_\varphi \sim 500\,\text{nm}$ up to 1μm in InSb nanowires [62], reproducible fluctuations of the conductance in the gate trace at low temperatures makes the extraction of the field effect mobility complicated for using the transconductance method.

Therefore, we extract the field effect mobility for electrons and holes following the method described in reference [41]. The field effect mobility is determined by a data fit to the measured conductance G using the following equation:

$$G(V_g) = \left(R_C + \frac{L^2}{\mu C(V_g - V_{th})}\right)^{-1}, \tag{3.19}$$

where G is the conductance, R_C is the contact resistances, L the channel length, V_{th} the threshold voltage and C the gate capacitance. The parameters R_C, μ and V_{th} are fitting parameters, while we estimate the capacitance C from a cylindrical gate capacitor model given by:

$$C = \frac{2\pi\varepsilon\varepsilon_0 L}{ln\left(\frac{h}{r}\right)}, \tag{3.20}$$

ε_0 is the vacuum dielectric constant, ε is the relative dielectric constant of HfO_2, r is the radius of the nanowire and h is the distance from the center of

the nanowire to the gate electrode. That gives the gate capacitance value of C = 2.64 fF.

A data-fit to the measured electron conductance is shown in figure 3.6a. The black dashed curve is the measured conductance and the solid red line is the data-fit obtained by using equation (3.19). The numerical fitting yields μ=1158±42 cm^2/V.s, V_{th} = 2.94 V and R_C = 2075 Ω at T= 4K for electrons. The extracted mobility at different temperatures for electrons and holes are presented in figure 3.6b and 3.6c. We observe that the electron mobility increases from the room temperature value of μ_e = 309 cm^2/Vs to 1158 cm^2/Vs at low temperatures. The corresponding increase for holes is from μ_h = 20 cm^2/V.s to 100 cm^2/V.s. The increase of hole and electron mobilities with decreasing temperatures is due to the suppression of phonon scattering. However, both electron and hole mobilities are much lower than their bulk values and could be explained by the following reasons:

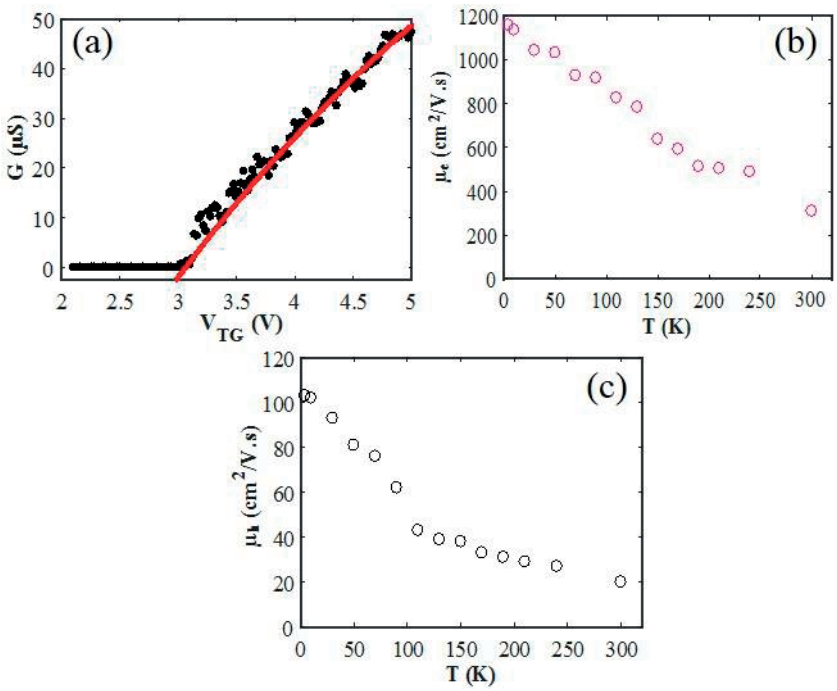


Figure 3.6: (a) Conductance G as a function of top gate voltage V_{TG}, at V_D= 10 mV, (black dashed line) for electron transport side. Electron Field-effect mobility is extracted from a fit (red solid line) to the measured conductance using equation (3.19). (b) Temperature dependence of the electron field-effect mobility μ_e extracted from data-fits for various temperatures. (c) Temperature dependence of hole field-effect mobility μ_h extracted from data-fits for various temperatures.

First, we did not consider the reduction of the classical capacitance by quantum confinement in the nanowire [41]. Therefore, we have overestimated the top gate capacitance; secondly, enhanced surface state scattering originating from the confinement typically reduces the mobility significantly [62]. Finally, charge traps induced by imperfections of the oxide semiconductor interface can also reduce the mobility [62].

An average field effect mobility of 25000 $cm^2/V.s$ for electrons has been reported for InSb nanowires with diameters of 100 nm grown by MOVPE [41]. Note that, the InSb NWs investigated in this thesis has smaller diameters of $\leq$ 60 nm. A reduction of the mobility with decreasing diameter has been reported [83]. Despite the factors mentioned above which limit the mobility, obtaining a higher field effect mobility of electrons and holes can be expected from the InSb nanowires investigated in this work. This can be achieved by improving the quality of the interface between nanowire and the gate oxide, and evacuating the sample in a higher vacuum during the measurement as investigated in ref. [41].

3.4 Conclusions and outlook

Top gate field effect transistors are fabricated with CVD grown InSb nanowires to investigate the electrical transport properties of the nanowires. Measurements are performed in various temperature ranges for the devices with channel lengths of 1μm and 260 nm. We observed ambipolar transport behaviour which exists in all temperature ranges up to room temperature. We extracted a bandgap energy of 220 meV from the temperature dependence measurements. We observed increased hole currents as the channel lengths decreased. Off state current shows strong dependence on temperature and channel lengths. At higher temperatures, the off current is increased because of thermal excitations of carriers through the bandgap. The off current also increases with decreasing channel lengths, with contributions from BTBT due to gate-drain induced electric fields. Finally, we extracted electron and hole field effect mobilities and investigated their temperature dependence. The phonon scattering was found to be the limiting factor for mobility at higher temperatures. Higher mobility can be expected by further improving device performance, such as reducing charge traps at the oxide-nanowire interface, evacuating samples in vacuum prior to measurements.

For future work, making the tunnelling field effect (TFETs) transistors with InSb nanowires is attractive to further study transport properties. The current level may be enhanced for InSb TFETs due to its low effective mass [57]. Appearance of ambipolar transport in the nanowires is interesting to use them for multifunctional

devices and logic gates to realize CMOS and multifunctional nanocircuits in the same nanowire.

Chapter 4
Quantum interference and spin relaxation in InSb nanowires

4.1 Introduction

For semiconductor nanowires, exhibiting a strong spin-orbit interaction can be the most important requirement to their applications in spintronics [84-86], spin-based quantum computations [87, 88] and for realization of Majorana fermions [89, 90]. A standard method to determine spin-orbit interaction relies on low-field magneto conductance measurements. Due to the quantum nature of electrons, they experience coherent back scattering during their travel in the nanowires. This results in making a closed loop path that leads to a reduction in the conductance lower than its classical value. This quantum interference effect is called weak localization [91, 92]. In the presence of the spin-orbit interaction, the spin of the electrons rotate during their back scattering and give rise to an increase in conductance, and this is called weak anti-localization [93, 94]. These quantum interference effects can be averaged out under applied low magnetic fields that allow us to extract the spin-orbit interaction lengths. In this chapter, the spin-orbit strengths of InSb nanowire, grown by chemical vapor deposition are studied. Characteristic lengths such as spin-orbit coupling length, phase coherence length and spin precession length are extracted from low field magnetoconductance measurements. This chapter begins with introducing theories related to experimental observation followed by discussions about main experimental findings.

4.2 Spin-orbit interaction

When a charged particle is moving through an electric field, it ‘feels’ an effective magnetic field acting with its spin. The magnetic field is generated by the Lorentz transformation of the electric field and interacts with the magnetic momentum of the charged particle, giving rise to the spin-orbit interaction (SOI). This relativistic effect for a charge moving in an atomic potential V, is given by:

$$H_{SO} = -\frac{\hbar^2}{4m_0^2c^2}\vec{\sigma}.\vec{p} \times \nabla V_0 \quad (4.1)$$

where $m_0$is the free electron mass, σ is the Pauli spin matrix, p is the momentum operator and V_0 is the Coulomb potential of the atomic core [95]. Therefore, the heaver the element is the stronger the SOI is. The equation (4.1) is known as Pauli spin-orbit interaction. In semiconductors, V_0 can be replaced with periodic potentials created by the ion-core, the deviation of the periodic potential due to defects or phonons, potentials from quantum confinements or external electric fields.

With the presence of both time-reversal and space-inversion symmetry in semiconductors, the electron spectrum satisfies the spin degeneracy of electron states. The space inversion symmetry ensures E_+ (K) = E_+ (-K), while the time-reversal symmetry inverts both the propagation direction and spin, giving rise to Kramer's degeneracy E_+ (K) = E_- (-K), here the index $\pm$ refer to the spin state for a given quantization axis. The combined effect of the above two symmetries keep the spin degeneracy of single-particle energies, E_+ (K) = E_- (K). However, in semiconductors, when an electron moves through the crystal lattice, it interacts with the electric fields from the charged atoms in the lattice, or the internal magnetic field B_0, giving raise to spin-orbit interaction. This SOI breaks the space-inversion symmetry leading to a splitting of the spin states without any external magnetic fields, therefore E_+ (K)≠ E_- (K). In that case, the spin degeneracy of the same k spaces are broken, whereas the time-reversal symmetry is remained. Hence, the absence of the space-inversion symmetry is a prerequisite for the emergence of spin-orbit coupling in semiconductors. For semiconductors, several types of space inversion asymmetry have been reported, for example, interface inversion asymmetry related to the chemical bonding within interfaces [96, 97], and strain induced inversion asymmetry [98]. However, the following two SOI are the most commonly referred to for semiconductors. The first one is called the Dresselhaus SOI caused by internal electric fields in semiconductors. In fact, it originates from a non-centro-symmetric lattice and occurs in some types of crystal structures like zincblende and wurtzite, therefore it is also known as bulk inversion asymmetry [99]. For the s-type conduction band of a bulk semiconductor, the Hamiltonian of the Dresselhaus SOI is described by [99]:

$$H_D^{3D} = \beta\left(p_x\left(p_y^2 - p_z^2\right)\sigma_x + p_y(p_z^2 - p_x^2)\sigma_y + p_z\left(p_x^2 - p_y^2\right)\sigma_z\right) \quad (4.2)$$

where β is the Dresselhaus coupling constant, *x*, *y*, and *z* indicate the main crystallographic directions [100], [010], [001]. The InSb we investigated in this thesis is grown in the [111] growth direction, hence, the Dresselhaus SOI is not expected to be present as reported in ref. [95]. However, experimental work with

InSb nanowire double quantum dots carried out by Nadj-Perge et al. reveals that there is another type of SOI presented in InSb NWs which is known as the Rashba spin-orbit interaction [100]. The Rashba SOI occurs in semiconductors due to the asymmetry from external electric fields, quantum confinement or built-in potentials [101, 102]. The Rashba SOI is of particular interest since it can be tuned by the electric field E with external gate voltages. Assuming a defined two dimensional system where a confinement potential varies in the z direction, we can write the Rashba SOI as [102]:

$$H_R^{2D} = \alpha\left(-p_y\sigma_x + p_x\sigma_y\right), \tag{4.3}$$

with α is the Rashba coupling constant which is proportional to the expectation value of the electric field in the z direction, $< E_z >$. For quasi one dimensional system, as example for a nanowire as sketched in figure 4.1a, the Rashba SOI reduces to:

$$H_R^{1D} = \alpha\left(p_x\sigma_y\right). \tag{4.4}$$

Now consider a spin degenerate one-dimensional (1D) sub-band without SOI and magnetic field, as shown in figure 4.1 (b). With the presence of SOI, the sinful subband shift laterally in wavevector resulted in lifting of the spin degeneracy. It can be understood mathematically in the following way: for B = 0, then the Hamiltonian for 1D nanowire including Rashba SOI can be written by [83]:

$$H = \frac{p_x^2}{2m^*} - i\hbar\alpha\sigma_y\frac{\partial}{\partial x}, \tag{4.5}$$

Solutions from the Schrodinger equation for (4.5) yields the eigenenergies:

$$E_\pm = \frac{\hbar^2 k_x^2}{2m} \pm \alpha k_x \tag{4.6}$$

The dispersion consists of two branches that are non-degenerate for $k_x > 0$, as seen in figure 4.1c.

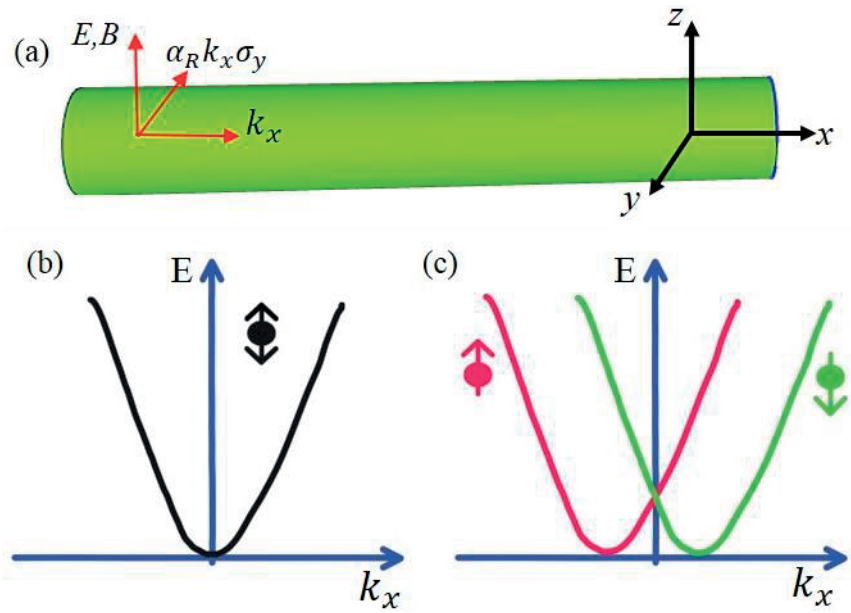


Figure 4.1: (a) Orientation of the nanowire and direction of relevant fields. The nanowire axis is in the *x* direction, spin-orbit field is in *y* direction and an external electric field and magnetic field are in *z* direction. (b) A spin degenerate sub-band absence of SOI. (c) The sub-band shift in k_x due to SOI.

4.3 Spin precession

Now we will discuss the influence of SOI on spins of electrons which travel along the *x*- direction in a 1-D system. In fact, SOI causes a polarization of electrons in *+y* and *–y* with the same energy but different wave vectors k_1 and k_2 while the electrons propagate in the *x* direction. Based on the equation (4.6), the energy of polarized electrons can be described explicitly by:

$$E_{+y} = \frac{\hbar^2 k_1^2}{2m^*} - \alpha k_1 \tag{4.7}$$

$$E_{-y} = \frac{\hbar^2 k_2^2}{2m^*} + \alpha k_2 \tag{4.8}$$

According to the equation (4.7) and (4.8), the energy of polarized electrons is raised by αk_2 or lowered by $-\alpha k_1$ with respect to the polarization direction, $\pm y$. From equations (4.7) and (4.8), a differential phase shift that is introduced between polarized electrons in $\pm y$ can be determined as [104]:

$$\Delta\theta = (k_1 - k_2)L = \frac{2m^*\alpha L}{\hbar^2} \tag{4.9}$$

where α is the Rashba coupling constant, m^* is the effective electron mass, L is the channel length. The equation (4.9) implies that under the influence of a momentum dependent magnetic field $\overrightarrow{B_{so}}(k)$ introduced by SOI, the spins of the electrons exhibit a precession with an angle $\Delta\theta$ during their travel in the x direction. This is depicted schematically in figure 4.2 for a ballistic device. The spin orbit magnetic field $\overrightarrow{B_{so}}(k)$ is given by [62]:

$$\overrightarrow{B_{so}}(k) = \frac{2\alpha}{\hbar}\left(\vec{k} \times \vec{y}\right) \tag{4.10}$$

The length l_R corresponds to the full rotation of spins with $\theta = 2\pi$ is called spin precession length and can be described by:

$$l_R = \frac{\pi\hbar^2}{m\alpha} \tag{4.11}$$

From the equation (4.11), it is noticeable that, the spin precession length l_R depends on the spin orbit coupling constant α. The stronger SOI is, the l_R is shorter for that material.

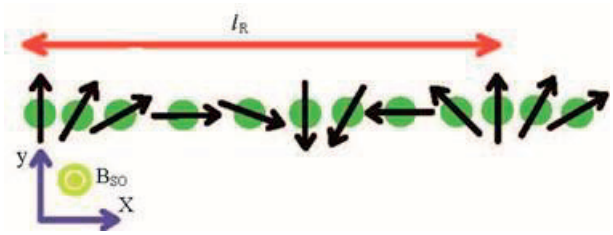


Figure 4.2: In ballistic regime the electron spin makes a full precession over a distance of l_R due to the Rashba SOI. B_{so} is assumed to be out of plane due to an electric field $\vec{E}$.

4.4 Spin relaxation

Spin relaxation is the decay of spin polarization parallel to an external field due to its interaction with its environment [98]. Generally, spin relaxation can be understood as a result of a fluctuating 'effective magnetic field' acting on the spins. The origins of the 'effective' magnetic fields can be SOI, exchange interactions or other spin effects [105]. Spin makes precessions with a frequency $\omega = \Delta/\hbar$ around the direction of the effective magnetic field for a typical time $\tau_c$until the direction and absolute value of the effective field change randomly. After the time τ_c, the spin

starts its precession around the new direction of the field. After repeating a number of such events, finally, the spin will lose its memory of initial spin direction. Depending on the value of spin precession angle two distinguished cases can be considered. If $\omega\tau_c \ll 1$, spin rotates slowly and the spin precession angle is small between subsequent scattering events. During the time *t*, the number of random steps is $N = t/\tau_c$ and consequently the uncorrelated steps in the precession angle can be determined by the spread of phase given by the standard deviation $\phi = \delta\phi\sqrt{N}$. The spin relaxation time can be defined as the time with the standard deviation becomes $\phi \approx 1$ [105], which can be described by:

$$\frac{1}{\tau_s} \sim \omega^2 \tau_c \tag{4.12}$$

It is worth pointing out that for this case $\tau_s \gg \tau_c$. If $\omega\tau_c \gg 1$, the spin makes many rotations around the direction of the magnetic field during the time τ_c. As a consequence, the spin projection transverse to the random magnetic field is completely destroyed, while its projection along the magnetic field is conserved during the time $1/\omega$. As a result, the spin projection will be reduced three times with respect to its initial value. The magnetic field changes its direction after the time τ_c leading to the disappearance of the initial spin polarization. Hence, the overall relaxation time is $\tau_s \sim \tau_c$. This two considerations can be applied to any spin relaxation mechanism.

Several mechanisms have been studied which relate to spin relaxation in semiconductors, for instance, the Bir-Aronov-Pikus mechanism [106,107], the Elliott-Yafet mechanism [108,109], g-tensor inhomogeneity mechanism [110,111] and the D'yakonov-Perel' mechanism [112,113]. For semiconductor quantum dot systems, the hyperfine interaction [114], and in magnetically doped semiconductors, the exchange interaction with magnetic impurities [98] play important roles in the spin relaxation. Narrow band gap semiconductor nanostructures like InSb and InAs among the other mechanisms, the Elliot-Yafet mechanism and D'yakonov-Perel' mechanism are most relevant [98]. The Elliott-Yafet (EY) mechanism is caused by scattering originating from lattice vibrations, charged impurities and boundaries. For phonons, the correlation time τ_c is comparable to the inverse frequency of a thermal phonon, as a result, the spin relaxation caused by phonons is weak at low temperatures. In the case of scattering by impurities, the direction of the random magnetic field is determined by the geometry of the individual collisions. Therefore, a random magnetic field exists only during the brief act of a collision and disappears between the collisions, hence the magnetic field cannot be characterized by a single correlation time. At each scattering, the electron spin rotates by a small angle, ϕ. The relaxation rate is $\frac{1}{\tau_s} \sim \frac{\langle(\phi)^2\rangle}{\tau_p}$ where τ_p the time between collisions [105]. Therefore, the relaxation rate caused by the EY mechanism is proportional to the

impurity concentration. A schematic of the EY mechanism is given in figure 4.3a. The EY mechanism can appear in both elemental semiconductor like Si and compound semiconductors such as GaAs irrespective of the existence of a centre of inversion symmetry or not [115]. The EY also appears in narrow band gap compound semiconductors which have strong spin-orbit interaction [115].

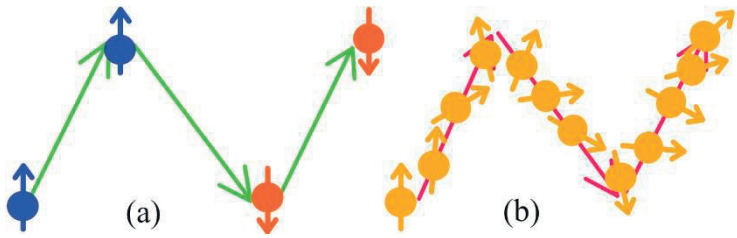


Figure 4.3: Spin relaxation mechanisms in semiconductors. (a) Elliott-Yafet mechanism, (b) D'yakonov-Perel' mechanism.

For compound III-V semiconductors the Dyakonov-Perel (DP) mechanism dominates the spin relaxation due to an absence of space inversion symmetry in these material systems. The SOI plays a significant role for the DP mechanism to occur. We will consider ballistic 2DEG plane to explain the DP mechanism. An internal effective magnetic field which depends on momentum is introduced by SOI. The spins of moving electrons rotate under the influence of the effective magnetic field until scattering, then the precession starts again after the scattering. However, the effective magnetic field changes with time since the direction of the momentum varies because of the scattering. That random change in the effective magnetic field leads to randomized spin orientations. A schematic illustration of the DP mechanism is given in figure 4.3b. For a small spin precession angle $\Omega\tau_e \leq 1$, the spin relaxation time τ_s for the spin direction has changed by an angle 2π is given by [98]

$$\frac{1}{\tau_s^{2D}} = \Omega^2\tau_e = \left(\frac{l_e}{l_R}\right)^2 \frac{1}{\tau_e}, \tag{4.13}$$

where l_R is the spin precession length, τ_e the scattering time, Ω is the spin precession frequency, l_e is the mean free path. In contrast to EY, the spin rotates between the collisions not during the collisions, and the relaxation rate is inversely proportional to the impurity concentration.

Our preceding discussions based on spin relaxation in 2D materials. For a 1D system, the spin relaxation differs from its counterpart 2D system. A 1D system enhances backscattering which challenges the spin precession in the forward direction leading an increase in the spin relaxation time. According to Kiselev [116], the spin relaxation lengths show a dependence on channel width w, as the channel width becomes smaller than the spin precession length l_R, $w < l_R$ longer spin

relaxation time is found $\tau_s \sim \tau_s^{2D}\left(\frac{l_R}{w}\right)^2$ with conditions of $l_R > l_e > w$. An another analytical study carried out by Kettemann, et al. [117] with channels made out of quantum wells found similar results that the spin relaxation time increases with decreasing channel widths w. For diffusive transport with the limitation of $w \ll l_R$, they found the spin relaxation time τ_s of:

$$\tau_s = 12\left(\frac{l_R}{w}\right)^2 \tau_s^{2D} \tag{4.14}$$

The above studies indicate that the spin relaxation increases in reduced dimensions or confined geometries. Although, the above expression were derived from channels defined in quantum wells, it can also be applied to nanowires. Increased spin relaxations have been experimentally found in InAs nanowires [118].

4.5 Quantum transport in narrow channels

4.5.1 Quantum ballistic transport

Ballistic transport was first proposed and subsequently realized by Sharvin [119] where a beam of electrons in a metal was injected and detected by point contacts which have much smaller widths than the mean free path. Based on the work in ref. [120], we will drive the conductance in the ballistic regime through a narrow channel with the size of L, connected to reservoirs. The motion of electrons is restricted in the transverse direction *y*, while electrons can propagate freely along the channel in the *x* direction. Therefore, the wave function can be written as:

$$\psi_n(k_x) = \xi_n(y,z)\frac{1}{\sqrt{L}}e^{ik_x x}. \tag{4.15}$$

In the case of a parabolic potential in the nanowire, solving the Schrodinger equation yields an energy spectrum of:

$$E_n(k_x) = (n-\frac{1}{2})\hbar\omega_0 + \frac{\hbar^2 k_x^2}{2m^*}, \tag{4.16}$$

Due to the quantization in the y direction, electrons are distributed in sub-bands *n* and travel in the *x* direction. The group velocity of electrons in each subband can be determined by: $\vartheta_n = \frac{\left(\frac{dE_n}{dk_x}\right)}{\hbar}$.When there is voltage bias difference between the

reservoirs $V_{sd} = {(\mu_s - \mu_d)}/{e}$, a current flows and for zero temperature, the net current I is given by:

$$I = e\sum_{n=1}^{N}\int_{\mu_d}^{\mu_s} dE\,\frac{1}{2}\rho_n(E).\vartheta_n(E).T_n(E), \tag{4.17}$$

where $\rho_n\,(E) = {2}/{\pi(dE_n/dk_x)^{-1}}$ is the 1D spin degenerate density of states, N is the number of channels and $T_n(E)$ is the transmission probability of each sub-band. It is obvious that the density of states and velocity cancels each other out and that the current I only depends on the $T_n(E)$ and bias V_{sd} as shown by:

$$I = \frac{2e^2}{h}\sum_{n=1}^{N} T_n(E)\,V_{sd}. \tag{4.18}$$

Hence the conductance $G = \frac{I}{V_{sd}}$ is quantized:

$$G = \frac{2e^2}{h}\sum_{n=1}^{N} T_n(E). \tag{4.19}$$

This leads to a step like increase of the conductance with chemical potentials, as presented in figure 4.4a. According to the equation (4.19), in the ballistic transport regime, the current is limited by the scattering of electrons at the sample boundary. At a finite temperature, the electrons have a Fermi-Dirac distribution which leads to a smearing out of the conductance.

In the presence of a magnetic field and SOI the quantization plateaus experience qualitative modifications due to significant changes in the band structures [103]. Following ref. [103], we will describe how band structures change with the influence of magnetic field, SOI and helical spin states modify the quantization conductance plateaus. For non-zero magnetic fields and electrical potentials in a nanowire, the Hamiltonian of a 1D nanowire given in equation (4.5) is extended to:

$$H = \frac{p_x^2}{2m^*} + eV(y) - i\hbar\alpha\sigma_y\frac{\partial}{\partial x} + \frac{g^*\mu_B}{2}\vec{\sigma}.\vec{B}. \tag{4.20}$$

$eV(y)$ is the electron confining potential in the *y* direction, μ_B is the Bohr magneton. The total magnetic field is assumed to be in plane $\vec{B} = B_x\hat{x} + B_y\hat{y}$. The Schrödinger equation inside the constriction can be written the forms of:

$$\psi = e^{ikx}\phi(y)\begin{pmatrix}\varphi_\uparrow\\ \varphi_\downarrow\end{pmatrix}, \tag{4.21}$$

with $\phi(y)$ the wave function due to the confinement potential, $\varphi_{\uparrow,\downarrow}$ denote the spinor components for spin up and spin down, respectively. The energy of the lowest two subbands can be determined as:

$$E_{\pm} = \frac{\hbar^2 k_x^2}{2m^*} \pm \sqrt{\left(\frac{g^*\mu_B B}{2}\right)^2 + \alpha k_x g^* \mu_B B sin\theta + (\alpha k_x)^2}, \tag{4.22}$$

where θ is the angle between external magnetic field and the k_x, g^* is the effective g-factor, and μ_B is the Bohr magneton, $\pm$ denotes the upper and lower subband.

In the absence of a magnetic field, the spinful sub-bands are shifted laterally due to the SOI as already shown in figure 4.2c. However, the conductance is still equal to $G = \frac{2e^2}{h}$, which is just the same as for the case of no spin orbit coupling. This is because the edges of the spinfull sub-bands are still degenerate. Now we will consider the effect of external magnetic fields for two cases depending on the direction of the B fields.

At a finite external magnetic field oriented perpendicular to the spin-orbit field B_{SO} and pointed along the nanowire (as shown in figure 4.1), θ = 0, the equation (4.22) can be reduced to:

$$E_{\pm} = \frac{\hbar^2 k_x^2}{2m^*} \pm \sqrt{\left(\frac{g^*\mu_B B}{2}\right)^2 + (\alpha k_x)^2}, \tag{4.23}$$

As is shown in figure 4.4b, the magnetic field causes an anti-crossing at $k_x = 0$. The size of the gap is determined by the Zeeman energy, $E_{zeeman} = g^*\mu_B B$. When the chemical potential is within this gap a conductance dip from $\frac{2e^2}{h}$ to $\frac{e^2}{h}$ appears. The conductance goes back to $\frac{2e^2}{h}$ as the chemical potential reaches the bottom of the next higher sub-band. This modification of the conductance can be understood as a consequence of helical states. The conductance of the helical state is given by [103]:

$$G = \frac{e^2}{h} \sum_{n,s} \sum_{n=1}^{N} \beta_i^{n,s} T_n(E), \tag{4.24}$$

where β_i is either +1 for a minimum or -1 for a maximum. The sum includes the extremal points of all the sub-bands. Therefore, the maximum points in a sub-band will reduce the conductance.

When the external magnetic field is parallel with the spin orbit field $\theta = \frac{\pi}{2}$, the equation (4.22) can be written as:

$$E_{\pm} = \frac{\hbar^2 k_x^2}{2m^*} \pm \left(\alpha k_x + \frac{g^* \mu_B B}{2}\right), \tag{4.25}$$

obviously, the square root in equation (4.23) is missing. Actually, the square root term determines whether the anti-crossing appears or not. The square term is always positive at a finite magnetic field, which leads to the existence of an anti-crossing energy gap. For the equation (4.25) the term inside the bracket can always reach zero at a finite field (with different k_x) resulting in no opening gap as shown in figure 4.4c. The conductance is identical to the case of no SOI and increases with steps of $\frac{e^2}{h}$.

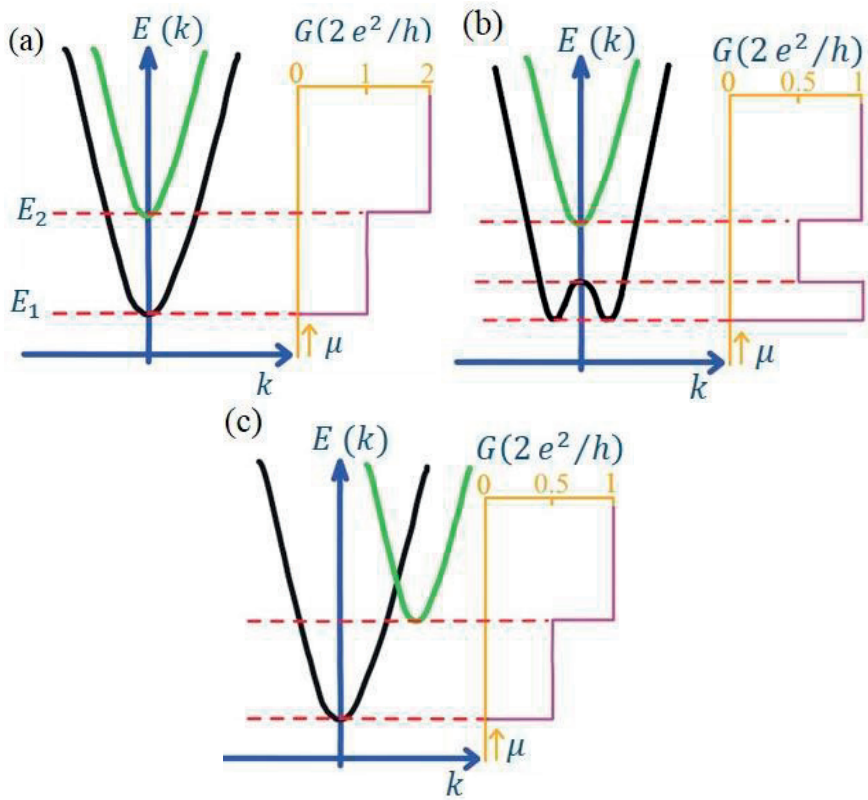


Figure 4.4: Energy spectra E (K) and conductance G as a function of chemical potential μ in a narrow channel. (a) $E_{SO} = E_{zeeman} = 0$. (b) $E_{SO} = E_{zeeman} \neq 0$, external magnetic filed is pointed along the wire θ=0^0, perpendicular to spin-orbit field. (c) $\theta = 90^0$, external magnetic field is parallel to the spin-orbit field. Note, the figure b and c show spectrum only the bottom of the first sub-band and corresponding conductance.

When B is at an intermediate angle, the equation (4.22) is used and both features of the conductance discussed for figure 4.4b,c can be expected to occur. The helical states in InSb nanowires were observed experimentally by the work in ref. [45].

4.5.2 Quantum diffusive transport

In contrast to ballistic transport, the diffusive transport is characterized by scattering of electrons many times during traversing a system of size L. It implies that for diffusive transport to occur in the system, it is required to meet the condition of $l_e \ll L$, where l_e is mean free path. Introducing of the phase coherence length l_φ separates the diffusive transport into two limited regimes, the classical regime and the quantum regime. These two regimes can be identified by comparing the length scales [121]:

$$Diffusive \begin{cases} classical & \lambda_F, \; l_\varphi, l_e \ll L \\ quantum & \lambda_F, \; l_e \ll L, l_\varphi \end{cases}$$

where λ_F is the Fermi wavelength. We will start with the basics of transport in the limit of the classical regime, then extend it to the quantum regime.

The classical transport is described by the Drude model, which was developed in the beginning of the 20th century. The model considers the electron systems as an ideal gas. The motion of a particle is characterized by scattering events via mutual collisions or local impurities. This is usually described by a scattering time τ, which is the averaged time integral between the scattering events where the particle will lose all its information such as kinetic energy, velocity and direction. According to the Drude model, the conductivity of the sample σ is correlated with τ and described by:

$$\sigma = \frac{e^2 n_e \tau}{m}, \tag{4.26}$$

where n_e is the electron density which is connected to the Fermi wave vector k_F and determined by the dimensionality of the system.

A quantitative approach which describes the conductivity σ in terms of density of states ρ is well known as the Einstein relation for the conductivity and is given by [121]:

$$\sigma = e^2 \rho D, \tag{4.27}$$

where D is the diffusion constant and depends on dimensionality [102]:

$$D_d = \frac{1}{d} v_F l_e = \frac{1}{d} v_F^2 \tau, \tag{4.28}$$

where d denotes the dimension of the system. The phase coherence length l_φ can be determined from D as $l_\varphi = \sqrt{D\tau_\varphi}$, τ_φ is the corresponding phase-coherence time. In fact, the equation (4.28) refers to how scattering effects correlations of the velocity of an individual particle before and after the scattering. According to the Drude model, there is no correlation between the velocities since the particle is assumed to lose all its memory after the scattering. However, if the correlation between the initial and final states of the electrons remain after the scattering, this will effect the value of the diffusion constant, hence the conductance.

At low temperatures and for nanostructures, quantum interference due to the wave nature of electrons leads to velocity-velocity correlations, giving rise to a correction of $\Delta\sigma$ to the classical conductance. In fact, it is the superposition principle of quantum mechanics that gives observable consequences on the macroscopic level. This can be understood by using the Feynman path method. Let us consider an electron moving from a location A to location B, as shown in figure 4.5. This can be described as the transfer of electron waves from A to B by the means of splitting and distribution of the electron wave over a number of partial waves Ψ_j, each of them travelling in the system along different paths p_j, experiencing many elastic scattering events until arriving at B. In order to use the Feynman path to determine the transmission probability, it is implicitly assumed that the electron follows a well-defined path without a too strong scattering on its characteristic length scale, λ_F. Then, the total amplitude Ψ (B) at B will be:

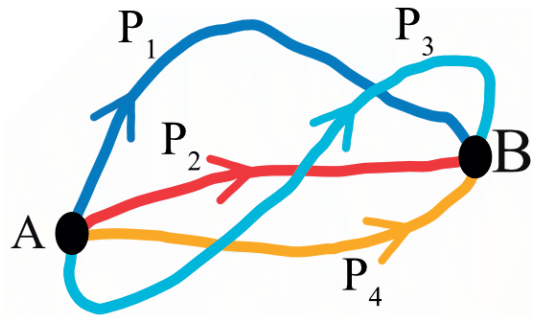


Figure 4.5: Electron waves travelling from its initial position A to final position B with split partial waves travelling along different paths Pi.

$$\Psi\,(\mathrm{B}) = \sum_J \Psi_j = \sum_j t_j e^{i\varphi_j}, \tag{4.29}$$

where φ_j is phases. The total quantum mechanical probability of an electron arriving at B can be obtained by the square of the amplitude Ψ (B) as:

$$P\ (B) = \ |\Psi(B)|^2 = \sum_j t_j^2 + \sum_{j\neq k} t_j t_k \cos(\varphi_j - \varphi_k) \qquad (4.30)$$

In equation (4.30) the first term is classical, while the second terms refers to the interference term which introduces a change to the classical probability. The phase φ is defined by $\varphi \sim \int \vec{k}.d\vec{l}$. Therefore, the gate voltage can effect the interference by changing the wave vector k. As we will discuss later in section 4.5, a magnetic field can also change the phase. In experiments, these interference terms introduce reproducible fluctuation in the conductance under applied gate voltages or magnetic fields. However, if a large number of paths j is involved to φ, yielding many positive and negative contributions, and the sum of the contributions from the interference term reduces to a small value, so the total probability is determined by the first term.

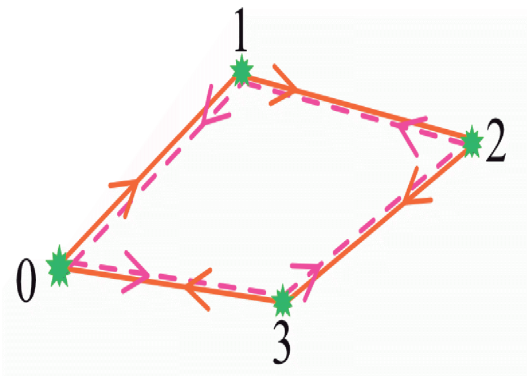


Figure 4.6: Schematics of an electron travelling in time reversed paths. Figure will be replaced.

Now consider an electron comes back to its initial position after travelling through a time reversed path as shown in figure 4.6. In this case, the electron waves travelling clockwise {0,1,2,3,0}and anticlockwise {0,3,2,1,0} will interfere. Since these two paths have identical lengths, the phase differences obtained during the travel are exactly the same. If we assume the amplitude of the wave travelling along a path p_j in a clockwise direction is A_1 and in anticlockwise is A_2, then the total probability of returning at the same place yields:

$$P_{0\to 0} = A_1^2 + A_2^2 + A_1 A_2 \cos(\varphi_j - \varphi_j) + A_2 A_1 \cos(\varphi_j - \varphi_j) = 4A_j^2 = 4t_j^2 \qquad (4.31)$$

where $A_j = A_1 = A_2$ and for convenience to compare it with the first term in equation (4.30) we write $A_j = t_j$, because A_j also refers to the classical probability. A factor of two comes from the fact that there are two trajectories per entry j. The

second factor of 2 is a consequence of constructive interference of the time-reversed electron waves in the closed paths.

In conclusion, time-reversed paths with coherent phases in a diffusive medium give rise to an increased probability for electrons to return to their initial positions. This is well known as coherent back scattering. Due to the coherent back scattering, electrons tend to return back to its initial position leading to a reduction of the conductance. This effect is commonly referred to as weak localization (WL). The WL quantitatively effects the conductance via a reduction of the diffusion coefficient by an amount of ΔD. Detailed discussions about the correction to classical conductance can be found in references [121, 122]. The $\Delta\sigma$ is described as:

$$\Delta\sigma = -\frac{2e^2}{\pi\hbar} D \int dt A(t) e^{-\frac{t}{\tau_\varphi}} \left(1 - e^{-\frac{t}{\tau_e}}\right), \tag{4.32}$$

where $A(t)$ denotes the classical probability of returning and τ_φ is the phase coherence time.

4.5.2.1 Effect of magnetic field

A quantum correction to the classical conductance introduced by WL is a small in amount and a common way to distinguish it from the classical conductance is by the application of a magnetic field [121]. According to quantum mechanics, the magnetic field effect on the momentum p with a vector potential A as described:

$$\vec{p} = \hbar\vec{k} - e\vec{A}, \tag{4.33}$$

If we consider an electron travelling along a path defined as l from position a to position b, then the required phase difference $\Delta\varphi_{a\to b}$ in presence of a magnetic field is:

$$\Delta\varphi_{a\to b} = \int_a^b \vec{k}\,.\,d\vec{l} = 2\pi\frac{m}{h}\int_a^b \vec{v}_F.\,d\vec{l} - 2\pi\frac{e}{h}\int_a^b \overrightarrow{A}.\,d\vec{l}, \tag{4.34}$$

hence, the phase is effected by the magnetic field via the second term in equation (4.34). Now, we will consider the influence of a magnetic field on time-reversed paths. Since, the trajectory of a time-reversed path implies a closed loop, the required phase can be described by a loop integral with an enclosed area S. Therefore, electrons travelling in clockwise and anticlockwise directions along the time-reversed paths give the phase difference $\Delta\varphi$ of:

$$\Delta\varphi = 4\pi \frac{BS}{\Phi_0}, \tag{4.35}$$

where $\Phi_0 = h/e$ denotes the flux quantum [122]. Hence, the magnetic field breaks the time-reversal symmetry. More precisely, the total probability of returning to the initial position given in equation (4.31) will be reduced to $\cos(\Delta\varphi(B))$ due to the phase-shift induced by the magnetic field [122]. Eventually, at larger magnetic fields, the WL is completely suppressed. A characteristic field B_c where the suppression become effective is given by:

$$B_c \sim \frac{\Phi_0}{l_\varphi^2} = \frac{h}{e l_\varphi^2}, \tag{4.36}$$

In experiments, the effect of a magnetic field to WL shows a positive conductance peak at zero magnetic field in magnetoconductance measurements, as shown in figure 4.7. It is worth pointing out that, for the above discussions the magnetic field is not considered large enough to effect to the classical path. Hence, the curvature of trajectories in a magnetic field due to the Lorentz force are negligible.

4.5.2.2 Effect of spin-orbit interaction

Spin precession and relaxation as a consequence of the SOI and other spin relaxation mechanisms have an impact on WL, and hence the conductance [117,120,123]. To explain the influence of the SOI on the electrons travelling along a time-reversed path, changes in direction of the electron spin have to be taken into account. Considering an initial spin state $|s\rangle$, the state after a clockwise rotation due to the SOI or scattering events can be described by:

$$|s'\rangle = R|s\rangle, \tag{4.37}$$

where R denotes a rotation, which implies changes of the spin direction between, or during the scattering events. Note that, R contains the product of a large number of small rotations $R_{1,2\ldots n}$. For the case of the electron (actually the partial wave) propagating counter clockwise, the rotation of the spin is reversed, and each rotation angle has to be inverted. As a result, a final state of the spin rotating in counter clockwise $|s''\rangle$ is given by:

$$|s''\rangle = \tilde{R}|s\rangle, \tag{4.38}$$

where $\tilde{R}$ is a rotation operator describing changes of spin direction along a counter clockwise path. In fact, the two operators are inverse to each other meaning that $\tilde{R}_i = R_i^{-1}$.

To determine the effect of the SOI on quantum interference it is required to calculate the interference contributions to the spin states, which can be given as:

$$\langle s''|s'\rangle = \langle \tilde{R}_s|R_s\rangle = \langle s|R^2|s\rangle, \tag{4.39}$$

If the spin-orbit interaction is weak, the spin will essentially remain polarized in the same direction during the propagation on a time reversed path, which yields R=1. The probability of coherent back scattering in equation (4.31) does not change. However, if the SOI is strong, the spin rotates in exactly the opposite direction as the electron travels along the time-reversed path. Therefore, the expectation value of R^2 has to be taken into account. Averaging of the interference term over many pairs of time-reversed paths gives $\langle s|R^2|s\rangle = -\frac{1}{2}$ [120]. It tells us that spin orbit interaction introduces destructive interference which leads a reduction of the quantum backscattering probability to half of the classical backscattering probability. Hence, the conductance will be increased which is well known as the weak antilocalization effect. The presence of magnetic fields restores the classical conductance, giving rise to a negative conductance as shown in figure 4.7

The combination of magnetic fields, spin orbit interaction and quantum interference yields a correction to the classical conductance for a nanowire as [124,125]:

$$\Delta G(B) = -\frac{2e^2}{h}\frac{D}{L}\int_0^{\infty} dtA(t)(1-e^{\frac{-t}{\tau_e}})e^{-\frac{t}{\tau_\varphi}}e^{\frac{-t}{\tau_B}}\frac{1}{2}\left(3e^{\frac{-4t}{3\tau_{so}}}-1\right), \tag{4.40}$$

where, L is the device length, τ_B is the magnetic dephasing time, τ_{so} the spin relaxation time, A(t) is the classical probability of returning, and $\Delta G(B) = G(B) - G(B=0)$.

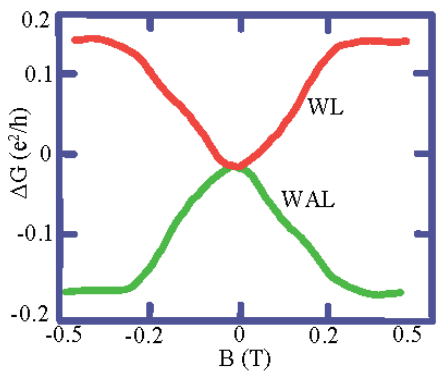


Figure 4.7: Schematic illustration of WAL and WL effect for magnetoconductance measurements at low magnetic fields.

4.6 Measurements and discussions

4.6.1 Device fabrication and characterization

In this section, we studied the SOI in InSb nanowires in the quantum diffusive regime where the system can be considered as a quasi 1D system and quantum confinement accounts for the presence of the SOI in the system. We determined the SOI strength based on the measurements of WAL with InSb nanowire devices. To achieve stronger tuning of the conductance we fabricated devices with a top gate geometry in combination with high k-dielectrics. We used InSb nanowires grown by CVD to make the devices. Before depositing the Ti/Au contacts, the native oxide layer of the nanowire was etched in diluted $(NH_4)S_X$ solutions. After depositing the contacts, 10 nm thick HfO_2 was grown onto the nanowires partially covering the contacts to fully control the conductance of the channel. Finally, the Ti/Au top gate metal electrodes were deposited onto the oxide layer by thermal evaporation. Note that, electron beam lithography was used to define the contacts, the oxide layer patterns, and the top gate electrodes. A SEM image of one of our measured devices is shown in figure 4.8a. In addition to the top gate, the devices also have a global back gate, which is separated from the nanowire by a 200 nm thick SiO_2 layer. However, we only used the top gate for all measurements, while the back gate was grounded. From the investigation of the device with SEM after the measurements, we find that the nanowire used for this typical device has a diameter of 75 nm. The separation space between the source and drain is 2 μm which is long enough to have sufficient scattering in the wire during the electron travelling along the nanowire from source to drain and also to suppress the Coulomb blockade effect at low temperatures. The magnetoconductance measurement is performed in a dilution fridge at 6K temperature with low magnetic field applied perpendicular to the nanowire and device substrate. We used a standard lock-in technique with an AC bias voltage of 100 μV to measure the two-terminal conductance.

Figure 4.8b shows the measured conductance as a function of top gate voltage V_{TG} at a temperature of 6K and zero magnetic field. The device shows ambipolar transport behaviour with pinch-off threshold voltages V_{Th} of 2.5 V and 0.04 V, extrapolated from the G-V_{TG} characteristics for the electron and hole transport sides, respectively. The hole conductance is found to be a factor of three less than the electron conductance. The lower conductance of the p transport side makes it difficult to determine characteristic lengths L_φ and L_{SO} of holes from magneto-conducatnce measurement (MC). We focused on the electron transport side for our MC measurements to determine L_φ and L_{SO} for electrons. Moreover, quantum conductance corrections due to the SOI and WL to the classical Drude's conductance is, in the fact, very small in amount. In order to extract quite accurate

phase coherence and spin-orbit length (spin relaxation length), contributions from contact resistances to the measured conductance must be considered and subtracted from the MC data obtained directly from the measurements. Due to the absence of the Fermi level pinning, unlike InAs nanowires, non-negligible contact resistances are expected for the devices with InSb nanowires. In order to extract the mobility and contact resistances we followed the same method as already used in chapter 3. First, the top gate capacitance C is calculated using equation (3.20) which gives a value of 7.43 fF.

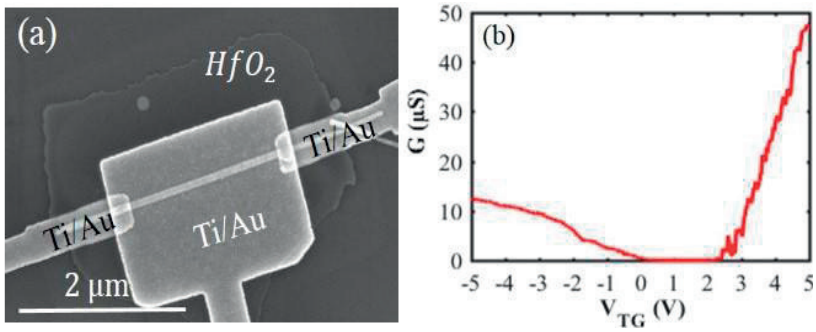


Figure 4.8: (a) SEM image of the measured device. (b) The measured conductance at 6 K and zero magnetic field.

Then the measured conductance G was numerically fitted to equation (3.19) where the electron mobility μ_e and the contact resistance R_C are the fitting parameters while the threshold voltage V_{Th} is obtained by extrapolating from the G-V_{TG} curves. The data fit to the measured conductance at a temperature of 6K is given in figure 4.9 where the red dots represent the measured conductance and the black solid line is a fit to the conductance. From the fitting, we obtained electron mobility of $\mu_e = 1500\ cm^2/V.s$ and a contact resistance of $R_C = 2\ K\Omega$ which consistent with typical contact resistances of InSb NW devices with Ti/Au contacts [62, 71]. Using the equation for the gate induced carrier concentration in FETs, which is given by:

$$n(V_{TG}) = \frac{V_{TG}-V_{Th}}{eLA}, \tag{4.41}$$

where $L = 2\mu m\ , V_{Th} = 2.5\ V,$ A is the cross-section of the wire [62], we determined electron concentration of $n_e = 8.1 \times 10^{18}\ 1/cm^3$ at V_{TG}= 4V. The mean free path l_e is obtained from $l_e = \tau_e u_F$ where τ_e is the scattering time and u_F is the Fermi velocity. The scattering time was determined from $\tau_e = \frac{\mu_e m^*}{e}$. The u_F is estimated using $u_F = \frac{\hbar}{m^*}(3\pi^2 n_e)^{1/3} = 5.1 \times 10^6\ s/m$ for a 3D density of states. Based on that, the obtained value of the mean free path for our device is $l_e \approx$

61 nm, and the Fermi wave length is $\lambda_F = \frac{2\pi}{K_F} \approx 11\ nm$ where K_F is the Fermi wave vector, given by $K_F = \frac{u_F m^*}{\hbar}$.

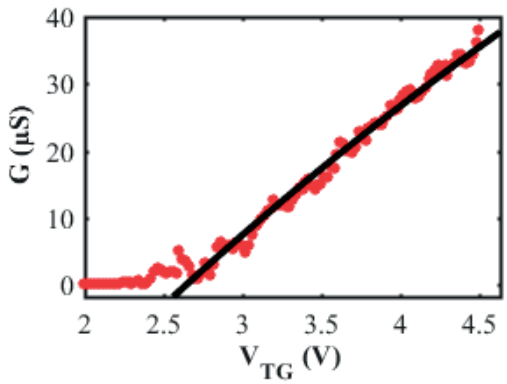


Figure 4.9: Data fit to the measured conductance using equation (3.19). The red circles denote the measured conductance and the black solid line is the fit to the conductance.

4.6.2 Extraction of spin relaxation, phase coherence length, and spin-orbit energy

We measured the MC using the top gate to tune the conductance of the device. In order to suppress the effect of conductance fluctuation, 18 MC measurements were performed for the same top gate values, after averaging these measurements the conductance fluctuations are greatly suppressed. Figure 4.10 depicts $\Delta G(B) = G(B) - G(B = 0)$ at different top gate values. At V_{TG} = 5V, a clearly negative conductance peak can be observed, which is a contribution of the WAL effect due to the presence of spin-orbit interaction in the InSb nanowires. As the top gate voltage V_{TG} decreases the WAL is suppressed. Finally, at the top gate voltage of V_{TG} = 2.8 V, a crossover from WAL to WL (positive conductance) occurs. Considering that the width of the InSb nanowire investigated in this work, $W \sim 75nm$, which is much smaller than the typical dephasing length $L_\varphi \sim 300 - 600\ nm$ of the InSb nanowires, quasi-1D localization theory can be properly applied to interpret our experimental observations [118, 126, 127]. Based on the field-effect electrical characterization at low temperature, we can use the quasi-1D localization theory in the 'dirty' limit, which implies $L \geq L_\varphi \geq W > l_e > \lambda_F$. For the quasi-1D model of weak localization, the conductance correction is given by:

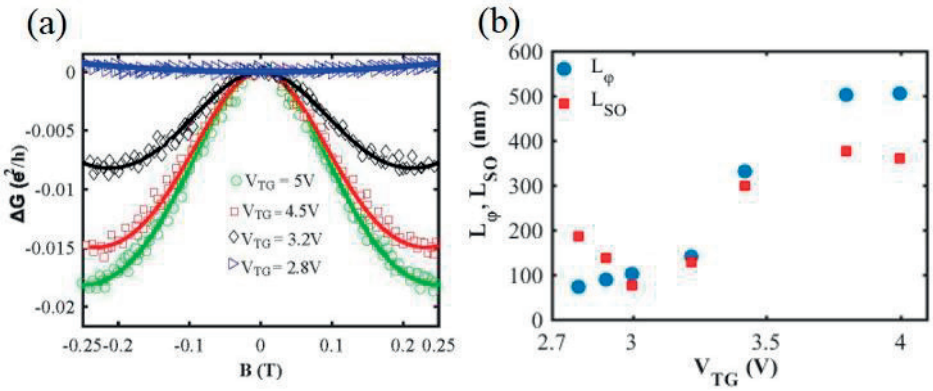


Figure 4.10: (a) ΔG (B) as a function of magnetic field B for different top gate voltages. Crossover from WAL to WL occurred at V_{TG} = 2.8 V, at 6K. (b) Extracted phase coherence Lφ and spin-orbit interaction L_{SO} lengths as a function of top gate voltage.

$$\Delta G(B) = -\frac{2e^2}{hL}\left[\frac{3}{2}\left(\frac{1}{L_\varphi^2}+\frac{4}{3}\frac{1}{L_{SO}^2}+\frac{1}{3}\left(\frac{eWB}{h}\right)^2\right)^{-\frac{1}{2}}-\frac{1}{2}\left(\frac{1}{L_\varphi^2}+\frac{1}{3}\left(\frac{eWB}{h}\right)^2\right)^{-\frac{1}{2}}\right], \quad (4.42)$$

where L_φ is the phase coherence length and L_{SO} is the spin relaxation (spin orbit interaction) length [127]. The measured MC data is fitted to the qusi-1D model for low magnetic fields, using equation (4.42) with L_φ, L_{SO} are as the fitting parameters. The solid lines in figure 4.10a represent the best fit to equation (4.42) indicating a good agreement between our measurements and the quasi-1D theory.

The extracted L_φ, L_{SO} for different top gate voltages V_{TG} are given in figure 4.10b. Both L_φ, L_{SO} show strong dependence on the top gates, which consistent with a previous report in InSb nanowires [128]. The phase coherence length shows a monotonous increase with increasing top gate from 71 nm to 514 nm for the corresponding top gate voltages of V_{TG} = 2.7 V and 4.3 V respectively. The decrease in L_φ with lowering gate voltages can be explained by a density dependence of the diffusion constants and also a density dependence of electron-electron interaction. In the lower carrier density regime (at lower gate voltages) Coulomb screening is expected to be reduced, which enhances the electron-electron interaction leading to a decrease in L_φ. The electron-electron interactions are often reported as the dominant source of dephasing in nanowires [129]. The transition from WAL to WL can be understood by the crossover between L_φ and L_{SO}. The spin relaxation length L_{SO} first reduces from 184 nm to 76 nm with increasing V_{TG}, then starts to increase again above 3V gate voltages and reaches 358 nm at V_{TG} = 4.3V. I. van Weperen et al. observed similar results from WL measurements on InSb nanowires [128]. As we mentioned earlier the most relevant mechanisms for spin relaxation in narrow

bandgap semiconductors are the EY and DP mechanisms corresponding to spin randomization at or in between scattering events due to spin precession, respectively. According to the EY mechanism, an estimated spin relaxation length is $L_{YE,SO} = 300 - 600\,nm$[128]. For the DP mechanism, we emphasize the absence of the Dresselhaus SOI based on the fact that our nanowires have zinc-blende crystal structure, grown in [111] direction. Thereby, we expect that the dominate source of spin relaxation in our nanowire is the Rashba SOI [128].

Next, we extracted the spin precession length l_R from which in principle, the Rashba SOI strengths can be estimated. The relation between the spin relaxation length and spin precession length is given by:

$$L_{SO} = \frac{\sqrt{3}}{d} l_R^2 \,, \tag{4.43}$$

where d is the diameter of the nanowire. We extracted the spin precession lengths and plotted them as a function of top gates, as shown in figure 4.11. We obtained the spin precession lengths of $l_R \approx 57\,nm - 124\,nm$, that allow us to estimate the corresponding Rashba spin orbit parameter of $\alpha_R = \frac{\hbar^2}{2m^* L_R} \approx 0.4\,eV\text{Å} - 0.87\,eV\text{Å}$. The related spin-orbit energy is $E_{SO} = \frac{m\alpha_R^2}{2\hbar^2} \approx 0.16\,meV - 0.77\,meV$.

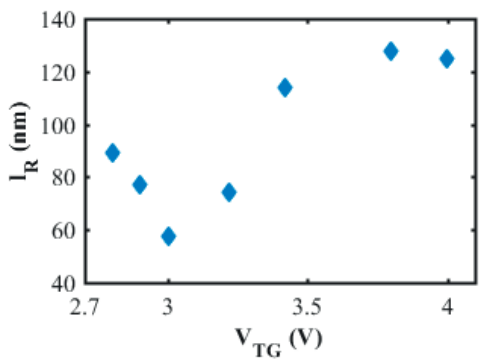


Figure 4.11: Spin precession length l_R as a function of top gates.

The spin-orbit strength α_R we extracted from our device is higher than some previously reported values for InSb based nanostructures. For examples, $0.03\,eV\text{Å}$ obtained from a MC measurement with an InSb quantum well [129], and $0.16 - 0.22\,eV\text{Å}$ from quantum dot systems [100]. However, as we already discussed different values of spin-orbit strengths can be expected depending on the dimensionality of the system. Slightly higher values of $\alpha_R \approx 0.5 - 1\,eV\text{Å}$ than our results have also been reported from MC measurements with InSb nanowires grown by MOVPE [128]. The diameter of the nanowires measured in ref [128] is

$\sim 100\, nm,$ which is thicker than the wire we studied in this work. A diameter dependence of the SOI has been reported for thin nanowires. The spin relaxation length increases with decreasing nanowire diameter [118]. Therefore, we assume that the slightly lower values of α_R in our nanowires than in ref [128], is due to the smaller diameters of our nanowires.

4.7 Conclusions and outlook

We performed low field MC measurements at low temperature with devices made from CVD grown InSb nanowires. We applied quasi-1D weak localization theory to interpret our experimental observations. We find very good agreement between the theory and our MC data. The MC measurements indicate that the InSb nanowires we studied have strong spin-orbit strength of up to $\alpha_R \approx 0.87\ eV$Å. This large SOI underlines the potential applications of CVD grown InSb nanowires for spin qubits and investigations of Majorana fermions. It will be interesting to further study the dependence of the characteristic lengths L_{SO} and L_{φ}on temperature, orientations of magnetic fields and diameters of the wires to further understand the spin relaxation mechanisms in these nanowires.

Although, InSb NWs have a small bandgap, observations of ambipolar transport at low bias in the open regime have been challenging. Hence, experimental studies related to spin relaxation and spin-orbit strength on the hole transport side of InSb nanowires in the open region have been missing. Observations of ambipolar transport in InSb NWs used in this work will allow us to study spin relaxation in the valence band. In fact, studying the WAL on the hole transport side of InSb nanowires have potential importance in both applications and fundamental studies. Moreover, the spin relaxation in the conduction band and in the valence band can be directly compared from the measurement on the same devices. Finally, considering the small diameters of the InSb nanowires which can be achieved by CVD, it would be interesting to explore helical states in this nanowire.

Chapter 5
Electron transports in single quantum dots

5.1 Introduction

Unlike what we have discussed in previous chapters, in this chapter we investigate the electron transport in a very small island in which the electron is confined in all three directions, giving rise to quantization of energy states, similar to 'A novel physics' that appears in an atom [130]. Since its earlier discovery in the late eighties, quantum dots have been used to study a wide range of quantum physics phenomena. Moreover, semiconductor quantum dots have been attracting a great deal of interest for the implementation of spin qubits [14]. Therefore, methods are required to prove and investigate the transport through quantum dots. A simple and common method to probe quantum dots is the transport measurements where one of the dot reservoirs is biased while the other one is used to measure the current through the quantum dot. By transport measurements, one can check the tunability of gates, device stability and perform level spectroscopy such as charging energy, quantization energy, transport mechanisms, like first order single electron tunnelling, co-tunnelling and so on.

Quantum dots formed in nanowires using several different methods have been reported, for example, using hetrostructure nanowires grown with materials of different bandgaps [131], confine electrons in a nanowire grown with different crystal structures [48], and locate electrons by electric fields generated using gates [35]. The side gate has several unique advantages over other gate techniques like bottom gates or top gates. For example, only a single lithographic step is needed to make a device including source-drain contacts and local finger side gates. Moreover, side gates can help to reduce charge traps at the interface between the gate oxide material and the nanowires since the vacuum is used as the gate dielectric material. Perhaps, more importantly, it can help to tune and control SOI efficiently, and therefore, is of fundamental importance for use in spin qubits. This is due to the fact that side gates have a flexibility of designing the gate structures and devices in such a way that the symmetry and charge distribution in the nanowires can be controlled

effectively. However, making a highly tunable quantum dot system with side gates has been hindered because of difficulties in device processing like placing the gate close enough to the nanowire and also making them as thin as possible. In this chapter, we overcome these challenges and make tunable quantum dots using side gate techniques.

This chapter begins with an introduction to electron transports on single quantum dots. Various transport phenomena that take place on single quantum dots are explained by a simple theoretical description which relies on a capacitance model. Electron transport in both the weak and strong coupling regimes of a single dot will be presented. Low temperature electron transports in InP-InAs core shell nanowires will be discussed at the end of this chapter.

5.2 Transport in single quantum dots

A quantum dot is a zero-dimensional system where the motion of electrons is restricted in all three directions. Irrespective of how the dot is created, a quantum dot can be treated as an island of charge which is connected capacitively through tunnel barriers to conducting reservoirs and purely capacitively to a gate as illustrated in figure 4.1. The Hamiltonian of the quantum dot can be described as:

$$H_{QD} = E_C \frac{N(N-1)}{2} - \frac{N_e}{C_{\sum C}}\left(C_g V_g + C_s V_s + C_d V_d\right) + \sum_{i,\sigma} N_{i\sigma} \mathcal{E}_{i\sigma}, \qquad (5.1)$$

$\sum_C$ denotes the sum of the capacitances of the reservoirs and the gate. The first term is the charging energy referring to the energy required to put an electron onto the dot. The charging energy is related to the capacitance of the dot and given by: $E_c = \frac{e^2}{C_\Sigma}$. Moreover, the charging energy varies inversely with the dot area. The second term is the Coulomb interactions of the electrons on the dot with electrons from nearby conductive reservoirs. According to the constant interaction model [132], the Coulomb interaction between electrons on the dot and the electrons in its surroundings are characterized by a single constant capacitance and not effected by electron-electron interactions, hence independent of the quantum state of each electron. The first two terms are classical and only require the quantization of charge. The last term in equation (5.1) describes the single-particle energy levels originating from the quantum confinement effect where the i-th level has an energy of $\in_{i\sigma}$ with the spin σ. The level spacing energy is responsible for the existence of a discrete energy in the system and is determined by the dot dimensions and effective mass of the carriers as:

$$\Delta = \frac{2\pi\hbar^2}{m^* A}, \tag{5.2}$$

where m^* is the effective mass and A is the area of the combined system. For a smaller the dot size, a larger level spacing energy is expected. At a low enough temperature, where the energy states are well resolved, quantum dots in the few electrons regime can reveal a shell structure in tunnelling transport measurements, similar to an atomic energy level, therefore, the quantum dots are commonly referred to as artificial atoms.

Beside the dot energy, the reservoirs have an energy which is given by a Hamiltonian, $H_a = \sum_{k\sigma} \epsilon_k N_{ak\sigma}$ where k denotes the states in the leads with spin σ, and $N_{ak\sigma}$ are occupations which is usually determined by the Fermi distribution, $N(\epsilon_k) = \frac{1}{\left(1+e^{\frac{\mu_a-\epsilon}{kT_a}}\right)}$ where $\mu = -eV_a$ is the chemical potential and T_a is the temperature of the reservoirs [133]. The coupling of the reservoirs to the dot can be represented by the term:

$$H_{QD-a} = \sum_{i,k,\sigma} t_{i,a,k,\sigma}(c_{i\sigma}^{+} c_{ak\sigma} + h.c), \tag{5.3}$$

with the tunnelling elements $t_{ia\sigma}$, $c_{i\sigma}^{+}$ creation and $c_{ak\sigma}$ annihilation operators, and h.c denotes the Hermiton Conjugate. Fermi's golden rule can be used to calculate the tunnelling rate for into and out of each level in the dot as follows:

$$\Gamma_{ai\sigma} = 4\pi\rho(\epsilon_{i\sigma})|t_a|^2 \tag{5.4}$$

where $\rho(\epsilon_{i\sigma})$ is the density of states in the lead (at the reservoirs), $\Gamma_{ai\sigma}$ has units of energy that gives the tunnelling time of $t_{ai\sigma} = \frac{\hbar}{\Gamma_{ai\sigma}}$, according to the uncertainty principle.

In the fact, transport through a quantum dot is usually related to the five energy scales as shown with the energy diagram of the dot in figure 5.1b [134]. The charging energy and the level spacing energy are related to the size of structures, and the geometry of the quantum dots. kT and eV_{sd} are involved to the leads, the Γ describes the coupling between the other energy scales. As a general principle, in order to observe quantum effects, for example Coulomb blockade in a quantum dot, two conditions must be fulfilled: the first condition is that the thermal energy must be less than the charging energy $K_BT \ll E_C$, and the second condition is that the tunnelling resistance to the source drain reservoirs must be larger than the quantum resistance h/e^2 =25.8 kΩ to ensure that the dot is isolated from its environment. The value of kT with respect to other energy scales, gives the following distinct transport behaviour for a closed quantum dot:

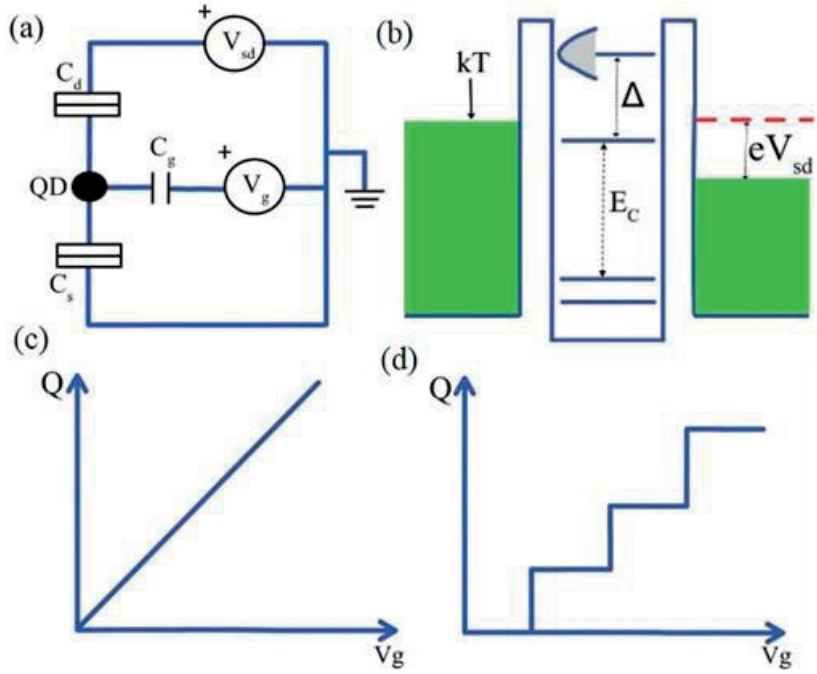


Figure 5.1: (a) Schematic of the equivalent circuit of a single quantum dot system. The quantum dot is connected to source and drain via tunnel barriers and capacitively coupled to the gate. (b) Five energy scales that determines the transport through the quantum dot. (c-d) Q-V relations for charge on a capacitor classically and quantum mechanically.

if the temperature is high, $kT > E_c$, the thermal excitation can access multiple charge states, the conductance will not be fully suppressed giving rise to de-localization of electrons in the dot. If kT is smaller than E_c, but still larger than the level spacing energy, $\Delta < kT < E_c$, the transport can be expected to be fully suppressed. However, for each charge state multiple energy levels can be found. Filling of the levels in the dot obey the Fermi distribution, just like the states in the reservoirs. This regime is known as the classical regime. If the temperature is further lowered and reaches the condition of $kT < \Delta$, the dot is driven into a quantum regime where the charge states are well separated and single energy levels can be expected to involve in the transport. Moreover, this regime can further be divided into two regimes: the thermally broadened regime $\Gamma < kT$, and the lifetime broadened regime $\Gamma > kT$. For this thesis, the measurements on quantum dots are performed at a low enough electron temperature, below 100 mK, ensuring the study of the dots in the quantum regime. In the following subchapters, we will discuss our single dot measurements.

5.3 Coulomb blockade and Coulomb oscillations

In terms of classical physics, the charge on a capacitor can be described by a continuous function of voltage across the capacitor $Q = CV$ as presented in figure 5.1c. This is true for a dot which contains a large number of electrons, where the Coulomb repulsion is not visible. However, when the Coulomb repulsion becomes strong in the system, tunnelling of electrons from one reservoir through the dot to another reservoir can be suppressed at low temperatures. The charge on the dot can only be integer multiples of the electron charge, $Q = Ne$, as illustrated in figure 5.1d. The number of electrons on the dot is determined by the quantum dot voltage V_{dot}, which is related to the gate voltage V_g by $V_{dot} = \alpha_g V_g$. The parameter $a_g = \frac{C_g}{C_\Sigma}$ is called the gate lever arm, which converts the applied gate voltage V_g to the actual voltage on the dot, V_{dot}.

We start our discussions with the current I through the dot as a function of gate voltage V_g at a small source-drain bias, V_{sd}. One of our such measurements performed at the small bias of V_{sd} = 25 μV is given in figure 5.2, in which periodic current peaks can be seen. The SEM images of the measured device is given in figure 5.7a. The dot is formed by applying negative voltages to the gates G3 and G4 to create potential barriers in the nanowires, and the dot energy levels are tuned by using the plunger gate G7. The quantum dot is in a few electron regime, which is indicated by unequal periodicity of the peak spacing. Each peak corresponds to tunnelling in and out of electrons through the dot while the valley represents Coulomb blockade [135]. The electron numbers fluctuate between N and N+1 at the peaks, while it is constant for all other gate voltage regions between each adjacent peak.

By taking into account the influence of the charging energy E_c and quantum confinement energy Δ, the Coulomb oscillation in figure 5.2 can be qualitatively interpreted following the energy diagrams illustrated in figure 5.3. As can be seen in figure 5.3 (a), at less positive gate voltages the quantum state of the dot is lifted up above the Fermi energy of the source drain reservoir and current is blocked, corresponding to the situation (a) in figure 5.2. As the gate voltage is increased towards more positive values, the quantum state of the dot is lowered. When it is aligned with the Fermi energy of the reservoirs (that corresponding to the diagram b in the figure 5.3) an electron can tunnel on and off the quantum dot, which gives a current peak, labelled (b) in figure 5.2. Further increasing the gate voltage brings down the first electron state below the Fermi energy of the leads, an electron can tunnel into the dot, but it cannot tunnel out since there are no energy states available in the lead. Therefore the electron stays on the dot. In order to tunnel a second electron onto the dot, the charging energy U_2 has to be overcome as illustrated in figure 5.3d. The current is blocked again resulting in a Coulomb valley as shown at

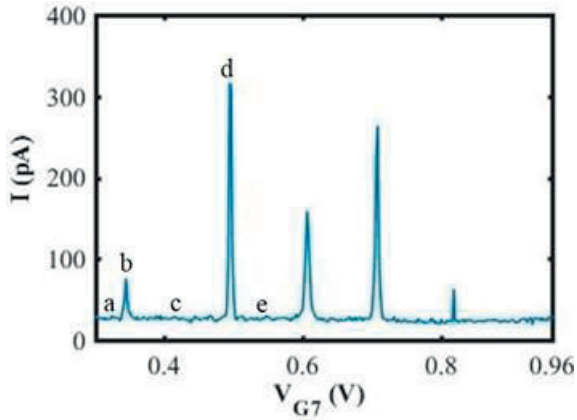


Figure 5.2: Coulomb blockade effect, the current I is measured as a function of gate voltage V_{G7} at V_{SD} = 25 μV.

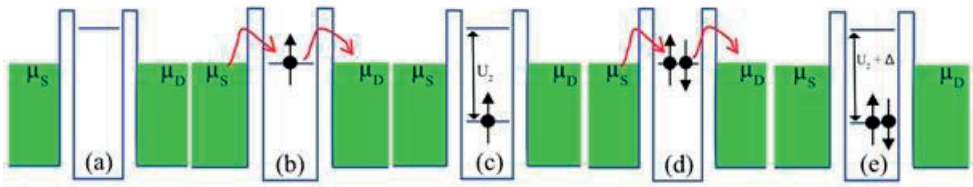


Figure 5.3: Energy diagram of the quantum dot corresponding to the mark letters in figure 5.2

at point (c) in figure 5.2. Further increasing the gate voltage enables a second electron to tunnel onto the dot, leading to an occupation of two electrons with spin up and spin down on the orbital ground states, as presented in figure 5.3e. At this degeneracy point, electrons can tunnel on and off allowing current to flow through the dot, corresponding to point (d) in figure 5.2. For the third electron, the orbital ground state is not available, and it has to tunnel to the next orbital state, which is an energy Δ above the orbital ground state. Therefore, the required energy for the third electron to tunnel onto the dot is U_3+ Δ, where U_3 is the Coulomb repulsion energy coming from the electrons in the dot as illustrated in figure 5.3f. The current I is blocked again, as shown with (e) in figure 5.2. Following this simple illustration, the fourth electron can share the same orbital as the third one with opposite spin with an additional energy U_4. However, it is not always true, even more complicated configurations can be expected when higher order cotunneling events take place as we will discuss later.

5.4 Excited state tunnelling

So far, we have discussed transport for the zero-bias case, where the reservoirs source and drain have the same chemical potentials. Therefore sequential tunnelling on and off of electrons can occur at degeneracy points, where the chemical potentials of the reservoirs align with the quantum states of the dot. However, at a finite bias there is a Fermi energy difference between the chemical potential of source and drain. This can usually be achieved in experiments by applying a finite bias to one of the leads while other one is fixed. We ground the drain lead by connecting it to the input of the current pre-amplifier, since the input usually provides with a virtual ground. When negative voltages are applied between source and drain, the Fermi energy of the source increases by eV_{SD} respect to the drain Fermi energy. Since the reservoirs are also capacitively coupled to the dot, the energy states of the dot shift as the Fermi energies of the leads are changed. Current can start flowing when the first orbital ground state of the dot lays between the Fermi energies of the leads as illustrated in figure 5.4a. At this degeneracy point electrons tunnel on and off through the dot leading a current peak in a Coulomb oscillation diagram, similar to the zero-bias case. A further increase in the bias voltage allows the first excited state to involve in the transport, as illustrated in figure 5.4b. At a sufficiently large bias voltage, several transport paths might be available to contribute to the transport, as shown in figure 5.4c.

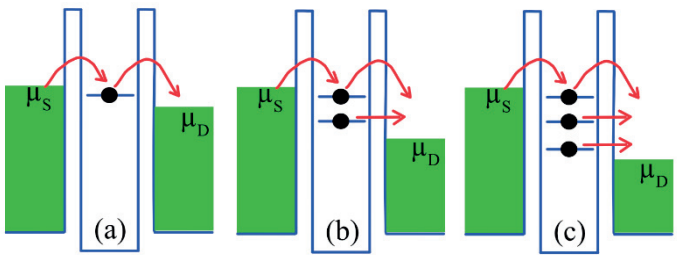


Figure 5.4: (a) Energy diagram of quantum dot at low bias where single quantum state contributed to the transport. (b,c). At large bias two or more states can involve to transport.

One of our experimental measurements for excited state tunnelling is presented in figure 5.5. The data is obtained from the same device and the same dot configurations as used in figure 5.3. Figure 5.5 depicts the differential conductance as a function of source-drain bias at a fixed gate voltage. Some transport features are marked with letters in figure 5.5 and can be interpreted as following, note that the gate voltage is fixed such that the dot is in the off state at zero bias and the current is blocked, corresponding to mark (d) in the figure 5.5. However, as a negative bias is applied to the source, the Fermi level of the source increases. As we discussed earlier this also leads to shifting of states in the dot by $e\alpha V_{SD}$ where $\alpha =$

$\frac{C_{SD}}{C_{\Sigma}}$, because of the capacitive coupling between the source and drain. That allows an electron to tunnel from source to drain giving rise to the appearance of a peak in the conductance as marked with (c) in figure. 5.5.

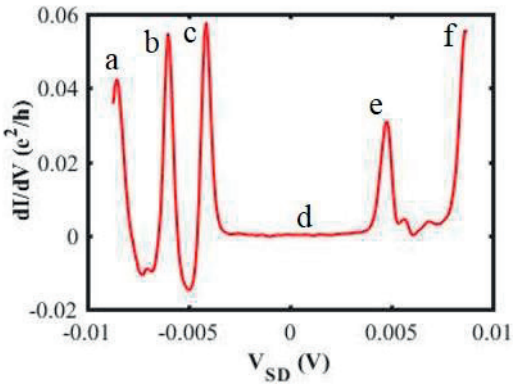


Figure 5.5: Differential conductance verses bias at fixed gate voltage. d corresponds to Coulomb blockade valleys, c and e transport through the ground states of the dot, while a, b and f refer to tunnelling of electrons via excited states of the dot.

Similarly, when positive bias voltages are applied to the source, the Fermi level of the source is lowered with respect to the drain Fermi level. Electrons can tunnel from drain to dot, resulting in a conductance peak as shown in figure 5.5 with the letter (e). At sufficiently negative or positive source drain bias, either of source or drain chemical potentials aligns with the excited state energy levels of the dot that provides an additional channel for the transport that correspond to the peaks marked with (a), (b) and (f) in the figure. 5.5. Tunnelling through excited states can also be observed with 2D maps where source drain bias and gate voltage change simultaneously. This yields Coulomb diamonds as we will discuss in the next subchapter.

5.5 Coulomb diamonds

As we have already discussed, the current which flows through a quantum dot can be measured in two ways, either sweeping the plunger gate voltages or the source drain bias while one of them is kept constant. Moreover, measuring current I or conductance through a quantum dot while simultaneously sweeping both the gate voltage V_g and source-drain bias V_{sd} gives a 2D current or conductance plot as a function of V_g and V_{sd}, called Coulomb diamonds as depicted in figure 5.6. Within the diamond, the current is blocked since the quantum state in the dots do not align

with either of the source-drain Fermi levels as illustrated in the diagram F. The number of electrons on the dot is fixed to an integer number in the diamond. The electron transport is not blocked outside of the diamond. The current I can flow through the quantum dot from one of the leads to other at the degeneracy points where quantum states in the dot align with at least either of the Fermi levels of source and drain as shown with energy diagrams in A, B, C, D, E. Tunnelling through excited states can be seen as additional transport lines which are parallel to the edges of the diamonds as shown with the dashed orange line in figure 5.6. The Coulomb diamonds are an invaluable tool for the understanding of transport features through the dot. The charging energy, level spacing energy, effective size of the dot, coupling strength of the gates and sources can be obtained from a charge diagram. Furthermore, higher order cotunneling features can also be identified and studied using a charge stability diagram.

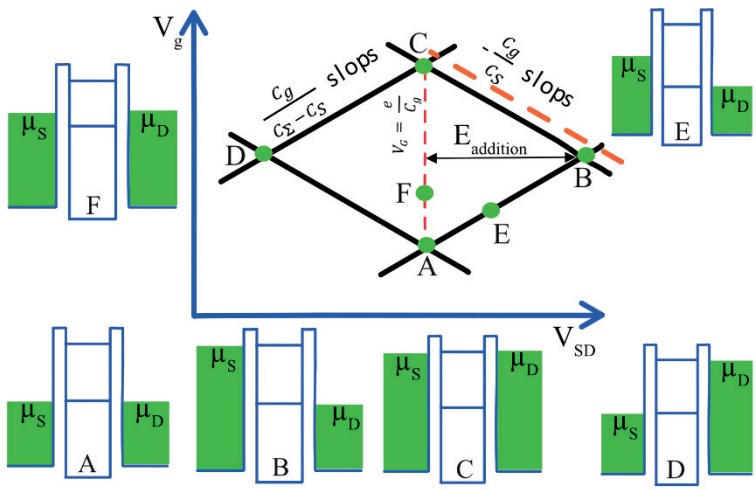


Figure 5.6: Charge stability diagram of a quantum dot as a function of source-drain and gate voltage. A-F various configurations of quantum dot states respect to the chemical potentials of source and drain. Slope of the lines determined by capacitance of the gate, source and drain are also sketched.

Figure 5.7c shows one of our charge stability diagrams where the differential conductance $\frac{dI_{SD}}{dV_{SD}}$ is plotted as a function of V_{G7} and V_{sd}. An SEM image of the device and schematic drawing are presented in figure 5.7a and figure 5.7b respectively. The dot is formed by using gates G3 and G4 with applied negative voltages -3.8V and -2.8V respectively in order to form potential barriers in the nanowire. Gate G7 is used as a plunger gate to tune the energy levels of the dot. Outside the diamonds, pronounced excited state spectra are shown by white dashed lines, which originated from zero-dimensional confinement. From the height of the smallest Coulomb diamond, we extracted an average charging energy of E_c = 6.1 meV and a level spacing energy of Δ_{ES} = 0.765 μeV is determined from excited state

spectra. Using the extracted charging energy, we estimated the capacitance of the quantum dot $C_{\Sigma QD1} = 26$ aF. From the lateral sizes of the small Coulomb diamonds we also extracted the plunger gate capacitance of C_{G7} =1.57 aF, and a gate conversion factor of $\alpha_{G7} = \frac{C_{\Sigma QD1}}{C_{G7}} = 0.06$.

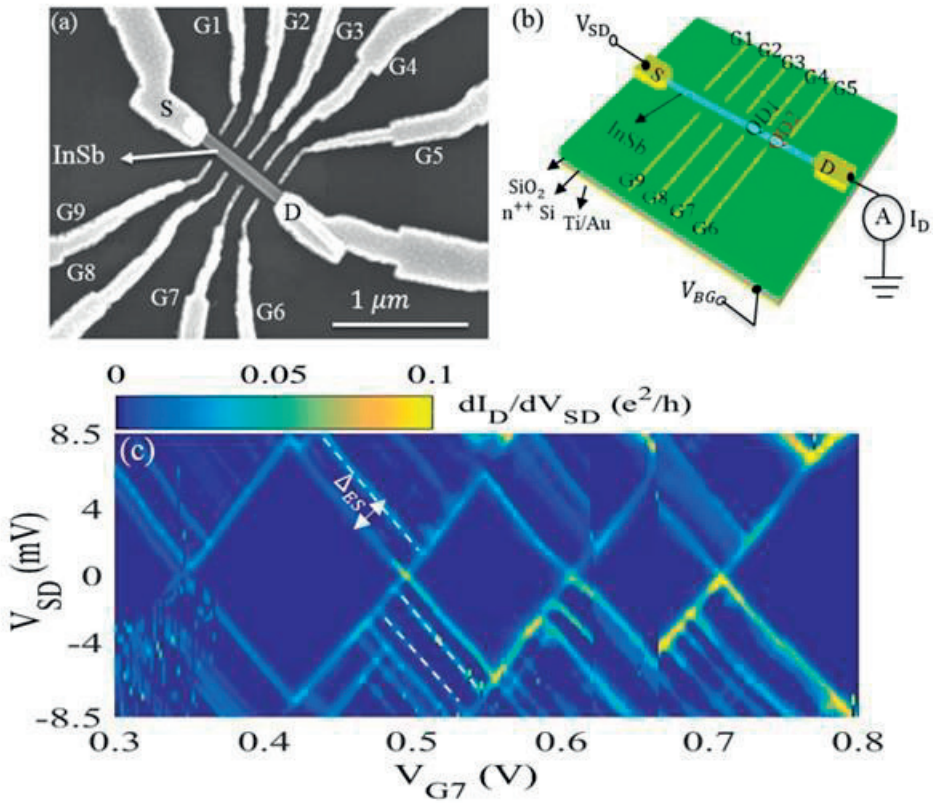


Figure 5.7: (a) SEM image of the device. (b) Schematic of the device in (a). (c) Charge stability diagram of the quantum dot where differential conductance is plotted as a function gate voltage V_{G7} and V_{SD}. The dot is formed using gates G3 and G4.

5.6 Cotunneling transport

Up to, we have discussed first order sequential tunnelling that happens at degeneracy points, and the current is suppressed within diamonds. However, under some conditions, transport features can be observed within diamonds where, in principle, transports are not expected to take place. Cotunneling can be divided into

elastic and inelastic cotunneling depending on whether total energy of the system is conserved or not after the transport.

5.6.1 Elastic and Inelastic Cotunneling

The cotunneling process can be considered as a higher order tunnelling process that involves two or more electrons tunnelling simultaneously [136-138]. Let us consider a second order tunnelling process where two electrons contribute to the transport. The electron on the ground state of the dot tunnel out to the right lead (drain), simultaneously one electron from the left lead (source) tunnel onto the ground state of the dot as shown in figure 5.8a. During the process the energy of the quantum dot

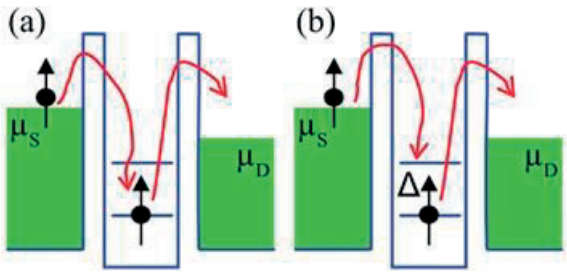


Figure 5.8: Illustration of (a) elastic (b) inelastic cotunneling involving two electrons.

remains unchanged, this process is called elastic cotunneling. The second possible mechanism of transport is one electron from the left lead tunnel onto the excited state of the dot while one electron tunnel out to right lead from the ground state of the dot as illustrated in figure 5.8b. This process called inelastic cotunneling. For inelastic tunnelling to take place, the bias energy must be at least equal to or larger than the level spacing energy Δ. Therefore, this process depends on the bias voltage but is independent of the gate voltages [139].

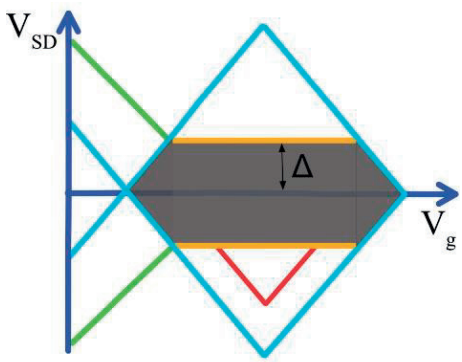


Figure 5.9: Schematics of elastic (grey area), inelastic (orange lines) cotunneling and cotunneling assisted sequential tunnelling (V shaped red lines) in a charge diagram.

The question is how this tunnelling process can be identified in a charge stability diagram? This is illustrated in figure 5.9, where the blue line on the edge of the diamond denotes the first order sequential tunnelling while the green line parallel to the blue line represents tunnelling through the first excited state of the dot, as we already discussed. The grey area within the diamond refers to elastic tunnelling which corresponds to the case in figure 5.8a. The transport features of the inelastic tunnelling process is shown by orange lines parallel to the gate voltage in the diamond indicating independence of the gate voltage.

Data from one of our experiments which demonstrates cotunneling process is given in fig 5.10. The data is obtained from measurements with another device (device 2) similar to the device in figure 5.7a. The dot is formed using side gates. The charge diagram shows the quantum dot is in many electron regime indicated by the equal size of diamonds and smaller charging energy compared with the charge diagram in figure 5.7c. The higher differential conductance shows that the dot is in

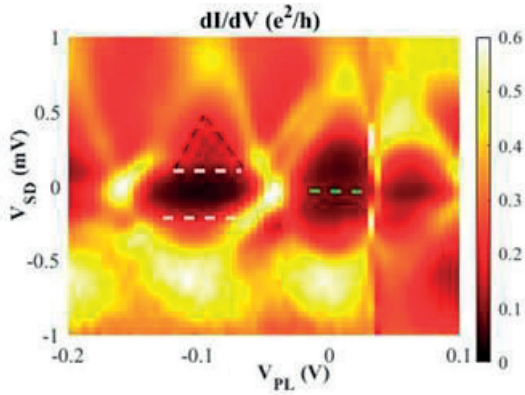


Figure 5.10: Differential conductance as a function of plunger gate voltage V_{PL} and bias voltages measured from device 2. Elastic and inelastic cotunneling transport lines are shown by the green and white dashed lines respectively. The V- shaped transport futures inside the diamond indicated by black dashed lines could be due to a contribution from CAST.

the strong coupling regime. The conductance features of elastic tunnelling are shown by green dashed lines. The transport lines shown by white dashed lines parallel to the plunger gate voltages within the left diamond contribute to the inelastic cotunneling process.

5.6.2 Cotunneling assisted sequential tunneling

From figure 5.9 another transport feature appears within the diamond, as shown by red lines parallel to the light blue sequential tunneling lines. Those transport lines can be explained by cotunneling assisted sequential tunneling (CAST) as illustrated in figure 5.11 [139]. According to figure 5.11a, a ground singlet state is

assumed to occupied by a spin up electron, which restricts the second electron with spin up to tunneling into the ground state. If the source drain bias is larger than the singlet-triplet splitting energy, the second electron can tunnel in to the dot via excited triplet states as illustrated in figure 5.11b.

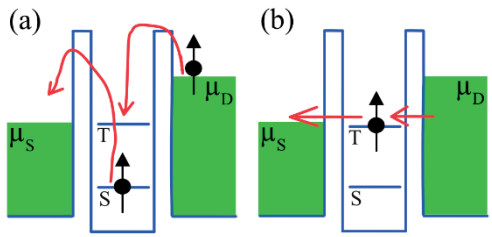


Figure 5.11: Schematic energy diagrams show the CAST features. (a) One spin up electron tunnels into the triplet state of the dot from drain. (b) The electron on the triplet state tunnels out to source.

Since the bias energy is larger than the singlet triplet exchange energy of the dot, it becomes energetically possible for the second electron to tunnel sequentially through the triplet state. Simultanously, the first electron on the singlet state tunnel out from the ground state of the dot to left lead, and CAST can contribute to the transport.The transport feature shown by the black dashed lines within the left diamond in figure 5.10 is likely contributions from CAST. However, in order to support that, further temperature or magnetic field dependent measurements need to be done.

5.7 Low-temperature electron transport in InP-InAs core-shell nanowires

Growth of nanowires in the axial direction provides complex heterostructures, like core-shell nanowires. Core-shell nanowires have potential applications in optoelectronics and quantum devices. For instance, due to the presence of built-in strains, core-shell nanowires can have high carrier mobility, which is promising for high speed transistors [140]. Core-shell nanowires also have been considered one of the suitable materials to investigate Majorana bound states [141]. Studying transport properties of core-shell nanowires, therefore, is of current interest. In this section, we describe low-temperature transport measurements with devices made of InP-InAs core-shell nanowires. The core-shell nanowires are grown by MOVPE with

selective area growth method. Figure 5.12a depicts grown core-shell nanowires. Investigations with SEM and TEM of the grown core-shell nanowires and core nanowires without any shell show that the entire nanowire has a hexagonal InP core and a triangular shell where three pockets of InAs are located at the three corners as shown with a schematic inset of figure 5.12b. To study transport properties of the nanowires, devices with multiple contacts (figure 5.13b) are fabricated on a n-doped silicon substrate covered with a 130 nm thick SiO_2 which is used as back gates in combination with Ti/Au metal electrodes deposited on the bottom of the wafer.

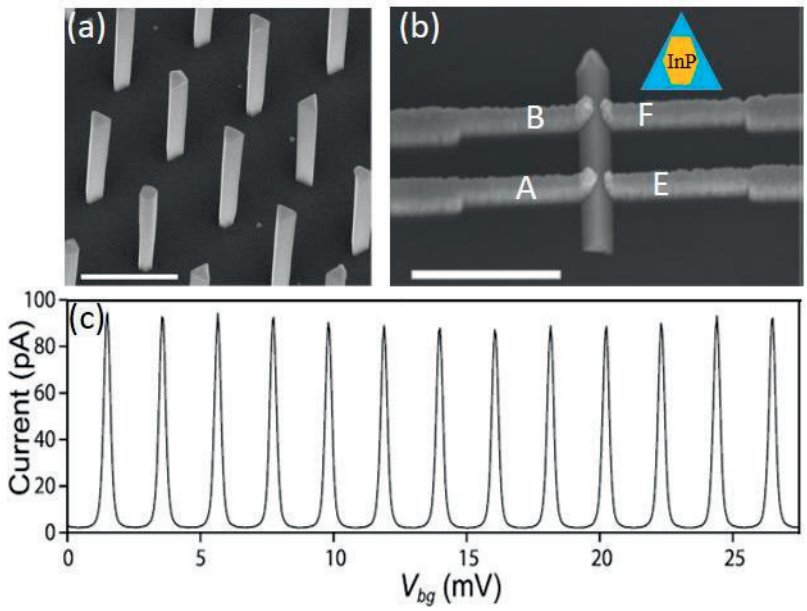


Figure 5.12: (a) SEM image of InP-InAs core-shell nanowires. (b) Multiple source-drain contact devices made of InP-InAs core-shell nanowires. (C) Measured current as a function of back gate voltages at 22 μV bias applied to the contacts EF, at T = 14 mK.

The measurements are performed in a dilution fridge, at a base temperature of 14 mK. Figure 5.12c displays the measured current from contacts EF as a function of back gate voltages at V_{sd} = 22 μV. Note that, the contacts which are not involved in the measurements are kept floating. Regular Coulomb blockade peaks with equal spacing can be seen. The extracted back gate capacitance from the peak spacing is $C_g = e/\Delta V_{bg} = 80\ aF$. To further understand the origin of the Coulomb blockade effect, the differential conductance of the device is measured as a function of back gate voltage and $V_{sd.}$ One of the charge stability diagrams measured for contacts E and F are presented in figure 5.13. From the height of the diamond in the source-drain bias voltage, a charging energy of $E_c \approx 250\ \mu eV$ is estimated. The same measurements with other pairs of contacts, A-B, A-E, and B-E give almost similar results with the same charging energies and back gate coupling. These results

confirm the existence of a quantum structure which extend over the entire length of the nanowire. It is likely due to the large band offset between InP and InAs, a quantum dot structure is defined through the InAs shell in the core-shell NW. An

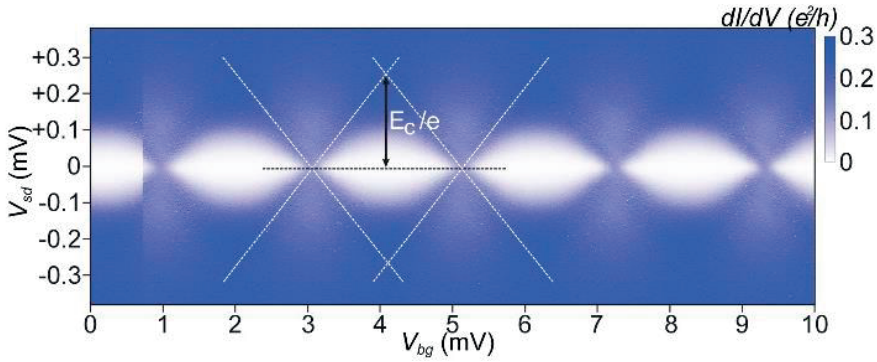


Figure 5.13: Charge stability diagram measured from contacts E and F. Differential conductance is plotted as a function of source-drain and back gate voltages.

analytical model is used to verify our conclusions. Following the reference [142], assuming an infinite plate, the back-gate capacitance is calculated using the equation:

$$C_g = 2\pi L\varepsilon_0\varepsilon_e / \operatorname{acosh}\left(\frac{t_{ox+r}}{r}\right), \tag{5.5}$$

where L = 1.357 µm, is the NW length, $\varepsilon_e = 1.95$ is the effective relative permittivity of oxide and vacuum, $r = 78\ nm$, is the radius of the wire, t_{ox} is the oxide thickness. Equation (5.5) yields $\frac{C_g}{L} = 69\ aF/\mu m$ which is in good agreement with the extracted values of $\frac{C_g}{L} = 59\ aF/\mu m$ from the measurements. This strongly supports our conclusion that the origin of the Coulomb blockade is a quantum structure formed over the entire NW.

5.8 Conclusions

In summary, we developed side gate techniques to define single quantum dots in InSb nanowires. Transport measurements were performed with quantum dots operating in strong and weak coupling regions. We observed higher order co-tunnelling transport futures from measurements with the dots in strong coupling regions. Our results show that tunable quantum dots can be formed in InSb nanowire by using side gates. Considering aforementioned advantages of side gates over other

gating techniques, InSb nanowire quantum dots defined with side gates are promising for applications in spin-based quantum computations.

We also studied low temperature electron transport properties of InP-InAs core-shell nanowires and observed quantum blockade effect. Measurements for charge stability diagrams with different contact configurations yields almost similar gate capacitance and charging energies, regardless of the space between the contacts indicating emergence of a quantum structures extended over the entire length of nanowires.

Chapter 6
Electron transports in double quantum dots

6.1 Introduction

In the previous chapter, we studied electron transport in single quantum dots. As has been proved by numerous experimental works, a single quantum dot shows discrete energy levels and spin filling following Hund's or Heisenberg's exchange rules and often the single quantum dot is referred to as an artificial atom. Moreover, a double quantum dot can also be realized in semiconductor quantum dot systems by dividing a large quantum dot into two dots in series, separated by a tunnelling barrier which is formed in most case by using a local gate. Due to its large gate tunability, a semiconductor double quantum dot system provides an excellent platform to study two level quantum systems, spin transport, and so on [143].

A theoretical background of transport in a double quantum dot and our experimental results based on electron transports in InSb and InAs nanowire double quantum dots defined by side gates will be discussed in this chapter.

6.2 Transport in double quantum dots

As we discussed in the previous chapter, electron transport through a single dot is mainly determined by two energy scales, the Coulomb repulsion between electrons on the dot and leads which is purely classical and gives rise the Coulomb blockade effect, and the other important energy scale is the quantum confinement effect which is quantum mechanical and responsible for discrete energy levels in the dot. Based on the single quantum dot physics, we will extend our discussion to electron transport through a double quantum dot where two dots can be coupled either in series or parallel. For the underlying physics of parallel double dots we refer the related work in Ref. [144-146]. Following the Ref. [143], we will discuss transport through a double quantum dots (DQDs) where two dots are coupled in series. The typical equivalent circuit of a double quantum dot is given in figure. 6.1a, where

two dots are tunnel-coupled to each other in series by a tunnel barrier with a capacitance of C_m that describes the interaction between the dots. Electron occupation on each single dot is controlled by two local gates with capacitances of C_{g1} and C_{g2} respectively. The first dot is capacitively coupled to the source while the second dot is capacitively coupled to the drain through the tunnel barriers.

The Hamiltonian of a double quantum dot can be described as:

$$H_{DQD} = \frac{E_{C1}}{2}N(N-1) - \frac{NE_{C1}+ME_M}{e}\left(C_{g1}V_{g1} + C_sV_s\right) + \sum_{i\sigma} N_{i\sigma}\epsilon_{i\sigma} + \frac{E_{c2}}{2}M(M-1) - \frac{ME_{c2}+NE_M}{e}\left(C_{g2}V_{g2} + C_dV_d\right) + \sum_{j,\sigma} M_{j\sigma}\epsilon_{j\sigma} + E_MNM + \sum_{i,j,\sigma} t_{ij\sigma}\left(C_{i\sigma}^{\dagger}C_{i\sigma} + h.c\right). \quad (6.1)$$

Where N and M are the occupations of the first and the second dot, the tunnel elements $t_{ij\sigma}$ couple states i in the first dot to the state j in the second dot. There are also additional terms to the full Hamiltonian related to the lead and dot-lead coupling which are identical to their single dot counterparts. Considering the capacitance of each single dot to be $C_{1(2)}$, the single dot charging energies can be described by:

$$E_{C1(2)} = \frac{e^2}{C_{1(2)}}\left(1 - \frac{C_m^2}{C_1C_2}\right)^{-1} \quad (6.2)$$

There is also one more new energy term known as the mutual charging energy which refers to the additional energy needed to add one electron to the first dot due to Coulomb repulsion from electrons on the second dot. The mutual charging energy is given by:

$$E_m = \frac{e^2}{C_m}\left(\frac{C_1C_2}{C_m^2} - 1\right)^{-1} \quad (6.3)$$

In the following discussions, we will assume that the cross-capacitances are zero which means that there is no coupling between the gate of first dot (gate 1) and the second dot (dot 2). In fact, conditions for localization of electrons on a single dot are also true for DQDs. Mixing of states on each dot would emerge as the tunnelling element $t_{ij\sigma}$ becomes comparable with the single dot level spacing energy Δ. Therefore, for the dots to be well separated, the tunnel element $t_{ij\sigma}$ must be smaller than the level spacing energy Δ.

We will start our discussions with the transport via the ground state of the dot where the source-drain bias is zero. Without losing the generality, as we did for single dots, we will only consider the classical terms of the Hamiltonian in equation (6.1) by

neglecting the purely quantum terms that is the last term of each line. We can write the classical energy of dots U (N,M) as:

$$U(N,M) = \frac{1}{2}E_{C1}\left(N - N_g\right)^2 + \frac{1}{2}E_{C2}\left(N - M_g\right)^2 + E_m\left(N - N_g\right)\left(M - M_g\right), \quad (6.4)$$

where $N_g = \frac{C_{g1}V_{g1}}{e} + K_1$, $M_g = \frac{C_{g2}V_{g2}}{e} + K_2$ and $K_{1(2)} = \frac{1-\frac{E_m}{E_{C1(2)}}}{2\left(1-\frac{E_m^2}{E_{C1}E_{C2}}\right)}$. (N, M) = (N_g, M_g) denote the ground state charge configurations for every set of gate voltages at which the corresponding $N_g and\ M_g$ are integers. The key factor here is the mutual charging energy E_M which describes interactions of the dots. Based on the E_M, or equivalently the inter-dot capacitance C_M, we can identify three different transport regimes. When, C_m= 0, the dots can be considered as two completely isolated dots where the energy of each dot is independent of each other. Adding one electron to the first dot by V_{gn} is not affected by adding one electron to the second dot by V_{gm}. Maps of the space $V_{gn} - V_{gm}$ yields a rectangular pattern as shown in figure 6.1b. Here, vertical and horizontal lines refer to changes in the number of electrons on dot 1 and dot 2, respectively. Now we turn our attention to completely opposite case, where $C_m\ is$ the dominant capacitance $\frac{C_m}{C_{1(2)}} \to 1$, and the system acts like a single dot with a total charge of $N_1 + N_2$, where the capacitance of each single dot $C_{1(2)}$ is defined as: $C_1 = C_S + C_{gn} + C_m$ and $C_2 = C_d + C_{gm} + C_m$. The charge stability diagram as a function of V_{gn} and V_{gm} for this regime is given in figure 6.1c.

At finite C_m, the charge stability diagram will turn into honeycomb patterns as illustrated in figure 6.1d. The gate capacitances determine the size of each honeycomb pattern according to:

$$\Delta V_{gn} = \frac{|e|}{C_{g\mathrm{n}}} \quad (6.5)$$

$$\Delta V_{gm} = \frac{|e|}{C_{g\mathrm{m}}} \quad (6.6)$$

Capacitive coupling between the dots yields a shift in energy at the crossing points of charge transition borders, which is equal to E_m. The shift in gate voltage is defined by:

$$\Delta V_{gn}^M = \Delta V_{gn}\frac{C_m}{C_2} \quad (6.7)$$

$$\Delta V_{gm}^M = \Delta V_{gm}\frac{C_m}{C_1} \quad (6.8)$$

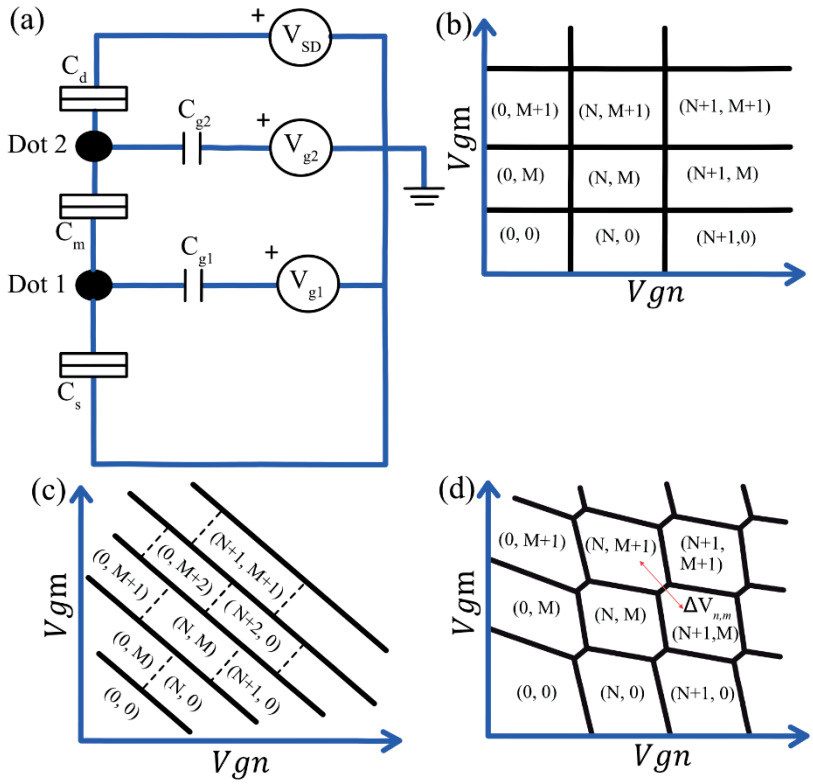


Figure 6.1: (a) A circuit schematic of a double dot. The double boxes represent the capacitor and resistor connected in parallel. (b), (c), (d) Charge stability diagrams of a double dot at low bias in three distinct transport regimes: weak, strong and intermediate coupling between the dots.

The corners of the honeycomb pattern are called triple points where three charge states are degenerate. At the triple point, transport takes place allowing current to flow through the double dot. Experimentally, the current is often observed along the honeycomb edges due to contributions of cotunneling events. Various charge configurations involved in the transport will be discussed in the experimental part of the thesis.

At a finite bias each triple point develops into a triangular shaped region as shown in figure 6.2a. If a negative bias voltage V_{SD} is applied to the source while the drain is kept grounded, the condition which determines the boundary of the triangle is $-|e|V \geq \mu_1 \geq \mu_2 \geq 0$. μ_1 and μ_2 are chemical potentials of the dots which refer to the energy needed to add one electron to either of the dots while the other dot is
occupied. For example, $\mu_1(n+1, m) = U(n+1, m) - U(n, m)$ and$\mu_2(n, m+1) = U(n, m+1) - U(n, m)$. The dimensions of the triangles are defined by the applied bias voltage as follows:

$$V_{sd} = \alpha_{gn}\delta V_{gn} \tag{6.9}$$

$$V_{sd} = \alpha_{gm}\delta V_{gm} \tag{6.10}$$

Elastic transport through the ground states of the dots only takes place at the lower right edge of the triangle, which is usually called the base line as shown with a red solid line in figure 6.2a. As $|eV| > \Delta$, we begin to see quantized energy levels in the dot within the triangle. In this case, excited states can contribute to transport, this is shown by additional lines of high currents parallel to the base line. Inside the triangle, the transport is inelastic leading a reduced current compare with the base line.

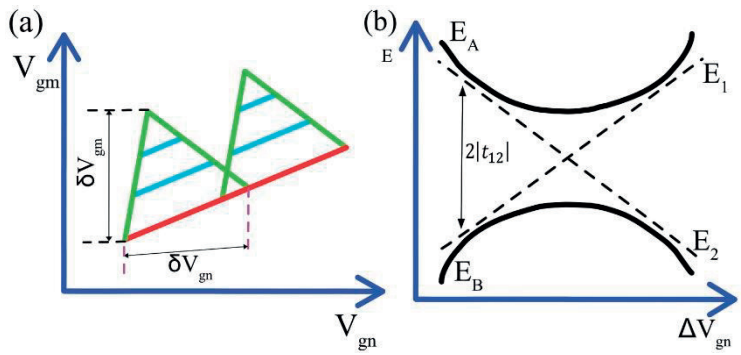


Figure 6.2: (a) Charge diagram as a function of gates Vgn and Vgm. At finite bias, triple pointes develop to triangles. Red solid line denotes the transport through ground state of the dots. Corresponding transports via excited states are shown by light blue lines within the triangle. (b) Avoided crossing as a function of detuning in a two-level system.

At last, we will consider the effects of the tunnel coupling term $t_{ij\sigma}$ in equation (6.1) on the transport in a double quantum dot system. This term has impact on the energy levels in the dots at the vicinity of triple points and the short segment connecting them. In this region, the double dot can be treated as a two-level system with the ground states of $(n, m+1)$ and $(n+1, m)$. Detuning between them can be controlled by a gate voltage $\Delta V_{n,m}$ along the diagonal line as shown in figure 6.1d. Introducing the tunnel coupling gives rise to an avoided crossing between these levels as illustrated in figure 6.2b. The energies of avoided crossing states can be expressed in terms of the tunnel matrix elements $\left|t_{1(2),2(1)}\right|$ as

$$E_B = E_M - \sqrt{\frac{1}{4}(\Delta E)^2 + |t_{12}|^2}, \tag{6.11}$$

$$E_A = E_M + \sqrt{\frac{1}{4}(\Delta E)^2 + |t_{12}|^2}, \tag{6.12}$$

Where $E_M = \frac{1}{2}(E_1 + E_2)\ and\ \Delta E = E_1 - E_2$. E_1, E_2 denote the energies of decoupled quantum dots. The normalized energy difference is $\Delta E^* = E_A - E_B = \sqrt{(\Delta E)^2 + 4|t_{12}|^2}$. It is worth pointing out that the smaller the ΔE the stronger the effect of coupling. When $\Delta E = 0$, we have an anti-crossing with $\Delta E^* = 2|t_{12}|$ which is the minimum bonding-antibonding energy difference. In the case of larger ΔE, the eigenenergies of a coupled double dot (E_A, E_B) approach the eigenenergies of decoupled dots, and the eigenstates of the $E_1\ and\ E_2$ are no longer stationary states. If at a time t the system is in the state $|\varphi_1\rangle$, the probability $P_{12}(t)$ of finding it in the state $|\varphi_2\rangle\ at\ the$ same time t is:

$$P_{12}(t) = |\langle\varphi_2|\psi\ (t)\rangle|^2$$

$$= \frac{4|t_{12}|^2}{4|t_{12}|^2+\Delta E^2} sin^2\left[\sqrt{(\Delta E)^2 + 4|t_{12}|^2}\ \ \frac{t}{2\hbar}\right], \qquad (6.13)$$

The equation (6.13) describes a coherent charge oscillation in the double dot system.

6.3 Experimental results and discussions

In this section, we will discuss low temperature transport measurements on double quantum dots formed in InSb and InAs nanowires. First, we start measurements on InSb nanowire double quantum dot devices. SEM images of the measured device is given in figure 5.7a. The device consists of 9 local side gates with widths of 28-30 nm and pitch of 140-150 nm. The gates G1-G5 are located 30 nm, and the gates G6-G9 are 50 nm away from the nanowire. All side gates show threshold voltages of between -2V to -5V except gate G8 which has a leakage current to the back gate. The gates G3, G4, G5, G6 and G7 are used for double dot measurements. Note that the other side gates (except G8) which are not involved to the measurements are grounded during the measurement. The two outermost potential barriers are created by applying negative voltages to gates G3 and G5 and the inter dot coupling is controlled by gate G4. G6 and G7 are used as plunger gates to change the electron occupation on each dot respectively. In order to illuminate the possible effect of Schottky barriers which may be present at the nanowire contact interface, we measured the current I_D as a function of source drain bias V_{DS} at an applied positive back gate voltage V_{BG}. At a back-gate value of V_{BG}= 4V, we see a linear I-V curve as presented in figure 6.3a indicating Ohmic-like contact properties at this value of the back gate. Therefore, we set the back gate to V_{BG}= 4V for all measurements. All the measurements are performed at an electron temperature of around 100 mK.

Figure 6.3b shows a charge stability diagram of a double dot where the drain current I_D is measured as a function of gate voltages V_{G7} and V_{G6} at a small source drain

bias of V_{SD}= 25μV. Applied static gate voltages are V_{G3} = -3.3 V, V_{G5} = -2.4 V and V_{G4} = -1.65 V.

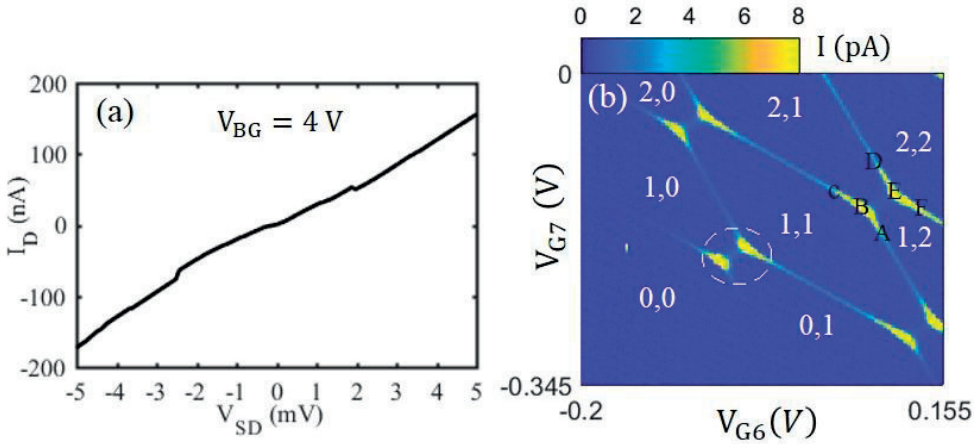


Figure 6.3: (a) Current I_D measured as a function of source-drain bias voltages at V_{BG} = 4 V. (b) Charge stability diagram of a quantum dot as a function of plunger gate voltages V_{G6} and V_{G7} in the weak coupling regime at low bias of 25 μV. White numbers in the diagram refer to electron numbers on left and right dot.

Well-defined honeycomb patterns with localization of electrons separately in each dot indicates that the double dot is in the weak interdot coupling region. White numbers in the charge diagram refer to effective electron numbers in each dot. In the weak coupling region of a double dot, current flows at triple points as shown with letters B and E in the charge diagram. This is due to sequential tunneling where the chemical potentials of the dot align with the chemical potentials of source and drain, as illustrated with B and E in the energy diagrams of figure 6.4. At the triple point B, an electron is transfered from drain to source and the corresponding charge configurations can be described as $(1,1) \rightarrow (1,2) \rightarrow (2,1) \rightarrow (1,1)$. For the degeneracy point E the cycle is $(2,2) \rightarrow (1,2) \rightarrow (2,1) \rightarrow (2,2)$. This can be explained as resonant tunneling of holes from the source contact to the drain contact. The very small current on the boundary of the honeycombs is contributed by a co-tunneling process. More precisely, at points A and D, the chemical potentials of the right dot align with the chemical potentials of source-drain, while the chemical potential of the left dot is misaligned. In contrast, at points C and F, the chemical potentials of the left dot are aligned with source-drain, but the chemical potential in the right dot is misaligned. From the whole size of a honeycomb, the extracted gate capacitance for G6 and G7 are $C_{G6} = 1aF$, and $C_{G7} = 1{,}25aF$.

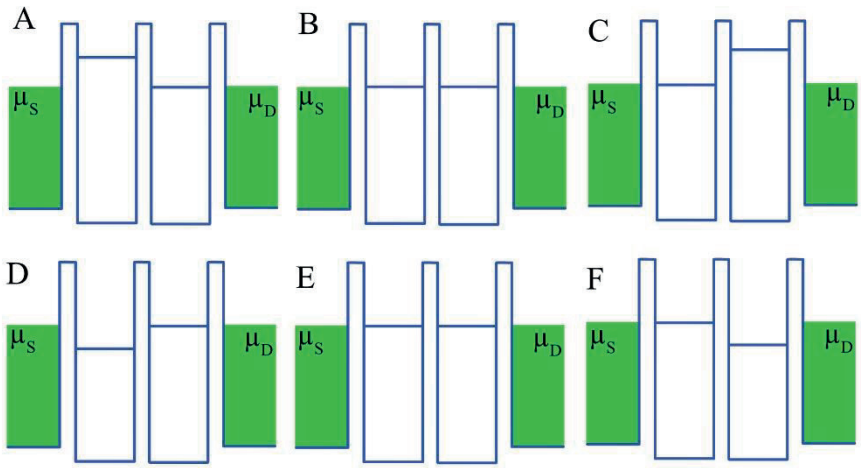


Figure 6.4: Alignment of double dot energy levels with respect to the fermi level of source drain at low bias. A-F correspond to transport features shown with letters A-F in the charge diagram in figure 6.3.

At a finite bias, the triple points of the honeycombs indicated by the white circle in figure 6.3b extend into the triangles shown in figure 6.5. Here the drain current I_D is measured as a function of V_{G7} and V_{G6} at a finite bias of V_{SD} = 3mV. Within the triangle, transport is allowed but anywhere else in outside of the triangle is a Coulomb blockade region, and no current flows through the dots.

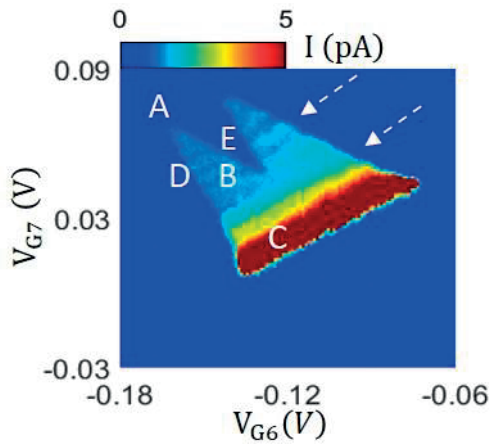


Figure 6.5: Charge stability diagram of a double dot at V_{SD} = 3 mV. The current is plotted as a function of V_{G6} and V_{G7}. At a finite bias triple points in figure 6.3 evolve into triangles.

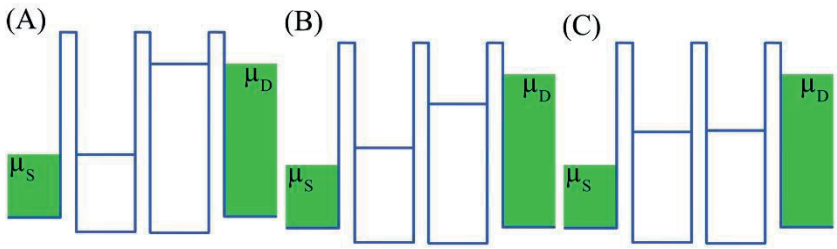


Figure 6.6: Energy diagrams of the double quantum dot show the energy state of the dots respect to source- drain chemical potentials, corresponding to A, B, C in figure 6.5.

At point C in figure 6.5 and 6.6, resonate transport through the double dot takes place where the ground states of both dots align to each other and lay between the bias windows. Along the base line, both dot levels move up or down with the same energy with respect to the source and drain chemical potentials. Point D (E) corresponds to detuned configurations, where the states in each dot are no longer matched to each other. The right (left) dot state aligns with the drain (source) chemical potential instead. At point B the dot states are detuned and are inside the bias window. At point A, the left dot state is aligned with the source potential and the right dot state is aligned with the drain potential. Transport through the excited states can also be observed in the charge diagram, as indicated by the dashed white arrows. Note that, energy diagrams corresponding to D (E) are not presented in figure 6.6, considering the cross capacitances.

Using equation (6.9) and (6.10), the extracted gate level arms are $\alpha_7 = \frac{V_{SD}}{\Delta V_{G7}} = 0.047, \alpha_6 = \frac{V_{SD}}{\Delta V_{G6}} = 0.042$, and the corresponding total capacitances of the dots are $C_6 = \frac{C_{G6}}{\alpha_6} = 23{,}8\ aF, C_7 = \frac{C_{G7}}{\alpha_7} = 26{,}6\ aF$. Based on these values, the estimated charging energies for each single dot are $E_{C,7} = \frac{e^2}{C_7} = 6mV$, $E_{C,6} = \frac{e^2}{C_6} = 6{,}7mV$. The mutual capacitance between the two dots is 5.3 aF which is consistent with a double dot in the weak inter-dot coupling regime [143].

6.4 Pauli spin blockade

Under certain configurations of a double quantum dot system, the current transport can be governed by the spin states of the system in a few electron double quantum dots, resulting in appearance of current rectification known as Pauli spin blockade [147].

Figure 6.7 shows current rectification due to Pauli spin blockade effect, the data was obtained from the same device shown in figure 5.7a. Figure 6.7 (a) presents the measured source drain current I_{SD} as a function of V_{G7} and V_{G6} at a finite bias of V_{DS} = - 3mV. The static gate voltages used for this measurement are V_{G3} = -3.83V, V_{G5} = -2.4 V, and V_{G4} = -2.3V. The whole triangle indicates sequential tunneling transport through the dots. High currents at the base line represent resonant transport via singlet states in the double quantum dot system. Within the triangle, the chemical potentials of the dots are detuned as discussed in the previous chapter. As a result, inelastic transport takes place and a smaller current than the base line is observed.

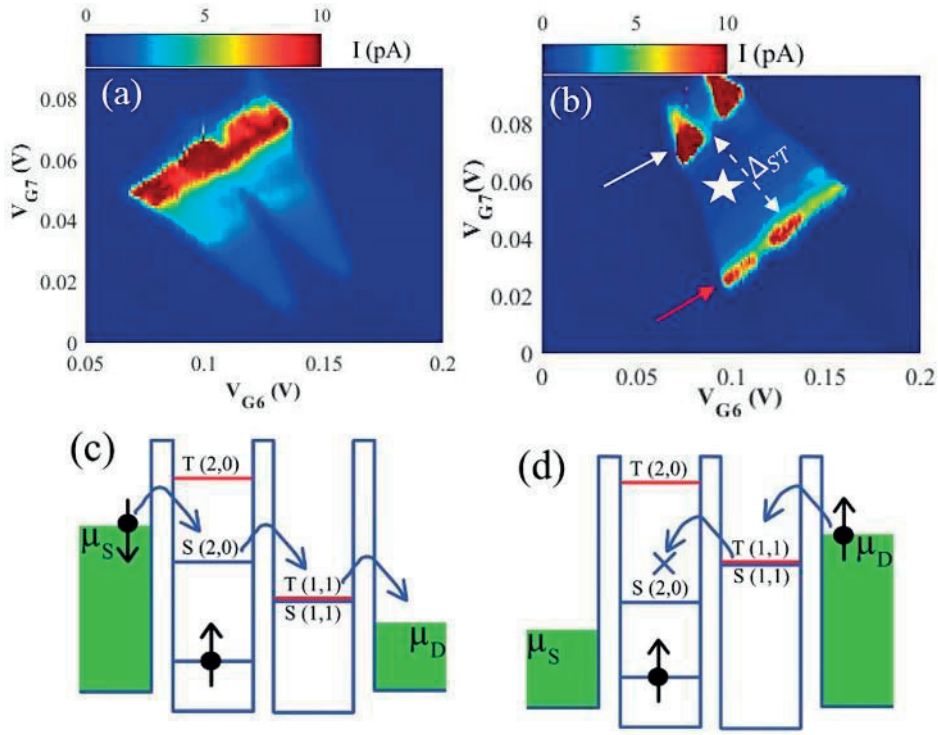


Figure 6.7: (a) The measured current I as a function of plunger gate voltages V_{G6} and V_{G7} at - 3mV bias. (b) The same measurements but with reversed bias of 3 mV. Current suppression occurs within the triangle shown by the black star. (c) and (d) dot energy level diagrams corresponding to (a) and (b), respectively.

However, the measurements with a reversed bias of V_{SD} = 3 mV clearly show current rectification inside the triangle as marked with the white star in figure 6.7. The current rectification can be explained as follows. Without losing generality, we consider unpaired spins on the dots, treating the rest of electrons as background charges. We further assume one electron with spin up on the left dot. When a negative bias is applied to the source, only electron with spin down is allowed to

tunnel into the left dot, forming a singlet S (2, 0) state. The electron can then tunnel to the right dot via virtual states to form a singlet S (1, 1) state. Tunneling out of the electron from the right dot to the states in the drain results in a flow of currents through the dots, without any current rectification. The energy diagram of a double dot which describes the process is presented in figure 6.7c. When a positive bias is applied, one electron with either up or down spin can tunnel into the right dot from the drain. Tunneling of one electron with spin down to the right dot from drain forms a S (1, 1) singlet state. Since the transport from S (1, 1) to S (0, 2) is allowed, no current rectification will occur in this case. However, as illustrated in figure 6.7d, if a spin up electron tunnels into the right dot, it forms T (1, 1) states. According to the Pauli exclusion principle, transport from T (1, 1) to S (0, 2) is prohibited. The energy of T (0, 2) states is high for tunneling of an electron to the left dot. If the T (1, 1) state is below the chemical potential of the drain, the electron stays on the left dot, and the current is blocked. If the energy levels of the two dots are detuned in such a way that the T (0, 2) state is lowered to align with the S (1, 1) and T (1, 1) states, the PSB can be lifted. In this configuration an electron may tunnel from source to drain via T (1, 1) - T (0, 2) states. The detuning parameter Δ can be determined by the difference in the energy states of T (1, 1) and S (0, 2), which is called singlet-triplet splitting energy as shown with the purple arrow in figure 6.7b. Moreover, at sufficiently large bias, T (1, 1) will align with T (0, 2) so that electrons with either spin can tunnel from source to drain, which leads to lifting of the PSB. This gives high current lines parallel to the base line which is shown by the white arrow in figure6.7b.

We observe a leakage current running along the base line indicated by the red arrow. A possible reason for this leakage current may be a contribution from the mixing of the S (1, 1) and the T (1, 1) states as a consequence of spin relaxation as reported in many experimental studies with double quantum dots [148,149]. The hyperfine interaction and spin orbit interaction are often reported as the main spin relaxation mechanism in quantum dot systems [150]. However, to identify each of their contributions to the leakage current, further detailed measurements with magnetic fields need to be performed.

6.4 Evoluation of singlet-triplet states in magnetic fields

Exploring transport features in the PSB region with applied external magnetic fields provide valuable information about effective g-factor of the system, and the spin-orbit interaction (SOI) energy. The direction of the SOI also can be identified if a vector magnetic field is applied in different orientations with respect to the nanowire axis and the substrate plane. In this section, we demonstrate the evoluation of energy states in PSB region as a function of magnetic fields from measurements with

double quantum dots formed in InAs nanowires. A SEM image of the measured device is presented in figure 6.8a.

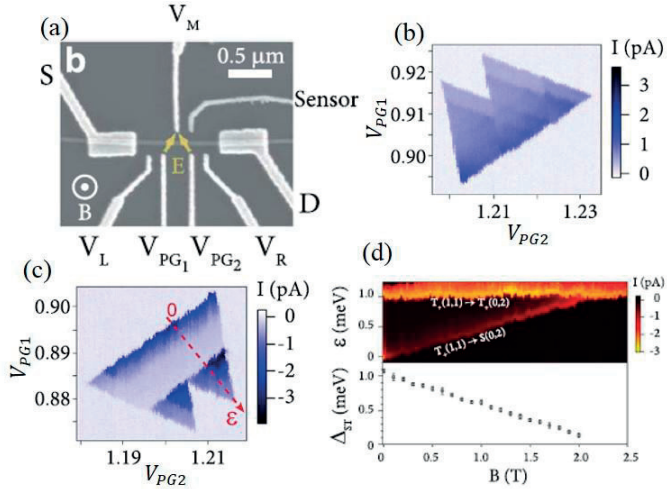


Figure 6.8: (a) A SEM image of the InAs nanowire double quantum dot device. (b) Current I measured as a function of gate voltages V_{PG1} and V_{PG2} at V_{SD} = 2 mV. (c) Current measured as a function of gate voltages V_{PG1} and V_{PG2}, V_{SD} = -2 mV. (d) Upper panel, evolution of the singlet-triplet states as a function of detuning energy and magnetic field. Lower panel, singlet-triplet splitting energy as a function of magnetic field.

Figure 6.8b displays the measured current I as a function of the plunger gate voltages V_{PG1} and V_{PG2} at V_{SD} = 2 mV. The data shows a full sized triangle, no current suppression is observed inside the triangle. Figure 6.8c displays the same measurement at a polarity bias voltage of V_{SD} = -2 mV. Current rectification within the triangle can be seen, indicating the presence of the PSB. We focused on investigating the effect of magnetic fields on the energy states in the PSB. The measured current modulated with the detuning energy and a magnetic field oriented perpendicular to the nanowires is given in the upper part of figure 6.8d. In the finite magnetic field, the spin degeneracy is lifted, resulting in triplet states T (1, 1) and T (0, 2) splitting to T_0 (1, 1), T_- (1,1), T_+ (1,1) and T_0 (0,2), T_- (0,2), T_+ (0,2) states due to Zeeman splitting. The singlet-triplet splitting energy Δ_{ST} is determined by the energy difference between the S (0, 2) and T_+ (0, 2) states and has a smaller value than for the zero magnetic field case. From the equation $\Delta_{ST}(B) = \Delta_{ST}(0) - S_z|g^*|\mu_B B$ with S_z is 1,0,-1, μ_B is the Bohr magneton, g^* is the effective g-factor, a linear decrease of Δ_{ST} with increasing magnetic field can be expected as seen in the lower panel of figure 6.7d. From the linear data fit, an effective g-factor value of $|g^*| = 7.9 \pm 0.3$ is extracted, which is in good agreement with previous reports on InAs nanowires [151,152].

Now we turn our attention to the upper panel of figure 6.8d. With increasing B, the high current line $T_+(1,1) \rightarrow T_+(0,2)$ does not change while the base current line $T_+(1,1) \rightarrow S(0,2)$ shifts towards a higher detuning energy ε. Beyond the magnetic field value of B = 2 T, these two states merge, showing the absence of a spin-orbit gap Δ_{SO}.The appearance of Δ_{SO}, as reported previously, depends on orientations of the applied external magnetic fields with respect to the direction of the spin-orbit field B_{SO} in the NWs. Nadj-Perge et al. [100] have reported that Δ_{SO} disappears when the external magnetic field is aligned with the B_{SO} in InSb nanowires. Maybe, the absence of Δ_{SO} in our devices is due to the B_{SO} is oriented highly out of the sample plane resulting from the electric field applied by the side gates.

6.5 Conclusions and outlook

Tuneable double quantum dots where two dots coupled in serial are successfully formed in InAs and InSb nanowires using side gates. From measurements with fabricated devices, we observe Pauli spin blockade effect. Magnetic field dependence measurements in PSB region of double quantum dots formed in InAs nanowires show absence of anti-crossing between the singlet-triplet states. This could be interpreted with device designs where transverse electric field generated by side gates lead to spin-orbit field B_{SO} strongly oriented out of sample plane. In future work, using combined gate architectures to manipulate orientations of electric fields applied to the devices to electrically control orientations of B_{SO} in nanowire quantum dots. Further, integrating with quantum point contacts for charge sensing measurements allows to detect last electrons in the dots to study spin states in two level systems.

Bibliography

[1] John Bardeen, Walter Brattain and Willian Schockley received the 1956 Nobel Prize in Physics, www.nobel.se/physics/laureates/1956/

[2] R. H. Dennard, F.H. Gaensslen, V. L. Rideout, E. Bassous, A.R. LeBlanc, *Design of ion-implanted MOSFET's with very small physical dimensions*, IEEE Journal of Solid-State Circuits. **9**, 256, (1974).

[3] Intel Corporation, the evolution of a revolution, http://download.intel.com/pressroom/kits/IntelProcessorHistory.pdf

[4] N. Z. Haron, and S. Hamdioui, *Why is CMOS scaling coming to an END?* 3rd International Design and Test Workshop, (2008), IEEE.

[5] J. A. del Alamo, *Nanometre-scale electronics with III-V compound semiconductors*, Nature, **479,** 317, (2011).

[6] J. Cartwright, *Intel enters the third dimensions*, Nature, doi:10.1038/news, 2011.

[7] I. Zutic, J. Fabian, and S. Das Sarma, *Spintronics: Fundamentals and applications,* ReV. Mod. Phys. **76,** 323, (2004).

[8] A. Montanaro, *Quantum algorithms: an overview,* Npj Quantum Information, **2**, 15023, (2016).

[9] M. H. Holzscheiter, *Ion-traped quantum computation*, Los Alamos Science **27**, 265, (2002).

[10] L. Childress, R, Hanson, *Diamond NV centres for quantum computing and quantum*, Cambride Core, **38**, 134, (2013).

[11] M. H. Devoret, R. J. Schoelkopf, *Superconducting circuits for quantum information: An Outlook,* Science, **339**, 1169, (2013).

[12] M. Fernando Gonzalez-Zalba, *Solid state qubits*, arxiv.org/abs/1801.06722, (2018).

[13] A. Stern, N. H. Linder, *Topological Quantum Computation—From Basic Concepts to First Experiments*, Science, **339**, 1179, (2013).

[14] D. Loss and D. Divincenzo, *Quantum computation with quantum dots*, Phys. Rev. A. **57**, 120, (1998).

[15] J. M. Kikkawa, I. P. Smorchkova, N. Samarth, and D. D. Awschalom, *Room-Temperature Spin Memory in Two-Dimensional Electron Gases*, Science **277**, 1284, (1997).

[16] J. M. Kikkawa and D. D. Awschalom, *Resonant Spin Amplification in n-type GaAs*, Phys. Rev. Lett. **80**, 4313, (1998).

[17] D. D.Awschalom and J. M. Kikkawa, *Electron Spin and Optical Coherence in Semiconductors*, Phys. Today. **52**, 33, (1999).

[18] J. A. Gupta, R. Knobel, N. Samarth, and D. D. Awschalom, *Ultrafast Manipulation of Electron Spin Coherence*, Science **292**, 2458, (2001).

[19] X. D. Hu, S. D. Sarma, *Charge-Fluctuation-Induced Dephasing of Exchange-Coupled Spin Qubits,* Phys. Rev. Lett. **96**, 100501, (2006).

[20] A. V. Khaetskii, and Yu. V. Nazorov, *Spin relaxation in semiconductor quantum dots*, *Phys*. Rev. B. **61**, 12639, (2000).

[21] D. Stepanenko and N. E. Bonesteel, *Spin-orbit coupling and time-reversal symmetry in quantum gates,* Phys. Rev. B. **68**, 115306, (2003).

[22] S. Debald and C. Emary, *Spin-orbit-driven coherent oscillations in a few-electron quantum dot,* Phys. Rev. Lett. **94**, 226803, (2005).

[23] C. Flindt, A. S. Sorensen, K. Flensberg, *Spin-orbit mediated control of spin qubits*, Phys.Rev. Lett. **97**, 240501, (2006).

[24] Pawel Wojcik, Andrea Bertoni, and Guido Goldoni, *Tuning Rashba spin-orbit coupling in homogeneous semiconductor nanowires*, Phys. Rev. B. **97**, 165401, (2018).

[25] V. T. Lahtinen, J. K. Pachos, *A short introduction to topological quantum computation*, Scipost. Phys. **3**, 021, (2017).

[26] L. Fu, C. L. Kane, *Superconducting Proximity Effect and Majorana Fermions at the Surface of a Topological Insulator*, Phys. Rev. Lett. **100**, 096407 (2008).

[27] J. D. Sau, R. M. Lutchyn, S. Tewari and S. Das Sarma, *Generic New Platform for Topological Quantum Computation Using Semiconductor Heterostructures*, Phys. Rev. Lett. **104**, 040502 (2010).

[28] J. Alicea, *Majorana fermions in a tunable semiconductor device*, Phys. Rev. B **81**, 125318 (2010).

[29] T. P. Choy, J. M. Edge, A. R. Akhmerov and C.W. J. Beenakker, *Majorana fermions emerging from magnetic nanoparticles on a superconductor without spin-orbit coupling*, Phys.Rev. B. **84**, 195442 (2011).

[30] J. Klinovaja, P. Stano, A. Yazdani and D. Loss, *Topological Superconductivity and Majorana Fermions in RKKY Systems*, Phys. Rev. Lett. **111**, 186805 (2013).

[31] A. Kitaev, *Unpaired Majorana fermions in quantum wires*, Phys.-Usp. **44**, 131 (2001).

[32] R. M. Lutchyn , J. D. Sau , S. D. Sarma, *Majorana fermions and topological phase transition in semiconductor-superconductor hetrostructures*, Phys. Rev. Lett. **105**, 077001, (2010).

[33] Y. Oreg, G. Refael, F. von Oppen, *Helical liquids and Majorana bound states in quantum wire*, Phys. Rev. Lett. **105**, 177002 (2010).

[34] S. Nadj-Perge, S.M. Frolov, E. P. A. M. Bakkers, L. P. Kouwenhoven, *Spin-orbit qubit in a semiconductor nanowires*,Nature **468**, 1084 (2010).

[35] C. Fasth, A. Fuhrer, M. T. Björk, L. Samuelson, *Tunable double quantum dots in InAs nanowires defined by local gate electrodes*, Nano Lett. **5**, 1487 (2005).

[36] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, *Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices*, Science **336**, 1003 (2012).

[37] M. T. Deng, C. L. Yu, G. Y. Huang, M. Larsson, P. Caroff and H. Q. Xu. *Anomalous zero-bias conductance peak in a Nb-Insb nanowire-Nb hybrid device*, Nano letters, 12, 6414 (2012).

[38] M. Hocevar, G. Immink, M. Verheijen, N. Akopian, V. Zwiller, L. P. Kouwenhoven, E. P. A. M. Bakkers, *Growth and optical properties of axial hybrid III-V/silicon nanowires*, Nat. Commun. **3**, 1266 (2012).

[39] T. O. Rosdahl, A. Manolescu, V. Gudmundsson, *Spin and impurity effects on flux-periodic oscillations in core-shell nanowires*, *Phys. Rev. B.* **90**, 035421 (2014).

[40] T. D. Stanescu, A. Sitek, A. Manolescu, *Robust topological phase in proximitized core-shell nanowires coupled to multiple superconductors*. Beilstein J Nanotechnol, **9**, 1512 (2018).

[41] Ö. Gül1, D. J. van Woerkom, I. van Weperen, D. Car, S. R. Plissard, E. P. A. M. Bakkers and L. P. Kouwenhoven, *Towards high mobility InSb nanowire devices*, Nanotechnology, **26**, 215202 (2015).

[42] S. Csonka, L. Hofstetter, F. Freitag, S. Oberholzer and C. Schönenberger, T. S. Jespersen, M. Aagesen and J. Nygård, Giant Fluctuations and Gate Control of the g-Factor in InAs Nanowire Quantum Dots, Nano Lett. 8, 3932 (2008).

[43] H. A. Nilsson, P. Caroff, C. Thelander, M. Larsson, J. B. Wagner, L-E, Wernersson, L, Samuelson and H. Q. Xu, *Giant, level dependent g-factors in InSb nanowire quantum dots*, Nano letter, **9**, 3151 (2009).

[44] J**.** van den Berg, S. Nadj-Perge, V. Pribiag, S. Plissard, E. Bakkers, S. Frolov, and L. Kouwenhoven, *Fast Spin-Orbit Qubit in an Indium Antimonide Nanowire,* Physical Review Letters **110,** 066806 (2013).

[45] J. Kammhuber, M. C. Cassidy, F. Pei, M. P. Nowak, A. Vuik, Ö. Gül, D. Car, S. R. Plissard, E. P. A. M. Bakkers, M. Wimmer, L. P. Kouwenhoven, *Conductance through a helical state in an InSb nanowire*, Nature communications, **8**, 478 (2017).

[46] S. M. Albrecht, A. P. Higginbotham, M. Madsen, F. Kuemmeth, T. S. Jespersen, J. Nygård, P. Krogstrup, C. M. Marcus*, Exponential protection of zero modes in Majorana islands*. Nature, **531**, 206 (2016).

[47] H. Zhang, C. X. Liu, S. Gazibegovic, D. Xu1, J. A. Logan, G. Z. Wang, N. van Loo, J. D. S. Bommer , M. W. A. de Moor, D. Car, R. L. M. O.H. Veld, P. J. van Veldhoven, S. Koelling, M. A. Verheijen, M. Pendharkar, D. J. Pennachio, B. Shojaei, J. S. Lee, C. J. Palmstrøm, E. P. A. M. Bakkers, S. D. Sarma, L. P. Kouwenhoven, *Quantized Majorana Conductance*, Nature, **556**, 74 (2018).

[48] N. Akopian, G. Patriarche, L. Liu, J.-C. Harmand and V. Zwiller, *Crystal Phase Quantum Dots*, *Nano. Lett.* **10**, (2010).

[49] C. Thelander, P.Agarwal, S. Brongersm, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, W. Riess, B. J. Ohlsson, U. Gösele, L.Samuelson, *Nanowire-based one-dimensional electronics*. Materials Today **9**, (2006).

[50] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, C. M. Lieber, *Growth of Nanowire Superlattice Structures for Nanoscale Photonics and Electronics*, Nature **415**, 617 (2002).

[51] T. Kuykendall, P. Ulrich, S. Aloni, P. Yang, *Complete composition tunability of InGaN nanowires using a combinatorial approach*, Nat. Mater. **6**, 951 (2007).

[52] M.T. Björk , C. Thelander , A.E. Hansen , L.E. Jensen , M.W. Larsson , L.R. Wallenberg , L. Samuelson, *Few-Electron Quantum Dots in Nanowires Nano*, Lett. **4**, 1621 (2004).

[53] R. E. Algra, M. A. Verheijen, M. T. Borgstrom, L. F. Feiner, G. Immink, W. J. P. van Enckevort, E. Vlieg , E. P. A. M. Bakkers, *Twinning superlattices in indium phosphide nanowires*, Nature, **456**, 369 (2008).

[54] R. S. Wagner, W. C. Ellis, *Vapor-Liquid-Solid Mechanism of Single Crystal Growth*, Appl. Phys. Lett. **4**, 89 (1964).

[55] K. Li, W. Pan, J. Y. Wang, H. Pan, S. Y. Huang, Y. J. Xing, and H. Q. Xu, *Growth of High Material Quality Group III-Antimonide Semiconductor Nanowires by a Naturally Cooling Process*. Nanoscale. Res. Lett. **11**, 222 (2016).

[56] P. Caroff, J. B. Wagner, K. A. Dick, H. A. Nilsson, M. Jeppsson, K. Deppert, L. Samuelson, L. R. Wallenberg, L-E. Wernersson, High-Quality InAs/InSb Nanowire Heterostructures Grown by Metal–Organic Vapor-Phase Epitaxy, Small, 4, 878 (2008).

[57] M. Shafa, S. Akbar, L. Gao, M. F. E. Alam and Z. M. Wang, *Indium Antimonide Nanowires: Synthesis and Properties*, Nanoscale Research Letters **11**, 164 (2016).

[58] S. F. Svensson, S. Jeppesen, C. Thelander, L. Samuelson, H. Linke and K. A. Dick, *Control and understanding of kink formation in InAs-InP heterostructure nanowires*, Nanotechnology **24**, 345601 (2013).

[59] K. A. Dick, C. Thelander, L. Samuelson, P. Caroff, Crystal Phase Engineering in Single InAs Nanowires, *Nano. Lett.***10**, 3494, (2010).

[60] J. Johansson, K. A. Dick, P. Caroff, M. E. Messing, J. Bolinsson, K. Deppert and L. Samuelson, *Diameter Dependence of the Wurtzite−Zinc Blende Transition in InAs Nanowires*, J. Phys. Chem. C, **114**, 3837 (2010).

[61] Ö. Gül, H. Zhang, F. K. de Vries, J. V. Veen, K. Zuo, V. Mourik, S. Conesa-Boj, M. P. Nowak, D. J. van. Woerkom, M. Q. Pérez, M. C. Cassidy, A. Geresdi, S. Koelling, D. Car, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, *Hard Superconducting Gap in InSb Nanowires*, Nano Lett.**17**, 2690 (2017).

[62] I. V. Weperen, *QuantumTransport in Indium Antimonide Nanowires-Investigating building blocks for Majorana devices*. PhD Thesis, Delft University of Technology (2014).

[63] R. Kim, M. S. Lundstrom, *Characteristic Features of 1-D ballistic transport in nanowire MOSFETs*, IEEE Transports on nanotechnology, **7,** 787 (2008).

[64] A. Rahman, J. Guo, S. Datta and M. S. Lundstrom, *Theory of ballistic nanotransistors*, IEEE Trans. Electron devices, **50**, 1853 (2003).

[65] R. H. Dennard, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, *Integrated nanoelectronics for the future*, Nature Materials, **6**, 810 (2007).

[66] H. A. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlström, L-E, Wernersson, *Temperature dependent properties of InSb and InAs nanowire field-effect transistors*, Appl. Phys. Lett. **96**, 153505 (2010).

[67] S. R. Das, C. J. Delker, D. Zakharov, Y. P. Chen, T. D. Sands, D. B. Janes, *Room temperature device performance of electrodeposited InSb nanowire field effect transistors*, Appl. Phys. Lett. **98**, 243504 (2011).

[68] H. A. Nilsson, M. T. Deng, P. Caroff, C. Thelander, L, Samuelson, L. E, Wernersson, H. Q. Xu, *InSb Nanowire Field-Effect Transistors and Quantum-Dot Devices*, IEEE Journal of selected topics in quantum electronics,**17**, 907 (2011).

[69] H. A. Nilsson, P. Caroff, E. Lind, M-E, Pistol, C. Thelander, L-E, Wernersson, *Unipolar and bipolar operation of InAs/InSb nanowire heterostructure field-effect* transistors, Journal of Applied Physics, **110**, 064510 (2011).

[70] S. Chuang, Q. Gao, R. Kapadia, A. C. Ford, J. Guo, A. Javey, *Ballistic InAs Nanowire Transistors,* Nano. Lett. **13**, 555 (2013).

[71] D. Fan, N. Kang, S. G. Ghalamestani, K. A. Dick, H. Q. Xu, *Schottky barrier and contact resistance of InSb nanowire field-effect transistors,* Nanotechnology, **27**, 275204 (2016).

[72] D. B. Suyatin, V. Jain, V. A. Nebol'sin, J, Trägårdh, M. E. Messing, J. B. Wagner, O. Persson, R. Timm, A. Mikkelsen, I. Maximov, L. Samuelson, H. Pettersson, *Strong Schottky barrier reduction at Au-catalyst/GaAs-nanowire interfaces by electric dipole formation and Fermi-level unpinning*, Nature communications, **5**, 3221 (2014).

[73] L. Aaron, V. S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing, T. S. Mayer, *Fabrication and Characterization of Axially Doped Silicon Nanowire Tunnel Field-Effect Transistors*, Nano Letter.**10**, 4813 (2010).

[74] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, S. Datta, *Temperature-Dependent I–V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET*, IEEE Electron Device Letters, **31**, 564 (2010).

[75] H. M. Chang, K. L. Fan, A. Charnas, P. D. Ye, Y. M. Lin, and C. H. Wu, *Experimental analysis of the Schottky barrier height of metal contacts in black phosphorous field-effect transistors*, J. Phys. D: Appl. Phys. **51**, 135306 (2017).

[76] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, (2007).

[77] J. Lin, D. A. Antoniadis, J. A. Del Alamo, *Off-State Leakage Induced by Band-to-Band Tunneling and Floating-Body Bipolar Effect in InGaAs Quantum-Well MOSFETs*, IEEE Electron Device Lett. **35**, 1203 (2014).

[78] J. Lin, D. A. Antoniadis, J. A. Del Alamo, *Physics and Mitigation of Excess Off-state Current in InGaAs Quantum-Well MOSFETs*, IEEE Trans. Electron Devices, **62** 1448 (2015).

[79] Y. Taur, *Fundamentals of Modern VLSI Devices*, 2nd edition, Cambridge University Press (2009).

[80] W. Yang, D. Pan, R. Shen, X. Wang, J. Zhao, Q. Chen, *Suppressing the excess OFF-state current of short-channel InAs nanowire field-effect transistors by nanoscale partial-gate*, Nanotechnology, **29**, 415203 (2018).

[81] D. K. Schroder, *Semiconductor material and device characterization*, John Wiley& Sons (2006).

[82] Y. Wang, J. Chi, K. Banerjee, D. Grützmacher, T. Schäpers, J. G. Lu, *Field effect transistor based on single crystalline InSb nanowire*, Journal of Materials Chemistry, **21**, 2459 (2011).

[83] A. C. Ford, J. C. Ho, Y. L. Chueh, Y. C. Tseng, Z. Y. Fan, J. Guo, J. Bokor, A. Javey, *Diameter-Dependent Electron Mobility of InAs Nanowires*, *Nano Lett.* **9**, 360 (2009).

[84] J. Schliemann, J. Egues, D. Loss, *Nonballistic Spin-Field-Effect Transistor*, Physical Review Letters, **90,** 146801 (2003).

[85] Y. Kunihashi, M. Kohda, H. Sanada, H. Gotoh, T. Sogawa, J. Nitta, *Proposal of spin complementary field effect transistor*, Applied Physics Letters, **100,** 113502 (2012).

[86] X. Cartoixa, D. Z.-Y, Ting, Y.-C. Chang, *A resonant spin lifetime transistor*, Applied Physics Letters **83,** 1462 (2003).

[87] C. Kloeffel, D. Loss, *Prospects for Spin-Based Quantum Computing in Quantum Dots*, Annual Review of Condensed Matter Physics **4,** 51 (2013).

[88] S. M. Frolov, S. R. Plissard, S. Nadj-Perge, L. P. Kouwenhoven, E. P. Bakkers, *Quantum computing based on semiconductor nanowires*, MRS Bulletin **38,** 809 (2013).

[89] Y. Oreg, G. Refeal, F. von Oppen, *Helical Liquids and Majorana Bound States in QuantumWires*, Physical Review Letters **105,** 177002 (2010).

[90] R. M. Lutchyn, J. D. Sau, S. D. Sarma, *Majorana fermions and a topological phase transition in semiconductor-superconductor heterostructures*, Physical Review Letters **105,** 077001 (2010).

[91] P. Anderson, E. Abrahams, T. Ramakrishnan, *Possible Explanation of Nonlinear conductivity in Thin-Film Metal Wires*, Physical Review Letters **43,** 718 (1979).

[92] G. Bergmann, *Weak localization in thin films: a time-of-flight experiment with conduction electrons*, *Physics Reports* **107,** 1 (1984).

[93] S. Hikami, A. I. Larkin, Y. Nagaoka, *Spin-Orbit Interaction and Magnetoresistance in the Two Dimensional Random System*, Progress of Theoretical Physics **63,** 707 (1980).

[94] S. V. Iordanskii, Y. B. Lyanda-Geller, G. E. Pikus, *Weak localization in quantum wells with spin-orbit interaction*, JETP Letters **60,** 206 (1994).

[95] R. Winkler, *Spin–Orbit Coupling Effects in Two-Dimensional Electron and Hole Systems*, Springer Berlin Heidelberg, Berlin, Heidelberg (2003).

[96] O. Krebs, P. Voisin, *Giant optical anisotropy of semiconductor heterostructures with no common atom and the quantum-confined pockels effect*, Phys. Rev. Lett. **77**, 1829 (1996).

[97] E. L. Ivchenko, A.Y. Kaminski, U. Rössler, *Heavy-light hole mixing at zinc-blende (001) interfaces under normal incidence*, Phys. Rev. B **54**, 5852 (1996).

[98] M. W. Wu, J. H. Jiang, M. Q. Weng, *Spin dynamics in semiconductors*, Physics Reports **493**, 61 (2010).

[99] G. Dresselhaus, *Spin-orbit coupling effects in zinc blende structures*, Phys. Rev. **100**, 580 (1955).

[100] S. Nadj-Perge, V. S. Pribiag, J. W. G. van den Berg, K. Zuo, S. R. Plissard, E. R. A. M . Bakkers, S. M . Frolov, and L. P. Kouwenhoven, *Spectroscopy of Spin-Orbit Quantum Bits in Indium Antimonide Nanowires*, Physical Review Letters **108,** 166801 (2012).

[101] Y. A. Bychkov, E. I. Rashba, *Oscillatory effects and the magnetic susceptibility of carriers in inversion layers*, J. Phys. C **17**, 6039 (1984).

[102] Y. A. Bychkov, E. I. Rashba, *Properties of a 2D electron gas with lifted spectral degeneracy*, JETP Lett. **39**, 78 (1984).

[103] Y. Pershin, J. Nesteroff, and V. Privman, *Effect of spin-orbit interaction and in plane magnetic field on the conductance of a quasi-one-dimensional system.* Physical Review B **69,** 121306 (2004).

[104] S. Datta and B. Das, *Electronic analog of the electro-optic modulator*, Appl. Phys. Lett. **56**, 665 (1990).

[105] M. I. Dyakonov, *Basics of semiconductor and spin physics*, Springer International Publishing AG (2017).

[106] G. L. Bir, A. G. Aronov, G. E. Pikus, *Spin relaxation of electrons due to scattering by holes*, Zh. Eksp. Teor. Fiz. **69**, 1382 (1975).

[107] A. G. Aronov, G. E. Pikus, A. N. Titkov, *Spin relaxation of conduction electrons in p-type III–V compounds*, Zh. Eksp. Teor. Fiz. **84**, 1170 (1983).

[108] Y. Yafet, *Solid State Physics*, vol. 14, Academic Press, New York, (1963).

[109] R. J. Elliott, *Theory of the effect of spin–orbit coupling on magnetic resonance in some semiconductors*, Phys. Rev. **96**, 266 (1954).

[110] M. W. Wu, C. Z. Ning, *A novel mechanism for spin dephasing due to spin-conserving scatterings*, Eur. Phys. J. B **18**, 373 (2000).

[111] C. F. Destefani, S. E. Ulloa, G. E. Marques, *Spin–orbit coupling and intrinsic spin mixing in quantum dots*, Phys. Rev. B **69**, 125302 (2004).

[112] M. I. D'yakonov, V. I. Perel', *On spin orientation of electrons in interband absorption of light in semiconductors*, Zh. Eksp. Teor. Fiz. **60**, 1954 (1971).

[113] M. I. D'yakonov, V. I. Perel', *Spin relaxation of conduction electrons in noncentrosymmetric semiconductors*, Fiz. Tverd. Tela (Leningrad) **13**, 3581 (1971).

[114] F. Meier, B. P. Zakharchenya, *Optical Orientation*, North-Holland, Amsterdam, 1984.

[115] S. Sugahara and J. Nitta, *Spin-transistor electronics: An overview and outlook*. Proceeding of the IEEE, **98**, 2124 (2010).

[116] A. A. Kiselev, K. W. Kim, *Progressive suppression of spin relaxation in two-dimensional channels of finite width*. Physical Review B **61,** 13115 (2000).

[117] S. Kettemann, *Dimensional Control of Antilocalization and Spin Relaxation in QuantumWires*, Physical Review Letters **98,** 176808 (2007).

[118] P. Roulleau, T. Choi, S. Riedi, T. Heinzel, I. Shorubalko, T. Ihn, and K. Ensslin, *Suppression of weak antilocalization in InAs nanowires*, Physical Review B **81,** 155449 (2010).

[119] Y. V. Sharvin and N. I. Bogatina, *Investigation of Focusing of Electron Beams in a Metal by a Longitudinal Magnetic Field*, Zh. Eksp. Teor. Phys. **29**, 419 (1969).

[120] Ihn, T. *Semiconductor nanostructures*, Oxford University Press, (2010).

[121] C. Harmans, *Mesoscopic Physics, an introduction*, TU Delft (2003).

[122] S. Chakravarty and A. Schmid, *Weak Localization: The quasiclassical theory of electrons in a random potential*, Physics Reports **140**, 193 (1986).

[123] G. Bergmann, *Weak anti-localization-An experimental proof for the destructive interference of rotated spin*, Solid State Communications **42,** 815 (1982).

[124] C. W. J. Beenakker, H. van Houten, *Boundary scattering and weak localization of electrons in a magnetic field*, Physical Review B **38**, 3232 (1988).

[125] C. Kurdak, A. Chang, A. Chin, T. Chang, *Quantum interference effects and spin-orbit interaction in quasi-one-dimensional wires and rings*. Physical Review B **46**, 6846 (1992).

[126] A. E. Hansen, M. T. Björk, I. C. Fasth, C. Thelander, and L. Samuelson, *Spin relaxation in InAs nanowires studied by tunable weak antilocalization*, Phys. Rev. B **71**, 205328 (2005).

[127] L. B. Wang, J. K. Guo, N. Kang, D. Pan, S. Li, D. X. Fan, J. H. Zhao, and H. Q. Xu, Phase-coherent transport and spin relaxation in InAs nanowires grown by molecule beam epitaxy, Appl. Phys. Lett. 106, 173105 (2015).

[128] I. van Weperen, B. Tarasinski, D. Eeltink, V. S. Pribiag, S. R. Plissard, E. P. A. M. Bakkers, L. P. Kouwenhoven, and M. Wimmer, Spin-orbit interaction in InSb nanowires, Physical Review B **91**, 201413 (2015).

[129] R. L. Kallaher, J. J. Heremans, N. Goel, S. J. Chung, and M. B. Santos, Spin-orbit interaction determined by antilocalization in an InSb quantum well, Physical Review B 81, 075303 (2010).

[130] M. A. Kastner, Artificial Atoms, Physics Today 46, 24 (1993).

[131] L. Romeo, S. Roddaro, A. Pitanti, D. Ercolani, L. Sorba, and F. Beltram, Electrostatic Spin Control in InAs/InP Nanowire Quantum Dots, *Nano Lett.* ***12***, 4490 (2012).

[132] L. P. Kouwenhoven, D. G. Austing, and S. Tarucha, *Few-electron quantum dots*, Rep. Prog. Phys. **64**, 701 (2001).

[133] S. D. Franceschi, R. Hanson, W.G. van der Wiel, J. M. Elzerman, J. J. Wijpkema, T. Fujisawa, S. Tarucha, L. P. Kouwenhoven, *Out-of-equilibrium Kondo effect in a mesoscopic device*. Phys. Rev. Lett. **89**, 156801 (2002).

[134] A. C. Johnson, *Charge Sensing and Spin Dynamics in GaAs Quantum Dots*, Ph.D. thesis, Harvard University (2005).

[135] H. Grabert and M. Devoret, *Single Charge Tunneling*, Plenum, New York (1992).

[136] S. De Franceschi, S. Sasaki, J. M. Elzerman, W. G. van der Wiel, S. Tarucha and L. P. Kouwenhoven, *Electron Cotunneling in a Semiconductor Quantum Dot*, Phys. Rev. Lett. **86**, 878 (2001).

[137] R. Schleser, T. Ihn, E. Ruh, K. Ensslin, M. Tews, D. Pfannkuche, D. C. Driscoll, and A. C. Gossard, *Cotunneling-Mediated Transport through Excited States in the Coulomb-Blockade Regime*, Phys. Rev. Lett. **94**, 206805 (2005).

[138] D. M. Zumbühl, C. M. Marcus, M. P. Hanson, and A. C. Gossard, *Cotunneling Spectroscopy in Few-Electron Quantum Dots*, Phys. Rev. Lett. **93**, 256801 (2004).

[139] J. Aghassi, M. H. Hettler, and G. Schon, *Cotunneling assisted sequential tunneling in multilevel quantum dots*, Applied Physics Letters **92**, 202101 (2008).

[140] X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, and C. M. Lieber, Nano Lett. **7**, 3214 (2007).

[141] A. Manolescu, A. Sitek, J. Osca, L. Serra, V. Gudmundsson, and T. D. Stanescu, *Majorana states in prismatic core-shell nanowires*, Phys. Rev. B **96**, 125435 (2017).

[142] O.Wunnicke, *Gate capacitance of back-gated nanowire field-effect transistors*, Appl. Phys. Lett. **89**, 083102 (2006).

[143] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, *Electron transport through double quantum dots*, Rev. Mod. Phys. **75**, 1 (2003).

[144] D. Sztenkiel and R. Świrkowicz, *Electron transport through parallel double quantum dots with interdot correlations*, Phys. Stat. Sol. **244**, 2543 (2007).

[145] W. J. Gonga, Y. Zheng, *Spin-dependent electron transport through a parallel double-quantum-dot structure*, Physica E **41**, 574-580, (2009).

[146] Malin Nilsson, *Charge and Spin Transport in Parallel-Coupled Quantum Dots in Nanowires*, PhD thesis, Lund University, (2018).

[147] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha, *Current Rectification by Pauli Exclusion in a Weakly Coupled Double Quantum Dot System*, Science **297**, 1313 (2002).

[148] F. H. L. Koppens, J. A. Folk, J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, I. T. Vink, H. P. Tranitz, W. Wegscheider, L. P. Kouwenhoven, and L. M. K. Vandersypen, *Control and detection of singlet-triplet mixing in a random nuclear field,* Science **309**, 1346 (2005).

[149] A. C. Johnson, J. R. Petta, J. M. Taylor, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hansson, and A. C. Gossard, *Triplet–singlet spin relaxation via nuclei in a double quantum dot*, Nature **435**, 925 (2005).

[150] J. Y. Wang, G.Y. Huang, S.Y. Huang, J. H. Xue, D. Pan, J. H. Zhao, and H. Q. Xu, *Anisotropic Pauli Spin-Blockade Effect and Spin–Orbit Interaction Field in an InAs Nanowire Double Quantum Dot*. Nano Lett.**18** 4741 (2018).

[151] M. D. Schroer, K. D. Petersson, M. Jung and J. R. Petta, Phys.Rev. Lett. **107,** 176811 (2011).

[152] A. Pfund, I. Shorubalko, K. Ensslin and R. Leturcq, *Spin-state mixing in InAs double quantum dots*, Phys. Rev. B **76** 161308, (2007).

Acknowledgments

The research presented in this thesis would not be possible without the enormous help and support from many people at the division of solid state physics who have been continuously offering their assistance over the last five years.

First of all, I would like to express my gratitude to my supervisor Prof. Hongqi Xu for giving me the opportunity to join his research group. I very much appreciate your support, inspiration and supervision that I have been receiving since the first day I came to the department.

I would also like to thanks to my co-supervisors Lars Samuelson, Martin Leijnse and Ville Maisi. It has been always a pleasure for me to work with you. Your insightful discussions and suggestions have helped me to make a lot of progress in my research. Ville, your guidance in the measurement lab was invaluable.

I am very grateful to my nanowire growers Philippe Caroff, Sepideh Gorji Ghalamestani and Kan Li for providing me with nanowires.

My sincere gratitude goes to the people who keep FTF and NanoLund running and for creating pleasant work place: Dan Hessman, Heiner Linke, Anneli Löfgren, Anders Gustafsson, Knut Deppert and Jonas Johansson. Special thanks to Dan, your incredible support and encouragement made it possible for me to complete the research presented in this thesis, I very much appreciate it.

I would like to express my gratitude to Claes and Adam for keeping your doors open for me. You had never said ’No’ to me whenever I needed some help from you. You are just wonderful men.

To my colleagues David Göransson and Chunlin Yu: I am very grateful to you for teaching me everything about device fabrication, helping to tackle endless problems I faced in research and for your friendships. It is my pleasure to remember a lot of funny discussions that we have had.

To my former and present office mates: Liq Hussein, Simon Abay, Erik Martensson, Alexander Berg, Olof Hultin, Yuwei Zhang and Vector Gomez. I enjoyed your company in office, thanks for your chats, your encouragements and the wonderful time we have had together.

I would also like to express my gratitude to Sören Jeppesen and Sofia Falhvik for teaching me CBE. To Dmitry Suyatin for your encouragement, support and sharing with me your valuable experience of doing PhD. My warm thanks extends also to Ivan Maximov, Maria Huffman, Håkan Lapovski, George Rydnemalm, Anders Kvennefors, Bengt Meuller, Mariusz Graczyk and all other engineers for their efforts to keep running every tool in the cleanroom all the time. Without your incredible work, I would not achieve anything. Leif Magnusson thank you very much for always supplying liquid helium, even during the Christmas holidays. I also thank Jane and Johanna for fixing problems with my computers and the computers in measurement lab. I would also like to thank Margareta Forsberg, Abdul-Rehman Hakim, Mia Hedin, Line Lundfald, Helena Edberg, Marica Kolobaric for your administrative support.

I sincerely thank all hard working, brilliant PhD students and postdocs for being with me at our great home FTF. I wish all of you success and bright achievements in your research work.

My a special thanks goes to my parents. Thanks Mom and Dad for everything you have been doing for me. Thanks to my brothers Muhammed and Ilisbek, my lovely sister Bekzat for your love and support to me.

Last, the most important people in my life, to my beloved wife Bizat and my son Beibars. I am very grateful for your unlimited support and being my happiness.