Automatic Gain Control In WCDMA Terminals

Alriksson, Peter; Bernhardsson, Bo; Lindoff, Bengt

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[1]Peter Alriksson, [2]Bo Bernhardsson and [2]Bengt Lindoff

[1]*Department of Automatic Control, Lund Institute of Technology*
Box 118, 221 00 Lund, Sweden
[2]*Research Department, Ericsson Mobile Platforms AB*
Nya Vattentornet, 221 83 Lund, Sweden

Abstract This article gives a presentation of the Automatic Gain Control algorithm used in WCDMA (3rd generation mobile networks). The focus is on how the controller bandwidth influences settling times and modulation distortion. This will be investigated through simulation for two different channel cases.

Keywords AGC, Automatic Gain Control, WCDMA , UMTS

1. INTRODUCTION

The purpose of this article is to present an industrial application of control theory, namely Automatic Gain Control (AGC). The AGC is used on the terminal side in the 3rd generation mobile network, from here on referred to as WCDMA. The control design presented in this article was developed at Ericsson Mobile Platforms in Lund before this project. The purpose of this project was to develop a simulator and to study how different AGC-parameters influence the receiver performance. In this article the tradeoff between settling time after a step change in received power and modulation distortion will be investigated through simulations. The design parameter is the controller bandwidth. There are many other parameters related to AGC that influence overall system performance. For more simulation results see (2).

2. A BASIC WCDMA SYSTEM

To be able to understand the function of the AGC and why it is used, a brief overview of the communication from base station to terminal in a simplified WCDMA system will be given.

The information bits are first coded and interleaved to reduce the effects of bit errors. This operation results in a new bit steam. The next step is to map groups of bits to symbols in the complex space, typically four (QPSK) or 16 (16QAM) different symbols are used. The sequence is then multiplied as complex numbers with a complex pseudo random sequence, the spreading sequence. Each new symbol after the multiplication is called a chip. The chip rate in WCDMA is fixed to 3840000 chips/s. A common unit is a slot that is defined as 2560 chips. Next the new complex sequence is mapped to two analog signals ,$I(t)$ and $Q(t)$, and I/Q modulated as

$$s_{HF}(t) = I(t)\sqrt{2}\cos(2\pi f_c t) - Q(t)\sqrt{2}\sin(2\pi f_c t). \quad (1)$$

The carrier down link (from base station to terminal) frequencies, f_c, in WCDMA range from 2110 MHz to 2170 MHz.

On the receiver side the signal is demodulated, filtered through the same filter as in the transmitter and finally AD converted. Because of the strong variations of received power, the AD-converter (ADC) has to have a large dynamic range. This is not power and cost effective, and

thus a series of variable gain amplifiers are inserted before the AD conversion stage. For a detailed description of digital communication theory see (1).

3. AUTOMATIC GAIN CONTROL

As mentioned in Section 2 the main function of the AGC is to limit the dynamic range of the AD converter. To achieve this the AGC must have a large dynamic range and a fast settling time after step changes in received power. According to the 3G specifications (see (3)) the receiver must be able to handle signal levels between -106.7dBm and -25dBm. A step in received power occurs for example when the WCDMA receiver makes measurements on the signal quality from neighboring base stations. One possible scenario is that a neighboring base station is transmitting at a different carrier frequency. The I/Q demodulator then changes carrier frequency for a short period of time, which leads to an abrupt change in received power. To minimize the measuring time, the AGC must compensate for the new received power as fast as possible.

To be able to understand the Automatic Gain Control or AGC algorithm, the surrounding blocks have to be briefly described. An overview of the AGC and the surrounding blocks can be found in Figure 1.

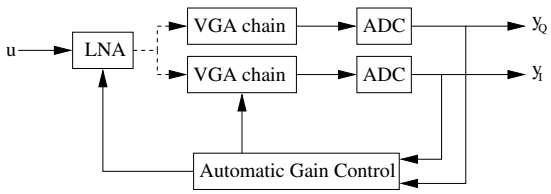

Fig. 1 Simplified view of Automatic Gain Control, Variable Gain Amplifier Chain and Low Noise Amplifier. The dashed lines represent the part of the receiver where the signal is demodulated to base band frequencies.

3.1 *Low Noise Amplifier*

The LNA is implemented in the radio frequency part of the receiver and thus the first amplifier the received signal encounters. The low noise property of the LNA is critical to the function of the receiver. The making of RF amplifiers with low noise properties is a difficult matter so therefore it is not efficient to have more than a few operating modes. The gain changes are modeled as instantaneous, which in reality of course is not the case.

3.2 *Variable Gain Amplifiers*

The next step after the LNA is two chains of Variable Gain Amplifiers or VGAs. The signal from the LNA is split up into its I and Q parts (see section 2) and then fed to the VGA chains. To be able to meet the dynamic requirements of 81.7 dB the VGA chain consists of a number of VGAs with gains in the interval -15 dB to 15 dB and with a resolution of between 0.5 dB and 2 dB.

3.3 *The AGC Algorithm*

The task of the controller is to control the two chains of VGAs and the LNA so that the estimated power is as close to a preferred value as possible. Because of the large dynamic range of the VGA chain the desired gain values A_k are represented in the logarithmic domain. A control algorithm that performs this task is presented below. The presented algorithm was developed at Ericsson Mobile Platforms and given to me as part of a simulator developed for studying system degradation due to AGC. The presentation in this section is based on an internal Ericsson document (4).

First the I and Q channels are fed to a power estimator. One way to develop a power estimator is to first form the instantaneous mean power of the I and Q channels as

$$\hat{P}_y = \frac{y_I^2 + y_Q^2}{2} \tag{2}$$

and then low pass filter $\hat{P}_y$ to form a time average of the received power. The low pass filter has bandwidth ω_{pow}, the choice of bandwidth is a tradeoff between speed and noise. A very low bandwidth will result in a slow tracking of received power which might lead to decreasing step response performance of the AGC. On the other hand a very high bandwidth will lead to a noisy power estimate which might lead to a lot of unnecessary gain changes.

Next the low pass filtered instantaneous power estimate is down sampled and compared to the reference value $Pref$. This control error is used as input to the controller which controls the VGA chain and LNA. The controller can send gain changes to the VGA chain and LNA one or several times per slot.

Now let us derive a simple model of the AGC. First let us assume that the LNA and VGA can be viewed as one amplifier placed after I/Q demodulation. If all VGA and LNA dynamics are neglected the output from the VGA chains and LNA can be written as

$$y_{I,Q} = \alpha e^{\beta A_k} u_{I,Q} \tag{3}$$

where α and β are constants depending on the dynamic range of the VGA chain. The instantaneous power of y can then be written as

$$P_y = P_u(\alpha e^{\beta A_k})^2 \quad (4)$$

where P_u is the instantaneous power of the input u. If the time constant of the low pass filter in the power estimator is much shorter than the update rate of the controller the dynamics are reduced to a time delay and the problem can be viewed as a linear control problem in the logarithmic domain. Taking the logarithm of (4) gives

$$\log(P_y) = \log(P_u) + 2\beta A_k + 2\log(\alpha) \quad (5)$$

Using the control structure presented above the problem can be viewed as a linear control problem with $\log(P_y)$ as the measured variable and A_k as controller output. The process to be controlled consists of a static gain 2β and a disturbance $\log(P_u) + 2\log(\alpha)$, see Figure 2.

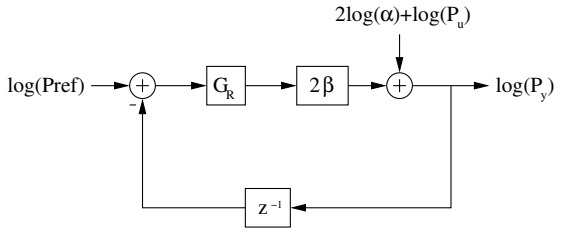

Fig. 2 The control problem in the logarithmic domain. The parameter β represents the LNA and VGA chain.

The measured output P_y can then be written as

$$\log(P_y) = G_1(z)\log(P_u) + G_2(z)\log(P_{ref}) \quad (6)$$

where

$$G_1(z) = \frac{1}{1 + 2\beta G_R(z)z^{-1}} \quad (7)$$

$$G_2(z) = 2\beta G_R(z)G_1(z) \quad (8)$$

There are two objectives in the choice of $G_1(z)$. The AGC should be able to track and compensate for variations in P_u and have a low settling time after a step change in P_u. This implies a high pass structure of $G_1(z)$ with cutoff frequency higher than the speed of the variations in received power. On the other hand the AGC must not destroy the modulation of the signal. That is, the cutoff frequency must not be too high. The only requirement on $G_2(z)$ is to be able to keep a constant reference value, this corresponds to a low pass structure with sufficiently high cutoff frequency. Choosing a PI-controller on the form

$$G_R(z) = K_P + \frac{K_I}{z-1} \quad (9)$$

gives the transfer functions

$$G_1(z) = \frac{(z-1)z}{z^2 + (2\beta K_P - 1)z + (K_I - K_P)2\beta}$$

$$G_2(z) = \frac{(zK_P + (K_I - K_P))2\beta}{z^2 + (2\beta K_P - 1)z + (K_I - K_P)2\beta} \quad (10)$$

One reasonable continuous time pole placement could for example be on the form $s^2 + 2\zeta\omega s + \omega^2$ with $\omega \approx 10^4$ rad/s and $\zeta \approx 0.4$. The controller is run 10 times per slot which corresponds to a sampling frequency of 15 kHz. The Bode diagram for $G_1(z)$ and $G_2(z)$ can be found in figures 3 and 4.

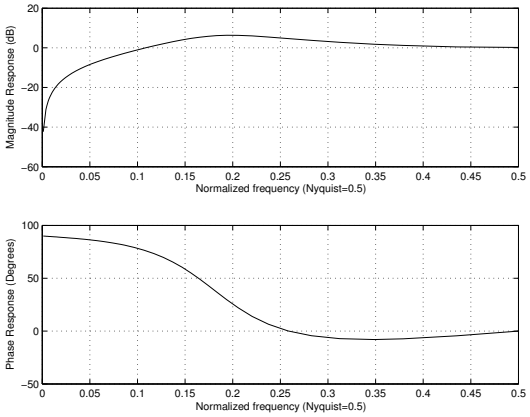

Fig. 3 Bode diagram for $G_1(e^{i2\pi f/f_s})$ with continuous time poles in $\omega \approx 10^4$ rad/s and $\zeta \approx 0.36$.

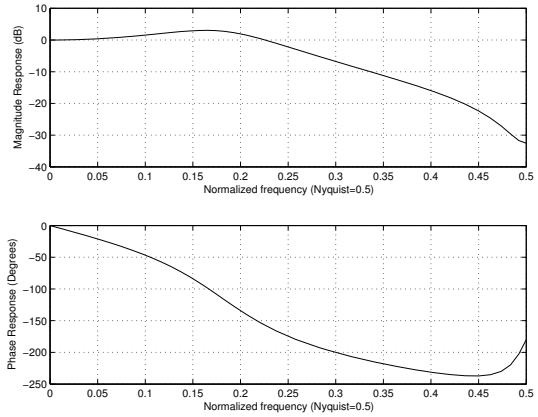

Fig. 4 Bode diagram for $G_2(e^{i2\pi f/f_s})$ with poles in $\omega \approx 10^4$ rad/s and $\zeta \approx 0.36$.

3.4 *Automatic Gain Control Simulations*

To illustrate the different signals and the basic principle of the AGC one short simulation was made. The most difficult channel cases for the AGC are the single path cases, that is when there is only one strong path from the base station to the terminal. Therefore one channel

case (VB120) with one path corresponding to a vehicle velocity of 120 km/h was simulated for 30 slots using 16QAM modulation. To only highlight the effects of AGC the channel was simulated without noise. In Figure 5 the real part of the input to the AGC together with the real part of the AD converted output is shown. The power estimate, AGC gain output and bit errors are also given.

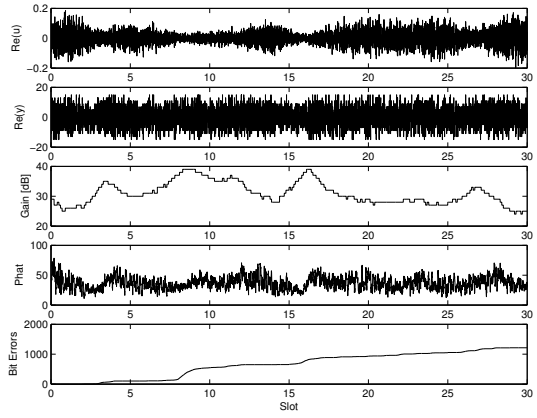

Fig. 5 Real parts of input and output together with power estimate gain output and bit errors. 1 path channel model corresponding to a vehicle velocity of 120 km/h. Control design with $\omega \approx 10^4$ rad/s.

In Figure 5 the terminal is traveling at a velocity of 120 km/h. The output from the AGC seems to be saturated at all times, but this is not the case. Because of the large amount of data points plotted the signal looks saturated.

3.5 *AGC Step Response Evaluation*

To gain a further understanding of the AGC problem two step response simulations were made (see figures 6 and 7). The step response was created by multiplying the incoming signal with a constant corresponding to the desired step amplitude. In the simulations a positive and negative step of 40 dB was used. The AGC algorithm is implemented so that when the LNA changes value the VGA chain must change the gain in the opposite direction to maintain the same gain level.

One observation that can be made is that the positive step response is faster than the negative. If we assume a 4 bit AD converter, the discrete power levels range between 1 and 225. The reference value used in this simulation is 35. The controller works in the logarithmic domain which implies that the maximum differences between desired power and the current power are -15 dB and 8 dB respectively. For a positive 40 dB step, the power level saturates at 1, which leads to a difference of -15 dB. For a negative step of 40 dB the power level saturates at 225 which gives a difference of 8 dB and thus leads to less control action than the positive step.

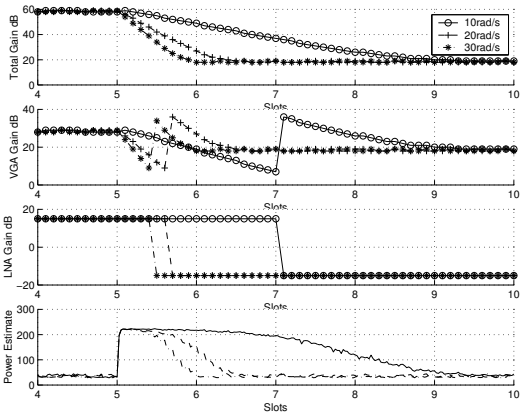

Fig. 6 Negative step of 40 dB at t=5 slots for three different AGC designs. All controllers have relative damping $\zeta = 0.36$. The AGC algorithm is implemented so that when the LNA changes value the VGA chain must change the gain in the opposite direction to maintain the same gain level.

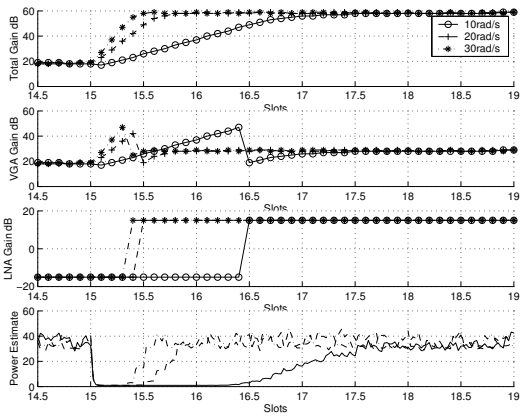

Fig. 7 Positive step of 40 dB at t=15 slots. The positive step is faster than the negative one in Figure 6. If we assume a 4 bit AD converter, the discrete power levels range between 1 and 225. The reference value used in this simulation is 35. The controller works in the logarithmic domain which implies that the maximum differences between desired power and the current power are -15 dB and 8 dB respectively. For a positive 40 dB step, the power level saturates at 1, which leads to a difference of -15 dB. For a negative step of 40 dB the power level saturates at 225 which gives a difference of 8 dB and thus leads to less control action than the positive step.

From the step response simulations we can draw the conclusion that a faster controller is preferable to a slower one.

4. BIT ERROR SIMULATIONS

In this section two bit error simulations were made, one with a channel model corresponding

to a pedestrian walking at 3 km/h (PA3) and the VB120 channel used in section 3.4. To be able to calculate the raw bit error, $2.56 \cdot 10^6$ bits where fed through the simulator and the bit error was calculated for different signal to noise ratios. The modulation technique used in this section is 16QAM. For a more detailed description of the different channel cases and other simulation parameters see (2).

As can be seen in Figure 8 the fastest AGC gives the worst bit error, whereas the two slower ones are almost equal in performance. In Figure 9 on the other hand, the worst bit error rates where achieved with the slowest controller. One observation is that the $2 \cdot 10^4$ rad/s controller gives good performance in both cases. The choice of optimal controller bandwidth is thus dependent on the channel model. If the variations in received power are slow a fast controller will only degrade performance and thus a slow controller is preferred. On the the hand, if the variations are very fast a faster controller is preferred. But increasing the bandwidth from $2 \cdot 10^4$ rad/s to $4 \cdot 10^4$ rad/s seems to give a very small performance gain.

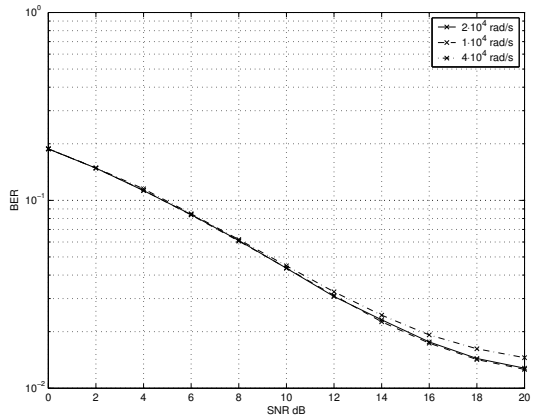

Fig. 8 Bit error for a typical pedestrian channel model for different signal to noise ratios. A faster controller degrades performance.

5. CONCLUSIONS

Because the pedestrian channel model is a more likely setting, it seems that a slower AGC design is preferred when compared to a faster one with respect to bit error rate. In the step response simulations however a faster AGC design is preferable. What controller to choose thus depends on the requirements of the step response and the most probable reception environment.

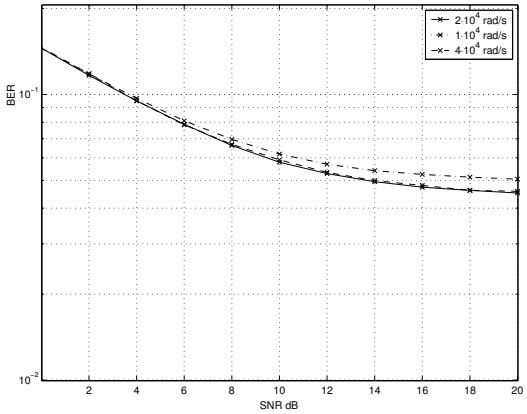

Fig. 9 Bit error for a vehicle channel model for different signal to noise ratios. A faster controller increases performance up to a certain point

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