Novel Processing and Electrical Characterization of Nanowires

Storm, Kristian

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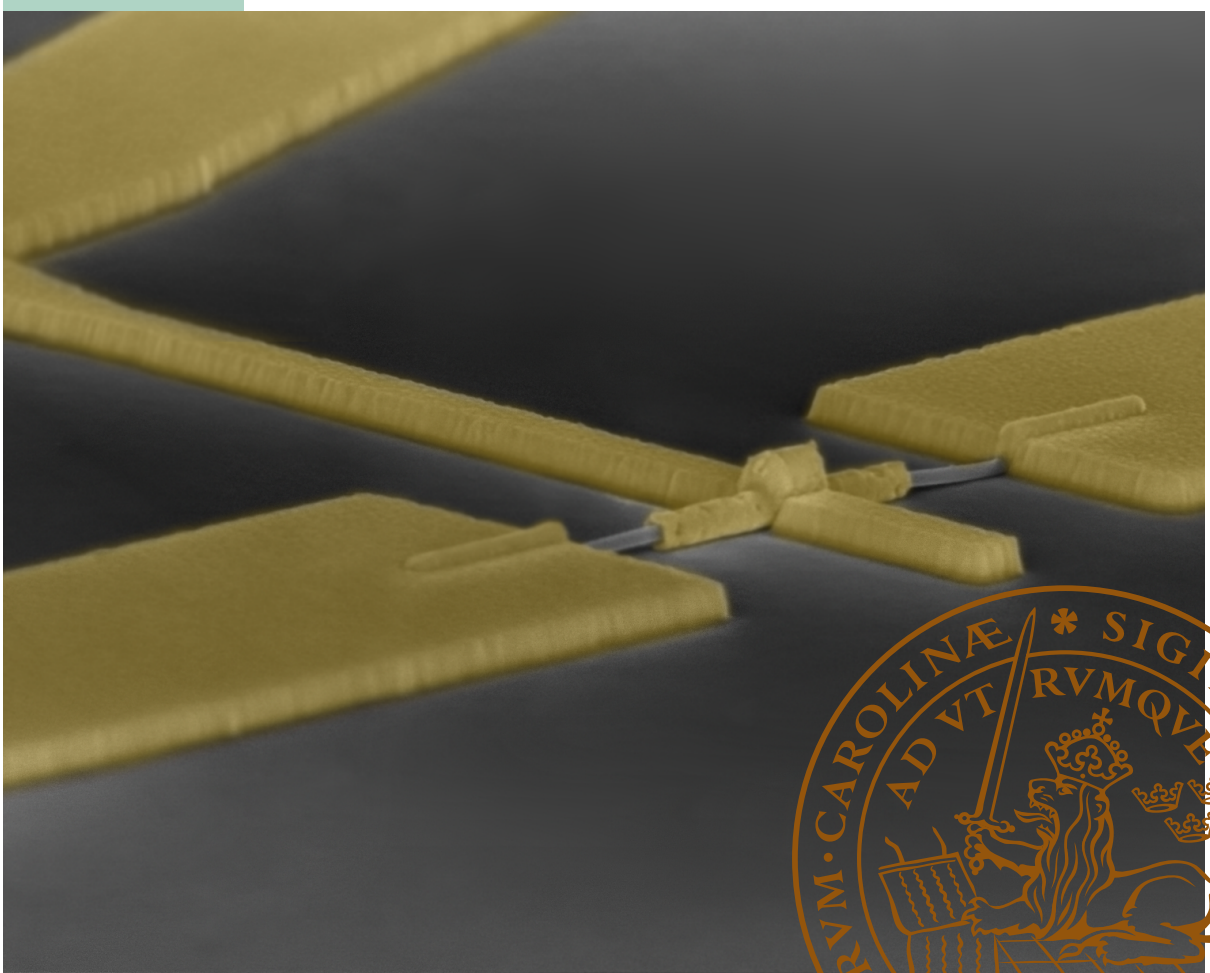

Novel Processing and Electrical Characterization of Nanowires

Doctoral Thesis

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LUND UNIVERSITY

Department of Physics
Division of Solid State Physics
Lund, Sweden, 2013

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Abstract
This thesis investigates novel electrical nanowire characterization tools and devices. Conventional characterization methods, long available to bulk semiconductor samples, have been adapted and transferred to the nanowire geometry. The first part of the thesis describes the development of Hall effect measurements, an entirely new characterization tool for nanowires. It is shown that Hall effect measurements can be performed on InP core-shell nanowires using a self-aligned lifting layer. By combining experimental data with results from simulations of band diagrams and current distribution under the influence of a magnetic field, the carrier density in the n-type nanowire shell can be determined. We found that the nanowire shell exhibits a doping gradient along the length of the nanowire. This doping inhomogeneity is important to account for and engineer when making devices using InP nanowires.

The second part of the thesis demonstrates how capacitance-voltage measurements can be performed on arrays of InAs nanowires. Using a novel device structure, the capacitance signal from the nanowires can be distinguished from parasitic capacitances. A model was developed to simulate the capacitance-voltage behavior of the nanowires and was fitted to the experimental data to extract the doping concentration. Furthermore, the hysteresis observed in the capacitance-voltage sweeps was used to calculate the trap density close to the InAs-HfO_2 dielectric interface.

Finally, studies of gate effects in nanowires are presented. We demonstrate how the gating efficiency is improved by means of wrapped or semiwrapped gates on nanowires. Field-effect transistors made from InP nanowires are described that exhibit both ambipolar behavior and gating efficiency only 13% lower than the theoretical limit. These properties were used to fabricate a field-effect diode, a device in which a p-n junction is formed without any doping incorporation in the active region. We also demonstrate how nanowires positioned laterally on a substrate can be equipped with a fully wrapped gate electrode. This device was developed as part of a platform to perform basic research in which a uniform gating effect is desired.

Key words
Nanowires, Processing, Characterization, InAs, InP, Hall effect, Capacitance, Gate, LED, Transistor

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Cover: SEM image of a laterally oriented InAs nanowire with a fully wrapped gate electrode.

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Contents

Abstract

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Populärvetenskaplig sammanfattning

Nanoteknik och nanotrådar omnämns ofta media idag, men vad är egentligen en nanotråd, och vad kan den användas till? Dagens datorer, lysdioder och solceller är till stor del beroende av *halvledare*. En halvledare är ett kristallint material där man enkelt kan ändra ledningsförmågan. Man kan dels bestämma ledningsförmågan när materialet tillverkas genom att tillföra ytterst små koncentrationer av andra ämnen, *dopämnen*, och dels efter att materialet formats till en komponent, med hjälp av elektriska fält. Denna egenskap hos halvledare är ytterst användbar och har möjliggjort såväl datorrevolutionen, som den sett ut de senaste 50 åren, som dagens effektiva lysdioder och solceller. Det i särklass mest kända halvledarmaterialet är kisel som används i bland annat integrerade kretsar och solceller, men det finns många andra grundämnen och kombinationer av grundämnen som också är halvledare.

Nanotrådarna som undersöks i den här avhandlingen är också uppbyggda av halvledarmaterial. Istället för kisel har två andra halvledare undersökts, nämligen InP (indium-fosfid) och InAs (indium-arsenid). Nanotrådar skiljer sig från de "klassiska" halvledarna genom att de är formade till en tunn tråd istället för att tillverkas i en stor klump. Detta medför flera fördelar jämfört med det klassiska sättet att tillverka halvledare. Nanotrådar har en väldigt liten diameter, i storleksordningen 50 nm eller en tusendel av diametern av ett hårstrå. Denna lilla diameter gör att man kan kombinera olika material, vilka vanligtvis är svåra att kombinera i klassisk halvledarteknologi, i olika lager i nanotråden utan att defekter uppstår i kristallstrukturen. Detta medför nya användningsområden och gör det även möjligt att optimera existerande komponenter ytterligare.

Under det senaste decenniet har forskningen på nanotrådar accelererat kraftigt och det har blivit möjligt att tillverka nanotrådar i många olika sorters halvledarmaterial. Det har även upptäckts hur man kan tillföra dopämnen till nanotrådar för att ändra deras ledningsförmåga och därmed tillverka nanotrådskomponenter som anpassas för olika tillämpningar. Trots att kunskapen om hur man tillverkar nanotrådar i olika material och med olika elektriska egenskaper utvecklats snabbt, har möjligheten att i detalj undersöka och mäta dessa egenskaper släpat efter. Det är dels de små dimensionerna hos nanotrådarna och dels deras tredimensionella form som gör det besvärligt att utveckla verktyg för att karaktärisera dem.

Denna avhandling handlar om hur vi utvecklat metoder för att elektriskt karaktärisera nanotrådar. Klassiska mätmetoder, som länge funnits tillgängliga för traditionella halvledarmaterial, har anpassats för att kunna användas på nanotrådar. Två av dessa, Hall- och kapacitans-karaktärisering, är metoder som används rutinmässigt på klassiska halvledarmaterial.

I en Hallmätning kör man en ström genom provet man är intresserad av och lägger samtidigt på ett magnetfält. Elektronerna som färdas genom provet påverkas av magnetfältet och det uppstår en spänning, en *Hallspänning*, vinkelrätt mot strömriktningen. Denna spänning kan mätas och från storleken på spänningen är det möjligt att beräkna koncentrationen av elektroner i provet. Denna egenskap är viktig att mäta eftersom den bestämmer ledningsförmågan hos halvledaren. Första delen av avhandlingen beskriver hur metoden anpassats och nu för första gången kan tillämpas på nanotrådar. Nanotrådarna som undersöks med Hallmätningar är främst tänkta att ingå som det aktiva elementet i lysdioder och solceller.

Kapacitansmätningar är en annan mätmetod som används på klassiska halvledare. För att göra kapacitansmätningar isolerar man först halvledaren med t.ex. en oxid och lägger sedan en metallkontakt ovanpå oxiden. När man lägger på en positiv spänning på metallkontakten dras det elektroner till ytan på halvledaren. Kapacitansen i provet är ett mått på hur många elektroner som dras till ytan per volt spänning som läggs på metallkontakten. Genom att mäta kapacitansen kan man beräkna olika egenskaper såsom koncentrationen av elektroner i halvledaren samt antalet elektronfällor i den isolerande oxiden och även för gränsytan mellan halvledaren och oxiden. I andra delen av avhandlingen beskrivs hur denna mätmetod anpassades och för första gången användes på nanotrådar som står upprätt på en provplatta.

Slutligen beskrivs hur en nanotrådstransistor kan tillverkas på ett helt nytt sätt. En transistor är beroende av en så kallad gate, en styrterminal som används för att öppna eller stänga flödet av ström. De transistorer som hittills tillverkats av nanotrådar är vanligtvis två olika sorter; antingen står ett stort antal trådar upp på provet och medger därför att den gate som används till trådarna har optimal verkningsgrad, eller så tillverkas de av enskilda trådar som ligger ner på ett prov. I det senare fallet har det tidigare inte varit möjligt att använda en gate som är lika optimal som när trådarna står upp. I den sista delen av avhandlingen beskrivs hur en ny tillverkningsmetod utvecklats för att kunna göra en gatekontakt i en optimal geometri till enskilda nanotrådar som samtidigt ligger ner på ett prov.

Arbetena som presenteras i den här avhandlingen utökar verktygslådan som finns tillgänglig för forskare som arbetar med nanotrådar. Detta leder till mer kunskap om hur man tillverkar och förbättrar avancerade nanotrådskomponenter och bidrar förhoppningsvis till att dessa finner tillämpningar inom solceller, lysdioder och transistorer.

List of papers

The author changed his last name from Nilsson to Storm during the course of his PhD studies.

I. Spatially resolved Hall effect measurement in a single semiconductor nanowire
K. Storm, F. Halvardsson, M. Heurlin, D. Lindgren, A. Gustafsson, P. M. Wu, B. Monemar and L. Samuelson
Nature Nanotechnology 7, 718-722 (2012)

I helped coordinate the project, took part in all measurements, performed the simulations and wrote the paper.

II. InAs nanowire metal-oxide-semiconductor capacitors
S. Roddaro, **K. Nilsson**, G. Astromskas, L. Samuelson, L-E. Wernersson, O. Karlström and A. Wacker
Aplied Physics Letters 92, 253509 (2008)

I contributed actively to planning the project, sample process development, measurements and discussions and participated in writing the paper.

III. Analysing the capacitance–voltage measurements of vertical wrapped-gated nanowires
O. Karlström, A. Wacker, **K. Nilsson**, G. Astromskas, S. Roddaro, L. Samuelson and L-E. Wernersson
Nanotechnology 19, 435201 (2008)

I participated actively in sample preparation, measurements and discussions and took part in writing the paper.

IV. Gate-induced Fermi level tuning in InP nanowires at efficiency close to the thermal limit
K. Storm, G. Nylund, M. Borgström, J. Wallentin, C. Fasth, C. Thelander and L. Samuelson
Nano Letters 11**,** 1127-1130 (2011)

I planned and took a leading role in processing and measurements and I wrote the paper.

V. Dual-gate induced InP nanowire diode
K. Storm, G. Nylund, M. Borgström, J. Wallentin, C. Fasth, C. Thelander and L. Samuelson
AIP Conf. Proc. 1399, 279-280 (2011)

I helped coordinate and plan the project, took a leading role in processing and measurements and I wrote the paper.

VI. Realizing Lateral Wrap-Gated Nanowire FETs: Controlling Gate Length with Chemistry Rather than Lithography
K. Storm, G. Nylund, L. Samuelson and A. P. Micolich
Nano Letters 12, 1-6 (2012), including cover artwork

I designed the structure, took a leading role in process development and electrical characterization, and participated actively in other measurements, discussions and in writing the paper.

The following papers are not included, because of overlapping content or because they deal with topics beyond the scope of this thesis.

VII. Doping Incorporation in InAs nanowires characterized by capacitance measurements
G. Astromskas, **K. Storm**, O. Karlström, P. Caroff, M. Borgström and L-E. Wernersson
Journal of Applied Physics 108, 054306 (2010)

VIII. Temperature and frequency characterization of InAs nanowire and HfO_2 interface using capacitance–voltage method
G. Astromskas, **K. Storm**, P. Caroff, M. Borgström, E. Lind and L-E. Wernersson
Microelectronic Engineering 88, 444–447 (2011)

IX. Scanning gate imaging of quantum dots in 1D ultra-thin InAs/InP nanowires
E. E. Boyd, **K. Storm**, L. Samuelson and R. M. Westervelt
Nanotechnology 22, 185201 (2011)

X. Transient studies on InAs/HfO2 nanowire capacitors
G. Astromskas, **K. Storm** and L-E. Wernersson
Applied Physics Lettters 98, 013501 (2011)

XI. Growth of vertical InAs nanowires on heterostructured substrates
S. Roddaro, P. Caroff, G. Biasiol, F. Rossi, C. Bocchi, **K. Nilsson**, L. Fröberg, J. B. Wagner, L. Samuelson, L-E. Wernersson and L. Sorba
Nanotechnology 20, 285303 (2009)

XII. A Comparative Study of the Effect of Gold Seed Particle Preparation Method on Nanowire Growth
M. E. Messing, K. Hillerich, J. Bolinsson, **K. Storm**, J. Johansson, K. A. Dick, K. Deppert
Nano Res 3, 506-519 (2010)

XIII. Charge pumping in InAs nanowires by surface acoustic waves
S. Roddaro, E. Strambini, L. Romeo, V. Piazza, **K. Nilsson**, L. Samuelson and F. Beltram
Semicond. Sci. Technol 25, 024013 (2010)

XIV. Electrical and optical properties of InP nanowire ensemble $p^+ - i - n^+$ photodetectors
H. Pettersson, I. Zubritskaya, N. T. Nghia, J. Wallentin, M. T. Borgström, **K. Storm**, L. Landin, P. Wickert, F. Capasso and L. Samuelson
Applied Physics Lettters 98, 013501 (2011)

XV. A cathodoluminescence study of the influence of the seed particle preparation method on the optical properties of GaAs nanowires
A. Gustafsson, K. Hillerich, M. E. Messing, **K. Storm**, K. A. Dick, K. Deppert and J. Bolinsson
Nanotechnology 23, 265704 (2012)

XVI. Geometric model for metalorganic vapor phase epitaxy of dense nanowire arrays
B. M. Borg, J. Johansson, **K. Storm** and K. Deppert

Journal of Crystal Growth 366, 15-19 (2013)

XVII. Transparently Wrap-Gated Semiconductor Nanowire Arrays For Studies of Gate-Controlled Photoluminescence
G. Nylund, **K. Storm**, H. Torstensson, J. Wallentin, D. Hessman and L. Samuelson
Submitted, ICPS 2012 Conference proceedings

Abbreviations

C–V	Capacitance–Voltage
CL	Cathodoluminescence
CMOS	Complementary Metal–Oxide–Semiconductor
EBL	Electron Beam Lithography
FET	Field-Effect transistor
LED	Light-Emitting Diode
MOSFET	Metal–Oxide–Semiconductor Field–Effect transistor
SEM	Scanning Electron Microscope

Chapter 1

Introduction

In his groundbreaking 1959 lecture *There's plenty of room at the bottom*, Prof. Richard Feynman considered how the ability to directly manipulate individual atoms could lead to scientific breakthroughs in semiconductor physics, chemistry and biology. In one example, he described the requirements for writing the entire 24-volume *Encyclopedia Britannica* on the head of a pin: Each page would need to be scaled down by a factor of 25 000 in both dimensions. Although the method described by Feynman—writing each letter or a representation of the letter in metal—does not lead to a commercially viable storage medium, it did offer a challenge that has inspired many of the semiconductor research efforts of the last 55 years.

Let us see how far we have come since this original proposal. By estimating the word count to be 44 million, an average of 5 letters per word and 1 byte necessary to store each letter, the space required to store all the text in *Encyclopedia Britannica* amounts to roughly 220 MB. The record in commercial hard disk drives as of October 2012 is 1.5 Tbits/in^2.[1] At this memory density, the head of the pin could hold approximately 580 MB, well surpassing the requirement. Feynman would be pleased indeed to see the original challenge realized in a commercial device of today!

This miniaturization has to a large extent been driven by the computer industry. Each generation of computer hardware has performed better than its predecessor, mainly thanks to the ability to scale the size of the basic building block, the transistor. From a size of about 10 μm in the 1970s, the gate length of transistors is today down to tens of nanometers, with almost 2 billion transistors packed on each semiconductor die.

There is, however, a fundamental change taking place in the industry today. For half a century, computing performance has been improved mainly by transistor scaling. We are now at a point where layers in the transistors are only a couple of atoms thick. It will soon be impossible to continue scaling the transistor in the

[1] http://phys.org/news/2012-10-tdk-hard-breakthrough-areal-density.html, accessed Feb 12, 2013.

straightforward manner that has been possible since the development of the first integrated circuits.

1.1 The emergence of nanowire research

The focus has thus shifted toward other ways to improve semiconductor devices. To this end, novel transistor geometries are being investigated, and semiconductor nanowires are promising candidates. As we will see, nanowires also exhibit properties that make them interesting for a wide range of application areas. Nanowires are thin wires with a diameter on the nanometer scale and essentially no limitation lengthwise, although they are commonly of the order of a few micrometers in length. The nanowire research field started in the 1960s [1]. Although not "nanowires" in the strictest sense, *silicon whiskers,* rod-like structures with a diameter in the micrometer and submicrometer range, were grown by Wagner and Ellis using a gold catalyst on silicon substrates. In their paper, the Vapor–Liquid–Solid growth process was proposed, a method still used to grow semiconductor nanowires with a metal catalyst.

In Vapor–Liquid–Solid growth, a metal catalyst, commonly gold, is placed on the surface of a semiconductor wafer. There are many ways to deposit gold particles on substrates, for example by letting a thin evaporated gold film self-organize into particles [2] or by using size-selected aerosol particles [3]. A common modern technique is shown in Fig. 1.1. An electron beam lithography (EBL) system is used to expose tiny holes in a resist film, and gold is deposited by thermal evaporation under high vacuum conditions (Fig. 1.1a–e). A scanning electron microscope (SEM) image of the resulting pattern of gold particles is shown in Fig. 1.1f.

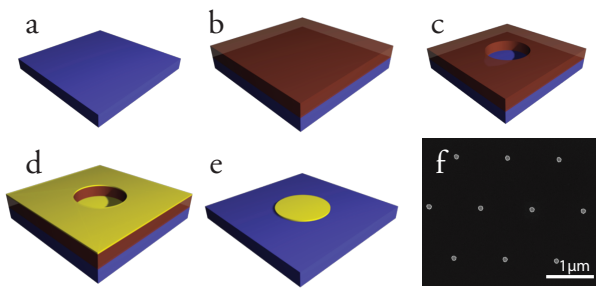

Figure 1.1: *Definition of gold particles with EBL. A semiconductor substrate (**a**) is covered by a thin resist film (**b**). An EBL is used to expose small dots in the film (**c**), and gold is evaporated (**d**). The sample is submerged in a solvent, which removes the resist and all gold except in the exposed regions (**e**). SEM image of the final particle pattern (**f**). Gold particles appear gray on a black background.*

The sample is then loaded into a growth reactor. Nanowires can be grown by many methods, for example chemical beam epitaxy (CBE) [4], metal-organic

vapor-phase epitaxy (MOVPE) [5] or molecular beam epitaxy (MBE) [6]. As the sample is heated, and growth material such as trimethylindium and tertiarybutylarsine in the case of InAs epitaxial growth is added to the chamber, the growth material is preferentially collected by the gold droplet. The material then precipitates at the bottom of the droplet, causing a pillar-like structure to grow, with the gold droplet riding on top. The diameter of the nanowire is primarily determined by the size of the gold droplet, and is typically designed to be less than 150 nm. Figure 1.2 shows an SEM image of an array of InAs nanowires standing vertically on a substrate. The nanowires in this example have an average diameter of 40 nm and length of 1 μm. The nanowires can either be processed as-is or broken off and transferred to a different substrate for further processing.

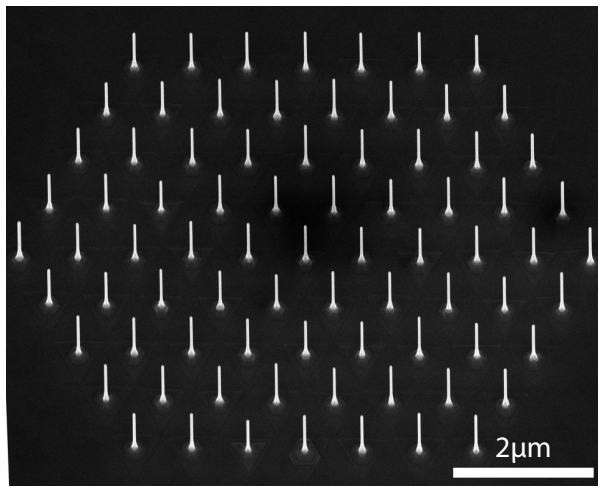

Figure 1.2: *SEM image of an array of InAs nanowires.*

In the years following the discovery by Wagner and Ellis, the materials available for nanowire growth were extended to include GaP [7], Ge [8], GaAs [9] and InAs [10], but progress was relatively slow, and nanowires had still not attracted the attention necessary for accelerated research efforts. In the early to mid 1990s, the nanowire research started to gain momentum, in particular owing to the successful efforts reported by the Hiruma group at Hitachi [11–13] on growth of GaAs and InAs nanowires, and the Lieber group at Harvard developing growth of carbide [14] and oxide [15] nanowires. In 2002, independent reports of heterostructured nanowires from the Samuelson group [4, 16, 17], the Lieber group [18] and the Yang group [19] were published, enabling further exciting experiments. Over the last decade, the research field of semiconductor nanowires has experienced a tremendous expansion. Figure 1.3 shows the number of *daily* journal publications containing the search term *nanowires*.[2] It is evident that the subject of nanowires is a heavily researched one, showing no trace of diminishing growth.

[2]Collected using http://www.sciencedirect.com

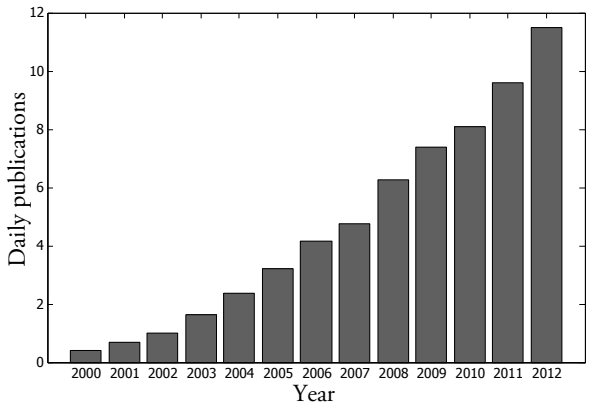

Figure 1.3: *Number of daily journal publications containing the search term* nanowires.

1.2 Nanowire applications

Why are nanowires interesting to study? They offer many benefits not readily available to bulk materials. This enables applications and optimizations difficult to realize in classical semiconductor systems. Thanks to their small footprint, crystal strain can be relaxed at the periphery of the nanowire [17–20]. This allows growth of non-lattice-matched materials not easily combined in the bulk geometry, such as the InP/InAs [16] and Si/Ge [21] material systems. Combined with the nanometer dimensions attainable using nanowires, this enables studies of fundamental quantum mechanical model systems [16, 22, 23] as well as integration of optically active materials on Si [24]. The development of radial nanowire heterostructures allows growth along crystal directions difficult or expensive to realize in planar epitaxial growth, for example along the nonpolar $\{1\bar{1}00\}$ m-plane of GaN [25, 26]. Finally, the near-cylindrical symmetry of nanowires lends itself naturally to electric gates that are wrapped around the entire semiconductor, enabling field-effect transistors [27, 28] and tunnel field-effect transistors [29] with the promise of optimized gate control, enhanced switching speed and lowered energy consumption.

Many of these inherent benefits of nanowires have already been translated into exciting devices that enable new physics or potential new commercial applications. Technologies enabling patterning of samples for growth of nanowires in ordered arrays, such as EBL, illustrated in Fig. 1.1, or even more promising, nano-imprint lithography [30], now allow the growth of highly optimized nanowire arrays over large-area substrates. These recent developments open up the possibility for large-scale production of nanowires and may enable implementation of nanowires in commercially viable devices.

1.2.1 Nanowire field-effect transistors

In a field-effect transistor (FET) the gate is used to open or close a channel in the semiconductor between the source and the drain terminals. To gate the device efficiently, the coupling of the gate to the channel needs to be optimized. Nanowires promise optimal gate control thanks to their near-cylindrical symmetry. This is quantitatively described in Section 4.1, but originates from the fact that gating a semiconductor is more efficient if the gate couples to the entire periphery of the transistor channel, as opposed to only acting from one side. This well-known fact has instigated numerous experiments where so-called *wrap-gate* or *gate-all-around* devices have been modeled, fabricated and analyzed.

In the wrap-gate design, an electric insulator is deposited onto the semiconducting nanowire, and the structure is then embedded in a gate electrode that wraps around the entire periphery of the nanowire (see Fig. 1.4). One of the first devices of this type was a vertical InAs nanowire transistor comprising multiple nanowires connected in parallel, demonstrated by Bryllert et al. [27]. This incited an intense research effort generating numerous publications. Notable papers describe a refined FET with a 50 nm gate length [31], InAs nanowire FETs integrated on silicon [28], silicon nanowire FETs [32] and high-frequency InAs devices integrated on silicon [33, 34]. Furthermore, complementary metal–oxide–semiconductor (CMOS) circuits have been realized in single nanowires [35, 36].

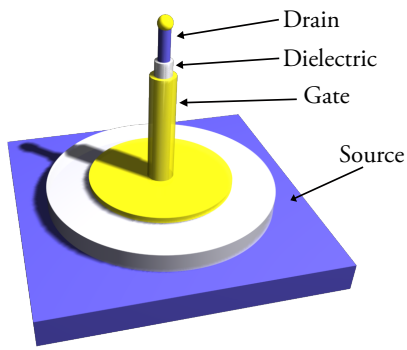

Figure 1.4: *Illustration of the components of a vertical nanowire wrap-gate transistor. The nanowire is insulated by a gate dielectric such as* HfO_2 *and capped with a conductive gate electrode. Typically, the source and drain are formed by electrical connections to the substrate and the tip of the nanowire.*

Traditional metal–oxide–semiconductor field-effect transistors (MOSFETs) have a minimum inverse subthreshold slope of 60 mV/dec at room temperature, causing high off-currents at low drive voltage. This makes them unsuitable for low-power applications. To this end, nanowires have also shown promise for novel transistor designs such as the tunnel FETs demonstrated in silicon [37–40] and InP/GaAs

[41] that promise an inverse subthreshold slope far below the 60 mV/dec limit. Other types of low-power transistors such as impact-ionization transistors using multiple gates are also being investigated in nanowire systems [42], reaching an impressive inverse subthreshold slope of 5 mV/dec.

One main driving force behind these experiments is further CMOS transistor scaling, in which it is necessary to solve issues such as high leakage current while maintaining high drive current. The optimized gate geometry is an attractive route, and the fact that Intel has already implemented the trigate transistor structure in their 22 nm node, a transistor geometry in which the gate is partially wrapped around the semiconductor channel, is a clear indication that geometries with optimized gate control are also of interest for commercial applications.

1.2.2 Light-emitting diodes

Conventional light-emitting diodes (LEDs) can now be made with emission wavelengths spanning the entire visible spectrum. High-efficiency LEDs emitting in the blue and green range are primarily made from the InGaN material system, whereas yellow, orange and red LEDs are primarily made from AlGaInP. Red and blue LEDs can be made with high luminous efficiency, whereas improving the efficiency of green LEDs remains challenging. This is sometimes referred to as the *green gap*. The InGaN material system can in principle cover the entire visible spectrum; however, the luminous efficiency rapidly drops for In compositions higher than 30%. This originates from the lattice mismatch between InN and GaN, together with the polarization fields present along the c-plane, the direction primarily used for InGaN LED growth. The polarization fields separate the electron–hole pairs in the LED quantum wells, decreasing the efficiency, an effect whose severity increases with increasing In content.

GaN nanowires grown in the c-direction, however, have nonpolar m-plane side facets [43]. It is believed that these m-plane facets allow high-efficiency electroluminescence and may enable one of the first commercially viable nanowire LED devices. Many nanowire implementations of LEDs have already been realized, for example cross-nanowire InP LEDs [44, 45], axial InP/InAs LEDs [46], radial GaN LEDs [47] and radial GaP LEDs [48], and multiple companies are working on developing commercially viable GaN LEDs, including the Lund-based GLO and the Grenoble-based HelioDEL.

Figure 1.5 shows SEM images of GaN nanowires implemented in nanowire LEDs by the GLO AB company. Nano-imprint lithography is used to produce openings in a Si_3N_4 film, and core–shell n–p junction nanowires with an active quantum well region are grown on 2 in wafers. Figure 1.5a and b show the uniformity and detail of as-grown GaN nanowires. The finished die, shown in Fig. 1.5c, consists of an anode, a cathode and an indium tin oxide transparent current spreading layer.

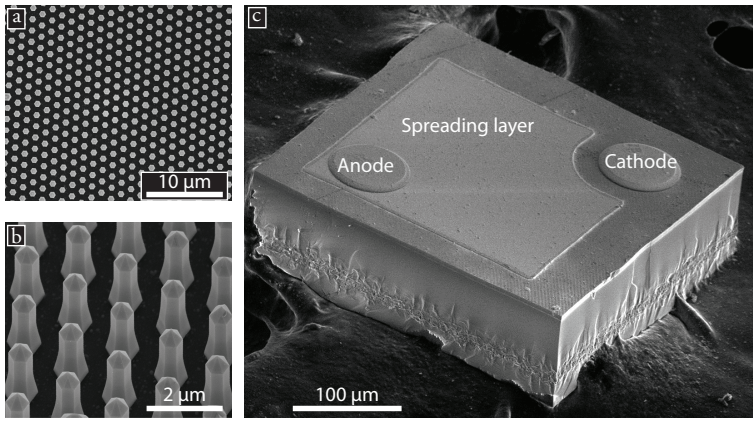

Figure 1.5: *GaN nanowire LED made by GLO AB.* ***a*** *and* ***b*** *array of GaN nanowires grown through a nano-imprint-lithography-defined mask on a 2 in wafer.* ***c*** *Finished LED die showing anode, cathode and indium tin oxide current spreading layer.*

The nonpolar m-plane facets of the nanowires grown in the c-direction promise light emission from nonpolar active regions, which alleviates the problems associated with the green gap. Together with strain relaxation offered by nanowires [49], this enables more efficient green, amber and red emitters made from the InGaN material system. Figure 1.6 shows GaN nanowire LEDs made by GLO emitting in the blue, green, amber and red spectrum regions. Another interesting aspect of nanowire emitters is the increased effective active area compared to substrate area. This enables higher luminous flux per unit area of LED die.

These benefits do not, however, come without challenges. The geometry makes nanowire LEDs complicated to process compared to their planar counterparts. Furthermore, careful engineering of the nanowire contacts and quantum wells must take place to ensure a homogeneous injection current density along the nanowire m-plane facets.

Figure 1.6: *GaN nanowire LEDs made by GLO AB, emitting in the blue, green, amber and red wavelength regions.*

1.2.3 Solar cells

The amount of solar power impinging on the earth corresponds to a couple of thousand times the power consumption of modern society [50]. Harvesting a small portion of this energy is therefore an attractive option, providing a "free" energy source without significant greenhouse gas emission or other environmental impacts. To utilize this enormous energy resource, cheap solutions must be found to produce reliable solar cells of high efficiency. Expensive multijunction solar cells are currently able to convert solar energy to electricity with an efficiency of 37.7% for cells that do not use sunlight concentration and 44% for those with concentration [51]. The record for solar cells produced on cheaper Si substrates is currently 25.0% [51].

One of the main problems of combining high-efficiency III/V solar cells with cheap Si substrates in the planar geometry is lattice mismatch, causing crystal defects that act as recombination centers. Nanowires offer the opportunity to realize these material combinations with much less strict restrictions on lattice constant matching. Over the last few years, nanowire solar cells in various material systems such as GaAs [52] and InP [50, 53, 54] have been implemented. Recently, a new record for nanowire solar cells was set at 13.8% using InP nanowires [55]. In that paper, it was shown that, with only 12% surface coverage of nanowires, the cells delivered 83% of the photocurrent density of corresponding planar solar cells. This remarkable observation originates in the fact that arrays of nanowires allow higher absorption than their planar counterpart. Furthermore, a novel fabrication method using aerotaxy was recently demonstrated [56] that, if it proves

possible to implement for solar cell applications, offers cheap mass production of nanowires. Although many challenges remain before the devices are commercially viable, nanowires appear to be an attractive route to highly efficient and cheap solar energy harvesting.

1.3 Challenges in nanowire characterization

It is clear that nanowires have many advantages not easily attainable in conventional bulk devices and promise novel device implementations. One of the most important, if not *the* most important, technological development necessary for fabricating and optimizing devices is the ability to precisely engineer and characterize doping profiles in the material. The ability to control the conductivity, and hence the potential landscape, of both axial and radial nanowire structures is crucial for the realization of most practical devices. The ability to characterize the material properties accurately is essential for device optimization.

The technology to dope semiconductor nanowires both n-type and p-type has been actively researched in the last two decades, and it is now possible to perform in-situ n-type and p-type doping of Si, Ge and essentially all III–V nanowires [57]. However, despite the progress in doping nanowire material, the ability to electrically quantify the carrier density of nanowires remains in the development stage.

The most common method involves fabricating MOSFET devices from the nanowires of interest, and studying their transfer characteristics. By determining the maximum transconductance, $g_m = \partial I_{sd}/\partial V_g$, from the source–drain current I_{sd} and gate voltage V_g of the transistor, the mobility, μ, can be deduced from

$$\mu = g_m \frac{L^2}{V_{sd} C}$$

where L is the channel length, V_{sd} is the source–drain voltage and C is the gate–channel capacitance. Once the mobility is known, the carrier density n can be determined from the relation $\sigma = qn\mu$, where σ is the material conductivity and q is the elementary charge.

This method, however, suffers from a number of limitations. The source and drain contact resistances should be lower than the channel resistance in the linear transconductance regime, and the gate capacitance must be accurately calculated. Owing to the nonmetallic density of states of moderately doped semiconductors [58–61], as well as the nonideal device geometries often used (see Section 4.1), the gate capacitance is difficult to estimate accurately, leading to errors in the mobility and doping calculations. Furthermore, field-effect measurements probe the mobility close to the surface of the semiconductor where surface scattering may have a substantial effect [62]. This is different from Hall measurements in bulk samples, in which the extracted mobility represents bulk carrier scattering. Although the Hall mobility and field-effect mobility can be correlated for different materials [63, 64], this is seldom done, resulting in the calculations yielding a lower bound for the mobility.

1.4 Aim of the thesis

This thesis describes the development of processing and characterization methods for nanowires. It specifically covers three aspects:

- Spatially resolved Hall effect measurements on single nanowires.
- Capacitance–voltage measurements on arrays of nanowires.
- Manipulation of the Fermi level in nanowires using wrapped and semiwrapped gates.

In Chapter 2 it is shown how the Hall effect can be used to quantify both carrier density and carrier mobility with spatial resolution in core–shell InP nanowires (Paper I). Hall measurements are traditionally used to characterize 2D epitaxial layers and is an extremely useful method that has never before been used on nanowire systems.

In Chapter 3, capacitance–voltage (C–V) measurements on nanowires are described (Papers II and III). C–V measurements have conventionally been used for the characterization of bulk semiconductors, and this chapter describes how the C–V method was applied to arrays of InAs nanowires for the first time.

Finally, in Chapter 4, gated nanowire devices are explored in more detail (Papers IV, V and VI). The field-effect method was applied to InP nanowires to measure the carrier mobility, and from the resulting MOSFETs, ambipolar behavior was demonstrated in the nanowires. This enabled the fabrication of a *field-effect diode*, a device in which two gates are used to induce a p–n junction in a nanowire without the need for impurity doping of the active region. A new process is also described that allows a fully wrapped gate to be implemented on a nanowire that is laterally positioned on a substrate.

Chapter 2

Hall effect measurements

Material characterization and control in nanowires have yet to reach the level of bulk semiconductor materials, despite many years of ever more intense research efforts (see Fig. 1.3). High controllability over growth parameters such as doping incorporation, carrier mobility, material composition and growth rate is essential for fabricating more advanced devices for basic research and moving past the proof-of-concept level for applied devices. To attain higher control and better material quality, powerful and routinely utilized characterization techniques are necessary. Unfortunately, the 3D nature of the nanowire geometry has long meant that the use of conventional electrical characterization techniques has been challenging. The ability to measure material properties accurately has therefore struggled to keep up with the rapid expansion of this research field.

Two key methods long used for the characterization of conventional bulk epitaxial layers are C–V spectroscopy and Hall measurements. In this chapter we discuss how Hall measurements are implemented on nanowires (Paper I). The Hall effect enables spatially resolved determination of carrier density and mobility and is a technique that has previously been unavailable to the nanowire community. We then discuss in Chapter 3 how C–V measurements can be implemented on nanowires.

2.1 Classical Hall effect measurements

Hall measurements are conventionally and routinely used to characterize semiconductor epitaxial layers and metal samples. This useful characterization method originates from the fact that a particle of charge q moving at velocity $\bar{v}$ in an electric field $\bar{E}$ and a magnetic field $\bar{B}$ experiences the Lorentz force $\bar{F}$,

$$\bar{F} = q\left(\bar{E} + \bar{v} \times \bar{B}\right).$$

Assume we source a current I through a slab of semiconductor of thickness t as shown in Fig. 2.1.

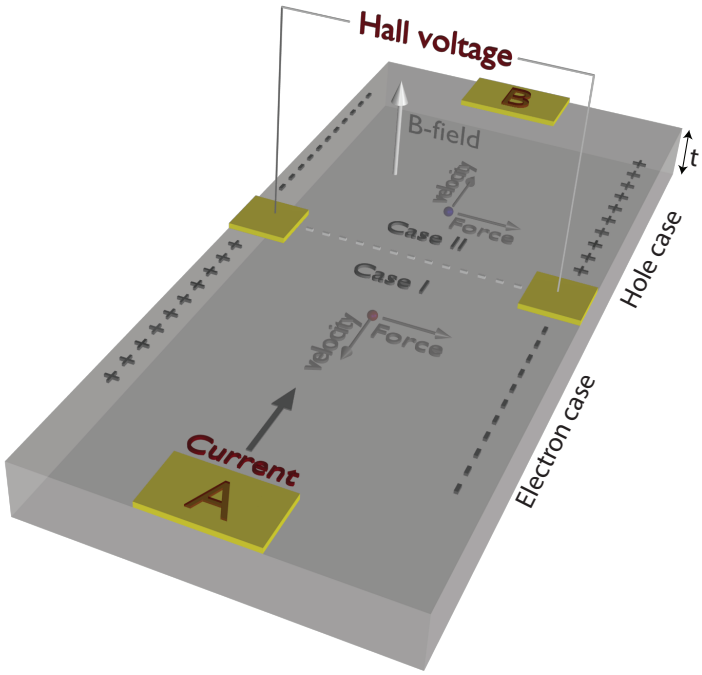

Figure 2.1: *Illustration of the Hall principle. A charged particle experiences a force due to an applied magnetic field. The case for negatively charged electrons carrying the current is shown as Case I, and that for positively charged holes as Case II.*

A magnetic field is applied perpendicular to the sample plane, and the current I is passed along the sample from terminal A to terminal B. Two electrodes oriented on opposite sides of the sample, on a line perpendicular to the current flow, are used to measure the Hall voltage V_H across the sample. For an n-type semiconductor of electron concentration n, the current is predominantly carried by electrons. This is illustrated in Case I in Fig. 2.1. Owing to the applied magnetic field, an electron moving from terminal B to terminal A will experience a force perpendicular to the current direction. For macroscopic samples in the nonballistic regime, electrons are curved between each scattering event. This gives rise to an inhomogeneous charge distribution in the sample and an electric field directed perpendicular to the current flow as illustrated in the figure. The resulting Hall voltage V_H can be derived as

$$V_H = \frac{BI}{qnt} \tag{2.1}$$

where B is the magnitude of the magnetic field. The corresponding case for a p-doped semiconductor, in which holes are dominant charge carriers, is illustrated in Case II. The Hall voltage measured in the case of hole conduction is identical in magnitude but with opposite sign. This is thus a convenient method to determine both the type of charge carrier in the sample and for determining the carrier density

by varying either the magnetic field B or the sourced current I. Once the carrier density is known, the mobility can be calculated from four-point measurements using the Drude conduction model

$$\sigma = q\,(n\mu_n + p\mu_p)$$

where p is the hole density and μ_n and μ_p are the electron and hole mobility, respectively.

2.1.1 Hall measurements for small samples

Measurements of the Hall effect in small samples introduce some challenges not present in a macroscopic sample. One of the main challenges arises because the physical dimensions of the Hall voltage-sensing terminals cannot be considered to be infinitesimal compared to the size of the sample. In the derivation of Eqn. (2.1) it is assumed that the distance between the Hall voltage terminals is equal to the width of the sample. We can easily check the validity of this approximation as the width of the sample is gradually decreased while maintaining a constant contact size. Figure 2.2 shows a simulation for a planar slab of semiconductor of thickness 200 nm, contact size $50 \times 50\,\mathrm{nm}^2$ and electron concentration $10^{18}\,\mathrm{cm}^{-3}$.

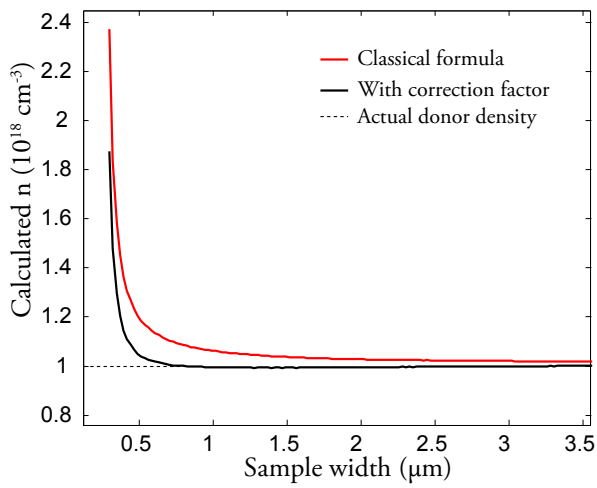

Figure 2.2: *Illustration of breakdown of validity of Eqn. (2.1). When the contact size is no longer infinitesimal compared with the sample width, the classical formula returns erroneous results. Taking the finite contact size into account improves the result but is nevertheless inadequate for the regime of sample width below ∼500 nm.*

The width of the sample is gradually changed, and the carrier concentration, calculated using the classical formula in Eqn. (2.1) from the simulated Hall voltage, is plotted on the vertical axis (red curve). For a sample width larger than a few micrometers, we see that Eqn. (2.1) approaches the correct result. In the regime

below 1 μm, however, we obtain erroneous results with an overestimated carrier density due to the finite size of the terminals.

However, Eqn. (2.1) can easily be partially mended by taking into account the finite contact size. The resulting equation modifies 2.1 by introducing a correction factor w_c/w, where w_c is the distance between the points at which the Hall terminals probe the potential and w is the width of the sample

$$V_H^* = \frac{BI}{qnt} \cdot \frac{w_c}{w} \tag{2.2}$$

From Fig. 2.2, we find that the modified expression (black curve) correctly extracts the carrier density down to approximately 500 nm sample width. However, it still does not adequately describe a nanowire system, in which the dimensions are typically smaller by a factor of two. As described in Section 2.2, simulation tools can be used to more accurately calculate the carrier density from the experimental data.

2.2 Hall effect in nanowires

Nanowires offer additional challenges for performing Hall measurements. Not only are we measuring a small sample, but we also need to take into account the complex nanowire geometry. In Paper I, Hall measurements on nanowires are demonstrated. For this study, InP nanowires were grown by metal-organic vapor-phase epitaxy. The growth takes place by first growing a p-type core on a nano-imprint lithography patterned substrate, using Zn as dopant. The sample is then taken out of the reactor, the gold catalyst is removed by KI/I_2 etching and an n-type shell is grown radially on top of the core using S as dopant material (see Fig. 2.3).

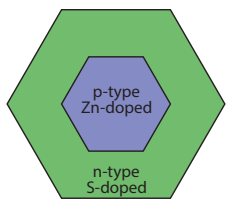

Figure 2.3: *Illustration of the cross-section of metal-organic vapor-phase-grown InP nanowires used for the Hall measurements.*

The nanowires are then transferred to an insulated silicon substrate, and metal connections are defined with EBL. The relatively large diameter of approximately 200–300 nm of these radial structures makes it challenging to directly deposit electrical contacts, owing to the vertices of the hexagonal nanowire cross-section causing discontinuities in the metal film. A novel lifting layer was therefore designed (see Fig. 2.4).

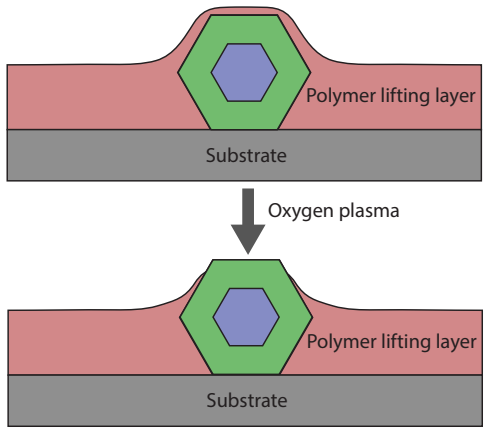

Figure 2.4: *Definition of the self-aligned polymer lifting layer.*

This lifting layer is defined by spinning a diluted photoresist thin film onto the sample. The thin film automatically aligns itself to the highest feature of the nanowire. By a short oxygen plasma process, the top facet of the nanowire is exposed, while the rest of the nanowire remains embedded in the polymer. This process, similar in concept to a previously published method using spin-on glass [65], allows contacts to be defined by EBL with high resolution and is one of the key enablers of the nanowire Hall measurements.

After the polymer layer has been deposited, the Hall devices are defined by a single EBL step combined with metal evaporation and lift-off. The resulting device is shown in Fig. 2.5. In this system, the current is sourced through the n-type shell of the nanowire using terminals AH (inset), and the pairwise terminals BC, DE and FG are used to measure the Hall voltage as a magnetic field is applied perpendicular to the substrate plane. Figure 2.6 shows an illustration of the cross-section of the device.

It is not immediately obvious that Eqn. (2.2) accurately describes the complex geometry of a nanowire system. In the core–shell geometry of the radially grown nanowire device, the layer probed by the Hall measurements forms a hexagonal thin film in contrast to the planar films traditionally characterized with the Hall method. Furthermore, the nanowire p–n junction gives rise to a depletion region that will affect the effective electrical thickness of the shell.

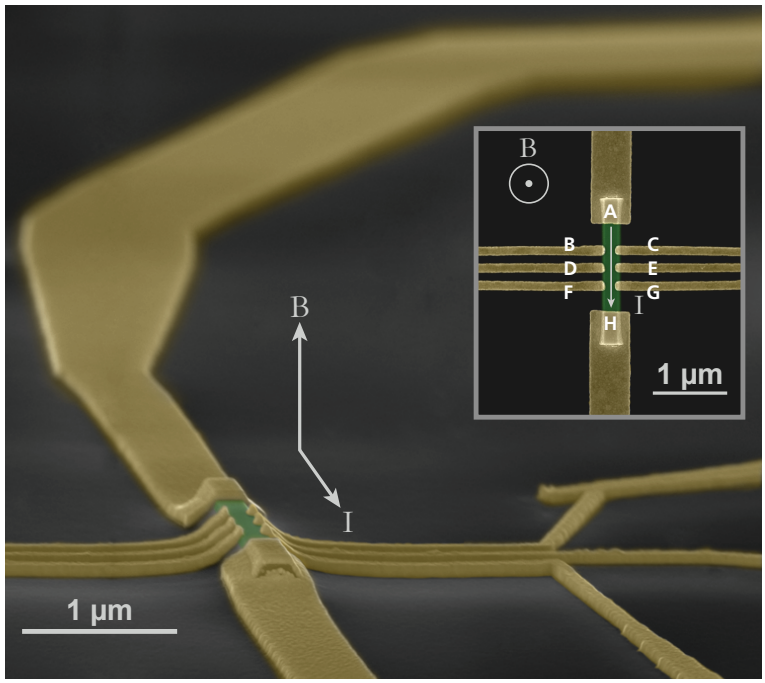

Figure 2.5: *The device used to measure Hall voltage in a core–shell InP nanowire. The inset shows details of the terminal layout.*

We can rewrite Eqn. (2.2) in a more general form that is also applicable to the nanowire geometry:

$$V_H^* = \frac{Bj}{qn} w_c \tag{2.3}$$

where j is the current density in the shell of the nanowire. It is fairly clear from the previous sections that an analytical approach to Hall effect measurements in nanowires has its inherent shortcomings. With the exception of cases in which the current is carried in a very thin layer close to the surface, such as the surface accumulation layer in InAs [66] where the resulting Hall voltage can be calculated from a resistor network model [67], the Hall effect in nanowires is nontrivial to calculate. Not only are nanowires small samples, in which the assumption of infinitesimal contact points compared to the sample size is no longer valid, but they also have a nontrivial geometry that further complicates the analysis. It is thus helpful to employ simulation methods to investigate how Hall effect measurements in a nanowire should be interpreted.

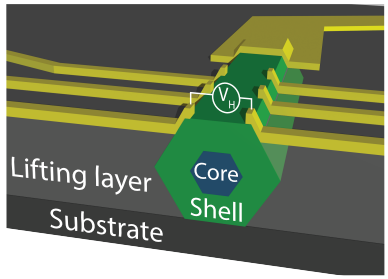

Figure 2.6: *Details of the design of the Hall device.*

2.2.1 2D Poisson simulations

Owing to the radial p–n junction present in this system, it is important to carefully consider how the properties of this junction may affect the conduction through the shell. The main contribution from the p–n junction is a decrease in the effective electrically active area due to the depletion region extending into the nanowire shell. In a conventional planar p–n junction, the Poisson equation can easily be solved analytically within the depletion approximation to find the depletion width. This has the well-known result that the impurity doping concentration of the low-doped side determines the extension of the depletion region, W_d, according to

$$W_d = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A \cdot N_D}\right)(V_{bi} - V_a)} \approx \underbrace{\sqrt{\frac{2\varepsilon}{q}\frac{1}{N_D}(V_{bi} - V_a)}}_{p^+-n} \approx \underbrace{\sqrt{\frac{2\varepsilon}{q}\frac{1}{N_A}(V_{bi} - V_a)}}_{p-n^+} \tag{2.4}$$

for the cases of a p$^+$–n ($N_A >> N_D$) and a p–n$^+$ ($N_D >> N_A$) junction. In Eqn. (2.4) N_A is the acceptor concentration on the p-side, N_D is the donor concentration on the n-side, ε is the material permittivity, V_{bi} is the built-in voltage of the junction and V_a is the voltage applied to the p-side.

We now compare the validity of different models to evaluate the effect from the junction in the case of a hexagonal p$^+$–n core-shell nanowire. We can simplify the discussion by approximating the hexagonal cross-section of a nanowire as a cylinder. Finding the solution for a cylindrically symmetric p–n junction is not as straightforward as the planar case, but it is possible with a combination of analytical and numerical approaches (see Appendix A.1 for a derivation). To illustrate the effect of the junction, Fig. 2.7 shows a comparison between simulated and analytical solutions for the conduction band energy for hexagonal, cylindrical and planar one-sided p$^+$–n junctions with core p-type doping $5{\cdot}10^{18}$ cm^{-3} and shell n-type doping 10^{17} cm^{-3}, calculated for an InP nanowire system. The simulations were done in the COMSOL Multiphysics environment.[1] Details on the simulation framework can be found in Appendix A.2. The potential for the hexagonal p–n junction has been evaluated along two paths: through the hexagon vertex and

[1] http://www.comsol.com

through the facet. For the cylindrical case, a radius r_j inscribed as shown in the inset with equivalent area as the core hexagon, $\pi r_j^2 = \frac{3\sqrt{3}}{2}t^2$, where t is the side length of the hexagon, is used as the metallurgical position of the junction.

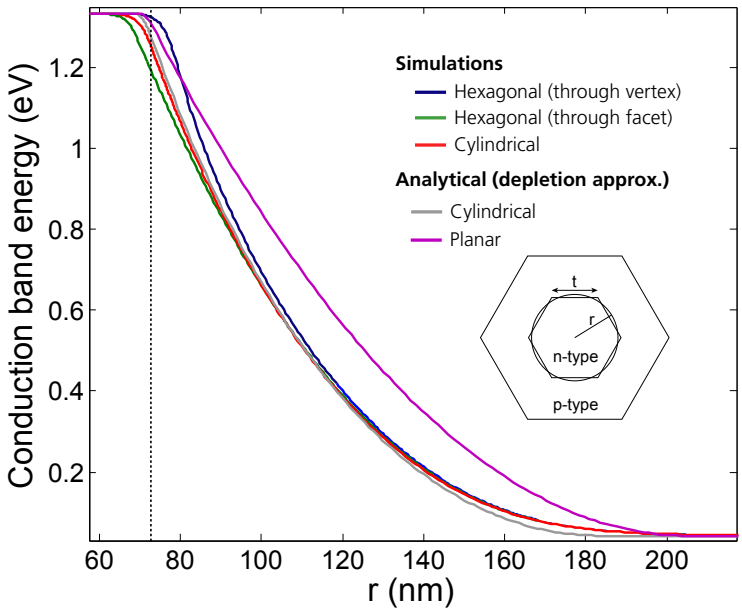

Figure 2.7: *Solutions for the conduction band in InP hexagonal, cylindrically symmetric and planar p–n junctions. The Fermi level is set at 0 eV and the side length of the hexagonal core is* $t = 80\,\mathrm{nm}$. *The dotted line marks the position of the metallurgical* p^+*–n junction for the cylindrically symmetric case.*

From Fig. 2.7, a number of conclusions can be drawn. As expected, the potentials evaluated through the vertex and the facet of the hexagonal p–n junction differ owing to the asymmetry of the geometry. The simulated potential for the cylindrical p–n junction acts as an average model for the hexagonal geometry, becoming approximately identical to both hexagon potentials at large radii. Furthermore, the analytical solution to the cylindrical p–n junction agrees reasonably well with the simulated cylindrical potential, except at the edges of the depletion region. We can thus conclude that the cylindrical approximation may be adequate for estimates of the depletion width for one-sided p–n junctions, but that the differences between the hexagonal case must be kept in mind. Finally, we note that the depletion approximation for a planar p–n junction has significant error throughout the depletion region and cannot satisfactorily be used to approximate the cylindrical p–n junction.

We now return to the nanowire p–n junction discussed in Section 2.2. Figure 2.8 shows a simulation of the potential for a matching core acceptor and shell donor concentration of $1 \cdot 10^{18}\,\mathrm{cm}^{-3}$. The solid hexagon in Fig. 2.8a shows the

position of the metallurgical junction. We find that the depletion region extends into the shell of the InP core–shell nanowire and may thus affect the analysis of the experimental Hall data. However, a closer look at the depletion width dependence on shell donor concentration reveals that the effect on electrical shell thickness is less than 5% for a shell doping higher than $1 \cdot 10^{18}\,\mathrm{cm}^{-3}$. For low donor concentration, this effect must therefore be taken into account, whereas it is negligible for higher donor concentrations.

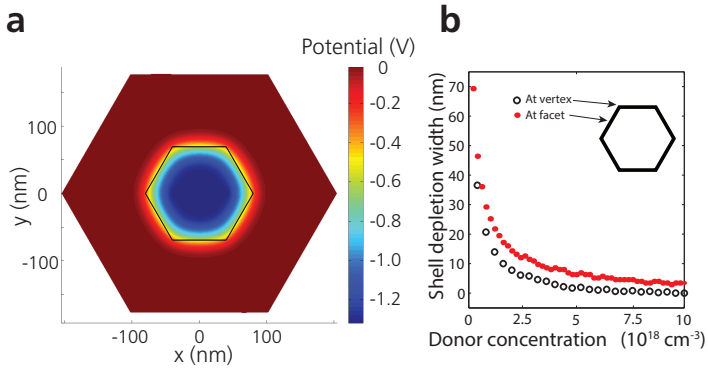

Figure 2.8: ***a*** *Simulation of the potential distribution in a radially grown InP nanowire p–n junction intended for Hall effect measurements.* ***b*** *The extension of the depletion region in the shell is calculated as a function of shell donor concentration.*

2.2.2 3D current-continuity modeling

Once the effective electrical thickness of the nanowire shell is known, the hexagonal shell is approximated as a conductive medium. As a current is fed through the length of the shell, we need to solve for the current distribution $\bar{J}(\bar{r})$ and potential $V(\bar{r})$ in the medium under the influence of a magnetic field. Here, $\bar{J}$ and V are related by Ohm's law

$$\bar{J} = -\bar{\sigma} \cdot \nabla V$$

where $\bar{\sigma}$ is the conductivity tensor

$$\bar{\sigma} = \sigma_0 \begin{pmatrix} \frac{1}{1+(\omega\tau)^2} & -\frac{\omega\tau}{1+(\omega\tau)^2} & 0 \\ \frac{\omega\tau}{1+(\omega\tau)^2} & \frac{1}{1+(\omega\tau)^2} & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

which takes into account the magnetic field $\bar{B} = (0, 0, B)$ through the cyclotron radius $\omega = qB/m$, where m is the mass of the particle. See Appendix A.3 for a derivation and a discussion of the conductivity tensor. Figure 2.9a shows the design for the COMSOL simulations. By adjusting the dimensions of the hexagonal shell and the Hall terminals to match the experimental conditions, the Hall voltage can be simulated as a function of current and carrier density.

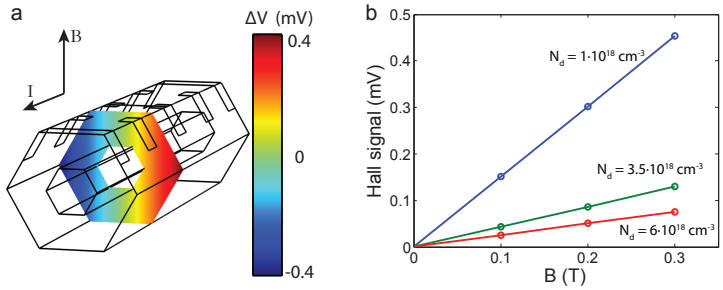

Figure 2.9: *3D current-continuity simulations.* ***a*** *The dimensions of the structure are chosen to correspond to the dimensions in the processed sample. An example of the simulated potential distribution is shown in the cross-section of the nanowire.* ***b*** *Examples of simulations for various doping densities.*

Figure 2.9b shows Hall voltage simulations for three carrier densities of the InP nanowire shell. This data can then be used to fit the experimental Hall data.

2.2.3 Experimental nanowire Hall characteristics

Figure 2.10 shows experimental Hall data for the device design demonstrated in Fig. 2.5. The three datasets correspond to measurements between the different terminal pairs BC, DE and FG. Running the simulations described in the previous sections yields carrier densities of $5.6 \cdot 10^{18}\,\mathrm{cm}^{-3}$, $1.7 \cdot 10^{18}\,\mathrm{cm}^{-3}$ and $7.5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ at the three different positions, respectively. These results can be compared with the carrier densities obtained by using the analytical approximation in Eqn. (2.3), which yields $3.3 \cdot 10^{18}\,\mathrm{cm}^{-3}$, $9.9 \cdot 10^{17}\,\mathrm{cm}^{-3}$ and $4.5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ from the same data. The analytical approach does yield reasonable, although slightly underestimated, values. These results indicate that the shell exhibits a doping gradient along the axis of the nanowire. This is somewhat surprising, but one explanation may be local height variations in the effective V/III ratio during growth. This effect is known in GaAs and has been shown in previous studies [68].

One way to verify the Hall measurements is to switch the current direction and redo the Hall measurements. However, the devices are highly rectifying, making this type of measurement challenging. This rectification is believed to arise from the contact resistances at terminals A and H. The direction of rectification is consistent with the nanowire end closest to terminals FG being rectifying and of high resistance, indicating a lower doping concentration in this region. This is thus consistent with the experimental Hall data. Furthermore, four-point conductivity measurements along nanowires grown on the same substrate indicates similar behavior in material conductivity, providing further evidence that a doping gradient does exist in the nanowire shell. It has been predicted that engineering of the doping concentration along the nanowire axis must be performed to optimize nanowire devices such as LEDs [69]. It is therefore of interest to study, and to control, this behavior and utilize it to produce optimally performing nanowire

devices.

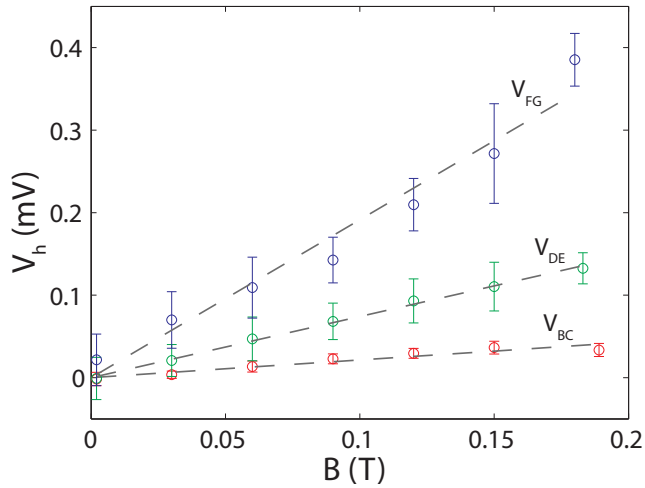

Figure 2.10: *Experimental data from Hall measurement on a single-nanowire device.*

One of the main benefits of the platform used to perform Hall measurements is the ability to employ optical characterization tools on the same set of samples. Additional measurements provide supplementary information on the optical properties of the nanowires. One of these tools is cathodoluminescence (CL).

In CL measurements, a beam of electrons from an SEM is used to excite the semiconductor material. The photons emitted from the semiconductor are then collected and analyzed. Thanks to the ability to focus the electron beam onto a small area, this method allows position-dependent optical measurements. CL measurements have previously been used to study, for example, how the seed particle preparation method affects the optical properties of GaAs nanowires [70] and how various axial and radial heterostructures affect carrier diffusion in GaAs and AlGaAs nanowires [71], as well as to study quantum dot structures in nanowires using CL combined with transmission electron microscopy [72].

In Paper I, CL was used to further study the carrier density gradient discovered using the Hall measurements. The setup used to perform the measurements is illustrated in Fig. 2.11. It was found that the peak emission wavelength shifted as a function of position on the nanowire. By correlating this shift with a theoretical model [73], the conclusion that a doping gradient was present in the nanowire shell was further corroborated.

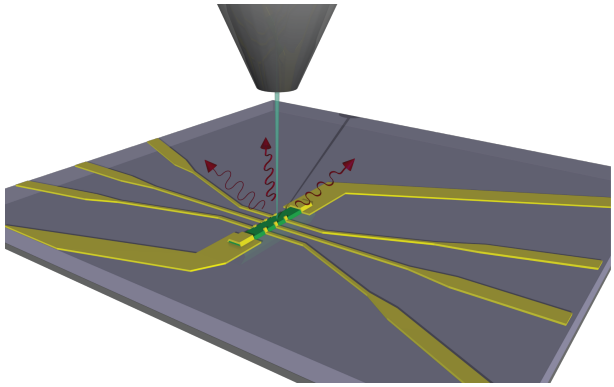

Figure 2.11: *Illustration of the setup used for cathodoluminescence measurements.*

2.2.4 Limits for nanowire Hall measurements

There are essentially two aspects that govern the range of applicability of the nanowire Hall measurements: the range of nanowire diameters that can be incorporated into Hall devices, and the magnitude of the Hall voltage. The main concern of Hall device fabrication for small diameters is the procedure of aligning the terminals to the nanowire. As shown in Fig. 2.12, using the current fabrication procedure, it is possible to produce Hall terminals with a separation of less than 30 nm and to align the terminals to nanowires of diameter 80 nm. However, to apply the structure to 80 nm or smaller nanowires, the process must be further optimized to attain a satisfactory yield. This can be achieved, for example, with optimized alignment markers [74].

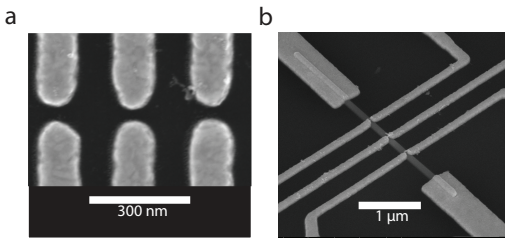

Figure 2.12: *SEM images showing the limitations of the Hall measurements.* ***a*** *Hall terminals of spacing ∼30 nm.* ***b*** *These closely spaced terminals can be aligned to nanowires of 80 nm diameter.*

Using the relation $j = qn\mu V_l/l$, where V_l is the longitudinal voltage necessary to reach a given current level, and l is the length of the sample, we can rewrite Eqn. (2.3) as

$$\frac{dV_h}{dB} = \frac{\mu V_l w_c}{l}$$

to briefly discuss the limitations of the Hall measurements. In this somewhat naïve model, the Hall signal dV_h/dB is proportional to both the carrier mobility μ and the applied longitudinal voltage V_l. The mobility depends on multiple factors, but the doping incorporation has greatest influence, with mobility decreasing as doping incorporation increases [75]. Thus, increasing the doping concentration increases the current density for a given applied longitudinal voltage, but the Hall signal will still decrease owing to the decrease in mobility. The second factor, V_l, does not take into account the contact resistivity. For low doping concentrations, the contact resistivity will increase and eventually prevent Hall measurements from being performed. We thus expect a range of carrier densities to be measurable using the Hall technique, but further studies are necessary to determine the exact range of application of the method.

2.3 Other single-nanowire characterization tools

As we have seen, using the Hall effect to characterize nanowires provides useful information on doping incorporation and carrier density. There are, however, other related single-nanowire electrical characterization tools that have been or are being developed. In this section we take a brief look at two of these emerging technologies.

2.3.1 Single-nanowire LEDs

As mentioned in Chapter 1, intense efforts are being invested in developing nanowire LEDs. For most low-power commercial applications, with LEDs in the mW range, each LED die must contain thousands of nanowires connected in parallel. However, for research and development purposes it is of interest to study single nanowires intended for LED integration. This enables studies of inhomogeneous light emission as well as emission properties that are not averaged over the thousands of nanowires in the die implementation.

The example presented in this section is based on GaN/InGaN nanowires and performed in collaboration with GLO AB. The InGaN material system allows emission primarily in the blue-green wavelength range and is expected to be one of the first material systems implemented in a commercial nanowire LED. Similar to the InP nanowires presented earlier in this chapter, the GaN nanowires are core–shell systems. They differ, however, in polarity, in which the core is grown n-type and the shell is grown p-type. The active LED layer is sandwiched between the n-type core and the p-type shell.

Electrical connections to the core and the shell of the nanowire are fabricated as shown in Fig. 2.13a. The base terminal connects to both the n-type core and the p-type shell. However, owing to the generally higher conductance of n-GaN compared to p-GaN, together with the contact being optimized for n-GaN, the shunt conductance created through the p-GaN is of minor concern. Multiple terminals connect to the shell of the nanowire LED, enabling studies of position-dependent emission by pumping different regions of the p–n junction (inset). This allows us

to optimize the homogeneity of the active layer and the uniformity of the current density through the junction. Figure 2.13b shows a photograph of the measurement setup. The emission from a single nanowire is clearly visible to the naked eye.

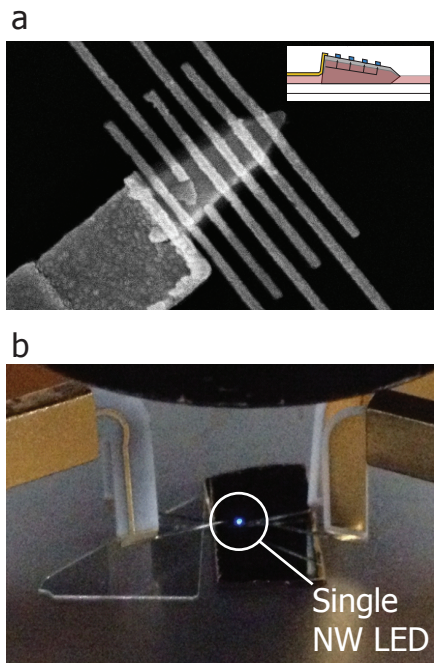

Figure 2.13: *Single-nanowire LED made from InGaN core–shell nanowires.* ***a*** *SEM image showing the finished device. Multiple contacts are connected to the shell of the nanowire to pump different positions of the p–n junction (inset).* ***b*** *Photograph of the measurement setup where the emission from the single nanowire is clearly visible. The photograph was taken with an iPhone camera.*

2.3.2 Multiple-probe measurements

Four-point and multiple-point measurements are a common technique to extract properties from planar films. Parameters that can be calculated from such measurements are the sheet resistivity and the contact resistivity between the contact and the semiconductor. A similar technique can be used on nanowires to determine the resistivity of the nanowire material and the contact–semiconductor interface. Figure 2.14 shows how such measurements can be performed. Figure 2.14a shows an SEM image of the device. In the example presented here, GaN core–shell nanowires similar to those presented in Section 2.3.1 are used. The self-aligning lifting layer developed for Hall measurements is implemented to improve the accuracy of contact deposition. In the figure, the terminals marked red are used to source a current through the shell of the nanowire, and the terminals marked

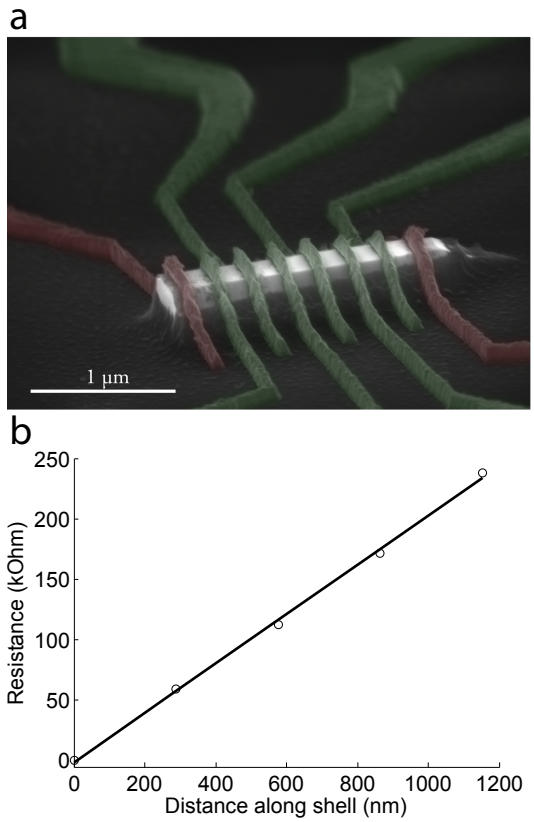

Figure 2.14: *Multiple-probe nanowire device.* ***a*** *The red terminals are used to source a current, and different combinations of the green terminals are used to sense the potential difference.* ***b*** *By plotting the resistance as a function of distance along the nanowire, the nanowire resistivity can be calculated.*

green are used to sense the potential difference along the shell. By using different combinations of the voltage-sensing terminals, the resistance of the nanowire can be extracted as a function of distance along the length of the nanowire. From the slope of the resulting data (Fig. 2.14b) together with nanowire geometry, the resistivity of the material can be calculated. Furthermore, by calculating the potential drop over the source terminals, the contact resistivity can be extracted. Although it is difficult to estimate the doping density from such measurements, they are a useful tool to characterize these basic material parameters.

Chapter 3

Capacitance–voltage characterization

In the mid 1930s, it was proposed that the conduction near the surface of a semiconductor could be controlled and modulated by applying an external electric field. This was soon followed by experiments, and in 1947 John Bardeen and Walter Brattain at Bell Labs were able to demonstrate transistor action in a Ge crystal. In 1960 John Atalla and Dawon Kahng, also at Bell Labs, patented the first functional MOSFET. One of the most important regions in a MOSFET is the semiconductor–oxide interface. A high state density at this interface causes hysteresis and screening by trapped carriers. One of the tools that have enabled the perfection of the Si–SiO_2 interface, and with it the exponential growth of the CMOS industry to date, is C–V measurements. C–V measurements enable studies of oxide, oxide–semiconductor interface and semiconductor properties and are an excellent tool to probe and optimize the quality of MOS structures. This chapter, along with Papers II and III, describes how this method can be implemented on arrays of InAs nanowires to extract valuable information such as doping density and interface trap density. For an in-depth treatment of C–V measurements, the book by Nicollian and Brews [76] is highly recommended.

3.1 MOS interfaces

A metal gate deposited on an insulated semiconductor is able to attract and repel charges at the semiconductor surface. For a moderately doped semiconductor, electrons can be attracted by applying a positive voltage to the gate, and holes are attracted by applying a negative voltage. Figure 3.1a shows an illustration of a cylindrical MOS capacitor with an n-type semiconductor.

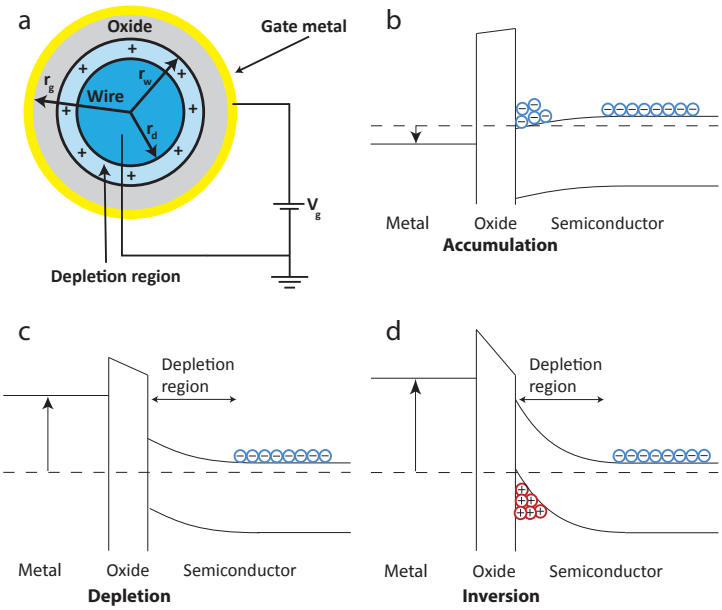

Figure 3.1: *MOS interface for an n-type semiconductor.* ***a*** *An illustration of a cylindrical MOS structure.* r_g *is the radius of the gate electrode,* r_w *is the nanowire radius and* r_d *is the inner radius of the depletion region.* ***b*** *In accumulation, the bands in the n-type semiconductor bend downward.* ***c*** *As a negative voltage is applied to the gate, a depletion region is formed.* ***d*** *For a larger negative voltage applied to the gate, an inversion layer may form at the semiconductor surface.*

Figure 3.1b–d show the MOS structure for various biasing conditions. The structure consists of a semiconductor insulated with a dielectric and capped with a conductive gate. Electric connections to the semiconductor and the gate allow a potential difference to be applied.

The semiconductor bands bend downward as a positive voltage is applied to the gate with respect to the semiconductor (Fig. 3.1b). No current flows across the interface, because the semiconductor and the metal are electrically insulated from one another in the MOS stack. The Fermi level in the semiconductor is thus constant, and the voltage applied between the metal and the semiconductor results in an offset between Fermi levels in the two materials. The applied voltage reduces the difference between the conduction band energy E_c and the Fermi level E_F at the surface of the semiconductor. The electron concentration, with an approximately exponential dependence on the difference $E_c - E_F$ (see Appendix A.2), increases with increasing positive applied voltage to the gate and accumulates at the semiconductor surface, placing it in *accumulation* mode.

Conversely, the bands bend upward for a negative voltage applied to the gate metal, decreasing the electron concentration (Fig. 3.1c). Here, the semiconductor

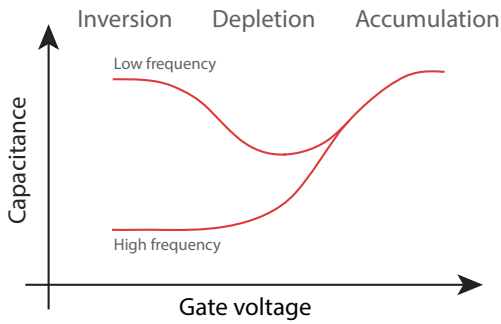

Figure 3.2: *Illustration of the C–V characteristics of an n-type MOS capacitor. In inversion, the capacitance can be high or low depending on the frequency of the applied voltage signal.*

is said to be in *depletion* mode. In this mode a depletion region, free from carriers, is formed at the semiconductor periphery. For sufficiently large negative gate voltage, holes are induced, and the MOS capacitor is in *inversion* mode (Fig. 3.1d).

The differential capacitance C is defined as the change in semiconductor charge Q in response to a change in gate voltage V_g, $C = dQ/dV_g$. The MOS impedance is measured by imposing a small AC modulation with magnitude of order $\delta V = 20\,\mathrm{mV}$ on top of a DC bias offset V_g. From the measured impedance, the capacitance is then calculated.

In accumulation mode, when the Fermi level is close to the conduction band at the surface of the semiconductor, a small change in gate voltage causes a large change in majority carrier concentration. The capacitance in this regime is therefore large (see Fig. 3.2).

As the gate voltage is tuned to more negative values, and the semiconductor is placed in depletion mode, the width of the region depleted of carriers starts to increase. As the depletion width increases, electrons that were screening the background charge provided by ionized donors are pushed away from the interface. This uncompensated donor charge makes up the positive charge on the semiconductor side of the capacitor. The donor charge is added farther and farther from the semiconductor surface, with the effect of smaller and smaller capacitance.

After onset of inversion, a small change in gate voltage again causes a large change of carrier density, in this case minority carriers close to the semiconductor surface. In this regime, the depletion region stops expanding, and the added positive charge is made up of holes close to the interface. The capacitance in inversion, however, depends strongly on the frequency of the applied AC modulation δV. Unlike electrons, which are majority carriers in the n-type semiconductor, holes cannot be supplied directly by the bulk semiconductor but must be supplied by generation. This is thus a slow process and the frequency of the applied AC modulation determines whether the holes are able to respond and follow the si-

nusoidal change of the applied voltage signal. In the high-frequency regime, the holes are unable to follow the signal applied to the gate, and the capacitance will remain at a low value, determined by the depletion capacitance. At low frequency, where the hole generation is able to follow the voltage signal, the capacitance will again start to increase to a high value. This is different from a MOSFET device in which the minority carriers are supplied by the source and drain contacts enabling high-frequency operation.

The simplest form of an equivalent circuit for the MOS capacitor is shown in Fig. 3.3. In the absence of influence from interface and oxide traps, the total capacitance of the MOS structure can be interpreted as the oxide capacitance C_{ox} connected in series to the depletion capacitance C_{dep}. The oxide capacitance is constant, whereas the depletion capacitance changes with applied gate voltage.

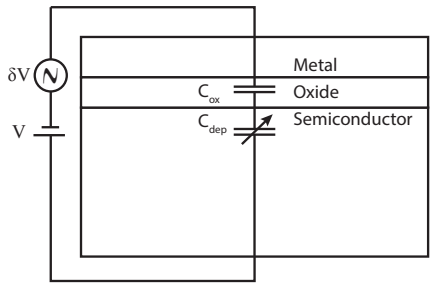

Figure 3.3: *Simplified equivalent circuit of the MOS structure.*

3.2 Nanowire capacitors

An overview of the nanowire capacitor design is shown in Fig. 3.4. Figure 3.4a shows an illustration of the nanowire device, and Fig. 3.4b shows an SEM image of the finished device. One main difference between the nanowire capacitor structure and the planar MOS capacitor is the introduction of the parasitic pad capacitance C_{pad}. The total capacitance measured between terminals A and B is the sum of the nanowire capacitance C_{nw} and the pad capacitance C_{pad} (see Fig. 3.4c). For this reason, a lifting layer is introduced in the nanowire MOS design to decrease the parasitic pad capacitance relative to the nanowire MOS capacitance: a technique that has also been adopted and used in other studies [77]. The importance of the lifting layer is quantified in Section 3.2.1.

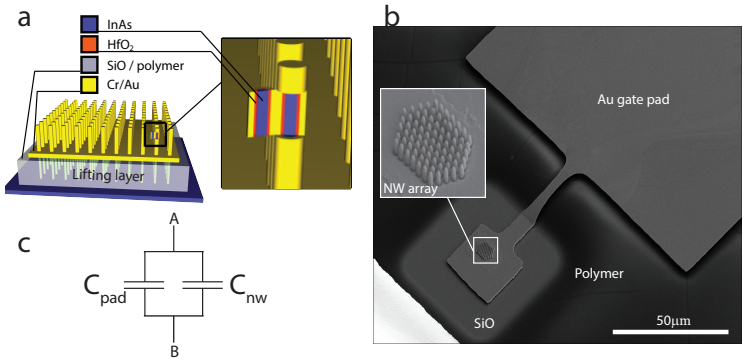

Figure 3.4: *Design of the C–V structure.* ***a*** *An illustration of the capacitor. A lifting layer is designed to decrease the parasitic capacitance from the substrate.* ***b*** *SEM image of the finished capacitor structure. The nanowires, the gate and the polymer lifting layer are shown.* ***c*** *The parasitic pad capacitance to the substrate connects in parallel to the nanowire capacitor.*

Another interesting difference between a nanowire capacitor and a planar capacitor is the possibility that the nanowire MOS diode will reach zero capacitance in depletion mode (Paper III). This situation arises if the nanowire is fully depleted of electrons before holes start to appear at the surface. A condition for a nonzero minimum capacitance is that the center of the nanowire remains populated with majority carriers when the inversion layer at the periphery is formed. For electrons and holes to coexist in an n-type nanowire MOS capacitor, the band bending must be such that, when the Fermi level reaches the valence band at the periphery of the nanowire, the Fermi level remains close to the conduction band at some radius within the nanowire. In a simple model, the electric field $E(r)$ at radius r in a fully depleted nanowire is given by Gauss' law, $E(r)2\pi r = \pi q N_d^{\text{coexist}} r^2/\varepsilon$, where N_d^{coexist} is the minimum donor concentration at which inversion is possible. Together with the necessary potential difference $|\Delta V| = \int_0^{r_{nw}} E(r)dr = E_g/q$, where r_{nw} is the nanowire radius and E_g is the semiconductor bandgap, this yields a condition for the doping density

$$N_d^{\text{coexist}} \geq \frac{4\varepsilon E_g}{q^2 r_{nw}^2} \tag{3.1}$$

This relation is plotted for InAs nanowires in Fig. 3.5a together with the results from a more accurate model described in Section 3.2.3.

Although a crude model, the result in Eqn. (3.1) provides a reasonable estimate of the required doping density. We find that, for an InAs nanowire of doping concentration $2 \cdot 10^{18}\,\text{cm}^{-3}$, the nanowire radius must be above 30–35 nm to ensure that inversion can take place. Because the ionized donors provide the background charge, and hence determine the band bending, a higher doping concentration means that the nanowire reaches inversion earlier. This is shown in Fig. 3.5b, where the C–V characteristics are plotted for different partial pressures of the dopant

Sn during growth of InAs nanowires. For the lowest doping concentrations, the capacitor reaches zero capacitance, whereas for higher doping levels, the minimum capacitance in depletion increases, indicating the formation of an inversion layer. The C–V curve also becomes increasingly flat in depletion owing to the increased voltage required to deplete nanowires with higher donor density.

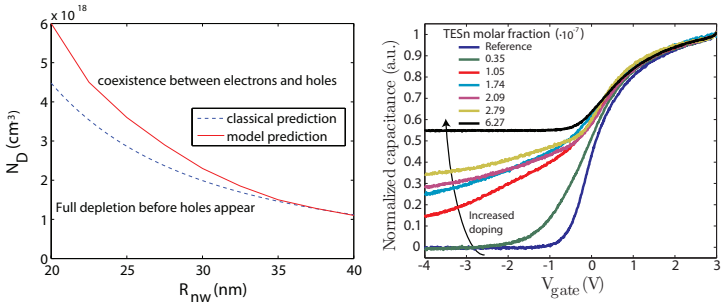

Figure 3.5: *Inversion effect in InAs nanowire capacitors.* ***a*** *For a given nanowire radius, a minimum doping density is necessary to allow electrons and holes to coexist in the nanowire.* ***b*** *The effect from adding n-type dopants during growth is seen in the C–V characteristics. As the tetraethyltin (TESn) molar fraction during growth is increased, the depletion capacitance increases. The measurements were performed at 100 MHz and room temperature.*

3.2.1 Nanowire capacitor design considerations

The main concern in designing the nanowire capacitor is to keep the parasitic pad capacitance C_{pad} small or comparable to the minimum value of the nanowire capacitance C_{nw} to ensure an adequate signal. Assume the lifting layer, illustrated in Fig. 3.4a, is of thickness t, the total nanowire length is l, the nanowire radius is r and the thickness of the nanowire dielectric is d. We further assume that all the nanowires of density ρ nanowires/m^2 are metallic cylindrical capacitors. Owing to the smaller density of states in a semiconductor compared to a metal, this is not entirely correct. It does, however, provide a simple estimate of the nanowire capacitance. The total *nanowire* capacitance per unit sample area is thus

$$C_{nw} = \rho \frac{2\pi\varepsilon_{\mathrm{ox}}\,(l-t)}{\ln\frac{r+d}{r}}$$

where $\varepsilon_{\mathrm{ox}}$ is the permittivity of the dielectric. To calculate the parasitic pad capacitance, we subtract the area covered by nanowire capacitors and calculate the total pad capacitance

$$C_{\mathrm{pad}} = \frac{\varepsilon_{\mathrm{lift}}\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}t + \varepsilon_{\mathrm{lift}}d} \cdot \left(1 - \rho\pi\,(r+d)^2\right)$$

where $\varepsilon_{\text{lift}}$ is the dielectric permittivity of the lifting layer. The ratio of expected nanowire capacitance to pad capacitance is thus

$$\frac{C_{\text{nw}}}{C_{\text{pad}}} = \frac{\varepsilon_{\text{ox}} t + \varepsilon_{\text{lift}} d}{\varepsilon_{\text{lift}}} \cdot \frac{2\pi\rho\,(l-t)}{\left[1-\pi\rho\,(r+d)^2\right] \ln\frac{r+d}{r}} \tag{3.2}$$

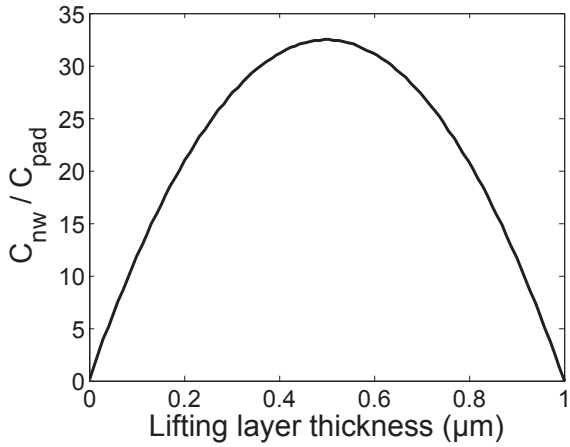

Figure 3.6: *The ratio of nanowire capacitance to parasitic pad capacitance as a function of lifting layer thickness. A lifting layer is desirable to obtain adequate signal strength from the nanowire capacitor.*

From Eqn. (3.2) it is found that the lifting layer should be designed to be $t = l/2 - \varepsilon_{lift} d/2\varepsilon_{ox} \approx l/2$ under the condition that the thickness d of the nanowire dielectric is small. Figure 3.6 shows a plot of this ratio as a function of lifting layer thickness for a typical InAs nanowire density of $1\,\mu\text{m}^{-2}$, nanowire dimensions $r = 20\,\text{nm}$ and $l = 1\,\mu\text{m}$, and dielectric thickness $d = 10\,\text{nm}$. The nanowire dielectric is assumed to be HfO_2 and the lifting layer to be a generic low-k material, with dielectric constants $\varepsilon_{\text{ox}} = 25\varepsilon_0$ and $\varepsilon_{\text{lift}} = 3\varepsilon_0$, respectively. If the lifting layer is omitted in the capacitor design, we expect the maximum nanowire-to-pad-capacitance ratio to reach only approximately 0.15, making the measurements challenging. By the relatively simple process of adding the lifting layer to the design, this ratio can be increased to approximately 30. In our approximations, we have assumed the nanowire capacitance to be equal to a cylindrical metal capacitor of equivalent geometry. In accumulation, the actual nanowire capacitance will be smaller than the oxide capacitance because of the limited density of states in a semiconductor, and in depletion the capacitance will be even smaller. It is therefore necessary to maximize the nanowire-to-pad capacitance ratio to achieve an adequate signal from the nanowire capacitors.

3.2.2 Hysteresis

A surface charge at the semiconductor–oxide interface that does not respond to the high frequency of the AC signal may still affect the C–V characteristics of the nanowire. It is common to find that the capacitance curve when sweeping the voltage in one direction differs from that when sweeping the voltage in the opposite direction. This is often associated with charging of traps. Figure 3.7a illustrates the case where a surface charge of density σ is located at the interface between the semiconductor and the oxide.

With Gauss' law, the potential difference introduced by a surface charge is found to be

$$\Delta V = \frac{\sigma r_{nw}}{\varepsilon} \ln \frac{r_{nw}}{r_{ox}}$$

where r_{nw} is the nanowire radius and r_{ox} is the radius of the gate–oxide interface. With the oxide capacitance

$$C_{ox} = \frac{2\pi\varepsilon L_{nw}}{\ln \frac{r_{nw}}{r_{ox}}}$$

where L_{nw} is the length of the nanowire, the expression can be rewritten as

$$\Delta V = \frac{S_{nw}\sigma}{C_{ox}} \tag{3.3}$$

where $S_{nw} = 2\pi r_{nw} L_{nw}$ is the nanowire mantle area. Thus, for two points in the C–V diagram of equal capacitance, the voltage difference is associated through Eqn. (3.3) with a surface charge (see Fig. 3.7b). By measuring the difference in voltage between points A and B, we can estimate the difference in surface charge. This technique was used in Paper II to estimate the trap density at the InAs–HfO_2 interface as a function of gate swing. The interface state density was found to be less than $10^{11}\,\mathrm{cm}^{-2}$ for gate swings smaller than 0.5 V.

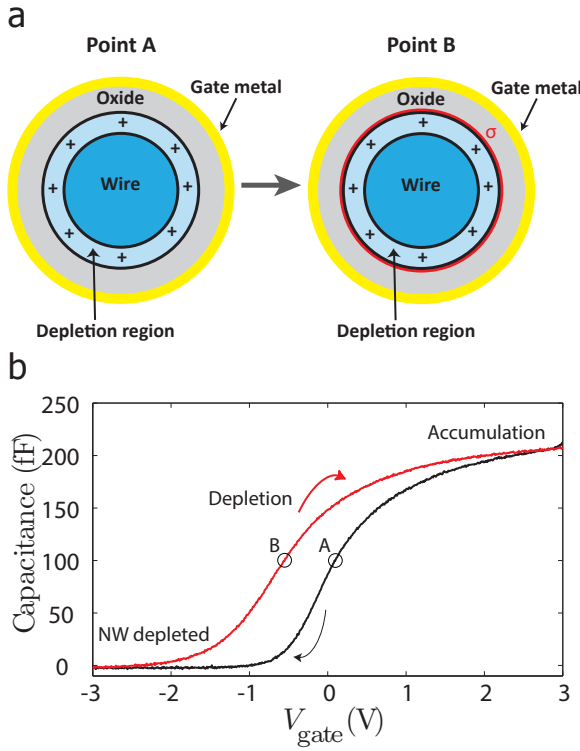

Figure 3.7: *Effect from a surface charge.* ***a*** *As the gate voltage is swept in different directions, a surface charge may build up.* ***b*** *The surface charge screens the gate and causes hysteresis. The voltage shift between points A and B is proportional to the difference in surface charge at the semiconductor–dielectric interface between the two sweeps.*

In later experiments, the interface state density D_{it} was studied in nanowires with various methods. For example, silicon nanowires have been characterized with the quasistatic method [77], which is a low-frequency method to investigate D_{it}, and with combinations of high- and low-frequency C–V [78]. As more C–V studies on nanowires are undertaken, conventional techniques are being adapted, and new techniques are likely to be developed.

3.2.3 Capacitance simulations

The full C–V characteristics of nanowire MOS devices are challenging to describe analytically. Some modeling is often necessary to correlate the measured capacitance to the semiconductor material properties. A common approach is to construct an equivalent circuit in which the various contributions such as bulk carriers, generation and recombination, and surface traps are implemented as conductances

and capacitors [76]. In Paper III a somewhat different model was employed, specifically geared toward the lower dimensionality exhibited by the nanowires.

In a simple model, a nanowire can be described as an infinite cylindrical potential well. The wave functions in this system are well known, and the eigenfunctions to the Hamiltonian are Bessel functions [79]. In a real n-type nanowire system, the semiconductor is populated with electrons as well as a fixed background charge from the ionized donors. The resulting charge distribution will affect the potential landscape of the nanowire. We therefore expect the potential V to deviate from the case of the infinite quantum well. Because the Bessel functions are eigenfunctions of the Hamiltonian for the infinite quantum well, we can use these functions as a basis set for constructing the solutions to the perturbed nanowire system.

For each bound state $\Psi_{n_r n_\phi}$ in the nanowire, indexed by a radial quantum number n_r and an angular quantum number n_ϕ, we assume a parabolic dispersion relation in the z-direction. We then use the Fermi–Dirac distribution to find the highest energy E_z for which to populate that subband with minimum energy $E_{n_r n_\phi}$. The electron density is then given by

$$n(r) = \sum_{n_r n_\phi} |\Psi_{n_r n_\phi}(r)|^2 \int_0^\infty \frac{g(E_z) dE_z}{\exp\left(\frac{E_z + E_{n_r n_\phi}}{kT}\right) + 1}$$

where $g(E_z)$ is the 1D density of states in the z-direction, k is Boltzmann's constant and T is the temperature. For a given electron population, we can then find the electrostatic potential by solving the Poisson equation. This generates a new potential, which is then used to solve the Schrödinger equation, and this process continues until convergence. Figure 3.8 shows the results from such a self-consistent simulation for an InAs nanowire with $r_{nw} = 27\,\text{nm}$, a donor concentration of $2.2 \cdot 10^{18}\,\text{cm}^{-3}$ and HfO_2 as the gate dielectric. Figure 3.8 a and b show the band diagram and electron density for a positive gate voltage, respectively, and Fig. 3.8 c and d are the corresponding graphs for a negative gate voltage.

The band bending is shown, and the peak density of the electrons changes, from the periphery of the nanowire for a positive gate voltage, to the center of the nanowire for a negative gate voltage. By changing the gate voltage in small increments, it is possible to calculate the change in the total amount of charge in the nanowire, and thus determine the capacitance.

This simulation technique was used in Papers II and III to determine the doping density of InAs nanowires (see Fig. 3.9). Typical C–V characteristics for an InAs nanowire array of average radius $r_{\text{nw}} = 27\,\text{nm}$ are shown together with fits for three donor densities. All of the fits deviate from the experimental data below 0 V owing to trapping of charge near the InAs–HfO_2 interface. This charging is accompanied by a clear kink in the C–V characteristics. Because the model does not take into account the trapped charge, the fit was applied only from accumulation down to the kink in the curve. The best fit was found for $N_d = 2.0 \cdot 10^{18}\,\text{cm}^{-3}$. Another notable property seen in Fig. 3.9 is that the simulated curve for $N_d = 4.0 \cdot 10^{18}\,\text{cm}^{-3}$ levels out at a finite capacitance. This is consistent with the result presented in Fig. 3.5 for this nanowire radius.

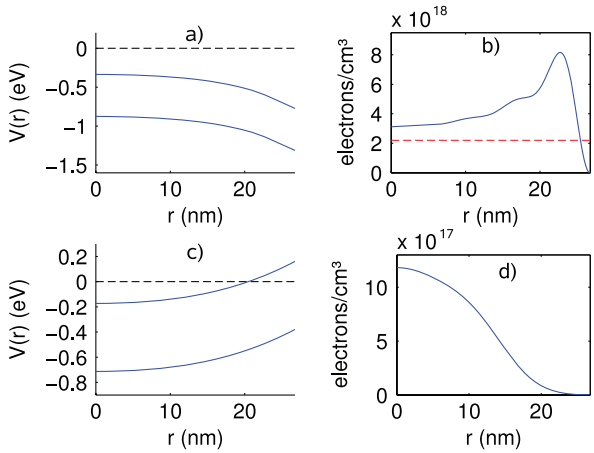

Figure 3.8: *Results from self-consistent Schrödinger–Poisson simulations of an InAs nanowire MOS capacitor. The band bending (**a**) and electron density (**b**) of the nanowire while a positive voltage is applied to the gate. The band bending (**c**) and electron density (**d**) while a negative voltage is applied to the gate.*

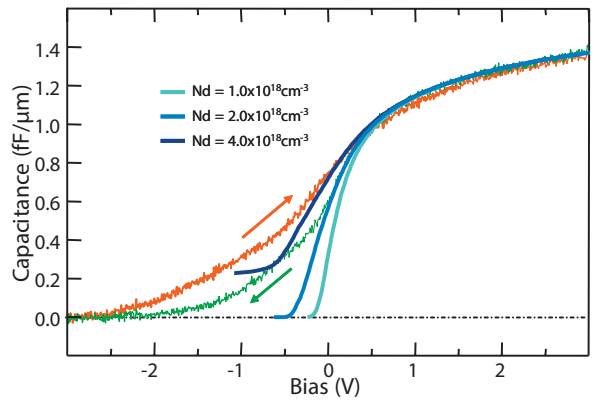

Figure 3.9: *Typical hysteresis behavior of C–V characteristics for an InAs nanowire MOS capacitor and examples of model fits to the C–V curve for three donor concentrations. Fits were made to the down-sweep as this was found to correspond to the equilibrium state in the surface charge.*

3.2.4 Progress in nanowire capacitors

The first study of nanowire C–V behavior was performed on single Ge nanowires positioned laterally on a substrate [80]. However, the measurement setup required to measure a single-nanowire capacitor below 1 fF was challenging. In Paper II, we demonstrate how these measurements can be performed on arrays of InAs nanowires connected in parallel using simple batch processing techniques and a lifting layer to improve the capacitance signal. The same year, Paper III was published, in which the simulation technique and analysis is described and further developed. This development has now been followed by techniques to extract the doping concentration of InAs nanowires with analytical models [81], dopant profiling and D_{it}-determination in Si nanowires [78], studies of dopant-induced trapping of carriers [82] and the implementation of deep-level transient spectroscopy techniques [83]. Recently, studies have also been performed on vertically aligned single-Si-nanowire capacitors [77], in which low-frequency methods were used to extract the interface state density. Capacitance spectroscopy has played a major role in the optimization of planar semiconductor technologies, and the interest and success in adopting the technique to nanowires indicates that it may be of similar importance in nanowires as new devices are implemented.

Chapter 4

Gate control in nanowires

As we saw in Chapter 3, gates are able to change the charge state and conductivity of underlying semiconductors. This effect can, however, be used not only to measure basic material properties, but also to make interesting and useful devices. In this chapter we investigate how novel devices can be fabricated by placing gates on nanowires. We first quantify the difference in gate geometries, comparing a gate acting only from one side with a gate that is wrapped around the nanowire connecting its entire circumference. This is followed by a discussion of Papers IV and V in which we explore how this effect can be used to create a p–n junction without any impurity doping gradients. Finally, a novel process is demonstrated in Paper VI that allows us to make a fully wrapped gate on a nanowire placed laterally on a substrate.

4.1 Gate control of semiconductors

The most common route to gating nanowires oriented laterally on a substrate has been with the use of a back-gate. In a back-gate geometry, the nanowire is placed on an electrically insulated substrate, which is used as the gate to control the device properties. The applicability of the back-gate geometry ranges from fundamental research devices, in which the gate can be used to observe fundamental physics such as Coulomb-blockade oscillations [84] and the physics of superconductor/semiconductor junctions [85], to more device-oriented research such as new designs for FETs [86].

However, it is well known that the back-gate geometry is far from ideal. In this geometry, the gate accesses the nanowire device from one side only, and thus it may cause an inhomogeneous carrier density effect inside the semiconductor [87]. This is troublesome if precise and homogeneous carrier density control is necessary. For enhanced gate control, a gate electrode that is wrapped around the entire semiconductor device is desired. In such a *wrap-gate* or *gate-all-around* geometry, the gate couples equally to all parts of the semiconductor channel periphery, and it is thus possible to control the behavior of the device more precisely.

Figure 4.1 shows the difference between these two geometries in a more quantitative manner. See Section 2.2.1 for more information on how the simulations were performed. The figure shows the carrier density distribution for an n-doped ($5 \cdot 10^{17}\,\mathrm{cm}^{-3}$) InP nanowire (a) in a wrap-gate geometry and (b) in a back-gate geometry with a negative voltage applied to the gate electrodes. Both geometries have a 10 nm HfO_2 film insulating the nanowire from the gate electrode. The gate voltage is tuned so that the nanowire in both geometries is depleted to an average electron concentration of $1 \cdot 10^{17}\,\mathrm{cm}^{-3}$. The back-gate gives rise to an asymmetric carrier density with a strong gradient in the vertical direction, whereas the wrap-gated nanowire exhibits an approximately cylindrically symmetric carrier density within a much smaller range. As is evident from Fig. 4.1c, the wrap-gate provides more efficient coupling to the nanowire channel, and the voltage required to deplete the back-gated nanowire to $1 \cdot 10^{17}\,\mathrm{cm}^{-3}$ is $V_g = -0.525\,\mathrm{V}$ compared with the wrap-gated nanowire, which requires only $V_g = -0.125\,\mathrm{V}$ to achieve the same level of depletion. This reduced gate swing requirement is demonstrated in Paper VI.

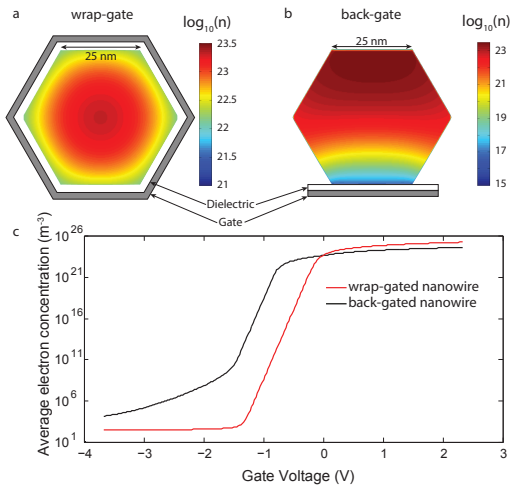

Figure 4.1: *Gate effect in different nanowire geometries.* ***a*** *The carrier density distribution of a wrap-gated nanowire.* ***b*** *The carrier density distribution in a back-gated nanowire. In both* ***a*** *and* ***b*** *the nanowire has been depleted to an average electron concentration of* $10^{17}\,\mathrm{cm}^{-3}$. ***c*** *The average electron concentration of both geometries as a function of gate voltage.*

With the use of wrap-gates, or semiwrapped gates, it is thus possible to exercise more optimized control of carriers inside a nanowire. It is also possible to use gates to define new types of devices, in which the potential landscape for the charge carriers in some regions is determined by external gates rather than by impurity doping incorporation.

4.2 The dual-gate field-effect diode

Since the first observation of junction emission in SiC in the early 20th century [88, 89] and the development of the understanding of p–n junction light emission in the 1950s and 1960s [90], the p–n junction has become one of the most famous and most implemented devices in modern technology. With an estimated 10% potential reduction in global power consumption through the implementation of LED devices for general illumination [91], combined with the promise of photovoltaics [92], there is no doubt that p–n junctions will continue to generate interest far into the future.

In a conventional p–n junction, the junction is defined by incorporating impurities—dopants—into the material (Fig. 4.2).

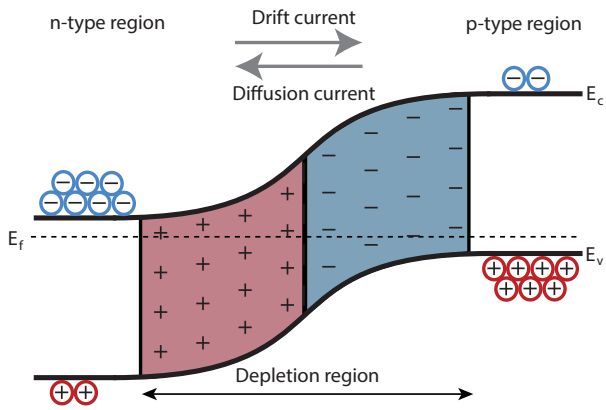

Figure 4.2: *Illustration of a p–n junction. In equilibrium, the drift and diffusion current components are equal, and the total current through the junction is zero.*

One side of the semiconductor is doped with donors, making it electron-rich, or n-type, and the other side is doped with acceptors, making it hole-rich, or p-type. Owing to the concentration gradients, holes from the p-side diffuse into the n-side, and electrons from the n-side diffuse into the p-side. The diffusion of carriers across the junction gives rise to a space charge made up of the uncompensated impurity background ions. This gives rise to an electric field that causes drift currents in the opposite direction to the diffusion currents. At equilibrium, the drift and diffusion current components are equal, and a balanced situation arises where the net current across the junction is zero.

The p–n junction is the basic building block for LEDs and photovoltaic cells and is technologically important. It is, however, inherently static. For various applications, it is of interest to explore the possibility of forming the p–n junction by external electric fields instead of by impurity incorporation.

Figure 4.3a shows a conventional p–n junction, with n- and p-type regions defined by donors and acceptors, respectively. In the concept of the field-effect diode, these two regions are replaced by gates, as illustrated in Fig. 4.3b. For

example, by tuning the p-gate to a positive (4.3c) or negative (4.3d) voltage, electrons or holes can be induced, respectively. For a positive voltage applied to both gates, the device is expected to exhibit ohmic properties allowing conduction in both directions. For opposite polarity applied to the gates, rectifying behavior is expected.

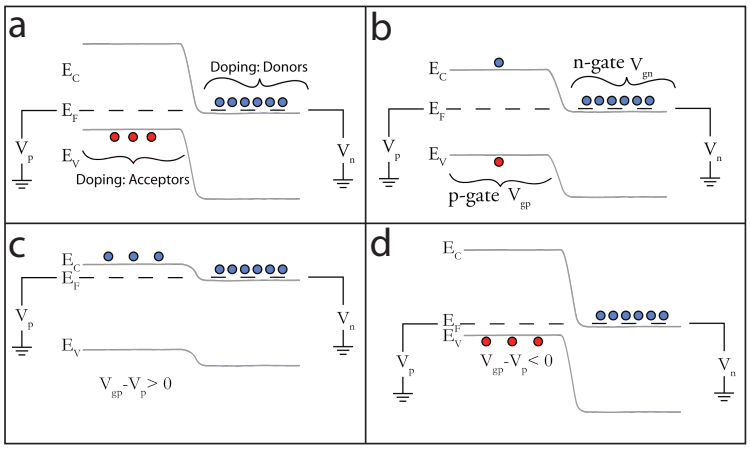

Figure 4.3: *Field-effect diode.* ***a*** *A conventional p–n junction formed by incorporating donors and acceptors.* ***b*** *By replacing the impurities with two external gates, a more dynamic device is formed. By applying a positive (****c****) or negative (****d****) voltage to the p-gate, electrons or holes can be induced, respectively, in this region of the device.*

The following sections describe such a device implementation. Two closely spaced gates, wrapped around the semiconducting nanowire, can be used to induce sequential p- and n-regions, forming a field-effect diode, and it is shown how the properties of the p–n junction can be tuned by controlling the voltages applied to the wrap-gates.

4.2.1 Individual carrier control with Ω-gates

A material in which the Fermi level can be tuned across the entire semiconductor bandgap to induce both p- and n-type behavior is required so as to realize the nanowire dual-gate field-effect diode. Furthermore, it is necessary to dope the ends of the nanowire to ensure optimal contact properties to cathode and anode. InP is a material in which both n- and p-type doping has been extensively studied [50, 57]. It also does not suffer from severe Fermi-level pinning, unlike, for example, InAs, in which a surface accumulation layer is formed [66]. As a result, sufficient electrostatic control of the conduction behavior is enabled by means of gates.

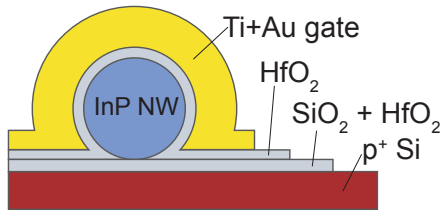

Figure 4.4: *The Ω-gate design used for single-nanowire FETs. The nanowire is positioned laterally on a silicon substrate insulated by* SiO_2 *and* HfO_2*. A metal gate is then deposited from above, resulting in an Ω-shaped gate. The gate dielectric between the nanowire and the gate is* HfO_2*.*

To further explore InP nanowires as candidates for constructing field-effect diodes, single-nanowire MOSFETs were fabricated (Paper IV). The devices were made by implementing an Ω-gate, a geometry illustrated in Fig. 4.4.

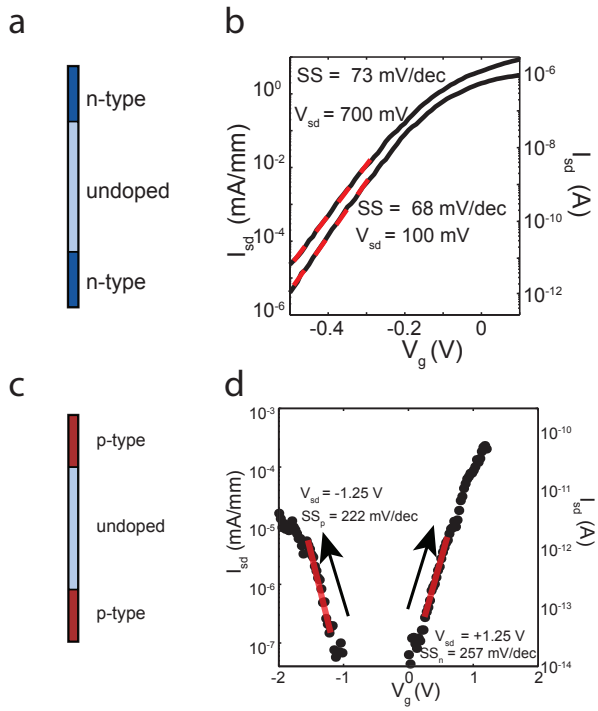

Figure 4.5: *Single-nanowire InP FETs.* ***a*** *An illustration of the n-type FET, with its transfer characteristics (****b****).* ***c*** *An illustration of the p-type FET, with its characteristics (****d****).*

Although not as efficient as a fully wrapped gate electrode, the Ω-gate offers a

reasonable compromise between ease of deposition and gating efficiency. Figure 4.5 shows the layout and properties of the nanowires used in the devices. To ensure electric contacts of adequate quality, the ends of the nanowires were doped n-type (Fig. 4.5a) and p-type (Fig. 4.5c) using hydrogen sulfide and diethylzinc respectively for the two types of transistors.

From the transfer characteristics (Fig. 4.5 b and d), it was found that the p-type InP nanowire exhibited ambipolar behavior. This is an important observation because it is a fundamental requirement for the functionality of the more advanced field-effect diode. Additionally, the n-type transistor exhibited an inverse subthreshold slope (SS) of 68 mV/dec, which is only 13% above the theoretical limit of 60 mV/dec at room temperature, demonstrating an excellent gate coupling to the channel. To the best of the authors' knowledge, this was also the best subthreshold slope ever measured for InP nanowires. This indicates that the semiwrapped Ω-gate provides a gate coupling with efficiency close to a gate fully wrapped around the FET channel.

4.2.2 Operation of the field-effect diode

The nanowire field-effect diode was then fabricated in a similar manner as the MOSFETs described in Section 4.2.1. Instead of using identical doping species for both ends of the nanowire, one end was doped p-type and the opposite end was doped n-type. Two Ω-gates were subsequently deposited on the nominally undoped region of the nanowire. The finished device is shown in Fig. 4.6.

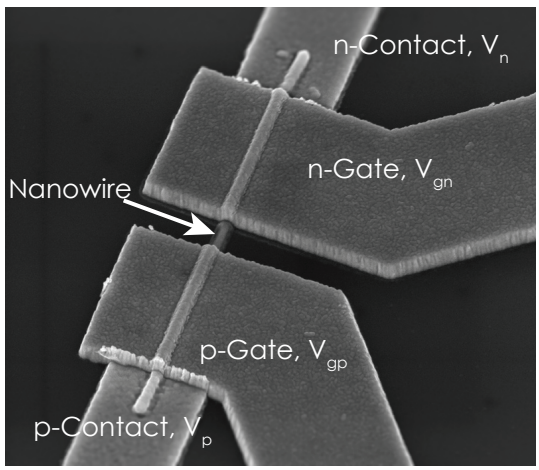

Figure 4.6: *SEM image of the field-effect diode. Two gates are used to induce sequential p- and n-type regions in the InP nanowire.*

In the field-effect diode, the two gates were used to induce a p–n junction in the central region of the semiconductor, as shown in Fig. 4.3. The electrical properties of this device are shown in Fig. 4.7. By keeping the voltage on the

n-gate, V_{gn}, constant and positive and by varying the potential difference between the p-gate, V_{gp}, and the p-contact, V_p, the device was switched from nearly ohmic at $V_{gp} - V_p = 4.0\,V$ to highly rectifying at $V_{gp} - V_p = -2.0\,V$. This is a clear indication that a p–n junction was induced between the gates.

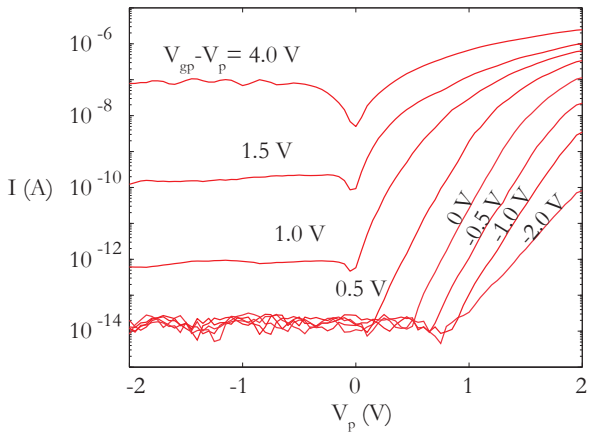

Figure 4.7: *The resulting I–V characteristics of the field-effect diode as the p-gate voltage is changed. For* V_{gp}-V_p=4 *V both regions are electron-rich and the device allows current to flow in both directions. For* V_{gp}-V_p<0 *V the junction acts as a rectifier and the built-in voltage is tuned by the voltage applied to the p-gate.*

Field-effect diodes in a planar geometry have been investigated as an alternative to MOSFETs [93–95], electrostatic discharge protection [96–98] and memory applications [99, 100]. As we will see in Chapter 5, nanowire field-effect diodes can also be used as a platform to study fundamental semiconductor physics. Owing to the improved gate coupling offered by the nanowire geometry, nanowires are an attractive system for studying the properties of field-effect diodes.

4.3 Lateral wrap-gated nanowire devices

As is evident from Fig. 4.5, Ω-gates provide efficient coupling to the nanowire channel; however, they do not achieve the same efficiency as fully wrapped gates (see Section 4.1). The present section explores how fully wrapped gates can be implemented on single nanowires that are positioned laterally on a substrate instead of vertically oriented.

Wrap-gated nanowire FETs have been extensively studied in the vertical geometry [27, 32, 101–103]. However, the vertical FET devices are complicated to process [104], and the measured characteristics are averaged over all nanowires in the array. For certain applications it is of interest to instead study the properties of single nanowires processed into FET devices. The most common scheme to design a single-nanowire device is to use the substrate as a back-gate. As shown

in Section 4.1, this may cause charge inhomogeneities, an effect that has also been studied in other work [87]. Other designs implemented to study single nanowires include placing nanowires on top of predefined gates [105] and the use of Ω-gates [106, 107].

However, the preferred geometry for single-nanowire studies would be one in which the gate surrounds the entire nanowire channel, even though the nanowire is placed laterally on a substrate. This presents challenges in achieving gate material deposition underneath the nanowire. To solve these issues, a new processing scheme was developed as described in Paper VI in which a wrap-gate was deposited on the nanowires while they remained standing on the original substrate. The nanowires were then transferred to an insulated silicon substrate, and the gate was selectively removed to gain access to the nanowire for electrical contacts (see Fig. 4.8). To the best of the Author's knowledge, this was the first time a laterally positioned nanowire was equipped with a gate fully wrapped around its circumference.

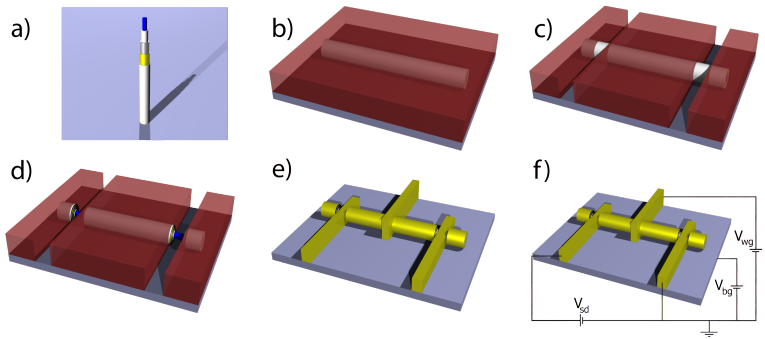

Figure 4.8: *Illustration of the processing technique to realize a fully wrapped gate on a laterally positioned nanowire. The gate is first deposited while the nanowire is standing up (**a**). In a series of lithography and etching steps (**b**–**d**) access to the nanowire is made, and nanowire and gate leads are deposited by evaporation (**e**). This device offers two gates: the wrap-gate and the back-gate (**f**).*

As shown in Fig. 4.8a, the nanowire was first coated by aluminum oxide, followed by a tungsten layer, a gold layer and finally an outer aluminum oxide layer. After the nanowire was transferred to the Si substrate, the sample was coated in resist (Fig. 4.8b), and the contact areas were opened up by EBL (Fig. 4.8c). A series of wet etch steps were then used to selectively remove the gate layers (Fig. 4.8d), and electrical contact was made with the nanowire (Fig. 4.8 e and f). The result is shown in Fig. 4.9.

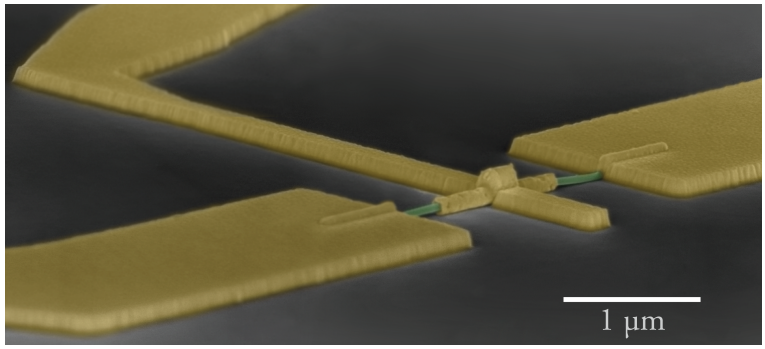

Figure 4.9: *SEM image of the finished device.*

The lateral wrap-gate design offers some benefits not available to the vertical wrap-gate design. As shown in Fig. 4.8f, two gates are available to control the nanowire properties. The wrap-gate V_{wg} can be used to gate the mid section of the wire with high efficiency, while the back-gate voltage V_{bg} can be used to improve the material conductivity at the ends of the nanowire as well as improve the contact regions. This is illustrated in Fig. 4.10, which shows the response of the nanowire to the voltage on the back-gate. This allows low-temperature measurements to be performed without the risk that the contacts or the lead regions of the nanowire may become highly resistive, thus enabling measurements such as quantized conductance [108].

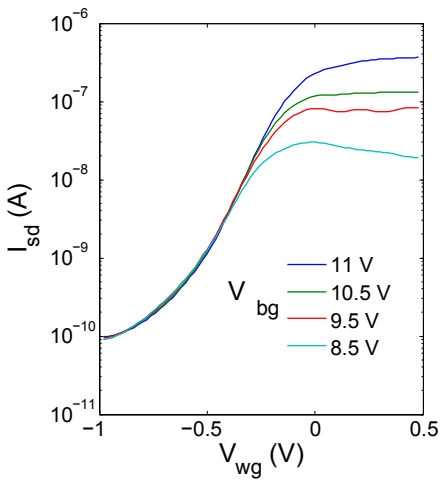

Figure 4.10: *Effect from back gate on the transfer characteristics of the lateral wrap-gated nanowire design shown in Fig. 4.9. The back-gate can be used to tune the resistivity of the lead regions not covered by the wrap-gate. The source-drain voltage was set to* 50 mV.

Chapter 5

Concluding remarks and outlook

In the last decade, nanowire research has leaped forward. We are now able to grow nanowires with most common materials and combinations of materials. We are also able to tune the conductivity of nanowires and dope essentially all common semiconductor nanowires, both n-type and p-type. However, as this thesis shows, the best methods to electrically characterize nanowire material are still being investigated. Electrical characterization methods that are fast and simple to implement are important for quick feedback when engineering new device structures.

Hall effect and C–V measurements stand out as potential future standard characterization methods. Initial demonstrations have shown substantial promise in terms of doping estimates and oxide trap density from C–V measurements, and carrier density and mobility information from Hall measurements. The C–V characterization method has had a few more years to mature than nanowire Hall characterization, but both of these methods have room for improvement, and many more interesting experiments remain to refine the methods.

In the case of Hall measurements, the electrode resolution and alignment needs to be improved to enable characterization of ultrathin nanowires. This can be achieved with optimized alignment markers, but there remains the opportunity for further refinement. The next phase for Hall measurements on nanowires will be to perform more studies to further verify the results. Hall measurements should be performed on simple nanowire systems such as homogeneously doped nanowires, and be correlated to field-effect measurements, preferably on the same nanowire. This should be fairly straightforward to achieve with Hall terminals defined first, and gate oxide and Ω-gates defined second. Furthermore, the simulations can be refined and more parameters can be taken into account. Specifically, for the core–shell nanowire structure, simple models can be developed to take into account the p–n junction depletion region. Fermi pinning at the surface may also give rise to a small depletion region that should be taken into account in the analysis. Moving beyond basic materials characterization, Hall effect measurements on nanowires

enable the exploration of fundamental physics. A possible exciting experiment is to grow a radial quantum well and perform low-temperature Hall characterization on a 2D electron gas wrapped around the nanowire. Room-temperature measurements on such a system would also be interesting in terms of characterizing the 2D electron gas for implementation in a radial high electron mobility transistor. Hall effect measurements in nanowires enable a whole new genre of experiments to be performed, and hopefully, they will be further refined and developed for the benefit of the entire nanowire community.

C–V measurements also enable exciting new experiments on nanowires. Deep-level transient spectroscopy is one of these techniques that have been extensively used for bulk semiconductor material, both in the case of p–n junctions and also by means of Schottky contacts. Deep-level transient spectroscopy has already been demonstrated on InAs nanowires [83], and, given the usefulness of this method to characterize deep traps in semiconductors as well as interface states, this is an area in which further experiments and developments are possible. Especially with the drive toward developing nanowire MOSFETs, there is a clear incentive to investigate and optimize the semiconductor–dielectric interface. This is particularly challenging with III/V channels such as InAs and InSb combined with high-k dielectrics such as HfO_2. In this regard, the C–V method has proven itself for bulk semiconductors, and it will be equally important in optimizing the interface of nanowire MOSFETs. C–V measurements also have other interesting applications such as dopant profiling and may prove an invaluable tool in the engineering of nanowire solar cells and LEDs.

The results on nanowire field-effect diodes presented in Paper V are only the proof of concept, and many interesting experiments remain. Besides the application areas discussed in Chapter 4, nanowire field-effect diodes can serve as a platform for exploring fundamental nanowire physics. An interesting application of the field-effect diode is illustrated in Fig. 5.1. By introducing a barrier between the two gates, it may be possible to study the properties of spatially separated excitons. In this system, the gates are used to tune the electron and hole concentrations on the n- and p-side, respectively. It is also of interest to investigate the emission properties of the dual-gated diode structure. Although it is unclear whether such a device can emit light with high efficiency, a possible application of the field-effect diode may be to introduce a graded barrier in the region of the induced junction. This may enable tuning of the emission wavelength by changing the voltages of the gates.

For some of these multiple-gate experiments, perhaps in particular for LED applications, it is beneficial to design a vertical structure, with multiple nanowires connected in parallel, instead of the lateral device primarily described in Chapter 4 (see Fig. 5.2). The vertical design requires two wrap-gates to be stacked on top of each other as well as an electrode connecting to the top of the nanowires. This is in principle similar to a recent experiment in which dual gates were vertically stacked to enable CMOS logics in a single nanowire [36].

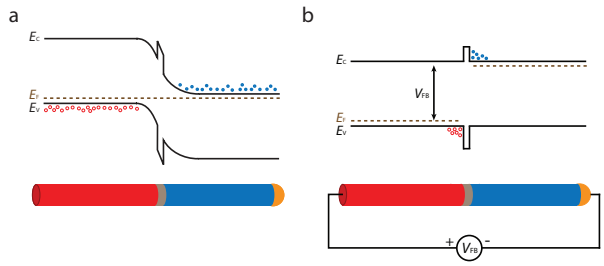

Figure 5.1: *Possible application of the nanowire field-effect diode by introducing a barrier in the junction region.* ***a*** *Illustration of the bands with all terminals grounded.* ***b*** *When the proper bias is applied, spatially separated excitons may be studied.* © *G. Nylund, modified and printed with permission.*

Section 4.3 described the development of a fully wrapped gate on laterally oriented nanowires. This development functions as an enabler and platform for single-nanowire research and characterization. The lateral single-nanowire design is often desirable so as to avoid averaging over a large number of nanowires and to gain freedom in engineering the gate design on nanowires. Furthermore, by enabling a fully wrapped gate, a more homogeneous gate effect is achieved which is important for many studies of fundamental nanowire physics. An emerging field in which this gate geometry will likely be of importance is that of Wigner crystallization in nanowires, because studies in this field require a homogeneous potential landscape inside the nanowire [109]. Other experiments that will benefit from this wrap-gate platform are those of quantized conductance in nanowires and more applied areas such as multiple-gate logic devices in which, for example, inverters can be realized using a single nanowire [35]. Nanowires have also been suggested as candidates for chemical and biological sensors owing to their large surface-to-volume ratio, and multiple sensors have been demonstrated [110–112]. The lateral wrap-gate design is also of interest in this application area since the gate can be thiol-functionalized [113] and used for sensor applications.

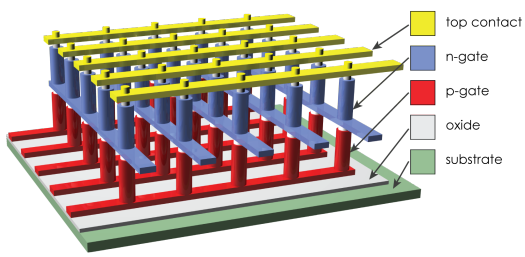

Figure 5.2: *The nanowire field-effect diode implemented in a vertical design. Multiple nanowires connected in parallel enable the signal strength to be improved for applications such as LED devices.*

Nanowire research is entering an exciting stage in which commercially viable applications are reaching a mature state. There are still investigations to be made and unknowns to be explored, but with systematic experiments, and proper characterization methods, the field of nanowire research holds great promise for the future. Hopefully, the work presented in this thesis contributes to the future of nanowire research by advancing our ability to measure and understand fundamental material properties. It is also hoped that this work will be built upon so that we may soon see nanowires implemented in devices present in our everyday lives.

Appendix A

Derivations

A.1 Cylindrically symmetric p–n junctions

We want to solve the Poisson equation for a cylindrically symmetric p–n junction. The nanowire system under study consists of an n-type core and a p-type shell. We formulate the problem in cylindrical coordinates

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dV}{dr}\right) = -\frac{\rho(r)}{\varepsilon},\ E(r) = -\frac{dV}{dr} \tag{A.1}$$

where r is the radial distance from the nanowire core, ε is the permittivity of the material, V is the potential, E is the electric field and $\rho = qN$ is the charge density, with N the doping density. We will here employ the depletion approximation, i.e. we assume that the depletion region is completely void of free carriers. We define the metallurgical junction to be positioned at radius r_j, with r_n and r_p the positions of the edges of the depletion region in the n-type core and p-type shell, respectively, R_{nw} the nanowire radius and $d = r_p - r_n$ the depletion width. We further assume a step function of the doping density

$$N = \begin{cases} N_D & 0 < r < r_j \\ -N_A & r_j < r < R_{nw} \end{cases}$$

Eqn. (A.1) is in a form that can be simplified to

$$(rE)' = \frac{qNr}{\varepsilon}$$

with the solution

$$E(r) = \frac{qNr}{2\varepsilon} + \frac{C}{r}$$

where C is an integration constant. Owing to the discontinuity in doping density, we will solve for E separately in the core and the shell of the nanowire. At the edges of the depletion region, we have zero electric field

$$E_p(r_p) = E_n(r_n) = 0\,\mathrm{V/m}.$$

This condition allows us to determine the integration constant and find a solution for the electric field

$$E(r) = \begin{cases} \frac{qN_D}{2\varepsilon}\left(\frac{r^2-r_n^2}{r}\right) & r_n \le r \le r_j \\ -\frac{qN_A}{2\varepsilon}\left(\frac{r^2-r_p^2}{r}\right) & r_j < r \le r_p \end{cases} \tag{A.2}$$

The solution (A.2) can easily be integrated to find the electric potential, and the integration constant is determined by defining the potential to be zero at the junction, $V(r_j) = 0\,\mathrm{V}$

$$V(r) = \begin{cases} \frac{qN_D}{2\varepsilon}\left(\frac{r_j^2-r^2}{2} + r_n^2 \ln\left(\frac{r}{r_j}\right)\right) & r_n \le r \le r_j \\ -\frac{qN_A}{2\varepsilon}\left(\frac{r_j^2-r^2}{2} + r_p^2 \ln\left(\frac{r}{r_j}\right)\right) & r_j < r \le r_p \end{cases}$$

Next we calculate r_n and r_p. Assuming the nanowire radius and doping concentrations are large enough that the entire depletion region can be accommodated by the nanowire, charge neutrality yields the condition

$$\pi\left(r_j^2 - r_n^2\right) N_D = \pi\left(r_p^2 - r_j^2\right) N_A. \tag{A.3}$$

By employing $d = r_p - r_n$, Eqn. (A.3) can be solved for r_n and r_p separately

$$\begin{cases} r_n = -N_A M \\ r_p = \quad N_D M \end{cases}$$

with

$$M = \frac{d}{N_A + N_d} + \sqrt{r_j^2 - d^2 \frac{N_A N_D}{N_A + N_D}}$$

Finally we determine an expression for the built-in voltage, V_{bi}, of the radial p–n junction. Assuming an external voltage V_a is applied to the p-type periphery of the nanowire, we find

$$\begin{aligned} V_{bi} - V_a &= V(r_n) - V(r_p) \\ &= \frac{q}{2\varepsilon}\left(r_n^2 N_D \ln\left[\frac{r_n}{r_j}\right] + r_p^2 N_A \ln\left[\frac{r_p}{r_j}\right]\right) \end{aligned}$$

Because r_n, r_p and thus $V_{bi} - V_a$ are single-valued functions of the depletion width d, these equations can all be solved numerically once the built-in voltage has been determined by a suitable method, e.g. by employing Eqns. (A.4) and (A.5) in the next section.

A.2 Hall effect simulation framework

A majority of the simulations were performed in the COMSOL Multiphysics Finite-Element Modeling suite. This software suite allows module-based physics modeling with powerful Finite-Element Modeling solvers. It is, however, still necessary to define a framework in which to perform the simulations.

We define the vacuum level as reference (zero-) potential. Because different materials have different electron affinity, this provides an unbiased point of reference. We use the distance between the Fermi level and the vacuum level as the potential in the material. We define $\phi(\bar{r})$ to be the potential at $\bar{r}$, $\chi(\bar{r})$ is the electron affinity, $E_g(\bar{r})$ is the semiconductor bandgap, $E_F(\bar{r})$ is the Fermi level and $E_i(\bar{r})$ is the *pseudo-intrinsic* energy level; E_i is defined to always be in the middle of the bandgap, regardless of differences in the effective density of states in the conduction and valence band.

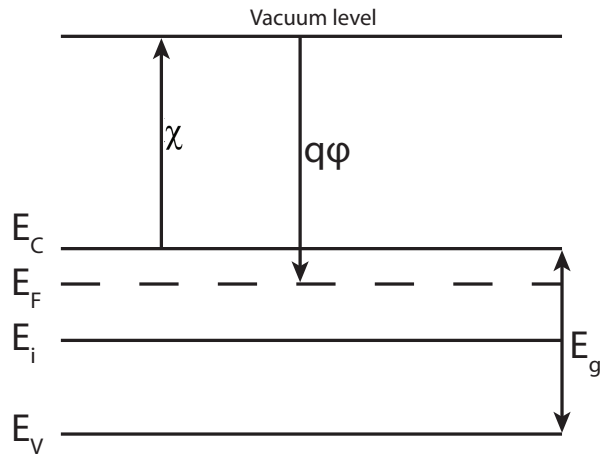

Figure A.1: *Definition of quantities used to define the potential, ϕ.*

From Fig. A.1 we find

$$q\phi(\bar{r}) = -\chi(\bar{r}) - \frac{E_g(\bar{r})}{2} + E_F(\bar{r}) - E_i(\bar{r})$$

To accommodate large carrier densities, we use the 3D density of states

$$D_{3D}(E) = \frac{1}{2\pi^2}\left(\frac{2m}{\hbar^2}\right)^{3/2}\sqrt{E}$$

together with the Fermi–Dirac distribution

$$f(E) = \frac{1}{1+\exp\left[\frac{E-E_F}{k_B T}\right]}$$

This allows us to calculate the electron concentration, n_0

$$\begin{aligned} n_0 &= \int_0^\infty D(E) f(E) dE = 2\left(\frac{2\pi m k_B T}{h^2}\right)^{3/2} \frac{2}{\sqrt{\pi}} \int_0^\infty \frac{\sqrt{\eta} d\eta}{1+\exp[\eta-\eta_F]} \\ &= N_c F_{1/2}(\eta_F) \end{aligned} \tag{A.4}$$

where $N_c = 2\left(\frac{2\pi m k_B T}{h^2}\right)^{3/2}$ is the effective density of states in the conduction band, $\eta_F = -(E_c - E_f)/(k_B T)$, and $F_j(\eta_F)$ is the Fermi–Dirac integral of order j

$$F_j(\eta_F) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{\eta^j d\eta}{1+\exp[\eta-\eta_F]}$$

where Γ is the gamma function. The hole concentration, p_0, can be calculated analogously

$$p_0 = N_v F_{1/2}\left(\eta_F - \frac{E_g}{k_B T}\right) \tag{A.5}$$

For a given device structure, we need to solve the Poisson equation

$$\nabla^2 \phi(\bar{r}) = -\frac{q}{\varepsilon} \rho(\bar{r})$$

where q is the elementary charge, ε is the material permittivity and $q\rho(\bar{r}) = q(N_d(\bar{r}) - N_a(\bar{r}) + p_0(\bar{r}) - n_0(\bar{r}))$ is the charge density, with N_d and N_a being the donor and acceptor concentration, respectively. It should be noted that, for more advanced semiconductor device simulations, where current flow is also of interest, the Poisson equation can be coupled with diffusion equations for electrons and holes.

A.3 Conductivity tensor

For a conductive medium, the current density $\bar{J}$ depends linearly on the material conductivity σ and the applied electric field $\bar{E}$

$$\bar{J} = \sigma \bar{E}. \tag{A.6}$$

For Hall effect measurements, however, we also apply a magnetic field $\bar{B}$. A charged particle moving in both the electric field and the magnetic field $\bar{B}$ experiences the Lorentz force

$$F = q\left(\bar{E} + \bar{v} \times \bar{B}\right).$$

The additional term originating from the magnetic field will result in a force acting perpendicular to the motion of the charged particle. Thus, to describe the current in a conductive medium when both an electric field and a magnetic field is applied, we cannot use the simple model of Eqn. (A.6), but need to introduce a conductivity tensor.

$$\bar{J} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{pmatrix} \cdot \bar{E} \tag{A.7}$$

We need to find the components σ_{ij} of the conductivity tensor as both electric and magnetic fields are applied.

Within the relaxation approximation, the motion of a charge carrier in a conductive medium is described by

$$m\left(\frac{d\bar{v}}{dt} + \frac{\bar{v}}{\tau}\right) = q\bar{E} + q\bar{v} \times \bar{B} \tag{A.8}$$

where t is time, m is the mass of the particle and τ is the scattering time. We now assume that the magnetic field is applied in the z-direction, $\bar{B} = (0, 0, B)$. This allows us to separate Eqn. (A.8) into x- and y-components

$$m\left(\frac{dv_x}{dt} + \frac{v_x}{\tau}\right) = q\left(E_x + v_y B\right) \tag{A.9}$$

$$m\left(\frac{dv_y}{dt} + \frac{v_y}{\tau}\right) = q\left(E_y - v_x B\right) \tag{A.10}$$

$$m\left(\frac{dv_z}{dt} + \frac{v_z}{\tau}\right) = qE_z \tag{A.11}$$

In steady state we have $\frac{dv_x}{dt} = \frac{dv_y}{dt} = \frac{dv_z}{dt} = 0\,\mathrm{m/s^2}$. This allows us to solve Eqns. (A.9–A.11) for v_x, v_y and v_z to yield

$$\begin{aligned} v_x &= \frac{q\tau/m\left(E_x + \omega\tau E_y\right)}{1 + \left(\omega\tau\right)^2} \\ v_y &= \frac{q\tau/m\left(E_y - \omega\tau E_x\right)}{1 + \left(\omega\tau\right)^2} \\ v_z &= \frac{q\tau}{m} E_z \end{aligned}$$

where $\omega = \frac{qB}{m}$ was introduced.

Using the individual components of $\bar{J}$ from A.7 allows us to identify the components of $\bar{\sigma}$

$$\bar{\sigma} = \sigma_0 \begin{pmatrix} \frac{1}{1+(\omega\tau)^2} & -\frac{\omega\tau}{1+(\omega\tau)^2} & 0 \\ \frac{\omega\tau}{1+(\omega\tau)^2} & \frac{1}{1+(\omega\tau)^2} & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

where σ_0 is the isotropic conductivity $\sigma_0 = \frac{q^2 n\tau}{m}$.

The effect from the magnetic field can perhaps be more clearly understood by using the resistivity tensor $\bar{\rho} = \bar{\sigma}^{-1}$.

$$\bar{\rho} = \frac{1}{\sigma_0} \begin{pmatrix} 1 & \omega\tau & 0 \\ -\omega\tau & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} = \begin{pmatrix} \rho_0 & B \cdot R & 0 \\ -B \cdot R & \rho_0 & 0 \\ 0 & 0 & \rho_0 \end{pmatrix}$$

where $R = \frac{1}{qn}$. From this we find that the magnetic field affects the transverse conductivity only, and the scattering time introduced in the expression for the conductivity tensor does not affect the measured Hall characteristics.

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Bibliography

[1] R. S. Wagner, W. C. Ellis, Vapor-Liquid-Solid Mechanism of Single Crystal Growth, Applied Physics Letters 4 (5) (1964) 89.

[2] K. Hiruma, H. Murakoshi, M. Yazawa, T. Katsuyama, Self-organized growth of GaAsInAs heterostructure nanocylinders by organometallic vapor phase epitaxy, Journal of crystal growth 163 (1996) 226–231.

[3] B. J. Ohlsson, M. T. Björk, M. H. Magnusson, K. Deppert, L. Samuelson, L. R. Wallenberg, Size-, shape-, and position-controlled gaas nano-whiskers, Applied Physics Letters 79 (20) (2001) 3335.

[4] M. T. Björk, B. J. Ohlsson, C. Thelander, A. I. Persson, K. Deppert, L. R. Wallenberg, L. Samuelson, Nanowire resonant tunneling diodes, Applied Physics Letters 81 (23) (2002) 4458.

[5] M. T. Borgström, M. A. Verheijen, G. Immink, T. D. Smet, E. P. A. M. Bakkers, Interface study on heterostructured GaP-GaAs nanowires., Nanotechnology 17 (16) (2006) 4010–4013.

[6] S. O. Mariager, S. L. Lauridsen, C. B. Sörensen, A. Dohn, P. R. Willmott, J. Nygård, R. Feidenhans'l, Stages in molecular beam epitaxy growth of GaAs nanowires studied by x-ray diffraction., Nanotechnology 21 (11) (2010) 115603.

[7] N. Holonyak, C. M. Wolfe, J. S. Moore, Vapor-Liquid-Solid Growth of Gallium Phosphide, Applied Physics Letters 6 (4) (1965) 64.

[8] E. I. Givargizov, Periodic instability in whisker growth, Journal of Crystal Growth 20 (1973) 217–226.

[9] F. Lefaucheux, M. C. Robert, GaAs whiskers grown by a thermal decomposition method, Journal of Crystal Growth 38 (1977) 29–37.

[10] M. Yazawa, M. Koguchi, K. Hiruma, Heteroepitaxial ultrafine wire-like growth of InAs on GaAs substrates, Applied Physics Letters 58 (10) (1991) 1080.

[11] K. Hiruma, M. Yazawa, T. Katsuyama, K. Ogawa, K. Haraguchi, M. Koguchi, H. Kakibayashi, Growth and optical properties of nanometer-scale GaAs and InAs whiskers, Journal of Applied Physics 77 (2) (1995) 447.

[12] M. Yazawa, M. Koguchi, A. Muto, M. Ozawa, K. Hiruma, Effect of one monolayer of surface gold atoms on the epitaxial growth of InAs nanowhiskers, Applied Physics Letters 61 (17) (1992) 2051.

[13] K. Hiruma, M. Yazawa, K. Haraguchi, K. Ogawa, T. Katsuyama, M. Koguchi, H. Kakibayashi, GaAs free-standing quantum-size wires, Journal of Applied Physics 74 (5) (1993) 3162.

[14] H. Dai, E. Wong, Y. Lu, S. Fan, C. Lieber, Synthesis and characterization of carbide nanorods, Nature 375 (1995) 769–772.

[15] P. Yang, C. M. Lieber, Nanorod-superconductor composites: a pathway to materials with high critical current densities, Science 273 (5283) (1996) 1836–1840.

[16] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, L. Samuelson, One-dimensional Steeplechase for Electrons Realized, Nano Letters 2 (2) (2002) 87–89.

[17] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, L. Samuelson, One-dimensional heterostructures in semiconductor nanowhiskers, Applied Physics Letters 80 (6) (2002) 1058.

[18] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, C. M. Lieber, Growth of nanowire superlattice structures for nanoscale photonics and electronics., Nature 415 (2002) 617–620.

[19] Y. Wu, R. Fan, P. Yang, Block-by-Block Growth of Single-Crystalline Si/SiGe Superlattice Nanowires, Nano Letters 2 (2) (2002) 83–86.

[20] S. Sburlan, P. Daniel Dapkus, A. Nakano, Critical dimensions of highly lattice mismatched semiconductor nanowires grown in strain-releasing configurations, Applied Physics Letters 100 (16) (2012) 163108.

[21] B. Eisenhawer, V. Sivakov, A. Berger, S. Christiansen, Growth of axial SiGe heterostructures in nanowires using pulsed laser deposition., Nanotechnology 22 (30) (2011) 305604.

[22] M. T. Björk, C. Thelander, A. E. Hansen, L. Jensen, M. W. Larsson, R. Wallenberg, L. Samuelson, Few-electron quantum dots in nanowires, Nano Letters 4 (9) (2004) 1621–1625.

[23] Y. Hu, H. O. H. Churchill, D. J. Reilly, J. Xiang, C. M. Lieber, C. M. Marcus, A Ge/Si heterostructure nanowire-based double quantum dot with integrated charge sensor., Nature nanotechnology 2 (10) (2007) 622–625.

[24] T. Mårtensson, C. P. T. Svensson, B. A. Wacaser, M. Larsson, W. Seifert, K. Deppert, A. Gustafsson, R. Wallenberg, L. Samuelson, Epitaxial III-V nanowires on silicon, Nano Letters 4 (10) (2004) 1987–1990.

[25] GaN nanorods for improved light emitting diode performance, Vol. 4.

[26] R. Koester, J.-S. Hwang, D. Salomon, X. Chen, C. Bougerol, J.-P. Barnes, D. L. S. Dang, L. Rigutti, A. de Luna Bugallo, G. Jacopin, M. Tchernycheva, C. Durand, J. Eymery, M-plane core-shell InGaN/GaN multiple-quantum-wells on GaN wires for electroluminescent devices., Nano letters 11 (11) (2011) 4839–4845.

[27] T. Bryllert, L. E. Wernersson, L. Fröberg, L. Samuelson, Vertical high-mobility wrap-gated InAs nanowire transistor, IEEE Electron Device Letters 27 (5) (2006) 323–325.

[28] T. Tanaka, K. Tomioka, S. Hara, J. Motohisa, E. Sano, T. Fukui, Vertical Surrounding Gate Transistors Using Single InAs Nanowires Grown on Si Substrates, Applied Physics Express 3 (2) (2010) 025003.

[29] K. Moselund, H. Schmid, C. Bessire, M. T. Björk, H. Ghoneim, H. Riel, InAs-Si Nanowire Heterojunction Tunnel FETs, IEEE Electron Device Letters 33 (10) (2012) 1453–1455.

[30] T. Mårtensson, P. Carlberg, M. Borgström, L. Montelius, W. Seifert, L. Samuelson, Nanowire arrays defined by nanoimprint lithography, Nano Letters 4 (4) (2004) 699–702.

[31] C. Thelander, L. E. Fröberg, C. Rehnstedt, L. Samuelson, L.-E. Wernersson, Vertical enhancement-mode InAs nanowire field-effect transistor with 50-nm wrap gate, Electron Device 29 (3) (2008) 206–208.

[32] J. Goldberger, A. I. Hochbaum, R. Fan, P. Yang, Silicon Vertically Integrated Nanowire Field Effect Transistors, Nano Letters 6 (5) (2006) 973–977.

[33] S. Johansson, S. G. Ghalamestani, M. Egard, M. Borg, M. Berg, L.-E. Wernersson, E. Lind, High frequency vertical InAs nanowire MOSFETs integrated on Si substrates, Physica Status Solidi (C) 9 (2) (2012) 350–353.

[34] M. Egard, S. Johansson, A.-C. Johansson, K.-M. Persson, a. W. Dey, B. M. Borg, C. Thelander, L.-E. Wernersson, E. Lind, Vertical InAs nanowire wrap gate transistors with f(t) $>$ 7 GHz and f(max) $>$ 20 GHz., Nano letters 10 (3) (2010) 809–812.

[35] A. Dey, J. Svensson, M. Borg, M. Ek, L.-E. Wernersson, Single InAs/GaSb Nanowire Low-Power CMOS Inverter, Nano Letters 12 (11) (2012) 5593–5597.

[36] X. Li, Z. Chen, N. Shen, D. Sarkar, N. Singh, K. Banerjee, G.-q. Lot, D.-L. Kwong, Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire, IEEE Electron Device Letters 32 (11) (2011) 1492–1494.

[37] M. T. Björk, J. Knoch, H. Schmid, H. Riel, W. Riess, Silicon nanowire tunneling field-effect transistors, Applied Physics Letters 92 (19) (2008) 193504.

[38] J. T. Smith, C. Sandow, S. Das, R. A. Minamisawa, S. Mantl, J. Appenzeller, Silicon nanowire tunneling field-effect transistor arrays: Improving subthreshold performance using excimer laser annealing, IEEE Transactions on Electron Devices 58 (7) (2011) 1822–1829.

[39] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, S. Lee, Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing (< 50 mV/decade) at Room Temperature, IEEE Electron Device Letters 32 (4) (2011) 437–439.

[40] A. L. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing, T. S. Mayer, Fabrication and Characterization of Axially Doped Silicon Nanowire Tunnel Field-Effect Transistors., Nano letters 10 (2010) 4813–4818.

[41] B. Ganjipour, J. Wallentin, M. T. Borgström, L. Samuelson, C. Thelander, Tunnel Field-Effect Transistors Based on InP-GaAs Heterostructure Nanowires, ACS Nano 6 (4) (2012) 3109–3113.

[42] Impact Ionization Nanowire Transistor with Multiple-Gates, Silicon-Germanium Impact Ionization Region, and Sub-5 mV/decade Subtheshold Swing.

[43] T.-W. Yeh, Y.-T. Lin, B. Ahn, L. S. Stewart, P. D. Dapkus, S. R. Nutt, Vertical nonpolar growth templates for light emitting diodes formed with GaN nanosheets, Applied Physics Letters 100 (3) (2012) 033119.

[44] X. Duan, Y. Huang, Y. Cui, J. Wang, C. M. Lieber, Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices., Nature 409 (4) (2001) 66–69.

[45] Y. Huang, X. Duan, C. M. Lieber, Nanowires for integrated multicolor nanophotonics., Small 1 (1) (2005) 142–147.

[46] E. D. Minot, F. Kelkensberg, M. van Kouwen, J. a. van Dam, L. P. Kouwenhoven, V. Zwiller, M. T. Borgström, O. Wunnicke, M. A. Verheijen, E. P. A. M. Bakkers, Single quantum dot nanowire LEDs., Nano letters 7 (2) (2007) 367–371.

[47] F. Qian, Y. Li, S. Gradecak, D. Wang, C. Barrelet, C. Lieber, Gallium nitride-based nanowire radial heterostructures for nanophotonics, Nano Letters 4 (10) (2004) 1975–1979.

[48] C. P. T. Svensson, T. Mårtensson, J. Trägårdh, C. Larsson, M. Rask, D. Hessman, L. Samuelson, J. Ohlsson, Monolithic GaAs/InGaP nanowire light emitting diodes on silicon., Nanotechnology 19 (30) (2008) 305201.

[49] S. Sburlan, A. Nakano, P. D. Dapkus, Effect of substrate strain on critical dimensions of highly lattice mismatched defect-free nanorods, Journal of Applied Physics 111 (5) (2012) 054907.

[50] M. Borgström, J. Wallentin, M. Heurlin, S. Fält, P. Wickert, J. Leene, M. Magnusson, K. Deppert, L. Samuelson, Nanowires with promise for photovoltaics, IEEE Selected Topics in Quantum Electronics 17 (4) (2011) 1050–1061.

[51] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, E. D. Dunlop, Solar cell efficiency tables (version 41) 21 (2013) 1–11.

[52] C. Colombo, M. Heiss, M. Grätzel, A. Fontcuberta i Morral, Gallium arsenide p-i-n radial structures for photovoltaic applications, Applied Physics Letters 94 (17) (2009) 173108.

[53] J. Wang, M. S. Gudiksen, X. Duan, Y. Cui, C. M. Lieber, Highly polarized photoluminescence and photodetection from single indium phosphide nanowires., Science (New York, N.Y.) 293 (2001) 1455–1457.

[54] H. Goto, K. Nosaki, K. Tomioka, S. Hara, K. Hiruma, J. Motohisa, T. Fukui, Growth of Core–Shell InP Nanowires for Photovoltaic Application by Selective-Area Metal Organic Vapor Phase Epitaxy, Applied Physics Express 2 (2009) 035004.

[55] J. Wallentin, N. Anttu, D. Asoli, M. Huffman, I. Åberg, M. Magnusson, G. Siefer, P. Fuss-Kailuweit, F. Dimroth, B. Witzigmann, H. Q. Xu, L. Samuelson, K. Deppert, M. T. Borgström, InP Nanowire Array Solar Cells Achieving 13.8% Efficiency by Exceeding the Ray Optics Limit, Science 339 (6) (2013) 1057–1060.

[56] M. Heurlin, M. H. Magnusson, D. Lindgren, M. Ek, L. R. Wallenberg, K. Deppert, L. Samuelson, Continuous gas-phase synthesis of nanowires with tunable properties., Nature 492 (2012) 90–94.

[57] J. Wallentin, M. T. Borgström, Doping of semiconductor nanowires, Journal of Materials Research 26 (17) (2011) 2142–2156.

[58] O. Wunnicke, Gate capacitance of back-gated nanowire field-effect transistors, Applied Physics Letters 89 (8) (2006) 083102.

[59] A. V. Kretinin, R. Popovitz-Biro, D. Mahalu, H. Shtrikman, Multimode Fabry-Perot conductance oscillations in suspended stacking-faults-free InAs nanowires., Nano letters 10 (9) (2010) 3439–3445.

[60] O. Karlström, A. Wacker, K. Nilsson, G. Astromskas, S. Roddaro, L. Samuelson, L.-E. Wernersson, Analysing the capacitance-voltage measurements of vertical wrapped-gated nanowires., Nanotechnology 19 (43) (2008) 435201.

[61] E. Lind, Y.-M. Niquet, H. Mera, L.-E. Wernersson, Accumulation capacitance of narrow band gap metal-oxide-semiconductor capacitors, Applied Physics Letters 96 (23) (2010) 233507.

[62] S. Chuang, Q. Gao, R. Kapadia, A. C. Ford, J. Guo, A. Javey, Ballistic InAs Nanowire Transistors., Nano letters 13 (2) (2013) 555–558.

[63] D. A. Anderson, N. Apsley, The Hall effect in III-V semiconductor assessment, Semiconductor Science and Technology 1 (3) (1986) 187–202.

[64] D. Kranzer, Hall coefficient factor in polar semiconductors, Journal of Physics and Chemistry of Solids 34 (1973) 9–13.

[65] M. a. Zimmler, D. Stichtenoth, C. Ronning, W. Yi, V. Narayanamurti, T. Voss, F. Capasso, Scalable fabrication of nanowire photonic and electronic circuits using spin-on glass., Nano letters 8 (6) (2008) 1695–1699.

[66] J. R. Weber, A. Janotti, C. G. Van de Walle, Intrinsic and extrinsic causes of electron accumulation layers on InAs surfaces, Applied Physics Letters 97 (19) (2010) 192106.

[67] C. Blömers, T. Grap, M. I. Lepsa, J. Moers, S. Trellenkamp, D. Grützmacher, H. Lüth, T. Schäpers, Hall effect measurements on InAs nanowires, Applied Physics Letters 101 (15) (2012) 152106.

[68] L. Samuelson, P. Omling, H. Titze, H. G. Grimmeiss, Electrical and optical properties of deep levels in MOVPE grown GaAs, Journal of Crystal Growth 55 (1981) 164–172.

[69] Simulation and design of core-shell GaN nanowire LEDs, Vol. 7597.

[70] A. Gustafsson, K. Hillerich, M. E. Messing, K. Storm, K. a. Dick, K. Deppert, J. Bolinsson, A cathodoluminescence study of the influence of the seed particle preparation method on the optical properties of GaAs nanowires., Nanotechnology 23 (26) (2012) 265704.

[71] J. Bolinsson, K. Mergenthaler, L. Samuelson, A. Gustafsson, Diffusion length measurements in axial and radial heterostructured nanowires using cathodoluminescence, Journal of Crystal Growth 315 (1) (2011) 138–142.

[72] K. Ishikawa, N. Yamamoto, K. Tateno, Y. Watanabe, Characterization of Individual GaAs/AlGaAs Self-Standing Nanowires by Cathodoluminescence Technique using Transmission Electron Microscope, Japanese Journal of Applied Physics 47 (8) (2008) 6596–6600.

[73] M. Bugajski, W. Lewandowski, Concentration-dependent absorption and photoluminescence of n-type InP, Journal of Applied Physics 57 (2) (1985) 521.

[74] J. Moers, S. Trellenkamp, D. Grützmacher, A. Offenhäusser, B. Rienks, Optimized marker definition for high overlay accuracy e-beam lithography, Microelectronic Engineering 97 (2012) 68–71.

[75] D. A. Anderson, N. Apsley, P. Davies, P. L. Giles, Compensation in heavily doped n-type InP and GaAs, Journal of Applied Physics 58 (8) (1985) 3059.

[76] E. Nicollian, J. Brews, MOS/metal oxide semiconductor/physics and technology, Wiley-Interscience (November 21, 2002), 1982.

[77] CV measurements of single vertical nanowire capacitors.

[78] E. C. Garnett, Y.-C. Tseng, D. R. Khanal, J. Wu, J. Bokor, P. Yang, Dopant profiling and surface analysis of silicon nanowires using capacitance-voltage measurements, Nature Nanotechnology 4 (March) (2009) 311–314.

[79] R. W. Robinett, Visualizing the solutions for the circular infinite well in quantum and classical mechanics, American Journal of Physics 64 (4) (1996) 440–446.

[80] R. Tu, L. Zhang, Y. Nishi, H. Dai, Measuring the capacitance of individual semiconductor nanowires for carrier mobility assessment., Nano letters 7 (6) (2007) 1561–1565.

[81] G. Astromskas, K. Storm, O. Karlström, P. Caroff, M. Borgström, L.-E. Wernersson, Doping Incorporation in InAs nanowires characterized by capacitance measurements, Journal of Applied Physics 108 (5) (2010) 054306.

[82] G. Astromskas, K. Storm, P. Caroff, M. Borgström, E. Lind, L.-E. Wernersson, Temperature and frequency characterization of InAs nanowire and HfO2 interface using capacitance-voltage method, Microelectronic Engineering 88 (4) (2011) 444–447.

[83] G. Astromskas, K. Storm, L.-E. Wernersson, Transient studies on InAs/HfO2 nanowire capacitors, Applied Physics Letters 98 (1) (2011) 013501.

[84] A. C. Bleszynski, F. a. Zwanenburg, R. M. Westervelt, A. L. Roest, E. P. a. M. Bakkers, L. P. Kouwenhoven, Scanned probe imaging of quantum dots inside InAs nanowires., Nano letters 7 (9) (2007) 2559–2562.

[85] H. A. Nilsson, P. Samuelsson, P. Caroff, H. Q. Xu, Supercurrent and multiple Andreev reflections in an InSb nanowire Josephson junction., Nano letters 12 (1) (2012) 228–233.

[86] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, K. C. Saraswat, Germanium nanowire field-effect transistors with SiO[sub 2] and high-κ HfO[sub 2] gate dielectrics, Applied Physics Letters 83 (12) (2003) 2432.

[87] D. R. Khanal, J. Wu, Gate coupling and charge distribution in nanowire field effect transistors., Nano letters 7 (9) (2007) 2778–2783.

[88] H. J. Round, A note on carborundum, Electrical world 49 (1907) 309.

[89] O. V. Lossev, Luminous carborundum detector and detection effect and oscillations with crystals, Philosophical Magazine 6 (39) (1928) 1024–1044.

[90] H. G. Grimmeiss, J. W. Allen, Light emitting diodes - How it started, Journal of Non-Crystalline Solids 352 (2006) 871–880.

[91] J. Tsao, Solid-state lighting: lamps, chips, and materials for tomorrow, Circuits and Devices Magazine, IEEE 20 (3) (2004) 28–37.

[92] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, E. D. Dunlop, Solar cell efficiency tables (version 40), Progress in Photovoltaics 20 (2012) 606–614.

[93] F. Raissi, A Brief Analysis of the Field Effect Diode and Breakdown Transistor, IEEE Transactions on Electron Devices 43 (2) (1996) 362–365.

[94] I. Sheikhian, F. Raissi, High-speed digital family using field effect diode, Electronics Letters 39 (4) (2003) 345–347.

[95] I. Sheikhian, F. Raissi, Simulation Results for Nanoscale Field Effect Diode, IEEE Transactions on Electron Devices 54 (3) (2007) 613–617.

[96] Field effect diode for effective CDM ESD protection in 45 nm SOI technology.

[97] S. Cao, A. Salman, J.-H. Chun, S. Beebe, M. Pelella, R. Dutton, Design and characterization of ESD protection devices for high-speed I/O in advanced SOI technology, IEEE Transactions on Electron Devices 57 (3) (2010) 644–653.

[98] Y. Yang, A. A. Salman, D. E. Ioannou, S. G. Beebe, Design and optimization of the SOI field effect diode (FED) for ESD protection, Solid-State Electronics 52 (10) (2008) 1482–1485.

[99] M. Amirmazlaghani, F. Raissi, Memory cell using Modified Field Effect Diode, IEICE Electronics Express 6 (22) (2009) 1582–1586.

[100] Scaling of the SOI field effect diode (FED) for memory application.

[101] C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, W. Riess, B. J. Ohlsson, U. Gösele, L. Samuelson, Nanowire-based one-dimensional electronics, Materials today 9 (10) (2006) 28–35.

[102] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, M. Meyyappan, Single Crystal Nanowire Vertical Surround-Gate Field-Effect Transistor, Nano Letters 4 (7) (2004) 1247–1252.

[103] Wrap-gated InAs nanowire field-effect transistor.

[104] C. Thelander, C. Rehnstedt, L. E. Fröberg, E. Lind, T. Mårtensson, P. Caroff, T. Löwgren, J. Ohlsson, L. Samuelson, L.-E. Wernersson, Development of a vertical wrap-gated InAs FET, IEEE Transactions on Electron Devices 55 (11) (2008) 3030–3036.

[105] C. Fasth, A. Fuhrer, M. T. Björk, L. Samuelson, Tunable double quantum dots in InAs nanowires defined by local gate electrodes., Nano letters 5 (7) (2005) 1487–1490.

[106] A. Pfund, I. Shorubalko, R. Leturcq, K. Ensslin, Top-gate defined double quantum dots in InAs nanowires, Applied Physics Letters 89 (25) (2006) 252106.

[107] S. A. Dayeh, C. Soci, P. K. L. Yu, E. T. Yu, D. Wang, Influence of surface states on the extraction of transport parameters from InAs nanowire field effect transistors, Applied Physics Letters 90 (16) (2007) 162112.

[108] I. van Weperen, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov, L. P. Kouwenhoven, Quantized Conductance in an InSb Nanowire., Nano letters 13 (2) (2013) 387–391.

[109] L. H. Kristinsdóttir, J. C. Cremon, H. a. Nilsson, H. Q. Xu, L. Samuelson, H. Linke, A. Wacker, S. M. Reimann, Signatures of Wigner localization in epitaxially grown nanowires, Physical Review B 83 (4) (2011) 041101.

[110] J. Du, D. Liang, H. Tang, X. P. a. Gao, InAs nanowire transistors as gas sensor and the response mechanism., Nano letters 9 (12) (2009) 4348–4351.

[111] X. P. A. Gao, G. Zheng, C. M. Lieber, Subthreshold regime has the optimal sensitivity for nanowire FET biosensors., Nano letters 10 (2) (2010) 547–552.

[112] P. Yang, R. Yan, M. Fardy, Semiconductor nanowire: what's next?, Nano letters 10 (5) (2010) 1529–1536.

[113] A. K. Wanekaya, W. Chen, N. V. Myung, A. Mulchandani, Nanowire-Based Electrochemical Biosensors, Electroanalysis 18 (6) (2006) 533–550.