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Linearity Enhancements of Receiver Front-end Circuits for Wireless Communication

Abdulaziz, Mohammed

2016

Document Version:
Publisher's PDF, also known as Version of record

Link to publication

Citation for published version (APA):
Abdulaziz, M. (2016). *Linearity Enhancements of Receiver Front-end Circuits for Wireless Communication*. [Doctoral Thesis (compilation), Department of Electrical and Information Technology].

Total number of authors:
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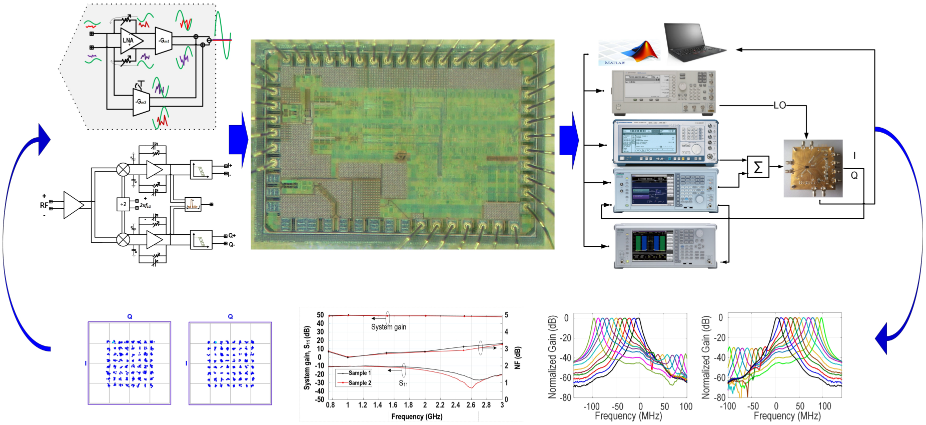
LNA
-Gm1
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+
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Q+
Q-
MATLAB
LO
Σ
I
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System gain
Sample 1
Sample 2
S11
System gain, S11 (dB)
NF (dB)
Frequency (GHz)
0.8 1 1.2 1.4 1.6 1.8 2 2.2 2.4 2.6 2.8 3
50 40 30 20 10 0 -10 -20 -30 -40 -50
5 4 3 2 1 0
Normalized Gain (dB)
0 -20 -40 -60 -80
Frequency (MHz)
-100 -50 0 50 100

Doctoral Dissertation

Linearity Enhancements of Receiver Front-End Circuits for Wireless Communication

Mohammed Abdulaziz

Department of Electrical and Information Technology,
Faculty of Engineering, LTH, Lund University, 2016.

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Department of Electrical and Information Technology
ISSN 1654-790X
No.82
ISBN 978-91-7623-693-2 (print)
ISBN 978-91-7623-694-9 (pdf)
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Mohammed Abdulaziz

LUND INSTITUTE OF TECHNOLOGY
Lund University

Doctoral Dissertation
Lund, May 2016

Department for Electrical and Information Technology
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P.O. Box 118
SE-221 00 LUND
SWEDEN

ISSN 1654-790X, no.82
ISBN 978-91-7623-693-2 (print)
ISBN 978-91-7623-694-9 (pdf)
Series of licentiate and doctoral dissertations.

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Produced using LaTeX Documentation System.
Printed in Sweden by *Tryckeriet i E-huset*, Lund.
May 2016.

To Fathia and Ebtehal

Abstract

Technology scaling in advanced CMOS nodes has been very successful in reducing the cost and increasing the operating frequency, however, it has also resulted in reduced transistor intrinsic gain and increased thermal noise coefficient, and most importantly, deteriorated linearity performance. At the same time, advanced wireless communication standards offer ever increasing data rates and pose more stringent requirements on coexistence, leading to very stringent linearity requirements.

The objective of this dissertation is therefore to investigate techniques for enhancing the linearity of the receiver front-end in CMOS technology. The bandwidth of two-stage operational transconductance amplifiers (OTAs) in closed loop configuration is addressed in paper I and a compensation technique is proposed using positive feedback RC links. Analysis shows that this introduces two left hand plane zeros and two high frequency parasitic poles. In paper II the compensated OTA is used in a fifth order active-RC channel select filter (CSF) for LTE-Rel 8. The filter's power consumption measures only 3.4mW, and the linearity at the band edge and out-of-band is not deteriorated.

In paper III, the linearity of the well-known triode OTA with feedback amplifiers is investigated, and feedforward linearization is proposed instead of using feedback amplifiers. Not only are the amplifiers removed along with their power consumption, but also state-of-the-art linearity is achieved.

Paper IV proposes a novel linearization technique suitable for high frequency OTAs. The linearization draws no bias current and measurements show that it is robust to mismatch as well as temperature and voltage variations. A low noise amplifier is simulated and a fourth order OTA-C filter was measured, demonstrating the performance of the technique.

Finally, in paper V a fully integrated receiver front-end with spectrum sensing is presented, including measurements with LTE signals. Different blocker scenarios were measured and it is concluded that spectrum sensing is very beneficial for blocker handling, resulting in significantly improved performance. Furthermore, the effect of noise cancellation and improvements of the OTA linearity are demonstrated on the overall front-end performance.

Populärvetenskaplig Sammanfattning

The consumer demands on the performance of high-end wireless handsets (e.g. smart phones) are ever increasing. A smart phone for example needs to be very fast at download and upload of data, at the same time it needs to be energy efficient, which is bench-marked by the time it can be used without the need of recharging the battery. Added to that, the phone user needs to be connected all the time, even in rural areas where signal is weak.

Next generation wireless standards must satisfy customer demands on speed, which is complicated by the band fragmentation. The cellular frequencies are divided between different operators, but the frequencies assigned to one operator are not necessarily close to each other. In other words, two contiguous channels don't necessarily belong to the same operator. This means that increasing the channel bandwidth requires special measures where several narrow channels are combined, called carrier aggregation. This will add to the complexity of the hardware.

To be able to integrate millions of transistors on the same chip performing advanced functions at high speed and low power consumption, extensive research is directed towards technology scale down. Unfortunately reducing the size of the devices also implies reducing the supply voltage, which directly limits the largest signal that can be linearly processed. Linearly processed means that the wanted signal is not distorted significantly. Therefore, technology scale down improves the operation speed and power consumption, but has negative impact on signal quality.

The linearity issue in advanced technologies is very challenging because distortion due to interfering signals appears and contaminates the desired signal due to nonlinearity. The strong signals can also saturate the receiver preventing reception of the wanted signal. This problem is similar to trying to listen to one talking while foghorn is sounding at the same time. Unless the one we want to listen to raises his/her voice or the other sound becomes quieter, it is very difficult to listen and understand.

In this dissertation, the problem of receiving weak signals in the presence of strong interference is addressed. Three channel select filters are designed and implemented with improved linearity, and a full receiver front-end for carrier aggregation with spectrum sensing is also implemented. These solutions are analyzed and simulated, and chips are fabricated and measured to verify the performance and compare to the analysis.

This work was supported by the Swedish foundation for strategic research (SSF) and the chips fabrication was sponsored by ST-Microelectronics.

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Preface

This work was funded by SSF - the Swedish foundation for strategic research. In this dissertation my work as a PhD student is presented.

Included Research Papers

The main research activities, analysis, and results reported are from the papers attached at the end of this thesis and are listed below:

[1] M. Abdulaziz, M. Törmänen, and H. Sjöland, "A Compensation Technique for Two-Stage Differential OTAs," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, vol. 61, no. 8, pp. 594–598, Aug. 2014.

[2] M. Abdulaziz, A. Nejdel, M. Törmänen, and H. Sjöland, "A 3.4mW 65nm CMOS 5$^{\text{th}}$ order programmable active-RC channel select filter for LTE receivers," in *RFIC*, Seattle, Washington, June 2–4 2013, pp. 217–220.

[3] M. Abdulaziz, M. Törmänen, and H. Sjöland, "A 4$^{\text{th}}$ order Gm-C filter with 10MHz bandwidth and 39dBm IIP3 in 65nm CMOS," in *Proc. of 40th IEEE ESSCIRC 2014*, Venice, Italy, Sept. 22–26 2014, pp. 367–370.

[4] M. Abdulaziz, W. Ahmad, M. Törmänen, and H. Sjöland, "A Linearization Technique for Differential OTAs," (Submitted).

[5] M. Abdulaziz, W. Ahmad, A. Nejdel, M. Törmänen, and H. Sjöland, "A Cellular Receiver Front-End with Blocker Sensing," in *RFIC*, San Francisco, California, May 22–24 2016, (Accepted).

Related publications

I have also co-authored the following papers, which are not considered as a part of this dissertation.

[6] W. Ahmad, M. Abdulaziz, A. Nejdel, M. Törmänen, and H. Sjöland, "CMOS Integrated Remote Antenna Unit for Fiber-fed Distributed MIMO Systems", (Submitted).

[7] A. Nejdel, M. Abdulaziz, M. Törmänen, and H. Sjöland, "A Positive Feedback Passive Mixer-First Receiver Front-End," in *RFIC*, Phoenix, Arizona, May 17–19 2015, pp. 79–82.

[8] W. Ahmad, M. Abdulaziz, M. Törmänen, and H. Sjöland, "CMOS Adaptive TIA with Embedded Single-Ended to Differential Conversion for Analog Optical Links," in *Proc. of IEEE International Symposium* *on Circuits and Systems, ISCAS'15*, Lisbon, Portugal, May 24–May 27 2015, pp. 658–661.

[9] R. Gangarajaiah, M. Abdulaziz, H. Sjöland, and L. Liu, "Digitally Assisted Adaptive Non-Linearity Suppression Scheme for RF front ends," in *Proc. of 25th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, PIMRC'15*, Washington DC, USA, Sept. 2–5 2015, pp. 623–627.

[10] R. Gangarajaiah, M. Abdulaziz, H. Sjöland, P. Nilsson, and L. Liu, "A Digitally Assisted Nonlinearity Mitigation System for Tunable Channel Select Filters," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, vol. 63, no. 1, pp. 69–73, Jan. 2016.

[11] M. Abdulaziz, M. Shakir, P. Lu, and P. Andreani, "A 2.7GHz dividerless all digital phase-locked loop with 625Hz frequency resolution in 90nm CMOS," in *Proc. of 29th NORCHIP Conference*, Lund, Sweden, Nov. 14–15 2011.

[12] M. Shakir, M. Abdulaziz, P. Lu, and P. Andreani, "A mixed mode design flow for multi GHz ADPLLs," in *Proc. of 29th NORCHIP Conference*, Lund, Sweden, Nov. 14–15 2011.

Patent applications

M. Abdulaziz, Waqas Ahmad, and Henrik Sjöland, "Amplifier, Filter, Communication Apparatus and Network Node", *International application* No. PCT/EP2015/072613, 2015

Acknowledgments

I would like to acknowledge and express my sincere gratitude to all the people who helped and supported me during my studies.

First of all, to my supervisor Professor Henrik Sjöland: you are one of the most talented people I have seen in my life, technical discussions with you always shed the light on the matter. Your unique guidance and encouragement from idea development to manuscript thorough review are the key reason of the success of this project, you are also truly a very kind and caring person. Thank you for giving me the opportunity to pursue my PhD in Lund University, it was a great honor to work with you.

To my co-supervisor Associate Professor Markus Törmänen: for your continuous help and support, I have always knocked on your door uninvited and I was always welcome, thank you.

I would like to thank all the past and present colleagues in the RF group for the technical discussions and all friendly coffee breaks. Having you around always made the long working hours seem shorter. I would also like to thank all the colleagues in EIT department for creating such a friendly environment, especially, the digital ASIC group, the nano-electronics group, the mixed signal group, and the DARE project team headed by Professor Pietro Andreani who always was positive and open to new ideas. Also to Dr. Johan Wernehag for his technical help, reading parts of this thesis and for his kindness.

I had the chance to do a research visit at University of Twente in Netherlands, many thanks go to the friends in Twente: Professor Eric Klumprink for his very long and fruitful meetings, Professor Bram Nauta for giving me time and support that made the visit successful and Dr. Anne-Johan Annema. Also Gerdien Lammers for helping me with administrative matters. My gratitude extends to all the PhD students who gave me a very warm welcome and made me feel home, and Gerard Wienk in the CAD tools support.

I also would like to give special thanks to Dr. Lars Sundström from Ericsson research for giving me time to meet and discuss technical problems and taking the time to reply to my spam emails with very long and informative replies, and Göran Jönsson for his great help and patience in the lab and for allowing me to teach in his courses. Also the people involved in the technical support specially: Andreas Johansson for his great help in the lab and Erik Jonsson for keeping the systems up and running and fixing computer issues even at midnight, Bertil Lindvall, Stefan Molund for CAD tools support, Martin Nilsson for lab help and Lars Hedenstjerna. My gratitude extends to all the people involved in the administrative support, especially Pia Bruhn.

Finally, I would like to thank my family: my mother (Fathia), words could not describe how I feel about you, my father (Abdullah) you taught me everything I know. My wife (Ebtehal) for your limitless love, patience and support and my wonderful son (Abood) you are the reason why I feel great about the future. My brother and best friend (Moneer) you have been the one everybody in the family depends on, thank you. My youngest brother (Hasan) and my sisters (Belqees, Sara, Amani). I would like also to acknowledge father-in-law (Ali), mother-in-low (Sayda), my friend and brother-in-low (Ahmed Al-ahsab), and Mohammed Al-kohlani. Also, to all my friends in Sweden, especially Essam, in Yemen and the ones scattered around the world. I did not mention many, so to all of you I say thank you.

In memory of Professor Peter Nilsson and Haj Abdullah Mayas.

Mohammed Abdulaziz

Our greatest weakness lies in giving up. The most certain way to succeed is always to try just one more time.
– Thomas A. Edison –

List of Acronyms

ADC	Analog-to-digital converter
ASIC	Application specific integrated circuit
CA	Carrier aggregation
CDS	Complementary derivative superposition
CG	Common gate
CML	Current mode logic
CMOS	Complementary metal oxide semiconductor
CS	Common source
CSF	Channel select filter
DC	Direct current
DS	Derivative superposition
EVM	Error vector magnitude
FDD	Frequency division duplex
GBP	Gain bandwidth product
GE	Gain error
I	In-phase signal
$\mathrm{ICP}_{\mathrm{1dB}}$	Input referred 1dB compression point
IF	Intermediate frequency
IIPn	The n-th order input-referred intercept point
IMD	Intermodulation distortion
IMn	The n-th order intermodulation distortion
IP	Intercept point
IPn	The n-th order intercept point
IRR	Image rejection ratio
LNA	Low noise amplifier

LNTA	Low noise transconductance amplifier
LTE	Long term evolution
MOS	Metal oxide semiconductor
NC	Noise canceling
NF	Noise figure
OPAMP	Operational amplifier
OTA	Operational transconductance amplifier
PD	Power detector
PLL	Phase locked loop
PVT	Process, voltage and temperature
Q	Quadrature phase signal
QAM	Quadrature amplitude modulation
RF	Radio frequency
RX	Receiver
SNR	Signal-to-noise ratio
TF	Transfer function
TIA	Transimpedance amplifier
TX	Transmitter
VCCS	Voltage controlled voltage source
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier

List of Symbols

A	Forward gain
$A\beta$	Loop gain
A_v	Voltage gain
C	Capacitance (F)
C_{ox}	MOS transistor oxide capacitance per unit area (F/m^2)
e_j	The j$^{\text{th}}$ error vector in the received IQ symbol
g	Conductance (S)
g_m	Transistor transconductance (S)
G_m	OTA effective transconductance (S)
g_n	The n$^{\text{th}}$ order conductance (A/V^n)
g_o	Transistor output conductance (S)
i_D	Drain current (A)
IM_n	The n$^{\text{th}}$ order intermodulation distortion (W)
L	MOS transistor length (m)
L_{eff}	MOS transistor effective length (m)
L_{gyr}	Gyrator's inductance (H)
P_{avg}	Average received power (W)
P_{in}	Input power (W)
Q	Quality-factor
T	Temperature (K)
v_{DS}	MOS drain-source voltage (V)
v_{GS}	MOS gate-source voltage (V)
V_{th}	MOS transistor threshold voltage (V)
W	MOS transistor width (m)
Z_{BB}	Base band impedance (Ω)

Z_f	Feedback impedance (Ω)
Z_{in}	Input impedance (Ω)
Z_L	Load impedance (Ω)
Z_o	Output impedance (Ω)
β	Feedback factor
γ	The thermal noise coefficient
$\Delta\theta$	Phase imbalance ($^\circ$)
ϵ	Amplitude imbalance
ξ_h	Horizontal electrical field (V/m)
ξ_v	Vertical electrical field (V/m)
θ	Mobility reduction constant (V^{-1})
μ_n	Average electron mobility in the channel ($\mathrm{m}^2/(\mathrm{V}\cdot\mathrm{second})$)
ω_o	Angular resonance frequency (rad/second)
ω_p	Angular frequency of a pole (rad/second)
ω_z	Angular frequency of a zero (rad/second)

Introduction

Introduction

Chapter 1

Introduction

1.1 Motivation of the Work

For battery operated consumer electronics, requirements on performance continue to expand in many dimensions. In particular, the high-end market demands have exploded. The number of wireless connectivity links as well as their data rates are ever increasing, while the power consumption must be low to increase the time between battery recharges. Most importantly, the consumer electronics market is cost driven, limiting the ASIC implementations to CMOS technology. To minimize the cost, today's radio frequency transceivers are pushed towards being integrated together with the digital base band ASIC. The number of expensive off-chip filters is also reduced [13–15], posing more stringent linearity requirements on the receiver front-end.

Recent wireless communication standards such as LTE-A are pushing towards higher data rates, which necessitates wider channel bandwidth. Added to that, simultaneous transmission and reception is also supported (also referred to as frequency duplex division (FDD)), resulting in a strong transmit signal at a small duplex frequency distance from the wanted signal. Due to the ever increasing channel bandwidth, the relative duplex distance decreases, resulting in stronger interference, further increasing the linearity requirements of the receiver front-end.

Unfortunately cellular band fragmentation limits the possibility of assigning contiguous frequency bands to the operators. As a result, intra-band non-contiguous carrier aggregation (CA) and inter-band CA are introduced. In this way several narrow band channels can be combined into a single effective wide-band channel. This significantly complicates the hardware implementation of the receiver front-end and requires more advanced digital signal processing. Especially non-contiguous CA is troublesome since a frequency gap exists between carriers which, belongs to a different operator and thus can contain strong interference. A receiver front-end designed for contiguous and non-contiguous CA needs to have detailed information about which blockers are stronger, the in-gap or the out-of-band ones, motivating the need for spectrum sensing.

To be able to integrate more and more devices into a single ASIC, CMOS technology feature size has been continuously scaled down starting from a MOS device length (L) of several μm in 1960s, the device length is less than 20nm in today's most advanced technologies. Scaling has been very successful in reducing cost and adding more functionality. Driven by integration and speed, advanced CMOS technologies operate on reduced voltage supply and oxide thickness as well. All of this allows billions of transistors to be integrated into a single chip. Despite the great success in the performance of the scaled digital circuits, analog performance is in many cases heavily degraded. The increased vertical electrical field results in mobility reduction of the charge carriers and the horizontal electrical field results in carrier velocity saturation. As a result, the MOS devices in sub 100nm do not have square law characteristic anymore. This leads to increased distortion of the signal. Limited voltage headroom results in large signal compression which limits the maximum possible input signal and gain. At the same time, as mentioned, wireless communication trends put increasing requirement on receiver linearity.

Apart from all mentioned challenges, process, voltage and temperature variations (PVT) of the circuits can result in significant shifts of their operating point. For this reason performance evaluation of the test circuits needs to be performed over supply and temperature variations (-20°C to 80°C). The fabricated chips in this dissertation did not include process variation, however, since it is a multi-project wafer run for universities and hence only one process corner is fabricated. Therefore process variations are instead extensively simulated.

MOS transistor nonlinearity limits the achievable receiver front-end performance. The two main sources of nonlinearity are the transconductance (g_m) and output conductance (g_o), where circuit level linearization schemes need to be investigated. Linearization schemes must be robust to PVT variations to guarantee required performance under all operating conditions. As a system level technique, spectrum sensing is powerful as it provides the information needed to perform the required steps that result in optimal performance.

This dissertation is focused on the challenges faced when designing receiver front-ends for 4G cellular (LTE) applications. The main emphasis is on techniques enhancing the linearity when implementing such demanding functionality in CMOS technology. Improvement in operational transconductance amplifier (OTA) closed loop speed is investigated. OTA linearization techniques implemented in OTA-C channel select filters (CSFs), low noise amplifiers (LNAs), and feedback amplifiers are presented. Added to that, a complete receiver front-end with fully integrated spectrum sensing to detect blocker amplitude and frequency is also described.

1.2 Outline of the Thesis

The dissertation started by motivating the need for linearity improvements in wireless receiver front-ends. Then the widely used homodyne receiver architecture will be described. Next, the most important performance metrics will be briefly explained, followed by circuit-level building blocks. Finally, OTA linearization techniques and CSF implementations will be described. The organizations of this thesis is as follows:

Chapter 1 includes motivation of the work and describes major challenges of the art.

Chapter 2 presents an introduction to high performance receiver front-ends and their key performance metrics. An overview of the performance, properties and the building blocks of cellular receiver front-ends will be provided.

Chapter 3 describes circuit-level receiver front-end building blocks.

Chapter 4 describes active filters and OTA linearization techniques. CSFs as well as complex filters and spectrum sensing are treated.

Chapter 5 provides a summary of the included papers, including conclusions and scientific contributions of each paper.

Chapter 6 is a discussion about possibilities of future work.

Paper I introduces the phase enhanced compensation technique for two-stage OTAs. Detailed analysis and simulations are presented to evaluate the performance and robustness of the technique.

Paper II presents an implementation of a tunable 5^{th} order CSF with OTAs compensated using phase enhanced compensation. The performance benefits of the phase enhanced compensation technique are demonstrated by the measurement results of the filter.

Paper III reports the design and measured results of a highly linear 4^{th} order OTA-C filter. In this case triode OTAs are used with capacitive feed forward for nonlinearity cancellation. Mismatch simulations, and temperature and voltage variation measurements are provided.

Paper IV introduces a nonlinearity cancellation scheme using a triode multiplier: a circuit that generates the second order nonlinearity of the input signal, which is effectively multiplied by the signal to generate and cancel the third order nonlinearity. Simulations of a wide-band LNA and measurements of a high frequency OTA-C filter are included.

Paper V presents a highly configurable receiver front-end supporting LTE-Rel. 11 [16] CA scenarios. Low noise figure is achieved thanks to a noise canceling low noise transconductance amplifier (LNTA) and high linearity is achieved thanks to a fully differential structure and a base band linearization technique. Measurements show that spectrum sensing is very beneficial to be able to counteract the effect of large interference.

Chapter 2

The Cellular Radio Receiver

Many different receiver architectures have been proposed over the last century [17–20]. Currently the homodyne receiver[1] is widely adopted due to its simple architecture and high level of integration. In this chapter the homodyne architecture is therefore described. A brief introduction to the most important quality metrics of receivers will also be provided.

2.1 The Homodyne Receiver

The homodyne receiver block diagram is shown in Fig. 2.1. The signal received by the antenna contains the wanted signal at frequency f_{RX}, accompanied by adjacent channel and in-band interference signals close in frequency to the wanted signal. In communication standards such as LTE and WCDMA, FDD is supported, implying concurrent operation of the transmitter (TX) and receiver (RX). For this reason the antenna is interfaced with a duplex filter to provide isolation of RX from TX. Commercial duplexers for cellular terminals provide an isolation of about 50dB [21, 22]. The remaining, still large TX self-interference together with the received signal are then amplified by the LNA and down converted by the quadrature mixer. After the quadrature mixer the wanted signal, centered at the local oscillator frequency (f_{LO}) before down conversion, is represented as two quadrature base band signals having a bandwidth equal to half the radio frequency (RF) signal bandwidth. The channel selection can thus be performed by low pass filters, suppressing interfering signals which will be located at higher frequencies. A variable gain amplifier (VGA), usually with first order filtering, is used to adapt the RX gain for optimal dynamic range together with the CSF and analog to digital converter (ADC). The CSF attenuates the interference signals further to relax the requirements of the ADC.

---

[1] also known as the direct conversion receiver

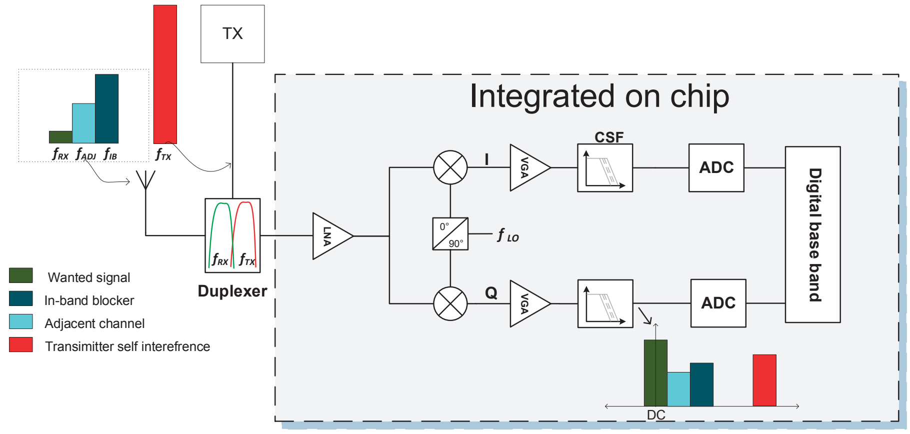

TX
fRX fADJ fIB
fTX
Integrated on chip
CSF
ADC
ADC
Digital base band
I
Q
VGA
VGA
LNA
0°
90°
f LO
fRX fTX
Duplexer
DC
Wanted signal
In-band blocker
Adjacent channel
Transimitter self interefrence

Figure 2.1: Block diagram of the homodyne receiver.

2.2 Dynamic Range

The signal received by the antenna contains both the wanted signal and interference. The far out-of-band interference is heavily attenuated by the duplex filter, leaving in-band interference and the attenuated TX signal. When TX is transmitting maximum power (close to 30dBm), TX signal at the RX input is close to -20dBm. This is likely to occur far from the base station, at the cell edge. The wanted signal is then very weak[2], further worsening the situation. Large interferers are also expected in-band (LTE-Rel. 11 specifies -25dBm interference [16]).

The signal and interference received can be one of three levels, small, medium, or large. Small signals will not give rise to any intermodulation distortion (IMD) products above the noise floor, in which case the performance is noise limited and more gain is desirable. Medium signals on the other hand will cause IMD products that, depending on their frequencies, may degrade the signal-to-noise ratio (SNR), in which case the gain must be reduced. Large signal levels will force the system into compression unless the gain and sensitivity are sacrificed. The effect of the different input signal levels on the receiver front-end results in corresponding performance:

- Small signal performance including sensitivity and selectivity.

- Medium signal performance related to the nonlinear behavior of the circuits, which is measured using intercept points (IP).

---

[2] the reference sensitivity in LTE-Rel. 11 is from -96dBm to -92dBm

- Large signal performance including clipping, slewing and reciprocal mixing. This is measured by desensitization in different scenarios

2.2.1 Small Signal Performance

The most important small signal performance metrics are sensitivity and selectivity. The noise performance of an RX chain is often reported using the noise figure (NF), which is defined as:

$$\mathrm{NF} = 10\log(\frac{SNR_{in}}{SNR_{out}}) \tag{2.1}$$

where SNR_{in} and SNR_{out} are the input and output SNR, respectively. Since there are several stages in the RX chain, Friis formula [23] can be used to calculate the system NF ($\mathrm{NF_{sys}}$) as:

$$\mathrm{NF_{sys}} = 10\log(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + ...) \tag{2.2}$$

where F_n is the noise factor (the linear value of the NF) of the $\mathrm{n^{th}}$ stage and G_n is the available power gain of that stage. Often in integrated designs, matched internal impedances are not used, therefore input noise voltage and voltage gain are used instead. Just like in (2.2), however, the result is that the first stage, the LNA, is the most important. It is seen from (2.2) that receiver NF is dominated by the LNA, given that it has sufficient gain. In modern RX chips, not only the VGA gain but also the LNA gain can be programmable to handle difficult blocking scenarios and achieve high sensitivity. In all cases the system gain should be high enough to ensure that the wanted signal is amplified and brought into the signal level range that the ADC can process.

Selectivity is a major small signal performance metric since receivers are wide-banded. The selectivity of a radio receiver is defined as the receiver ability to select the wanted signals and reject the other undesired ones. For homodyne receivers, further filtering is required after the duplex filter, see Fig. 2.1. The signal is down converted to base band, therefore low pass filters are used for channel selection for both I and Q signal paths. CSFs considerably relax the dynamic range requirements of the ADCs, which then don't have to process strong interference after filtering.

2.2.2 Receiver Linearity

Linearity is the main bottleneck in today's low cost RX chips, which is a result of the CMOS technology scaling. The linearity performance is measured at medium signal levels, i.e. the system is not driven into compression, but significant intermodulation distortion is generated.

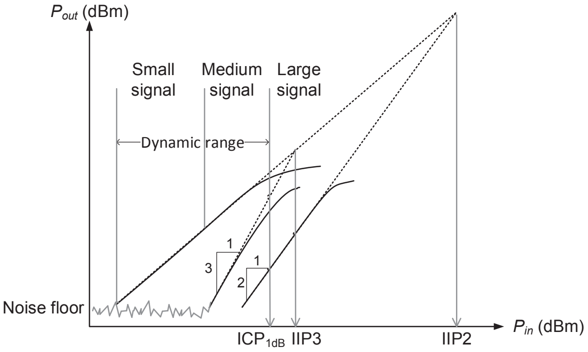


Figure 2.2: Intercept diagram with dynamic range illustration.

Input-referred intercept points (IIP) are used to characterize the linearity of the receiver and its building blocks. The second and third order IIP (IIP2 and IIP3) are widely used to bench-mark the linearity performance. Two-tone tests can be performed to simulate or measure IIP. For IIP2 two closely spaced sinusoidal signals with equal power level P_{in} at frequencies f_1 and f_2 are applied, and the level of the second order IMD ($IM2$) at frequency $|f_1 - f_2|$ is then observed as P_{in} increases. The frequencies are chosen such that the intermodulation product falls inside the received signal band. The IIP2 is the level where the interpolation of P_{out} equals that of P_{IM2}, see Fig. 2.2. For IIP3 the $IM3$ component at $2f_1 - f_2$ or $2f_2 - f_1$ is instead observed, at the receiver output down converted by f_{LO}.

Higher order IIP can be relevant if the interference levels are high. The IIPn value can be calculated using one measured value (extrapolation point) of IMn by

$$\text{IIPn} = \frac{nP_{in} - IIMn}{n-1} \tag{2.3}$$

where n is the order of the nonlinearity. It is, however, important to ensure that the point of extrapolation is located on a slope of n line in the intercept diagram.

The IIP2 and IIP3 curves are illustrated in an intercept diagram in Fig. 2.2. It is seen that the IMn term has a slope that is proportional to n. The IIP2 is higher than IIP3 if differential structures are adopted, as the differential circuits provide $IM2$ cancellation. Some mismatch is, however, always present, making the IIP2 finite but high. Differential structures are therefore adopted for all the works in this dissertation, in single ended implementations, however, IIP2 is usually lower than IIP3.

Considering an amplifier with soft nonlinearity, a Taylor series expansion can be used to describe its transfer characteristics. Since medium signal levels and soft nonlinearity are assumed, a third order polynomial can be used

$$Y = g_0 + g_1X + g_2X^2 + g_3X^3 \tag{2.4}$$

where X is the input signal, Y is the output signal, and g_n is the n^{th} order coefficient. Letting $X = Acos(\omega_1 t) + Acos(\omega_2 t)$ in a two-tone test, one can calculate the IIP2 and IIP3. The IIP2 is the value of A that will make the $IM2$ level equal to that of the fundamental tone. The IIP2 becomes

$$\mathrm{IIP2} = \frac{g_1}{g_2} \tag{2.5}$$

Performing similar calculations for IIP3 results in

$$\mathrm{IIP3} = \sqrt{\left|\frac{4g_1}{3g_3}\right|} \tag{2.6}$$

2.2.3 Large Signal Performance

A fundamental limitation on the maximum signal that can be received is amplifier saturation, which is aggravated by the limited voltage headroom in deep submicron CMOS technologies. The input referred 1dB compression point ($\mathrm{ICP_{1dB}}$) is commonly used to compare the large signal performance of receiver front-ends. $\mathrm{ICP_{1dB}}$ is defined as the power level where the gain is reduced by 1dB compared to the small signal case. Gain compression can result from a large wanted signal, which can be solved easily by gain reduction in the RX chain. If gain compression on the other hand results from large blockers, more actions are required. Still, in some situations with strong blockers and a weak wanted signal, reception may be interrupted. Fig. 2.2 shows the three different input power regions, indicating the gain compression at high levels of P_{in}.

Considering up to third order nonlinearity to dominate, and assuming a compressive behavior, the $\mathrm{ICP_{1dB}}$ can be calculated as [24]

$$\mathrm{ICP_{1dB}} = \sqrt{\left|\frac{4g_1}{3g_3}\right|}\sqrt{0.11} = \mathrm{IIP3} - 9.6\mathrm{dB} \tag{2.7}$$

It is seen in (2.7) that the $\mathrm{ICP_{1dB}}$ is 9.6dB lower than IIP3. This relation holds for many circuits. However, if linearization techniques are employed to improve IIP3, the improvement in IIP3 does not imply improvement in $\mathrm{ICP_{1dB}}$, because signal compression is limited by the voltage headroom. Therefore medium signal linearization techniques can improve IIP3 considerably, but $\mathrm{ICP_{1dB}}$ remains unchanged. A survey of common techniques that help improving the amplifier linearity is reported in [24].

Another issue related to large signals is reciprocal mixing which occurs in the presence of strong out-of-band blocker. This issue is due the non-ideal LO signals driving the mixers which also contain phase noise. Since phase noise appears as skirts around the LO tone, phase noise mixing with the strong out-of-band blockers produces noise in-band. Therefore, depending on the level of phase noise in the LO signals and the out-of-band blockers, the receiver desensitization increases.

2.3 Wide-Bandwidth Receiver Impairments

Wider and wider channel bandwidths are necessary as higher data rates are supported in advanced communication standards. The increased bandwidth results in more stringent blocking requirements, because the relative frequency distance between the blocker and the wanted signal is reduced. Added to that, with their increased frequency separation the in-band signals will experience different path losses. This calls for increased quadrature accuracy of the LO generation, mixer, and base band circuits of the homodyne receiver. Increasing the requirement of the image rejection ratio (IRR).

Moreover, CA concept has been introduced, where more than one carrier is received simultaneously. For LTE specifications [16] the different CA scenarios are illustrated in Fig. 2.3. Contiguous CA, Fig. 2.3(a), makes the design of the receiver front-end straight forward. If the LO frequency is placed at the center, between the carriers, out-of-band blockers remain the only ones that need to be dealt with. Non-contiguous CA, Fig. 2.3(b), on the other hand is more difficult to handle since the gap between the carriers can contain interference. Added to that, adjacent channels that have higher amplitude (an LTE test case assumes 25.5dB higher) than the wanted signal can fall on the image frequency of the carrier 2, see Fig. 2.4. The requirements, besides high out-of-band linearity, are high in-band linearity and very high IRR. The inter-band CA scenario, Fig. 2.3(c) requires two parallel receiver chains if the bands are widely spaced in frequency. Each receiver chain is conventional, but great care must be taken in the design of the LO generation circuitry to avoid disturbances due to unwanted interaction.

2.3.1 Image Rejection

The homodyne receiver has inherently image rejection. The image rejection is the ability to distinguish a signal coming from a positive offset frequency from the LO from one coming from the same but negative offset. In a homodyne receiver an in-band frequency component always has a corresponding in-band frequency component (image) at the opposite sign offset frequency, i.e. the image falls in-band. To be able to distinguish between positive and negative frequencies in the wanted signal, and hence provide image rejection, quadra-

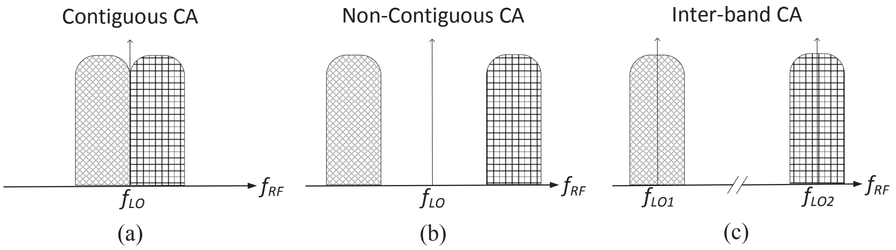

Contiguous CA
Non-Contiguous CA
Inter-band CA
f_{LO}
f_{RF}
f_{LO1}
f_{LO2}
(a)
(b)
(c)

Figure 2.3: CA scenarios (a) contiguous, (b)non-contiguous, and (c) inter-band.

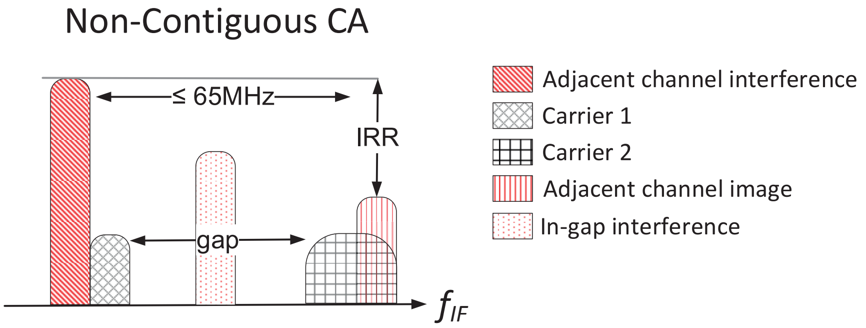

Non-Contiguous CA
≤ 65MHz
IRR
gap
f_{IF}
Adjacent channel interference
Carrier 1
Carrier 2
Adjacent channel image
In-gap interference

Figure 2.4: Image problem in LTE non-contiguous CA scenario.

ture down conversion is used. It can be shown that perfect image rejection is achieved for perfect quadrature, i.e. exactly 90° phase shifted LO signals and identical gain in I and Q signal paths. Mismatches in the circuitry will, however, introduce phase and amplitude errors. The resulting IQ imbalance contains base band frequency independent errors which are usually due to mismatches in the mixers and LO generation, and base band frequency dependent errors due to mismatch between the CSFs bandwidth. The IQ imbalance results in power from the image frequency to leak on top of the wanted signal. The IRR is defined as the ratio of the gain for the wanted signal to the gain for the image signal. IRR can be derived as

$$\mathrm{IRR} = \frac{(1+\epsilon)^2 + 2(1+\epsilon)cos(\Delta\theta) + 1}{(1+\epsilon)^2 - 2(1+\epsilon)cos(\Delta\theta) + 1} \approx \frac{4}{\epsilon^2 + \Delta\theta^2} \tag{2.8}$$

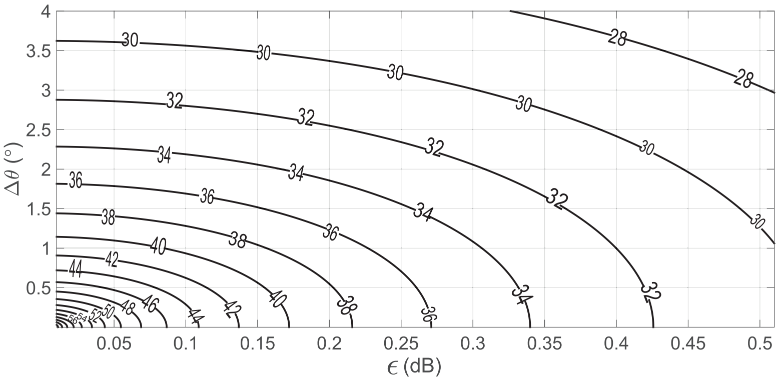


Figure 2.5: Contour of IRR vs. phase and amplitude errors.

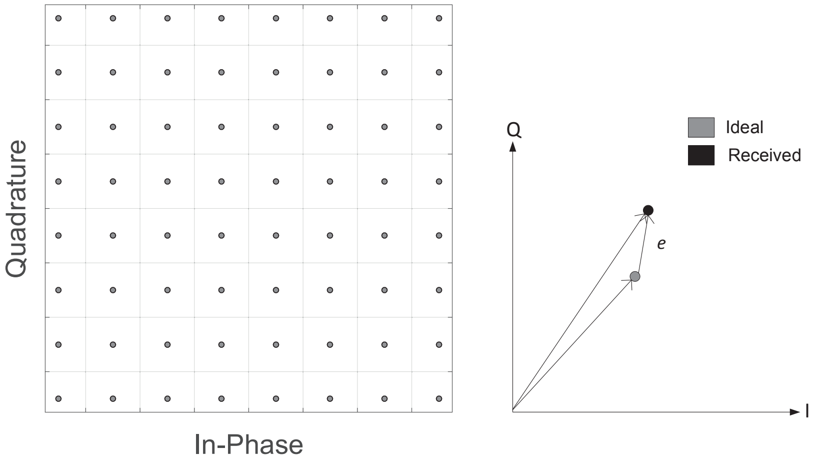
where ϵ is the IQ gain error and $\Delta\theta$ is the phase error in radians. Fig. 2.5 shows IRR contours in the error plane using (2.8). As can be seen an IRR of 40dB can be achieved e.g. by a 1° phase error and an 0.1dB gain error.

2.3.2 Error Vector Magnitude

Receiver front-ends are complex systems and many performance metrics are used to measure different non-ideal behaviors, however, this often results in limited insight into the overall receiver performance. For this reason there is a need for overall performance measurements in realistic scenarios.

Signal constellation diagrams are used to plot all the target values of the I and Q signals. For example 64 quadrature amplitude modulation (64-QAM) is shown in Fig. 2.6. The non-idealities of the circuitry will shift the points in Fig. 2.6 from the ideal target values. Different non-idealities will have different impact on the constellation points. For example, LO phase noise will cause the points to move along an arc with a size proportional to the phase noise level and the distance from the origin. Thermal noise will randomly move the constellation points creating circular clouds. IMD terms falling in the signal band, similar to noise, will also result in corruption of the demodulated signal. The performance of the receiver front-end with all non-idealities in the signal chain can be evaluated using the error vector magnitude (EVM).

EVM is the magnitude of the vector difference between the received symbol and the ideal symbol, divided by the received average power (P_{avg}), see Fig. 2.6. The average EVM is used to evaluate the performance of the receiver and it is


Quadrature
In-Phase
Q
I
e
Ideal
Received

(a) (b)

Figure 2.6: (a) 64-QAM constellation diagram, (b) EVM measurement illustration.

given by (2.9)

$$EVM_{avg} = \frac{\sum_{j=1}^{N} |e_j|^2}{NP_{avg}} \tag{2.9}$$

where N is the number of IQ symbols received, and e is the error vector, see Fig. 2.6(b).

Chapter 3

Receiver Circuit Implementations

In this chapter circuit level building blocks for receiver front-ends are introduced. It starts with different LNA topologies in section 3.1. Then the passive mixer is briefly explained in section 3.2. Frequency dividers are described in section 3.3, then the base band OTAs are introduced and the transimpedance amplifier (TIA) configuration is discussed in section 3.4.

This chapter focuses on receiver front-ends operating in current domain, however, voltage domain receiver front-ends have a similar architecture except for the TIA, which is then replaced by a voltage amplifier, and the LNTA which is replaced by an LNA. The current mode receiver front-end is shown in Fig. 3.1. The output current is down converted to base band using mixers, and the capacitor at the mixer output sinks high frequency out-of-band signal current. The base band currents from the mixers are converted into voltage signals using TIAs, which also provides first order filtering. The main advantage with the current mode configuration is that the LNTA and mixer signal voltage swings are small, making the receiver front-end more linear and capable of handling larger signals.

3.1 LNAs

The LNTA in a current mode receiver front-end is an LNA whose output is intended to be connected to a low impedance. The design of the LNTA is crucial as it is the most important block in determining the sensitivity of the receiver front-end. The LNTA also provides an input match to the duplexer, which is important as the duplexer needs to see the correct impedance to perform as expected. Furthermore, the linearity of the receiver front-end is determined by the LNTA for out-of-band blockers.

In literature, various LNA implementations are proposed (e.g. [25–29]). Fig. 3.2 shows frequently used topologies: common gate (CG), cross coupled common gate (CC-CG) [26], common source with inductive degeneration (CS), shunt feedback common source (R_f-CS), and the noise canceling common gate common source (NC-LNA) [27].

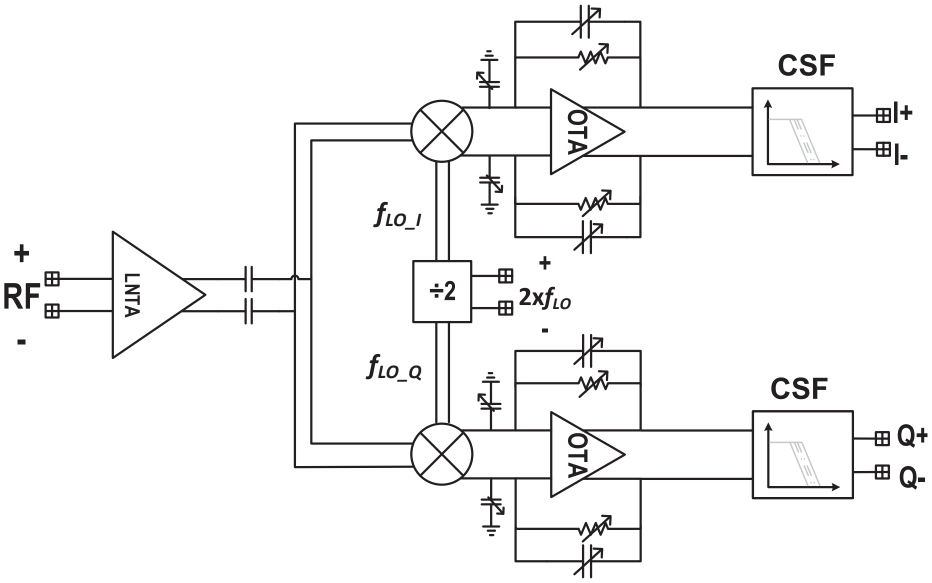


Figure 3.1: Current mode receiver front-end architecture.

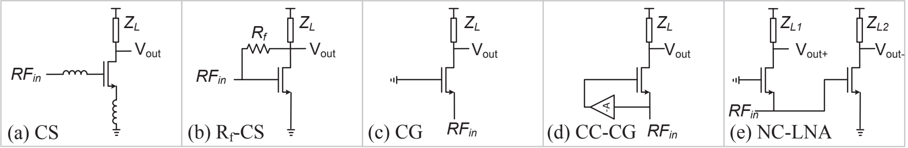

(a) CS (b) R$_f$-CS (c) CG (d) CC-CG (e) NC-LNA

Figure 3.2: Different LNA topologies.

All the LNA configurations in Fig. 3.2 can be used as LNTAs, except for the R_f-CS. The reason is that the input impedance of the R_f-CS LNA (Z_{in}^{LNA}) is strongly dependent on the load impedance. Using the simple π transistor model (found in e.g. [30]) and ignoring the reactive elements for simplicity, Z_{in}^{LNA} becomes

$$Z_{in}^{LNA} = \frac{R_f + Z_L}{g_m Z_L + 1} \tag{3.1}$$

It is seen in (3.1) that if the output of the LNA is connected to low impedance (effectively making Z_L low) then $Z_{LNAin} \approx R_f$. Then choosing R_f for matching (50Ω) will result in poor NF. The input impedance of CG LNAs is also

Table 3.1: Comparison of different LNA topologies.

Parameter	CS	R_f-CS	CG	CC-CG	NC-LNA
RF range	P	G	G	G	M
Noise	G	M	P	M	G
Linearity	M	M	G	G	M
Current	M	M	G	G	P

G=good, M=medium and P=poor

dependent on the load, fortunately the effect is less dominant than in R_f-CS LNAs.

The key performance metrics for LNAs are NF, input matching (which is quantified by S_{11}), frequency range, power consumption, linearity, chip area and power consumption. In Table 3.1 a rough performance comparison of different LNA topologies is presented. It can be seen that an LNA that has low NF, high linearity, wide input match and RF frequency range, and consumes low power is a myth. For this reason a lot of research is performed to improve the overall performance of LNAs, especially on improving the linearity of receiver front-ends and achieve blocker resilience, see e.g. works published in [31–35]. However, with the increased channel bandwidths, the LNA linearity is becoming less and less dominant, and instead the base band circuity is becoming the linearity bottleneck. This is due to the increasing base band frequencies, which leads to reduced loop gain in the base band amplifiers and the ever reducing frequency ratio between the 3dB bandwidth and blockers, causing less blocker attenuation at the base band, so that close out-of-band interference may easily saturate the base band amplifiers.

3.1.1 Linearized LNA

Using CMOS technology, complementary devices in push-pull configuration is attractive. The transconductance is then doubled leading to reduced current consumption. Furthermore, the output voltages do not exceed the supply voltage which is beneficial for reliability in nanometer CMOS technologies. Cascode devices are also used to increase the reverse isolation (S_{12}) and gain. Unfortunately, to function properly cascode devices require a voltage drop, reducing the signal headroom and thereby also the linearity.

A differential complementary R_f-CS LNA with linearization is shown in Fig. 3.3 (from paper IV [4]). The devices (M_5) form a second order distortion generator whose output is connected to the gate of the cascode devices (M_3). The cascodes (M_3) act as source followers and the drain of (M_4) is thus modulated by the second order term. Multiplication in M_4 then results in third order nonlinearity cancellation as described in paper IV.

Device	W/L (μ m)
M_1	200/0.06
M_2	60/0.06
M_3	120/0.06
M_4	400/0.06
M_5	7.5/0.2

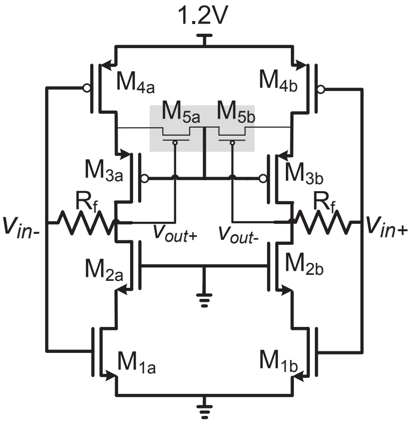
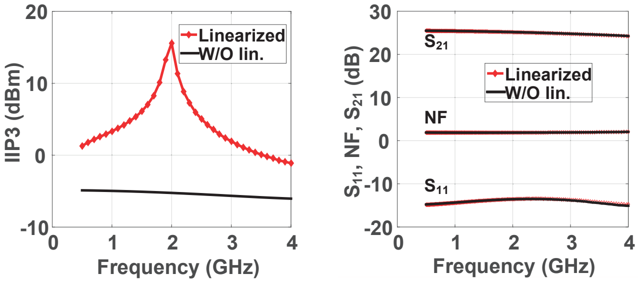


Figure 3.3: Shunt feedback LNA with linearization (biasing is omitted).



(a) (b)

Figure 3.4: Simulation of the LNA (a) IIP3, (b) S_{21}, S_{11}, and NF.

A simulation of IIP3 with linearization enabled/disabled is shown in Fig. 3.4(a). It can be seen that the IIP3 is increased significantly by the linearization, while the NF, S_{11}, and gain (S_{21}) remain unaffected, see Fig. 3.4(b).

3.1.2 Differential Noise Canceling LNTA

To be able to use the R_f-CS in a current mode receiver front-end, a first R_f-CS amplifying stage must be followed by a second transconductance stage. Noise cancellation functionality can also be added using an auxiliary CS stage path with a gain that matches that of the main path.

Shown in Fig. 3.5 is the differential noise canceling LNTA used in paper V [5]. Noise cancellation is achieved since the noise at the output of stage-1 is

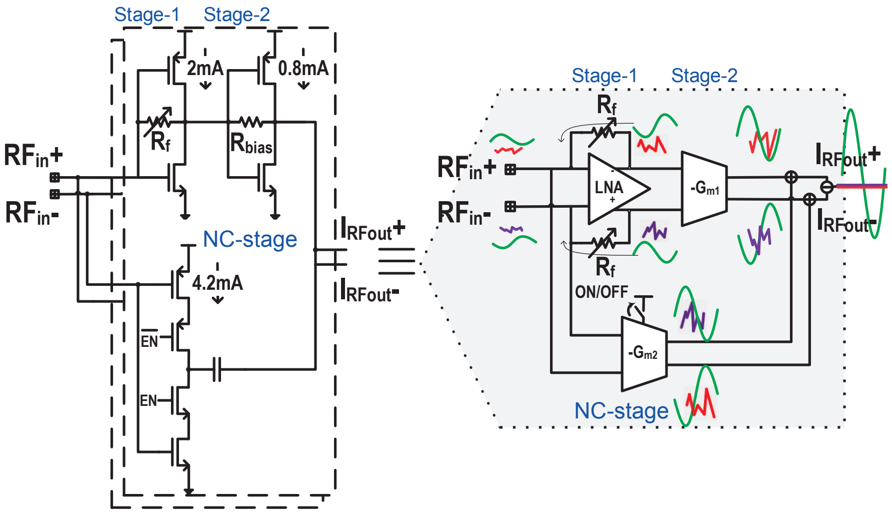

Stage-1
Stage-2
2mA
0.8mA
Rf
Rbias
RFin+
RFin-
NC-stage
4.2mA
IRFout+
IRFout-
EN
EN
Stage-1
Stage-2
Rf
RFin+
RFin-
LNA
-Gm1
IRFout+
IRFout-
Rf
ON/OFF
-Gm2
NC-stage

Figure 3.5: Schematic and block diagram of the noise canceling LNTA.

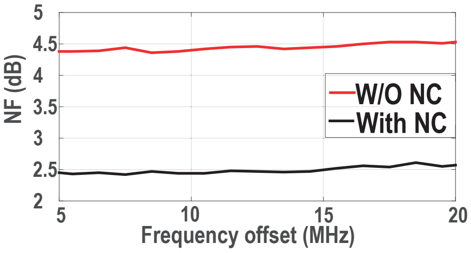


Figure 3.6: Measured NF of the receiver front-end in [5] at base band.

fed back through R_f and then amplified by the noise canceling stage. At the output the noise from the two paths will be in anti-phase. If the gain of the noise canceling-stage matches that of stage-1 and stage-2, optimal cancellation occurs. The noise canceling path can be turned off if high sensitivity is not required, resulting in 60% less current consumption. The measured NF of the receiver front-end at base band output is reported in paper V [5], see Fig. 3.6. It can be seen that when noise cancellation is activated the NF is reduced by 2dB.

The linearity of this noise canceling LNTA is limited by the R_f-CS stage, since it has a substantial voltage gain. For this reason, the use of cascode devices was avoided to obtain maximum output voltage swing.

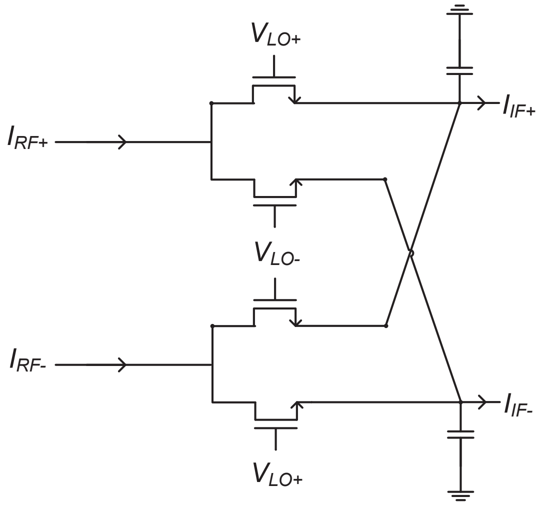


Figure 3.7: Double balanced passive mixer with a capacitive load.

3.2 Mixers

The mixer multiplies the RF input signal with the LO signal to get frequency translation (down conversion for receivers). There are, two main types of MOS mixers, the first is the active mixer which can provide conversion power gain, and the second is the passive mixer which uses the MOS devices as switches. Description of active mixer properties can be found in literature (e.g. [36–38]).

Despite some unattractive properties of passive mixers, such as requiring large LO signal amplitudes, and having significant signal power loss resulting in poor NF, they are widely used in high performance transceiver chips. This is because they offer unique advantages such as high linearity and close to zero flicker noise as no DC current passes through the transistors. Passive mixers, double balanced version shown in Fig. 3.7, also offer an attractive property of impedance frequency up conversion. Since the passive mixer is a bidirectional time variant circuit, driving it with an RF current, the voltage at the RF input of the mixer is for frequencies around the LO signal shaped by the base band impedance (Z_{BB}). This means that Z_{BB}, translated in frequency by f_{LO}, is directly seen at the output of the LNTA [39,40]. A capacitive load of the mixer will then result in pass band filtering at RF, which is the core concept of N-path filters [41,42]. This results in better blocker handling and the LNTA faces less problems with compression at its output.

Smaller duty cycle LO signals are employed, and it can be shown that 25% improves the conversion gain of the mixer by 3dB compared to 50% duty

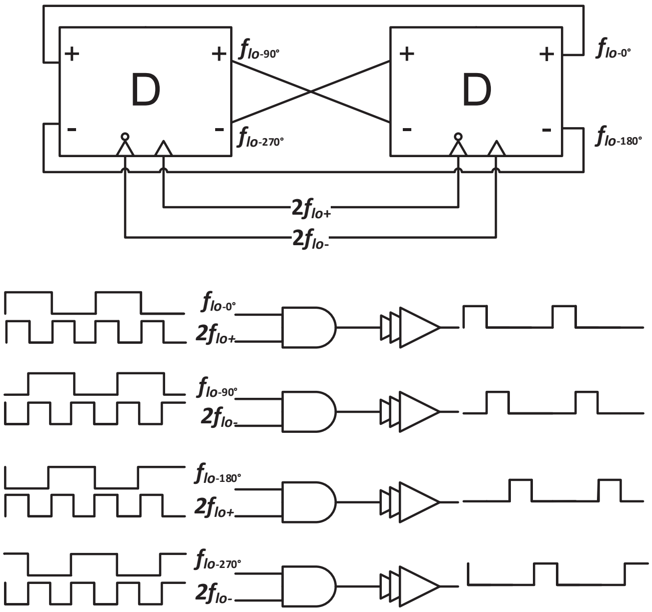


Figure 3.8: LO generation of quadrature signals with 25% duty cycle.

cycle LO signals [14, 43]. Having quadrature (I & Q) passive mixers, using 25% duty cycle is also a very efficient way of avoiding mixer interaction due to simultaneous conduction. Unfortunately, reducing the duty cycle requires more complex LO generation circuitry.

3.3 LO Generation

For passive mixers, rail-to-rail LO signals are required to multiply (down convert) the wanted signals to base band with high linearity. High spectral purity is required to avoid reciprocal mixing, and quadrature signals are needed for image rejection. Finally, shorter duty cycle results in reduced mixer conversion loss and IQ interaction. Digital circuits lend themselves well to generate such short pulses. To generate 25% duty cycle quadrature signals a divide-by-2 circuit is typically used, therefore the phase locked loop (PLL) needs to operate at twice the LO frequency. Since differential voltage controlled oscillators (VCOs) are often used in the PLL, differential divide-by-2 circuits are adopted. A divide-by-2 circuit using delay latches is shown in Fig. 3.8, also shown in the figure is the generation of the 25% duty cycle using an AND gate.

Since high RF is supported in many modern wireless communication sys-

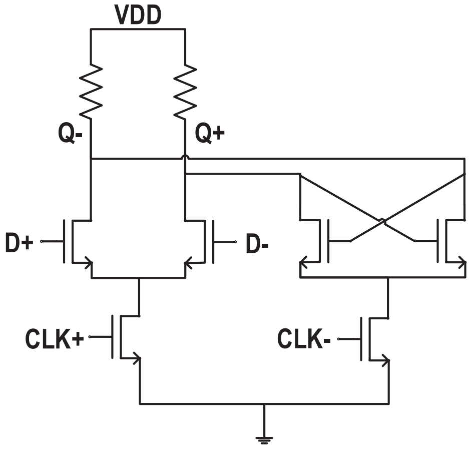


Figure 3.9: Schematic of the CML latch.

tems, high speed frequency dividers are needed, and current mode logic (CML) is frequently used to implement such dividers. The CML latch is shown in Fig. 3.9.

3.4 The TIA

The down converted signal current needs to be converted to voltage, then further filtering is performed before feeding the signal to the ADC. The current to voltage conversion is performed by a TIA, which can also provide first order filtering.

The TIA can be implemented using a CG stage, however, excess noise and limited linearity make this implementation suitable mainly for very low power implementations. Feedback configurations on the other hand offer very good characteristics in terms of linearity, noise, and configurability (see Fig. 3.1).

Since a MOS transistor in the active region behaves as a voltage controlled current source (VCCS), OTAs are easier to design and consume less power than true operational amplifiers (OPAMPs) with low output impedance. The amplifiers are therefore implemented as OTAs.

Unfortunately, single-stage OTAs in deep-submicron CMOS offer limited transconductance g_m, and a multi-stage OTA is usually needed to boost the effective transconductance (G_m) of the OTA. Multi-stage OTAs have multiple poles in the transfer function (TF), and the use of such OTAs in feedback configurations increases the risk of instability in the system. A brief introduction to compensation schemes and stability assurance of the system is discussed in chapter 4 and paper I [5] in this dissertation. For now assuming that the OTA

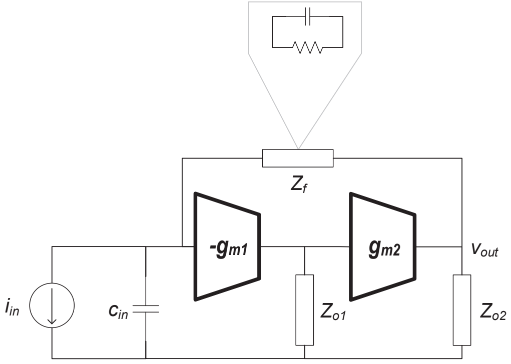


Figure 3.10: A model of the TIA using a two-stage OTA.

is compensated for TIA configuration with enough phase margin to guarantee stable operation. The compensated OTA can be modeled by adjusted values of each stage output capacitance (c_o) which together with the output resistance (r_o) of that stage form a pole at the same frequency as the one in the compensated OTA.

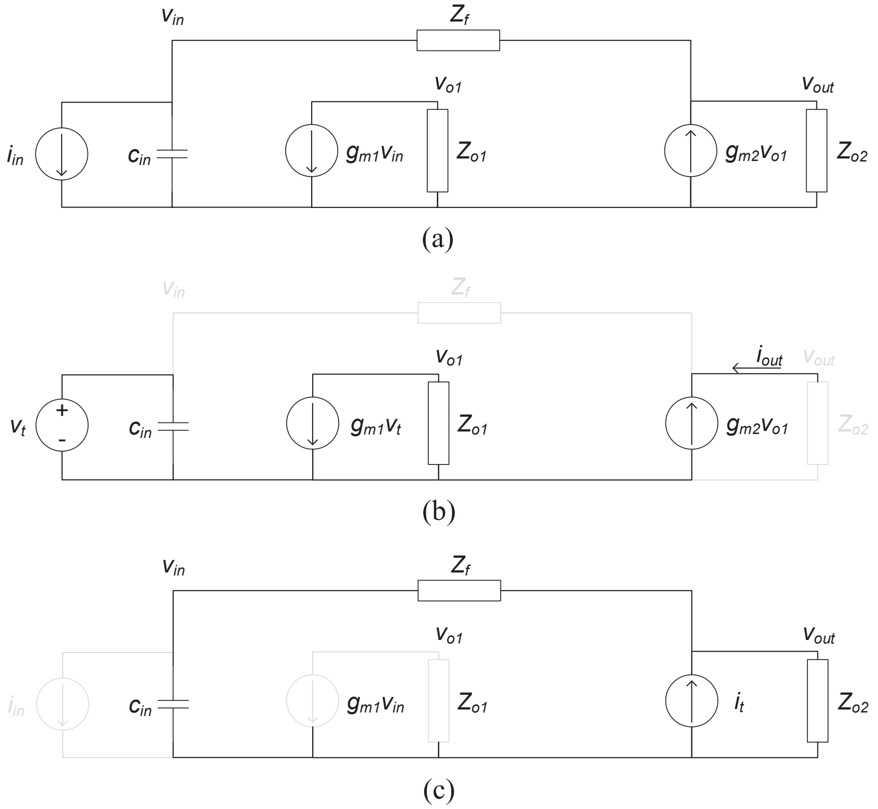
3.4.1 Loop Gain and Stability Analysis

A two-stage OTA provides sufficient loop gain ($A\beta$), where A is the forward gain and β represents the feedback gain. A well-compensated OTA should have similar gain characteristic as a single-stage (single-pole) OTA at lower frequencies, which is accomplished by pushing the second pole to a high frequency.

Fig. 3.10 shows a model of a TIA employing a two-stage OTA. Since the OTA is assumed to be compensated, pole spacing is increased. Shown in Fig. 3.10, c_{in} is a capacitor placed to sink the current of the out-of-band blockers, g_{m1} and g_{m2} are the transconductances of the first and second stages of the OTA, and similarly Z_{o1} and Z_{o2} are the output impedances which form the first and the second pole of the OTA. Finally, Z_f is the feedback impedance that sets the TIA gain.

The small signal model of the TIA is shown in Fig. 3.11(a). To analyze $A\beta$, A is first calculated using Fig. 3.11(b), where a test voltage at the input is used to calculate the output current i_{out}. For β, Fig. 3.11(c) is used, where a test current i_t at the output is used to calculate the input voltage v_{in}. It can be shown that

$$A\beta = \frac{i_{out}}{v_t}\frac{v_{in}}{i_t} = -g_{m1}Z_{o1}g_{m2}Z_{o2}\frac{Z_{c_{in}}}{Z_f + Z_{c_{in}} + Z_{o2}} \tag{3.2}$$



vin
Zf
vo1
vout
iin
cin
gm1vin
Zo1
gm2vo1
Zo2
(a)
vin
Zf
vo1
iout
vout
vt
+
-
cin
gm1vt
Zo1
gm2vo1
Zo2
(b)
vin
Zf
vo1
vout
iin
cin
gm1vin
Zo1
it
Zo2
(c)

Figure 3.11: Model of (a) two-stage OTA, (b) calculation of A, and (c) calculation of β.

Taking into account that Z_f consists of R_f and c_f in parallel, and Z_o of r_o and c_o in parallel, results in

$$A\beta = -g_{m1}r_{o1}g_{m2}r_{o2}\frac{R_f c_f s + 1}{As^3 + Bs^2 + Cs + 1} \tag{3.3}$$

where

$$A = c_f c_{in} c_{o1} R_f r_{o1} r_{o2} + c_f c_{o1} c_{o2} R_f r_{o1} r_{o2} + c_{in} c_{o1} c_{o2} R_f r_{o1} r_{o2} \tag{3.4}$$

$$\begin{aligned} B =& c_{in} c_{o1} r_{o1} r_{o2} + c_{o1} c_{o2} r_{o1} r_{o2} + c_f c_{in} R_f r_{o2} + c_f c_{o1} R_f r_{o1} + \\ & c_f c_{o2} R_f r_{o2} + c_{in} c_{o1} R_f r_{o1} + c_{in} c_{o2} R_f r_{o2} \end{aligned} \tag{3.5}$$

$$C = R_f c_f + R_f c_{in} + c_{in} r_{o2} + c_{o1} r_{o1} + c_{o2} r_{o2} \tag{3.6}$$

Miller capacitor [30, 44] decreases the frequency of the first pole resulting in large effective c_{o1}. If c_{in} is made very large to sink the blocker currents and provide low impedance for the LNTA, the $A\beta$ will be reduced heavily since its dominant pole frequency is

$$P_1^{A\beta_{c_{in}=large}} \approx -\frac{1}{(R_f + r_{o2})c_{in}} \tag{3.7}$$

For wide-band applications this directly impacts the in-band/close out-of-band linearity. Added to that, the two-stage OTA is a two pole system and therefore to evaluate the stability of the TIA, the effect of c_{in} on the pole spacing is important. To study the effect of c_{in} we first assume that it is removed ($c_{in} = 0$). The expression for $A\beta$ in (3.3) then reduces, and the pole frequencies become

$$P_1^{A\beta_{c_{in}=0}} = -\frac{1}{R_f c_f} \tag{3.8}$$

$$P_2^{A\beta_{c_{in}=0}} = -\frac{1}{r_{o1} c_{o1}} \tag{3.9}$$

$$P_3^{A\beta_{c_{in}=0}} = -\frac{1}{r_{o2} c_{o2}} \tag{3.10}$$

and the zero frequency remains unchanged

$$Z_1^{A\beta_{c_{in}=0}} = -\frac{1}{R_f c_f} \tag{3.11}$$

It can be seen that (3.8) and (3.11) have the same frequency and therefore cancel, and that the system has two loop gain poles identical to the poles in the forward path A. This implies that if the use of a small value of c_{in} is intended then compensating the OTA standalone will ensure stability of the TIA. It can also be concluded that the optimal value for c_{in} to improve the $A\beta$ is zero. Unfortunately, a large c_{in} is required to suppress the tones due to LO switching at the TIA input, and to provide low impedance for out-of-band signals. The TIA input impedance (Z_{in}) thus needs to be analyzed for larger values of c_{in}.

Since all the capacitors need to be considered to evaluate the stability of the TIA, the expressions for the pole frequencies become very large and an insight from the expressions is not easily gained. Instead the TIA used in [5] was modeled according to Fig. 3.10. The input capacitance (c_{in}) was then swept, plotting the gain and phase, see Fig. 3.12. It can be seen that the phase margin

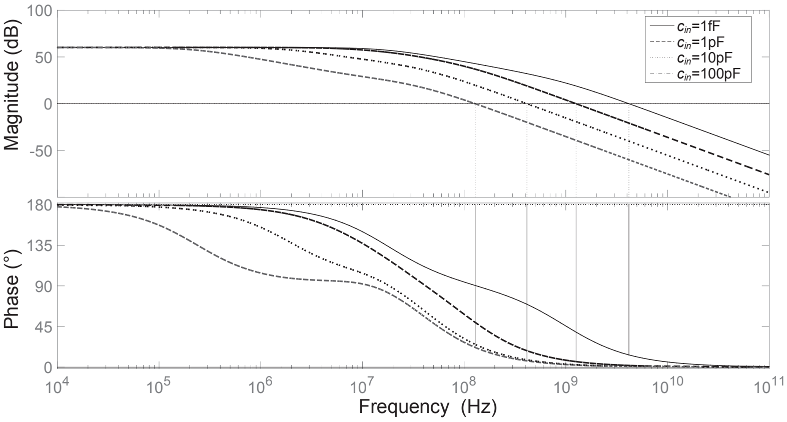


Figure 3.12: $A\beta$ phase and amplitude for different c_{in} values.

reaches a minimum as c_{in} is increased, then it increases again. For this reason c_{in} needs to be carefully investigated for the minimum phase margin to ensure stability. Very large values of c_{in} will in general increase the phase margin while heavily reducing $A\beta$.

3.4.2 Z_{in} Analysis

Minimizing Z_{in} is crucial to ensure high linearity and avoid LNTA output compression. Analysis of Z_{in} for both in-band and out-of-band is very important. Z_{in} in the transition between in-band to out-of-band will also be studied.

From the model in Fig. 3.10 Z_{in} is calculated to

$$Z_{in} = \frac{Z_{c_{in}}(Z_f + Z_{o2})}{Z_f + Z_{o2} + Z_{c_{in}}(1 + g_{m1}g_{m2}Z_{o1}Z_{o2})} \tag{3.12}$$

First, Z_{in} at low frequencies is investigated, since at very low frequencies all impedances are resistive making simplifications possible, the input impedance can then be approximated by

$$Z_{inDC} \approx \frac{R_f + r_{o2}}{g_{m1}g_{m2}r_{o1}r_{o2}} \tag{3.13}$$

In (3.13) it can be seen that in-band the input impedance is inversely proportional to the OTA voltage gain, so in order to ensure low impedance the voltage gain should be maximized. As can be seen in (3.12), when $Z_{c_{in}}$ becomes small at very high frequencies or if c_{in} is large, then Z_{in} reduces to $Z_{c_{in}}$.

At low frequencies Z_{in} is low according to (3.13), and at very high frequencies Z_{in} is also low ($Z_{in} \approx Z_{c_{in}}$), at intermediate frequencies Z_{in} will first increase as $A\beta$ starts to roll off due to limited amplifier bandwidth, then $Z_{c_{in}}$ will start dominating causing Z_{in} to decay again. In other words, Z_{in} can be approximated by a parallel RLC resonant circuit. At resonance the magnitude of Z_{in} is maximum, and depending on the magnitude, a blocker at that frequency may heavily compress the receiver front-end.

Unfortunately, the intermediate frequencies are typically the most important ones where blockers are strongest. Analyzing (3.12), the zero frequencies are given by

$$Z_1^{Z_{in}} = -\frac{1}{r_{o1}c_{o1}} \tag{3.14}$$

$$Z_2^{Z_{in}} = -\frac{1}{R_f \| r_{o2}(c_f + c_{o2})} \tag{3.15}$$

The first pole frequency is given by

$$P_1^{Z_{in}} \approx -\frac{1}{R_f c_f} \tag{3.16}$$

and the next two complex conjugate poles frequencies are

$$P_{2\&3}^{Z_{in}} \approx -\frac{1}{2R_f c_f} - \frac{1}{2r_{o2}c_f} - \frac{1}{2r_{o2}c_{in}} - \frac{1}{2r_{o1}c_{o1}} \pm i\frac{\sqrt{A_v}}{\sqrt{r_{o1}r_{o2}c_{o1}c_{in}}} \tag{3.17}$$

where A_v is the DC voltage gain of the OTA, given by

$$A_v = g_{m1}g_{m2}r_{o1}r_{o2} \tag{3.18}$$

A zero in Z_{in} will cause the impedance to increase and is therefore not desirable, while a pole is desirable as it causes reduction instead. It can be seen in (3.14-3.17) that the first zero frequency is at the OTA's dominant pole frequency, which indicates that the bandwidth of the OTA should be maximized. The first pole (3.16) is determined by the feedback network ($R_f \| c_f$), which will counteract the zero in (3.14) if OTA's 3dB bandwidth $\geq (c_f R_f)^{-1}$. This condition is difficult to meet as the bandwidth continues to grow with increased data rates limiting (3.16), but in general the distance between (3.14) and (3.16) needs to be minimized. The second zero (3.15) is located at higher frequencies, causing further peaking in Z_{in}. To limit the peaking the complex conjugate poles frequency in (3.17) needs to be decreased using c_{in}.

The TIA used in paper V [5] was modeled using the model shown in Fig. 3.10. In the pole-zero map with c_{in} swept from 1pF to 100pF (see Fig. 3.13), it can be seen that zero frequencies and pole frequency in (3.16) remain unchanged. The pole frequencies in (3.17) on the other hand reduced are as c_{in} increases.

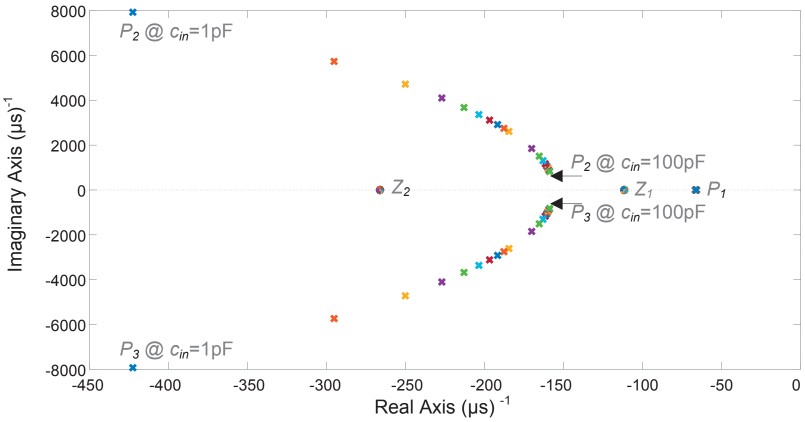


Figure 3.13: Pole-zero map of Z_{in} for different values of c_{in}.

The magnitude of Z_{in} of the modeled TIA used in paper V [5], using the model in Fig. 3.10, is plotted in Fig. 3.14 for different values of c_{in}. The peak Z_{in} ($Z_{inmax} = max(\mid Z_{in} \mid)$) deviates from the SPICE simulations of the TIA at high frequencies since more poles and zeros exist in the more accurate model (SPICE simulations are not shown), however, the resonance frequency (ω_o) of Z_{inmax} matches the SPICE simulations even at higher frequencies. It can be seen in Fig. 3.14 that increasing c_{in} decreases Z_{in}. Unfortunately, ω_o also decreases to frequencies where large blockers are expected (100MHz to 200MHz offset in this case).

Assume that the pole in (3.16) cancels the effect of the zero in (3.14). Then left is the complex conjugate poles given by (3.17) and the zero given by (3.15) (see the example TIA pole-zero map in Fig. 3.13), ω_o can be estimated.

The two complex conjugate poles have a high Q (notice the Y-axis scale in Fig. 3.13), resulting in peaking with a high Z_{inmax}. Z_{in} then becomes [45]

$$Z_{inapprox} \approx K \frac{s+\omega_z}{s^2+\frac{\omega_o}{Q}s+\omega_o^2} \tag{3.19}$$

where ω_z is the zero frequency given by (3.15), and K is a scaling factor.

The approximation of Z_{in} can also be written as

$$Z_{inapprox} \approx K \frac{s+Z_2^{Z_{in}}}{s^2+(P_2^{Z_{in}}+P_3^{Z_{in}})s+(P_2^{Z_{in}}P_3^{Z_{in}})} \tag{3.20}$$

The accuracy of the $Z_{inapprox}$ was compared to (3.12), for the TIA of paper V [5] for c_{in} =10pF and c_{in} =100pF, see Fig. 3.15. As can be seen in the figure,

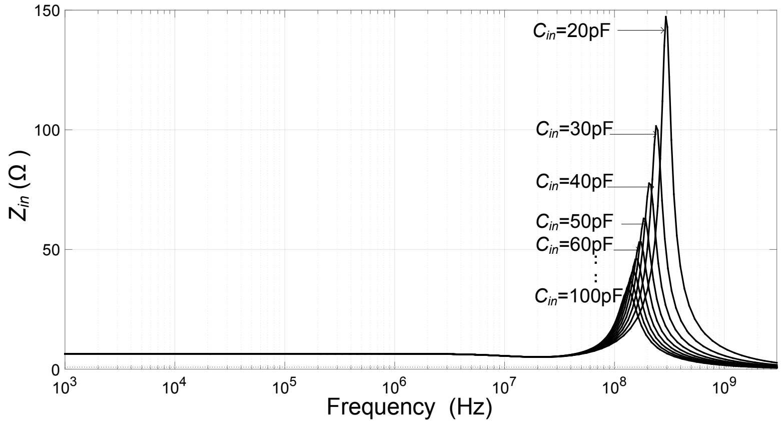


Figure 3.14: Z_{in} peaking for different values of c_{in}.

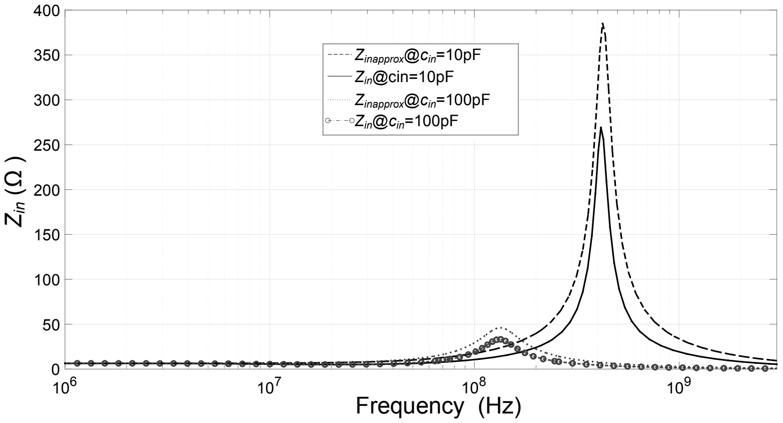


Figure 3.15: Modeled vs. approximated Z_{in} for two c_{in} settings.

the approximation accurately predicts ω_o. The approximation of ω_o becomes

$$\omega_o \approx \sqrt{(-\frac{1}{2R_f c_f} - \frac{1}{2r_{o2}c_f} - \frac{1}{2r_{o2}c_{in}} - \frac{1}{2r_{o1}c_{o1}})^2 + \frac{g_{m1}g_{m2}}{c_{o1}c_{in}}} \tag{3.21}$$

The peaking in Z_{in} can be reduced by decreasing the Q of $P_2^{Z_{in}}$ and $P_3^{Z_{in}}$, i.e. the ratio of the imaginary and real part. As can be seen in (3.17) this can be accomplished by increasing c_{in} or decreasing r_o. The second choice directly impacts the performance of the OTA and is therefore not desirable. Increasing g_m helps reducing the impedance, but leads to increased current consumption.

Although an expression that accurately predicts the value Z_{inmax} is very large, a short intuitive expression can be estimated. First, (3.13) predicts the value of Z_{inDC}. The two complex conjugate poles in (3.17) will then cause the impedance at ω_o to increase from Z_{inDC} by a factor approximately equal to their Q value [45]. The effect of the zero in (3.17) is a further increase in impedance by the ratio $(\frac{\omega_o}{\omega_z})$. Therefore Z_{inmax} can be approximated by

$$Z_{inmax} \approx \frac{\omega_o}{\omega_z} Z_{inDC} Q \tag{3.22}$$

where Q is calculated as the ratio of the imaginary and real part of (3.17).

Chapter 4

OTA Linearization and Filter Implementations

The final stage of the analog receiver front-end is the CSF, which suppresses adjacent channels and out-of-band interference signals before analog to digital conversion. The CSF linearity is a key factor that limits the receiver performance. In particular, band edge and out-of-band linearities are important.

In this chapter the dominant nonlinearities in MOS devices are first described, followed by a brief introduction to linearity enhancement methods for OTAs. Finally, the main CSF architectures are summarized.

4.1 MOS Nonlinearity

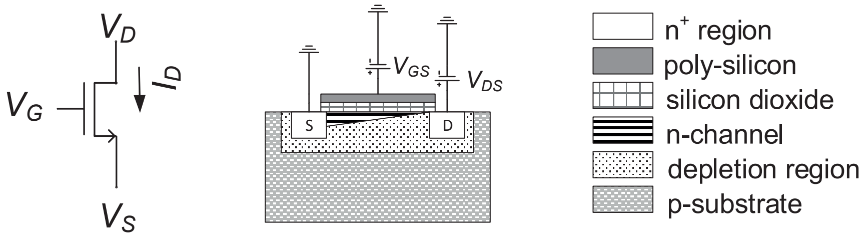
The symbol and conceptual cross section of an nMOS device operating in saturation are shown in Fig. 4.1. The different regions of operation of a MOS device and the physical description can be found in integrated circuits and semiconductor physics literature such as [30, 46, 47]. The pMOS device is the dual of the nMOS, more about nMOS and pMOS can also be found in [30, 46, 47].

The long channel approximation of the current of an nMOS device in saturation region is given by

$$i_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L_{eff}} (v_{GS} - V_{th})^2 (1 + \lambda v_{DS}) \approx \frac{\mu_n C_{ox}}{2} \frac{W}{L_{eff}} (v_{GS} - V_{th})^2 \quad (4.1)$$

where i_D is the drain current, W is the device width, L_{eff} is the effective length of the device, C_{ox} is the gate oxide capacitance per unit area, μ_n is the electron mobility in the channel, λ is the channel length modulation factor, V_{th} is the threshold voltage, and v_{GS} and v_{DS} are the gate-source and drain-source voltages, respectively. From (4.1) it is clear that the second order is the highest order of nonlinearity, however, effects in submicron devices cause also higher order nonlinearities to exist. The most dominant short channel effects are:

–**Velocity saturation** is one of the most important effects in nanometer devices. If the voltages are not scaled at the same rate, the horizontal electric



(a) (b)

Figure 4.1: (a) Symbol of nMOS, (b) conceptual nMOS cross section.

field (ξ_h) increases with decreased channel length, therefore the charge carrier velocity also increases. At very high ξ_h, however, the carrier velocity approaches the thermal velocity and saturates. The field strength at which the charge carrier velocity saturates is called the critical electric field (ξ_c). The effect of velocity saturation can be modeled by a degeneration resistor (R_{vs}) at the source terminal, and (4.1) becomes

$$\mathrm{i_D} \approx \frac{\mu_n C_{ox}}{2(1+\mu_n C_{ox}\frac{W}{L_{eff}} R_{vs}(v_{GS}-V_{th}))}\frac{W}{L_{eff}}(v_{GS}-V_{th})^2(1+\lambda v_{DS}) \tag{4.2}$$

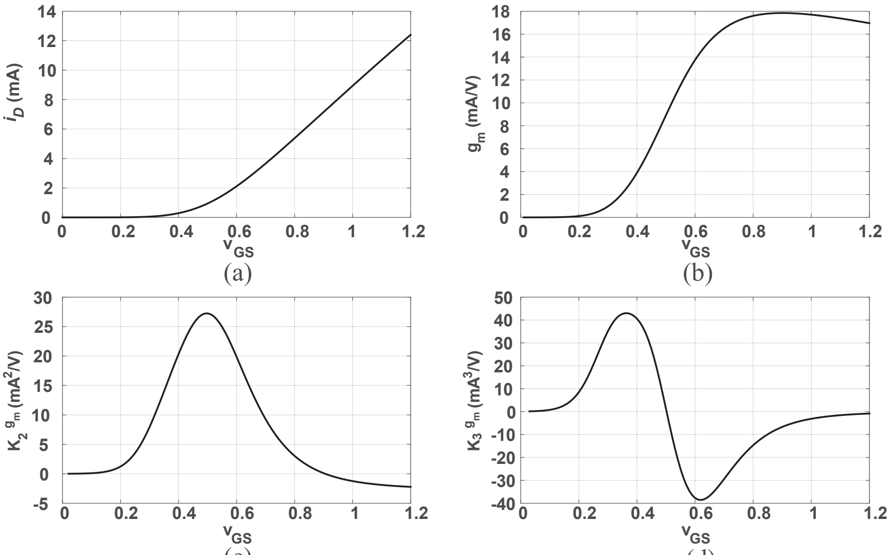
–**Mobility degradation** is also an effect of high electrical field strength (ξ), but in this case in the vertical direction of the field (ξ_v). High ξ_v arises from high gate voltage V_G, which causes the charge carriers to be pulled towards the silicon surface, this reduces their mobility. The effective mobility can be modeled as

$$\mu_{\text{eff}} \approx \frac{\mu_n}{1+\theta(v_{GS}-V_{th})} \tag{4.3}$$

where θ is the mobility reduction parameter. Although the mobility degradation effect is also found in long MOS devices, θ is inversely proportional to the oxide thickness t_{ox} making the mobility degradation worse in new CMOS technologies where t_{ox} is reduced [30, 46].

Many other effects described in literature result in more nonlinear behavior of the drain current i_D [46]. These effects on i_D can be described using Taylor series expansion [48]

$$\begin{aligned} i_D = \mathrm{I_{DC}} &+ g_m v_{gs} + K_2^{g_m} v_{gs}^2 + K_3^{g_m} v_{gs}^3 \dots \\ & g_o v_{ds} + K_2^{g_o} v_{ds}^2 + K_3^{g_o} v_{ds}^3 \dots \\ & K_2^{g_m \delta g_o} v_{gs} v_{ds} + K_3^{g_m^2 \delta g_o} v_{gs}^2 v_{ds} + K_3^{g_m \delta g_o^2} v_{gs} v_{ds}^2 \dots \end{aligned} \tag{4.4}$$



(a) (b)

(c) (d)

Figure 4.2: Simulation of nMOS i_D coefficients in STM 65nm CMOS.

where g_m and g_o are the device transconductance and drain-source conductance, respectively. The memory elements (mainly capacitors) are ignored for simplicity, and only static linearization mechanisms are described for easier understanding. More accurate expressions can, however, be obtained using Volterra series analysis [49].

Before different linearization techniques are explained, it is crucial to better understand the nonlinear behavior of the short channel MOS device. For this reason, i_D of an nMOS transistor in a 65nm CMOS technology process with an aspect ratio of $\frac{20\mu\text{m}}{60\text{nm}}$ (minimum allowed length) was simulated and its first three derivatives were plotted, seen in Fig. 4.2. Since the nominal supply voltage in 65nm technology is 1.2V, V_{DS} is often set to 600mV for optimal signal swing. The value of V_{DS} can be significantly lower than 600mV when using cascode devices, however, MOS devices are in general less sensitive to V_{DS}. Therefore, in Fig. 4.2, V_{GS} was swept from 0V to 1.2V with V_{DS} =600mV. As can be seen in the figure, when V_{GS} is set to 0V the device is in the cut-off region and conducts no current. By increasing V_{GS} the nMOS starts to conduct current (at about V_{GS} =200mV) and enters the weak inversion region. As V_{GS} is further increased above V_{th} the nMOS enters the moderate and strong inversion regions. Looking at Fig. 4.2(d), it can be seen that the third order nonlinearity has two peaks with opposite signs when operating in weak and strong inversion.

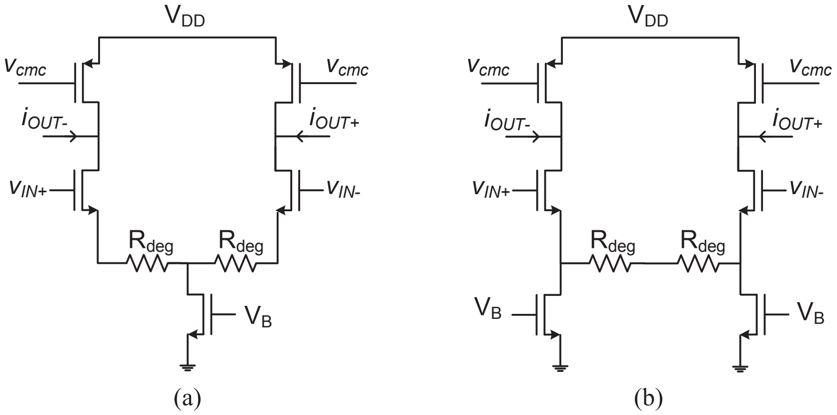


Figure 4.3: (a) Differential, and (b) pseudo differential common source OTA with degeneration.

4.2 OTA Linearization Techniques

The OTA is a major cause of nonlinearity in many active circuits, particularly in OTA-C filters where they operate in open loop configuration. Several linearization techniques have been therefore proposed over the years to improve the linearity of the OTA. A brief introduction to the most well-known techniques is given below. Further introduction can be found in e.g. [24, 50–52].

4.2.1 Source Degeneration

Source degeneration is a brute force technique that results in direct reduction of the effective transconductance (G_m) of the OTA. The basic idea of source degeneration is to implement local feedback by connecting a resistor (R_{deg} in Fig. 4.3) in series with the source terminal. The resistor senses i_D and its voltage appears in series with the input. The effective G_m will therefore approach a value close to the inverse of the resistance for large device g_m. The pseudo-differential structure is frequently used as there is no DC voltage drop over R_{deg}, and its resistance value is thus not limited by $\mathrm{V_{DD}}$, see Fig. 4.3(b).

Small signal analysis can be used to calculate G_m as

$$G_m \approx \frac{g_m}{1 + R_{deg}(g_m + g_{mb})} \tag{4.5}$$

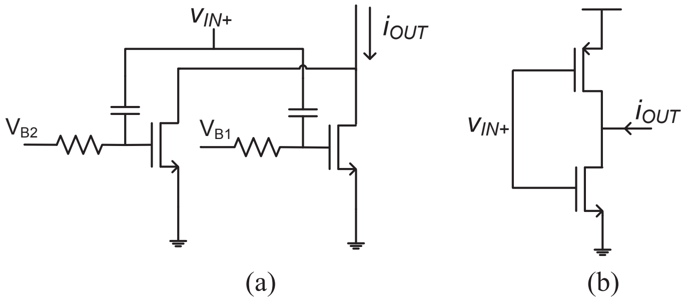


Figure 4.4: Implementation of (a) DS, and (b) CDS.

where g_{mb} is the body transconductance of the input MOS devices. The effective output resistance R_o of the OTA, ignoring the load devices, becomes

$$R_o \approx R_{deg} + r_o(1 + (g_m + g_{mb})R_{deg}) \tag{4.6}$$

where r_o is the output resistance of the input devices.

From (4.5, 4.6) it can be seen that G_m is reduced, which has a negative impact on the noise performance, while the output resistance desirably increases.

4.2.2 Derivative Superposition

One of the most effective and widely used linearization techniques is the derivative superposition (DS) linearization. DS linearization is based on the summation of currents from MOS devices with opposite nonlinearity polarities.

As shown in Fig. 4.2(d), the MOS third order nonlinearity coefficient will switch sign based on the operating region. To cancel the third order nonlinearity one can thus connect two MOS devices in parallel, with one biased in strong inversion and the other biased in weak inversion [50, 53] (see Fig. 4.4(a)). For high frequency circuits DC blocks are used, whereas level shifters (e.g. source followers) can be used for base band circuits.

The complementary-DS (CDS) is instead used to cancel even order nonlinearities based on the fact that pMOS devices are the dual of nMOS devices and may therefore be biased to operate under complementary bias conditions of the nMOS [51, 54]. The CMOS inverter is a widely used circuit which benefits from CDS linearization (see Fig. 4.4(b)). The values of g_m for nMOS and pMOS have to be matched for optimum nonlinearity cancellation. Therefore tuning may be needed for one of the devices to compensate for process variations.

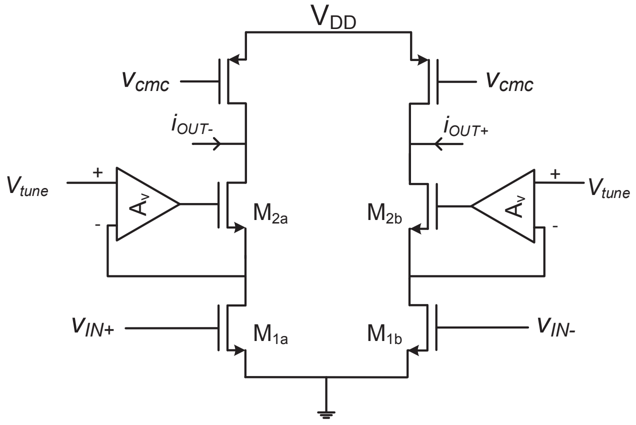


Figure 4.5: The triode OTA.

4.2.3 Triode OTA

The triode OTA is shown in Fig. 4.5, where devices M_1 are biased to operate in the triode region. Using long channel equations, i_D of a MOS device operating in triode region is linearly dependent on v_{GS}, as given for an nMOS transistor by

$$i_D = \mu_n C_{ox} \frac{W}{L_{eff}} (v_{GS} - V_{th}) v_{DS} - \frac{\alpha v_{DS}^2}{2} \tag{4.7}$$

The triode OTA [52, 55] is based on making v_{DS} constant and equal to V_{tune}. Differentially the output current using (4.7) will then equal

$$i_{OUT} = i_{OUT+} - i_{OUT-} = \mu_n C_{ox} \frac{W}{L_{eff}} (v_{IN-} - v_{IN+}) V_{tune} \tag{4.8}$$

As can be seen in (4.8) the voltage to current conversion is linear. This requires that the gain of the voltage amplifier (A_v) in Fig. 4.5 to be high over the frequency range of interest, so that the variation in v_{DS} can be minimized.

This technique is very effective assuming long channel approximation, however, as mentioned before the MOS nonlinearity is affected by high electric fields in advanced technologies. The mobility degradation will affect also the operation in the triode region, thus limiting the achievable linearity, as seen in Fig. 4.2(d) at increased v_{GS}.

To achieve even higher linearity one can use the cascode input for nonlinearity cancellation, as described in paper III of this dissertation [3] (see Fig. 4.6). The input signal is fed forward to the cascode devices (M_2) through a capacitive attenuator. The cascode device acts as a source follower, making the

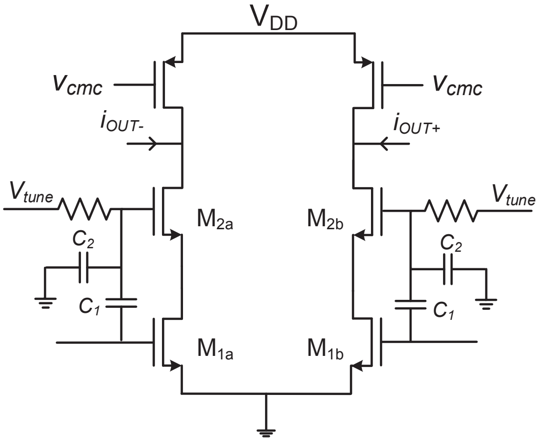


Figure 4.6: The triode OTA with capacitive feed forward.

attenuated input signal αv_{IN} appear at the drain of the input device ($\mathrm{M_1}$) . The current of the input nMOS operating in the triode region is thus given by

$$i_D = (g_m v_{IN} + K_2^{g_m} v_{IN}^2 + K_3^{g_m} v_{IN}^3 + ...)(\mathrm{V_{DS}} + \alpha v_{IN}) \tag{4.9}$$

In strong inversion $K_3^{g_m}$ and $K_2^{g_m}$ have opposite signs, and third order nonlinearity cancellation can then be achieved if α is chosen such that $K_3^{g_m} V_{DS} = -\alpha K_2^{g_m}$. Should, however, due to biasing conditions $K_3^{g_m}$ and $K_2^{g_m}$ have the same sign, cross-coupling can be used instead to achieve cancellation.

Although the triode OTA is highly linear, with reduced g_m due to triode region operation, it is in general only suitable for low to medium operating frequencies.

4.2.4 Triode Multiplier Linearization

The triode multiplier based linearization technique was proposed in paper IV [4], see Fig. 4.7, where it is applied to the OTA proposed in [56]. The multiplier is shown in the shaded area, where the generated second order nonlinearity is fed to the output stage load devices, and cancellation is achieved using the cross terms in the MOS characteristic as explained in the paper.

4.2.5 Negative Feedback

A very effective technique used to linearize circuits is negative feedback, where the output signal is scaled and subtracted from the input signal as shown in Fig. 4.8. The amplifier stage has a gain A, called the forward gain, and the

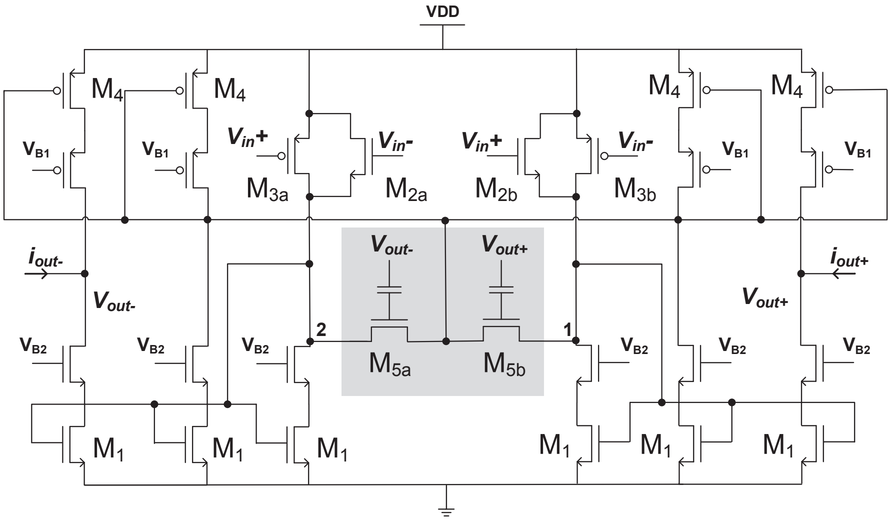

VDD
M4
M4
M4
M4
VB1
VB1
VB1
VB1
Vin+
Vin-
Vin+
Vin-
M3a
M2a
M2b
M3b
iout-
iout+
Vout-
Vout+
Vout-
Vout+
VB2
VB2
VB2
VB2
VB2
VB2
2
1
M5a
M5b
M1
M1
M1
M1
M1
M1

Figure 4.7: Schematic of a fully differential OTA with triode multiplier linearization.

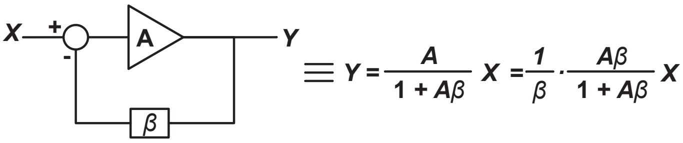

X
+
-
A
Y
β
≡ Y = A/(1 + Aβ) X = 1/β · Aβ/(1 + Aβ) X

Figure 4.8: A conceptual diagram of negative feedback.

feedback has a gain of less than unity, called the feedback factor (β). Recalling from chapter 3, the product $A\beta$ is called the loop gain. If A is weakly nonlinear as described by (2.4), the resulting system transfer is given by [24]

$$Y = a_1X + a_2X^2 + a_3X^3 \tag{4.10}$$

where

$$\begin{aligned} a_1 &= \frac{g_1}{1 + A\beta} \\ a_2 &= \frac{g_2}{(1 + A\beta)^3} \\ a_3 &= \frac{g_3 - \frac{2g_2^2}{g_1}}{(1 + A\beta)^4} \end{aligned} \tag{4.11}$$

Compare at the same output level without feedback:

$$y = g_1 x + g_2 x^2 + g_3 x^3 \tag{4.12}$$

The relative distortion level becomes

$$\frac{g_2 x + g_3 x^2}{g_1}$$

Since with feedback

$$X = (1 + A\beta)x \tag{4.13}$$

the relative distortion when using feedback then becomes

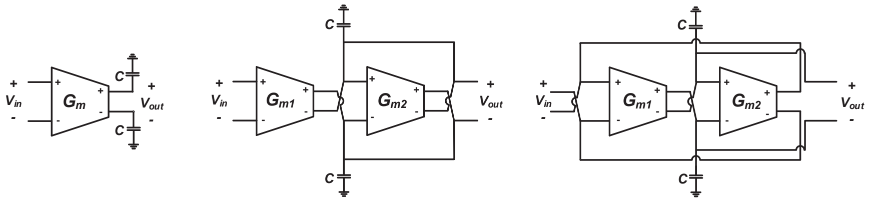
$$\frac{a_2 X + a_3 X^2}{a_1} = \frac{g_2}{g_1}\frac{1}{1 + A\beta}x + (\frac{g_3}{g_1} - \frac{2g_2^2}{g_1^2})\frac{1}{1 + A\beta}x^2 \tag{4.14}$$

In (4.14) it can be seen that the relative distortion level has been reduced by a bout a factor of $1 + A\beta$. As can also be seen in (4.14) a high $A\beta$ will considerably improve the linearity performance as the distortion level is scaled accordingly. As will be shown later in this chapter, however, it is very difficult to maintain a high $A\beta$ over a wide frequency range, since loop stability needs to be ensured to avoid self-oscillation due to positive feedback. Therefore, feedback is most effective in base band applications. Nonetheless, feedback can also be applied successfully to improve RF performance through frequency translational loops [57–60].

4.2.6 Other Linearization Techniques

Since nonlinearity is perhaps the most urgent issue in modern wireless tran–sceivers, a lot of research effort is spent on linearization techniques. Post-distortion for example, can be used to improve the system linearity by cascading a nonlinear stage with one having the inverse nonlinearity [61]. For example, a stage with expanding characteristic can be added at the output of an amplifier which is compressing. Predistortion is in concept the same as post-distortion except for that the inverse transfer stage is instead applied to the signal before the nonlinear stage to compensate for. Predistortion and post-distortion can also be applied in the digital domain for the TX and RX, respectively. The advantage is to be able to tune for optimal cancellation using powerful digital signal processing algorithms.

In nonlinearity summation (e.g. [62]) the nonlinearity is canceled by subtraction. Currents with opposite signs and equal magnitudes of the nonlinear terms are summed, which is similar to DS. However, in nonlinearity summation usually two separate OTAs are used and their output currents are summed. For example, in [63] the third order nonlinear term was generated and the subtraction was performed in the digital domain.



(a) (b) (c)

Figure 4.9: Basic building blocks of an OTA-C filter: (a) integrator, (b) lossy integrator, and (c) a gyrator with capacitive load.

4.3 Channel Select Filter Architectures

Two architectures are frequently used to implement active filters, active-RC and OTA-C. The active-RC filters have superior linearity since they operate with the amplifiers in closed loop configuration, while OTA-C filters can instead operate at very high frequency, but with poor linearity due to open loop configuration. Therefore OTA linearization is needed to improve the dynamic range when OTA-C filters are adopted.

In this section, a brief introduction to filter configurations and biquad architectures is presented. For more in-depth material on filter design the reader is directed to e.g. [45, 64].

4.3.1 OTA-C Filters

OTA-C filters are implemented using OTAs and capacitors, which explains their name. There are generally two ways to implement an OTA-C filter:

–**LC ladder simulation** where a passive filter is first designed using inductors and capacitors. The inductors are then replaced by gyrators and capacitors (active inductors). More about different filter responses and how to simulate an LC ladder can be found in e.g. [45, 64].

–**Cascade of biquads** where the filter TF is divided into second order stages, each with a complex pole and/or zero pair, and a first order stage in case of odd order filters. The biquads are then cascaded to get the overall desired filter TF.

Assuming ideal OTAs, the basic building blocks are the integrator, Fig. 4.9(a), the lossy integrator, Fig. 4.9(b), and the gyrator, Fig. 4.9(c). The TF of the integrator is given by

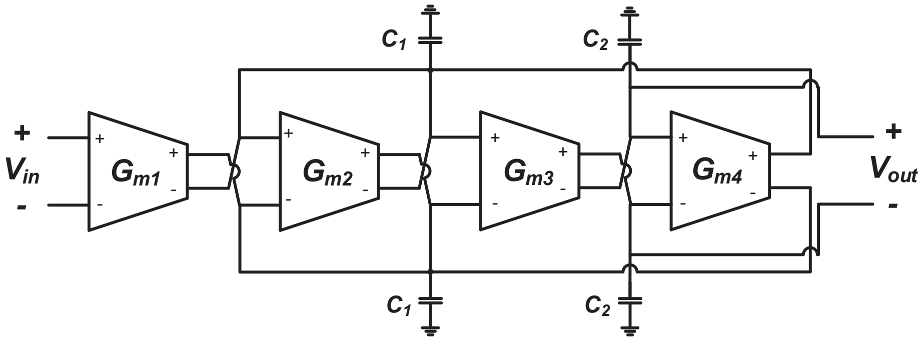


Figure 4.10: Block diagram of an OTA-C biquad.

$$TF_a = \frac{G_m}{sC} \tag{4.15}$$

and the TF of the lossy integrator is easily calculated as

$$TF_b = \frac{G_{m1}}{sC + G_{m2}} \tag{4.16}$$

and the input impedance of the gyrator becomes

$$Z_{gyr} = s\frac{C}{G_{m1}G_{m2}} = sL_{gyr} \tag{4.17}$$

where L_{gyr} is the gyrator simulated inductance.

A second order low pass filter (biquad) is shown in Fig. 4.10, where the TF is given by

$$TF_{biquad} = \frac{G_{m1}G_{m3}}{s^2C_1C_2 + sC_2G_{m2} + G_{m3}G_{m4}} \tag{4.18}$$

Feed forward capacitors can be used if a zero is needed in the transfer function, and the output can be taken at the G_{m4} stage for a band pass characteristic [45].

The TF in (4.18) was calculated assuming OTAs without parasitic capacitance and with infinite input and output impedances. The non-ideal behavior of the OTAs includes non-zero output conductance (G_o) and finite input and

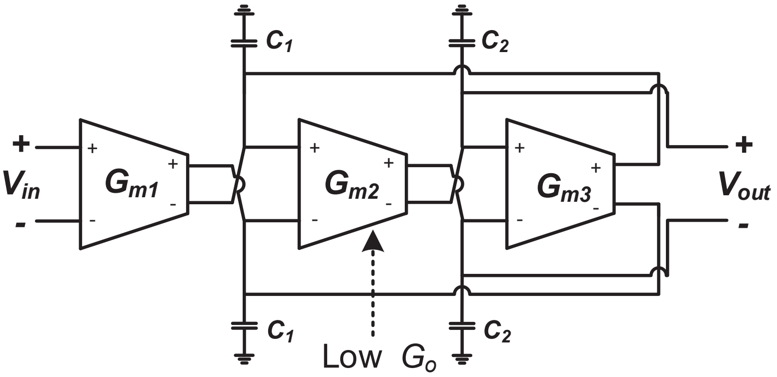


Figure 4.11: Block diagram of the second order OTA-C biquad using three OTAs.

output capacitance (C_i, C_o). The TF of the biquad in Fig. 4.10 then becomes

$$\frac{V_{out}}{V_{in}} = \frac{G_m^2}{As^2 + Bs + C}$$

$$A = C_{tot1}C_{tot2} \tag{4.19}$$

$$B = [C_{tot2}(G_m + 3G_o) + C_{tot1}G_o]$$

$$C = [G_m^2 + G_mG_o + 3G_o^2]$$

Where the OTAs have been assumed to be identical for simplicity[3], $C_{tot1} = C_1 + 3C_o + 2C_i$, and $C_{tot2} = C_2 + C_o + C_i$. In (4.19) the DC gain is less than unity, but more importantly the highest achievable frequency is limited by C_i, C_o, and G_m. Furthermore, following the scaling trend it is known that for a MOS device, $g_o \propto L_{eff}$. This means that reduction in MOS device dimensions will result in significant effects on the OTA. For this reason in paper IV [4], G_o was incorporated into the TF of the filter. This was achieved by using the proposed biquad shown in Fig. 4.11, where the TF is given by

$$\frac{V_{out}}{V_{in}} = \frac{G_{m1}G_{m2}}{C_{tot1}C_{tot2}s^2 + (C_{tot1}G_{o2} + C_{tot2}(G_{o1} + G_{o3}))s + G_{o2}(G_{o1} + G_{o3}) + G_{m2}G_{m3}} \tag{4.20}$$

---

[3] this is also a common practice to improve the matching between the cells

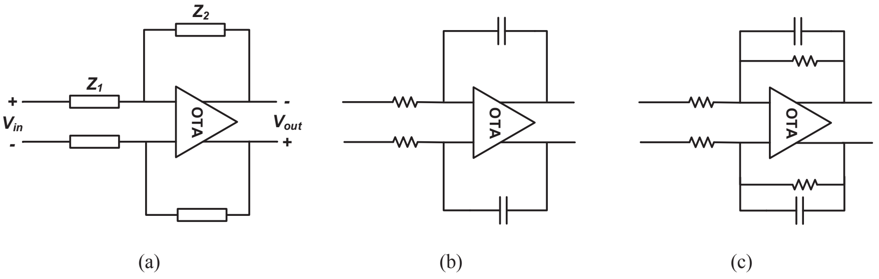


Figure 4.12: Basic building blocks of an active-RC filter: (a) a general amplifier, (b) an integrator, and (c) a lossy integrator.

It is clear from (4.20) that non-negligible G_o can be turned into an advantage. To reduce the insertion loss, G_{o2} can be reduced, e.g. by using cascode devices as shown in Fig. 4.7. This reduces (4.20) to

$$\frac{V_{out}}{V_{in}} \approx \frac{G_{m1}G_{m2}}{C_{tot1}C_{tot2}s^2 + (C_{tot2}(G_{o1} + G_{o3}))s + G_{m2}G_{m3}} \tag{4.21}$$

The resulting biquad benefits from CMOS technology scaling and reduces the number of OTAs, which leads to reduced power consumption.

4.3.2 Active-RC Filters

Contrary to OTA-C filters, active-RC filters operate the amplifiers in closed loop configuration. Therefore they have attractive properties such as high linearity, and ease of configuration of different filter parameters such as gain, bandwidth, and even response [65, 66]. The name active-RC comes from that the feedback loop around the active forward gain amplifier is closed using capacitors and resistors. Fully differential structures are often used, since they have very attractive properties such as rejection of supply noise, increased linearity, and higher signal swing. The basic configurations of differential active-RC first order amplifiers (filters) are shown in Fig. 4.12. Assuming an ideal amplifier (OTAs are used in this dissertation), the TF is given by

$$\frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_1} \tag{4.22}$$

Second order biquads using only one OTA have been proposed (e.g. the Rauch and the Sallen-Key biquads) and can be found in e.g. [45]. However, gain, pole frequency, and Q of these biquads are not linearly tunable, and as

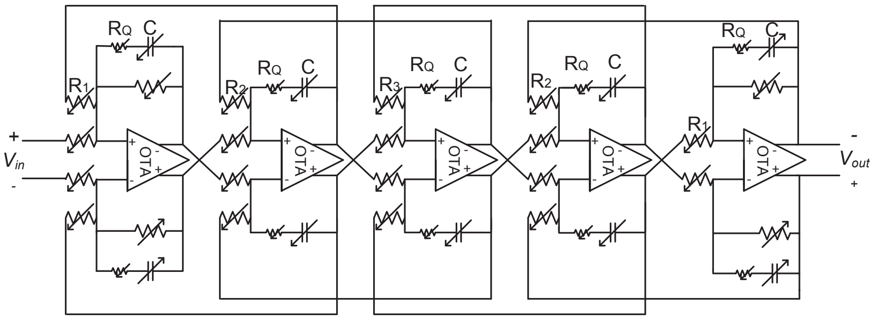

RQ
C
R1
R2
R3
R2
R1
OTA
+
-
Vin
Vout

Figure 4.13: Schematic of the 5th order Chebyshev filter presented in [2].

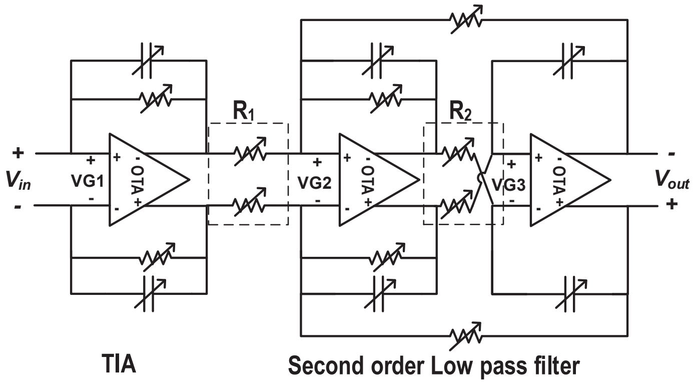

R1
R2
+
Vin
-
VG1
VG2
VG3
OTA
-
Vout
+
TIA
Second order Low pass filter

Figure 4.14: Cascade of TIA and second order filter forming the 3rd order Chebyshev filter used in [5].

reconfiguration is crucial for wireless receivers such topologies were not considered in this dissertation.

Higher order active-RC filters, similar to OTA-C filters, are implemented using:

–**LC ladder simulation** which is also known as leap-frog filter, where an LC ladder filter prototype is first designed, the voltage and current relations are then obtained and simulated by the active-RC filter. The design procedure can be found in e.g. [45]. In Fig. 4.13 the fifth order Chebyshev active-RC filter presented in paper II [2] in this dissertation is shown.

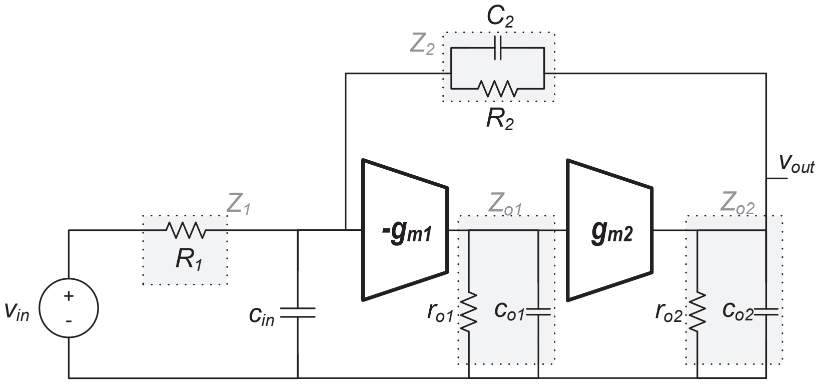


Figure 4.15: Model of a two-stage OTA in inverting voltage amplifier configuration.

–**Cascade of biquads** where the filter TF is divided into first and second order stages with different Q-factors, which are then cascaded to get the desired overall TF. This facilitates the pole of the TIA to be included in the CSF TF. The CSF used in the receiver front-end presented in paper V [5], seen in Fig. 4.14, uses this concept. In resistors R_1 and R_2 fine tuning of phase and amplitude is achieved using programmable banks of large parallel resistors [67, 68].

OTA Requirements

The basic structure of active-RC filters has been introduced, but to understand their implementation trade-offs and limitations, insight into the OTA characteristics and performance requirements is needed. This is because all the feedback loops need to be stable, and also due to that sharp filters with high bandwidth increase the OTA speed requirements significantly. Linearity is also very important as the OTA signal amplitude can be high for band edge/out-of-band signals as $A\beta$ rolls off.

The TIA loop gain analysis of chapter 3 is also applicable to the inverting voltage amplifier configuration, see Fig. 4.15. The $A\beta$ at DC is given by

$$A\beta_{DC} = -g_{m1}g_{m2}r_{o1}r_{o2}\frac{R_1}{R_1 + R_2 + r_{o2}} \tag{4.23}$$

it can be seen in (4.23) that $A\beta$ is reduced for small values of R_1, but on the other hand large values of R_1 will instead increase the thermal noise. Larger values of R_1 can be used, however, if the signal is sufficiently amplified by the LNTA and the TIA, making the receiver less sensitive to noise in the CSF. Assuming c_{in} and c_{o2} are kept small compared to C_2, the pole and zero frequencies can be approximated as

$$P_1^{A\beta} \approx -\frac{1}{r_{o1}c_{o1}} \tag{4.24}$$

$$P_2^{A\beta} \approx -\frac{1}{(R_1 \| (R_2 + r_{o2}))C_2} \tag{4.25}$$

$$P_3^{A\beta} \approx -\frac{1}{(R_1 \| r_{o2})(c_{o2} + c_{in})} \tag{4.26}$$

$$Z_1^{A\beta} \approx -\frac{1}{R_2 C_2} \tag{4.27}$$

The closed loop 3dB bandwidth of the amplifier is equal to the frequency of the zero in the feedback path, given by (4.27). If then the open loop 3dB bandwidth of the OTA, given by (4.24), matches that of the amplifier in closed loop, only the effect of the two poles of (4.25) and (4.26) will determine the phase margin. This significantly simplifies the compensation of the OTA to ensure the required phase margin. It can be concluded as well that the OTA 3dB bandwidth needs to be high if the base band bandwidth is high to ensure high linearity throughout the base band frequency range.

It must be emphasized that the requirements on OTA bandwidth are dependent on the CSF filter response [66]. For example, for the same filter bandwidth and order, a maximally flat response requires less OTA bandwidth than a Chebyshev due to difference in Q values of the pole pairs. The required bandwidth of the OTA puts a limit to the maximum achievable CSF bandwidth, preventing the use of active-RC filters in high frequency applications.

To better understand the OTA impact on the filter performance, the OTA model introduced in chapter 3 is used, seen in Fig. 4.15. The TF of a lossy integrator can then be obtained as

$$\frac{V_{out}}{V_{in}} = \frac{-Z_2(g_{m1}g_{m2}Z_{o1}Z_{o2}) - Z_{o2}}{Z_1 + Z_2 + Z_{o2} + Z_1 g_{m1}g_{m2}Z_{o1}Z_{o2}} \tag{4.28}$$

The gain error (GE) can be approximated by

$$GE \approx \frac{(c_{o1}r_{o1}s + 1)(R_2 + R_1 + C_2R_2R_1s)(R_2 + r_{o2} + C_2R_2r_{o2}s)}{R_1R_2g_{m1}g_{m2}r_{o1}r_{o2}(C_2R_2s + 1)} \tag{4.29}$$

A zero in (4.29) is not desirable since it will cause the GE to increase. Unfortunately, there are three zeros in (4.29), located at angular frequencies $Z_1^{GE} = -(c_{o1}r_{o1})^{-1}$, $Z_2^{GE} = -(C_2(R_1 \| R_2))^{-1}$, and $Z_3^{GE} = -(C_2(R_2 \| r_{o2}))^{-1}$. There is also one pole at $P_1^{GE} = -(C_2R_2)^{-1}$. It can also be noted that increasing the voltage gain of the OTA ($g_{m1}g_{m2}r_{o1}r_{o2}$), and R_1, will reduce GE.

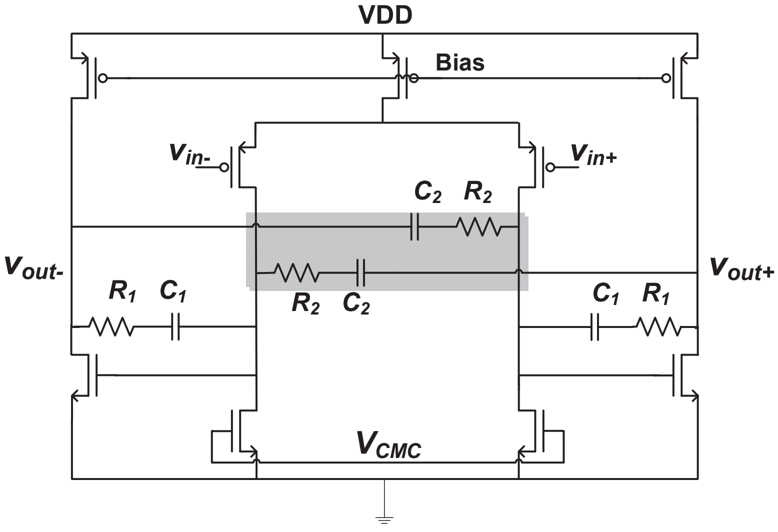


Figure 4.16: A two-stage OTA with phase enhanced compensation.

To summarize, a good rule-of-thumb is to make the OTA open loop bandwidth ($-(c_{o1}r_{o1})^{-1}$) match the wanted closed loop bandwidth ($-(C_2R_2)^{-1}$). This cancels Z_1^{GE} and P_1^{GE}, leaving Z_2^{GE} and Z_3^{GE}. Since Z_3^{GE} is located close to the 3dB frequency, and depending on the closed loop gain Z_2^{GE} is located only a bit further up in frequency. The conclusion is it seems inevitable that the errors start to increase near the band edge. Furthermore, with the increasing channel bandwidths of wireless systems, matching the open loop bandwidth to the closed loop seems to rule out phase compensation techniques like Miller, which heavily reduce the OTA speed. However, with sufficiently large R_1 the GE will start increasing at relatively higher frequencies. The GE increase is relative to its value at DC, which motivates increasing the voltage gain of the OTA.

OTA Compensation

The problem of reduced OTA bandwidth has received a lot of attention, and many compensation techniques have been proposed to increase the speed of the OTA. Some examples can be found in [69–74]. In particular, for high frequency applications the feed forward technique has been widely adopted. In feed forward a fast auxiliary path is added in parallel to the main path. Requiring the OTA to have sufficient gain and bandwidth to dominate the

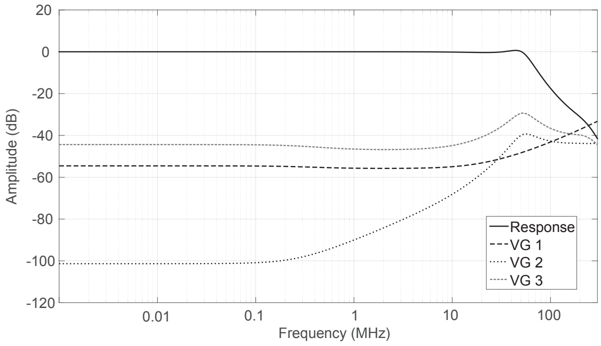


Figure 4.17: Normalized response at the virtual ground node of the OTAs, and the response of the CSF in Fig. 4.14.

gain and phase margin at higher frequency, which leads to increased power consumption.

In paper I [1], the phase enhanced compensation technique is proposed, which considerably improves the bandwidth of the OTA by using positive feedback RC links (as shown in the shaded area of Fig. 4.16). In the figure a two stage OTA is shown but, the proposed technique is also scalable to higher order OTAs.

Although a lot of effort has been spent on increasing the bandwidth of OTAs, the increasing channel bandwidth in wireless systems still makes the OTA design a major challenge. Added to that, highly configurable designs imply more switches, which increase the parasitic capacitance, considerably impacting the OTA bandwidth. For these reasons, a small resistor in series with the integrator feedback capacitor can be used to create a transfer function zero, tuned to cancel the effect of the second pole, e.g. the resistors labeled R_Q in the filter shown in Fig. 4.13. This results in a more ideal behavior of the integrator.

OTA Linearity

The linearity of the OTA is critical for wide-bandwidth CSFs, especially, at frequencies near the band edge. Considering the third order filter shown in Fig. 4.14, the normalized amplitude to the CSF gain at the virtual ground node of each OTA is shown in Fig. 4.17. It can be seen that the signal amplitudes are considerably increased at the band edge, leading to deteriorated linearity.

To improve the linearity, the $A\beta$ needs to be increased at higher frequencies. Another reason why the OTA 3dB bandwidth is recommended to be as high as the filter bandwidth. The linear input voltage range needs to be increased as well, which for instance can be achieved using push-pull stages.

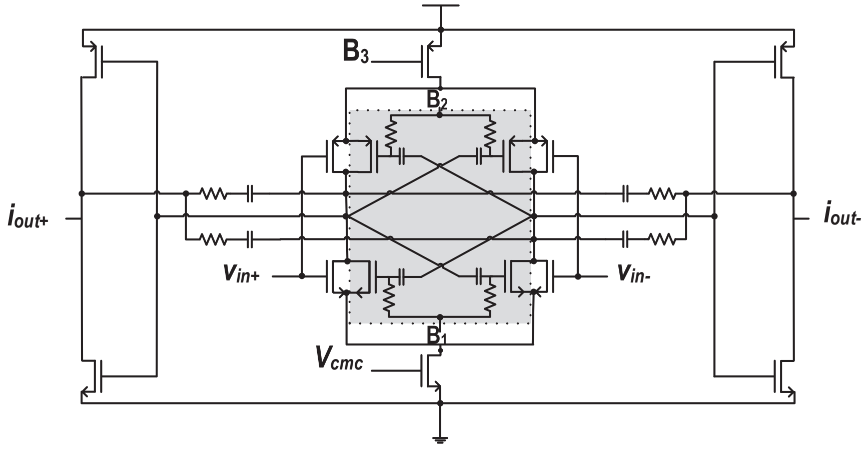


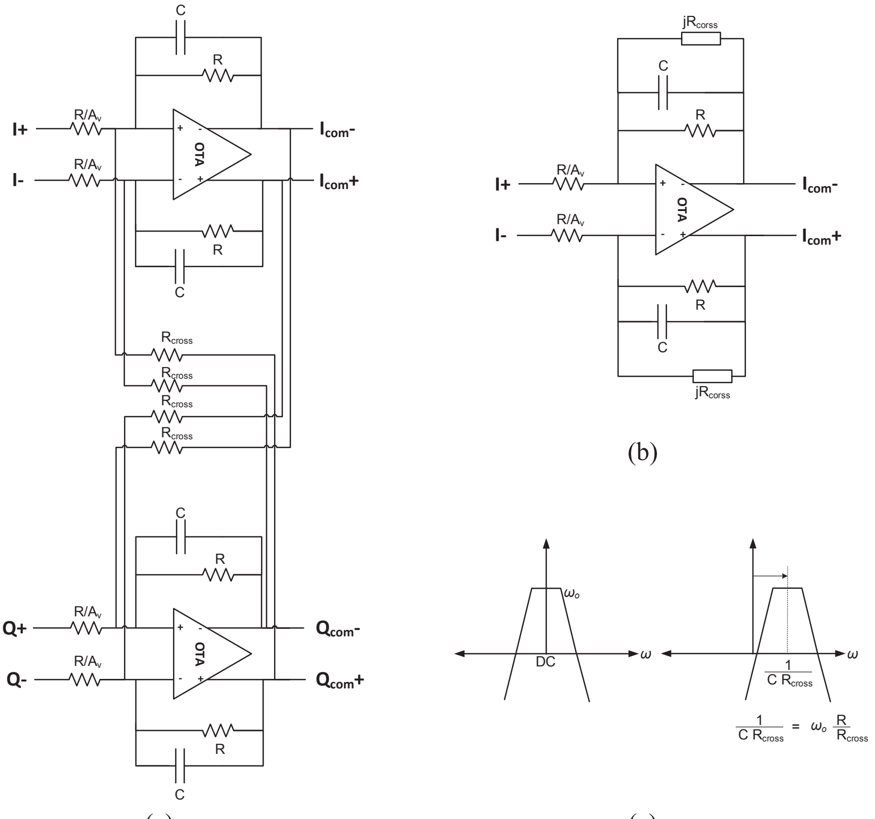
Figure 4.18: Schematic of the linearized OTA used in [5].

In Fig. 4.18, the OTA used in paper V [5] is shown. The DS linearization technique has been widely used in open loop configuration, but here it is proposed for use in closed loop as shown in the shaded area Fig. 4.18. The feedback of the amplified signal allows for the use of small auxiliary devices, with reduced g_m. This is beneficial for wide-bandwidth applications, since as discussed before, c_{in} negatively impacts the speed of the OTA.

4.3.3 Complex Active-RC Filters and Spectrum Sensors

The widely used homodyne receiver uses quadrature signals where the center frequency of the channel is down converted to DC. In low intermediate frequency (IF) receivers the channel is instead centered at a non-zero but low IF [75, 76]. In low IF receivers, the CSF needs to suppress the interfering signals around the IF, including the image at -IF. Since conventional bandpass filters will not suppress signals at the image frequency, complex filters are used to suppress one side of the spectrum. This is achieved by using low pass filters and moving their frequency response to the desired IF using coupling paths between the I and Q-channel filters. The RF part of the low IF receiver is very similar to that in the homodyne.

The first order complex filter is shown in Fig. 4.19, higher order filters can be realized similarly using crossing resistors for each integrator stage. The resistors provide the coupling responsible for the frequency shift, and by using programmable resistors the pass band frequency can be changed. To move the pass band to negative frequencies instead, the Q path needs to be switched with the I path.


C
R
R/Av
I+
R/Av
I-
OTA
Icom-
Icom+
R
C
Rcross
Rcross
Rcross
Rcross
C
R
R/Av
Q+
R/Av
Q-
OTA
Qcom-
Qcom+
R
C
jRcorss
C
R
R/Av
I+
R/Av
I-
OTA
Icom-
Icom+
R
C
jRcorss
ωo
DC
ω
ω
1 / C Rcross
1 / C Rcross = ωo R / Rcross

(a) (b) (c)

Figure 4.19: (a) Schematic of an active-RC complex filter, (b) equivalent representation of the I path, and (c) effect on the TF.

In paper V [5], the complex filtering concept is incorporated into the spectrum sensor (shown in Fig. 4.20). The I and Q signals at the output of the TIA are fed to a 4^{th} order complex Butterworth filter, which has a programmable center frequency (ω_c). The resistance values used are very large ($32\text{k}\Omega$), and therefore the noise performance of the receiver front-end is not affected, while the dynamic range of the spectrum sensor is slightly reduced. The output of the complex filter is fed to a power detector (PD), which squares the filtered signal [77, 78]. The squaring results in low frequency components representing the power of the signal, and high frequency components which are suppressed using a low pass RC filter. The low frequency (DC) signal is then digitized and its value represents the power of the signal in the current component frequency bin selected by the filter.

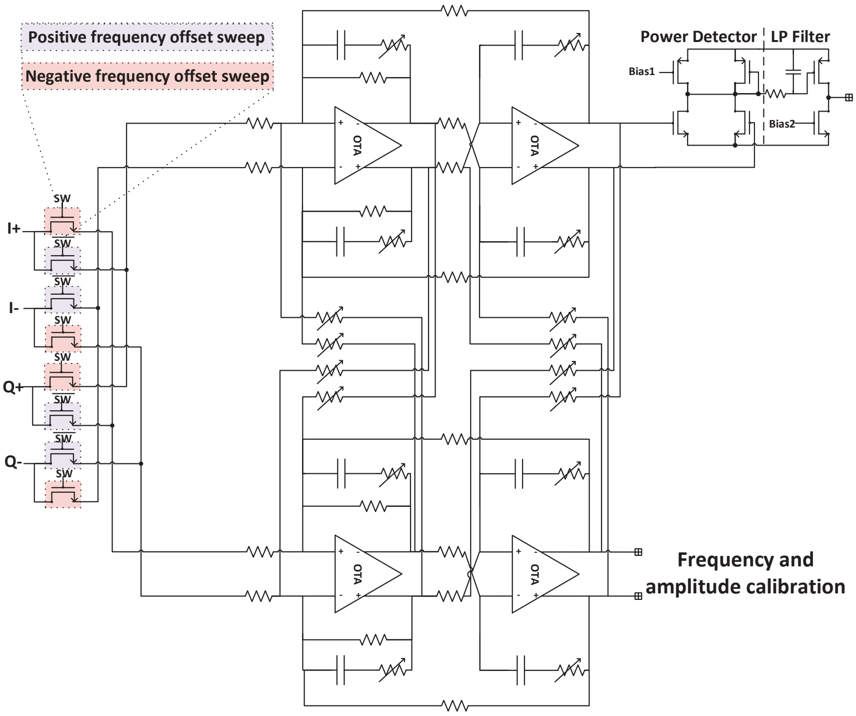

Positive frequency offset sweep
Negative frequency offset sweep
SW
I+
I-
Q+
Q-
OTA
Power Detector
LP Filter
Bias1
Bias2
Frequency and amplitude calibration

Figure 4.20: Schematic of the proposed spectrum sensor.

To enable both positive and negative frequency sweeps, switches are used to swap the I and Q paths at the input as shown in Fig. 4.20. The switches at the input also enable calibration of the DC level, by first disabling all the switches and measuring the DC output of the spectrum sensor. The switches are then enabled for a sweep. A spectrum sweep is performed using the input switches to select frequency sign and R_{cross} to select frequency magnitude. After a full spectrum sweep, blocker levels are compared to stored threshold values, and decisions can be taken to apply settings that improve the performance of the receiver front-end. For example, if the desired in-band signal is strong, then low noise mode can be turned off to save current, and possibly base band gain reduction is required to avoid ADC saturation. As also shown in paper V [5], spectrum sensing is needed for correctly tuning many parameters in a reconfigurable receiver front-end such as the capacitance at the output of the mixers, base band gain etc.

Chapter 5

Summary and Scientific Contribution of Included Papers

An introduction to wireless receiver design and the main challenges of nanometer CMOS implementations is presented in the previous chapters. In this chapter, a summary of the papers included in this dissertation is provided, together with conclusions comparing measured and simulated results to analysis. For each paper a summary of scientific contributions is also provided to state its significance.

I contributed to the papers with background research, state-of-the-art review, and idea development. I also performed majority/all of the analysis, design, simulations, implementation, and measurements. Valuable help and input was received from my co-authors during different phases of each work. My supervisors' contributions from the idea and design development up to manuscript production significantly improved the quality of work.

5.1 Paper I: A Compensation Technique for Differential Two-Stage OTAs

Summary

The paper introduces the phase enhanced compensation technique where positive feedback is used to improve the phase margin of the OTA, while the Miller effect is eliminated. The OTA speed is therefore only slightly reduced compared to the uncompensated case, while the phase margin is enhanced. Detailed analysis and simulations of two-stage differential OTAs with phase enhanced compensation, together with a comparison to the well-known Miller compensation are presented. The performance of the compensation technique is extensively investigated for different process corners, against temperature variations, and process mismatch. Added to that, capacitive load variations and the slew rate performance are also investigated.

The technique introduces two zeros with frequencies determined by time constants (τ) of the RC links. Two parasitic poles are also introduced by the

RC links. The zero frequencies are tuned to cancel two poles, left are two poles. The dominant pole frequency is not reduced by Miller effect and therefore is high in frequency, and the non-dominant pole frequency is set by the parasitic capacitance whose frequency is also very high.

To prove the technique an OTA was designed in 65nm CMOS, which consumes 0.625mA from a 1.2V supply. It shows more than three times improvement in 3dB bandwidth and gain-bandwidth product (GBP) when compared to conventional Miller compensation, the slew rate is also doubled.

To conclude, in this paper a new compensation technique for two-stage OTAs is presented. The proposed technique significantly increases the OTA bandwidth by enhancing the phase margin through positive feedback. Compared to Miller compensation, it provides an improved 3dB bandwidth and GBP. Simulations of the proposed technique show that it is robust against process and temperature variations. Moreover, simulations of a three stage OTA show that the proposed technique can be extended to amplifiers with more than two stages.

Scientific Contributions

- A proposed phase compensation technique for two-stage differential OTAs that drastically improves frequency response and slew rate without any current consumption overhead.
- The proposed technique can also be used in OTAs with more than two-stages (i.e. nested phase enhanced compensation).

5.2 Paper II: A 3.4mW 65nm CMOS 5^{th} Order Programmable Active-RC Channel Select Filter for LTE Receivers

Summary

To demonstrate the phase enhanced compensation technique, a low power fifth order Chebyshev active-RC low pass filter, which requires high speed OTAs was designed. The filter meets LTE RX bandwidth requirements and was designed with programmable bandwidth and overshoot. The OTA used in the filter benefits from phase enhanced compensation, resulting in reduced power consumption and improved band edge and out-of-band linearity.

Designed for homodyne LTE-Rel. 8 receivers, filter bandwidths from 700kHz to 10MHz are supported. The filter was implemented in 65nm low power CMOS technology with a core area of 0.29mm^2, as shown in Fig. 5.1. The total current consumption was 2.83mA from a 1.2V supply. The measured input referred noise was $39\text{nV}/\sqrt{\text{Hz}}$, the in-band IIP3 was 21.5dBm, at the band edge the IIP3 was 20.7dBm, the out-of-band IIP3 was 20.6dBm, and the $\text{ICP}_{1\text{dB}}$ was 0dBm with an in-band gain of 4.5dB.

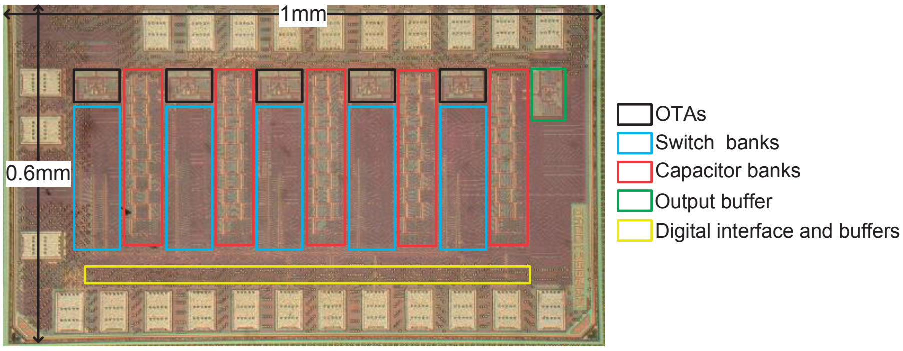


Figure 5.1: Die micrograph of the 5$^{\text{th}}$ order Chebyshev active-RC CSF.

In summary, a low power fifth order Chebyshev active-RC filter for LTE receivers has been fabricated in 65nm CMOS technology. The OTA used in the filter benefits from phase enhanced compensation, resulting in low power consumption and improved performance of the filter. Confirming the simulation results the filter measurements show a high dynamic range, combined with wide-bandwidth tuning and Q-factor ranges to handle the different operating scenarios.

Scientific Contributions

- A low power CSF for LTE-Rel. 8 receivers has been implemented with OTAs compensated using the phase enhanced compensation technique proposed in [1]. The measurements validated the compensation technique, showing that the improvement of OTA speed enables low power implementations of high performance filters for wireless communication.

5.3 Paper III: A 4$^{\text{th}}$ Order Gm-C Filter with 10MHz Bandwidth and 39dBm IIP3 in 65nm CMOS

Summary

In this paper a highly linear CSF filter is presented. A triode OTA is used in the filter, however, instead of using feedback amplifiers to reduce the variations in v_{DS} of the triode region input devices, a feed forward technique is used for nonlinearity cancellation. This technique is demonstrated in the low power 4$^{\text{th}}$ order 10MHz Butterworth OTA-C low pass filter. Measurements show that the technique effectively reduces nonlinearities in the filter.

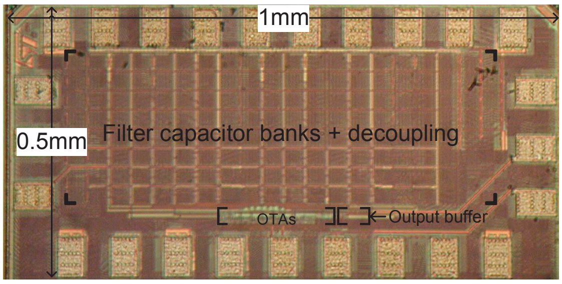


Figure 5.2: Die micrograph of the 4th order 10MHz CSF.

The filter was implemented in 65nm CMOS technology with a core area of 0.19mm^2 (see Fig. 5.2) and a total current consumption of 3.5mA from a 1.2V supply. The measured input referred noise was $31\text{nV}/\sqrt{\text{Hz}}$, and the filter achieved an IIP3 of 39dBm in-band, and 34dBm out-of-band. Thanks to the triode input devices, the measured $\text{ICP}_{1\text{dB}}$ was 8.2dBm.

In conclusion, a highly linear 4th order CSF fabricated in 65nm CMOS technology is presented. It benefits from a linearized triode OTA improving the overall linearity. The filter thus achieves state-of-the-art IIP3 and dynamic range. The effectiveness of the linearization technique makes it attractive for implementing high dynamic range filters in advanced technology nodes. Supply and temperature variation measurements prove the linearization technique to be robust, as the optimal control voltage is not shifted significantly and high performance is maintained without control voltage readjustment.

Scientific Contributions

- A passive nonlinearity cancellation scheme [3] was applied on a triode OTA, resulting in significantly improved linearity. A 4th order CSF using the proposed OTA measures high linearity thanks to the linearization. Measurements over temperature and supply variations also show that the linearization still holds and state-of-the art dynamic range is achieved.

- This solution was found to be more effective than the widely used triode OTA with feedback amplifiers, and also less expensive in terms of power consumption and area.

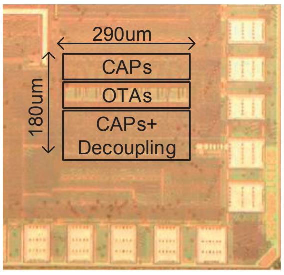


Figure 5.3: Die micrograph of the 4^{th} order 80MHz CSF.

5.4 Paper IV: A Linearization Technique for Differential OTAs

Summary

A novel OTA linearization technique based on triode region devices acting as signal multipliers is proposed. Detailed analysis and simulations are presented in the paper. The triode multiplier linearization was applied to a wide-band shunt feedback LNA. Simulations of the LNA show that the IIP3 improvement can exceed more than 20dB, and mismatch simulations show that the linearization is robust against process variations and device mismatch. Simulations also show that its effects on gain, NF, and input match are negligible.

The triode multiplier linearization was also applied to the OTAs of a 4^{th} order Butterworth CSF with a bandwidth of 80MHz. The CSF was implemented using six OTAs instead of the conventional eight, thus reducing the power consumption and area. Simulations and measurements of the CSF show the effectiveness of the triode multiplier linearization technique.

The filter was implemented in 65nm low power CMOS, with a core area of 0.05mm^2, shown in Fig. 5.3, and consumed 12.6mA from a 1.2V supply. Three samples were measured and the measured in-band noise was below $42\text{nV}/\sqrt{\text{Hz}}$, while the measured IIP3 improvement using OTA linearization was up to 17dB in-band and about 3dB out-of-band. Less improvement at lower frequencies was measured due to the DC blocks, but this can easily be solved by instead using level shifters for biasing. Supply and temperature variation measurements show that the linearization is effective without any bias adjustment.

To conclude, a novel linearization technique using a triode multiplier that effectively cancels the third order nonlinearity is presented. The technique was implemented in a wide-band LNA and a 4^{th} order 80MHz OTA-C filter. Simulations of the LNA show significant improvement of the linearity while the gain, power consumption, and noise performance remain unaffected. The filter was fabricated in 65nm low power CMOS and measured robust improved linearity performance over supply and temperature variations. The filter has a

very competitive core area of just 0.05mm^2 and the measured performance is well in line with state-of-the-art. Simulations and measurements confirm the effectiveness of the proposed technique.

Scientific Contributions

- A novel triode multiplier based OTA linearization technique that significantly improves the linearity. The triode multiplier is attractive since it consumes no DC current, eliminating the power overhead, is immune to flicker noise and has negligible effect on the other OTAs performance. The linearization technique is suitable for high frequency circuits and does not affect the noise performance, making it attractive also for LNAs [4]. Detailed analysis verified by simulations in [4] show that the linearization is robust. Added to that, measurements of the 4$^{\text{th}}$ order Butterworth OTA-C filter shows significantly improved performance compared to the nonlinearized case, which also holds over temperature and supply variations.
- The filter structure uses six OTAs instead of eight, reducing the power consumption. It also supports technology scaling reduced MOS intrinsic gain by using G_o of the OTA in the filter TF.
- The triode multiplier may also be used as a nonlinear impedance that has higher resistance at higher differential output voltage amplitudes, which results in increased gain for larger signals. The compression point and linearity can then be increased. This is very useful for example in improving the performance of power amplifiers.

5.5 Paper V: A Cellular Receiver Front-End with Blocker Sensing

Summary

In this work a receiver front-end with a third order Chebyshev CSF supporting contiguous and non-contiguous intra-band LTE-A CA scenarios is presented. The receiver front-end also includes a fully integrated spectrum sensor that consists of a 10MHz complex filter followed by a power detector and a low pass filter. The spectrum sensor is set to detect signals after quadrature down conversion at both positive and negative frequencies. The spectrum sensor can detect both in-gap and out-of-band blockers. In-gap blockers may occur in non-contiguous CA scenarios, which means that the linearity in-band is then as important as the out-of-band.

The LNTA has a noise canceling path that can be turned off to save current, and the OTAs used in the base band have improved GBP thanks to the

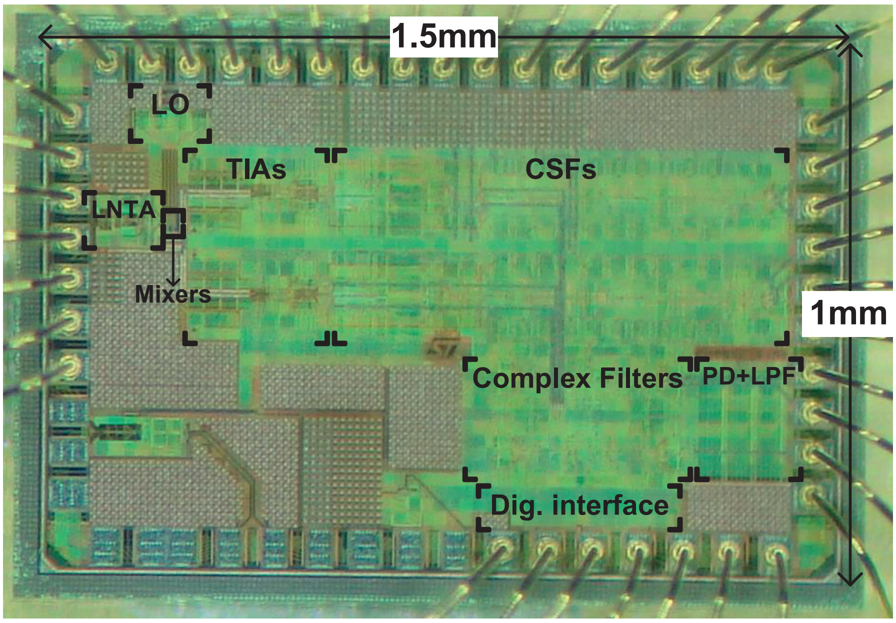


Figure 5.4: Die micrograph of the spectrum sensing receiver front-end.

phase enhanced compensation technique proposed in [1]. The OTA linearity is enhanced by using push-pull stages, and added to that a linearization scheme is also proposed, which improves the overall linearity of the receiver front-end both in-band and at the band edge. The out-of-band linearity is limited by the LNTA.

The receiver front-end was implemented in 65nm CMOS technology, seen in Fig. 5.4. Measurements of the receiver front-end showed an NF of 2.5dB using noise canceling in the LNTA, and the linearized OTAs provided an IIP3 improvement of up to 6.5dB in-band and 11dB at the filter band edge. Thanks to the high speed OTAs the spectrum sensor could detect blocker levels in 22 frequency bins of 9MHz each between -100MHz and 100MHz. The system consumed between 36.6mA and 57.6mA from a 1.2V supply.

EVM measurements of the receiver front-end with LTE modulated signals showed that information about the frequency and amplitude of the blockers is necessary to be able to tune the receiver chain for optimal performance.

To summarize, a receiver front-end with third order CSF and fully integrated spectrum sensing has been designed and measured. It has low NF thanks to a differential noise canceling LNTA, and a proposed OTA linearization scheme improves its linearity. Furthermore, phase enhanced compensation improves the bandwidth of the base band OTAs, which increases the linearity of the filters at higher frequencies. Parallel banks with large resistors are used to achieve fine tuning of IQ filter phase and amplitude imbalance. The spectrum sensor detects amplitude and frequency of signals up to ±100MHz IF. Measurements with LTE signals show that accurate spectrum sensing is required for finding optimal performance settings.

Scientific Contributions

- A wide-band receiver front-end with noise canceling LNTA, wide-bandwidth third order Chebyshev CSF, and a fully integrated spectrum sensor. The spectrum sensor can detect the amplitude and frequency offset for both in-band and out-of-band signals.
- The OTAs used in the CSF benefit from the phase enhanced compensation proposed in [1] to synthesize a Chebyshev response of more than 50MHz bandwidth at low power consumption. A linearization scheme is also applied to the OTA in closed loop configuration, improving the receiver front-end linearity.
- Highlights new challenges encountered when designing receiver front-ends for LTE-A, especially for CA scenarios. It is found that fast spectrum sensing is needed to be able to tune the different parts of the receiver front-end for optimal operation in different scenarios.

Chapter 6

Future Perspectives

This dissertation has investigated the design of wireless receiver front-ends and building blocks in CMOS technology. The main focus has been techniques to improve the linearity, and to address the increasing demands on dynamic range and bandwidth in new wireless systems. Improvements in the linearity of the RF part were achieved using push-pull stages, and a triode multiplier based linearization technique is also proposed. Enhancements in the base band were achieved by proposing linearization techniques that do not degrade the noise performance, and by improving the closed loop bandwidth of the OTAs without increasing their power consumption.

With phase enhanced compensation technique, the speed of the OTAs is improved compared to basic techniques like Miller compensation. Perhaps a more interesting comparison would be to the more advanced compensation techniques based on feed forward. OTAs with similar performance should then be designed and their power consumption compared. To further improve the performance, incorporating feed forward together with phase enhanced compensation appears to be an attractive solution.

The proposed triode multiplier linearization technique has proven to be both robust and wide-band. Extending the technique to cancel also higher order nonlinearities thus has the potential to greatly improve the performance of the system. This could be achieved by properly weighting the higher order terms and directly subtracting them from the output signal. A successful attempt was published by Keehr *et al* [63, 79], however, the generated distortion products need to be digitized, and adaptive signal processing is used to compensate for the path delay. A triode multiplier based higher order distortion generator is fast and would thus not need this, and the subtraction can be performed in the analog domain. Eliminating the need for digitization minimizes the power consumption overhead.

The spectrum sensing receiver front-end highlights the importance not only of blockers presence detection, but also of their power and frequency. It is also shown that different actions are required for not so different blocker scenarios. This is especially the case when the blocker frequency is neither considered in-band nor out-of-band, but rather in between. Since the channel bandwidths increase in advanced communication standards, but the blocker frequency offsets are not necessarily scaled, this scenario will become frequent. In CA blockers in-band (in-gap) are also introduced. A receiver front-end that does not adaptively tune different parts in the chain will then become very expensive in nearly all aspects. There is still room for current consumption reduction in the base band of the spectrum sensing receiver front-end, however, by reducing current for reduced channel bandwidths. New algorithms should also be developed to efficiently use the data from the spectrum sensor and quickly tune the front-end for optimal performance. A closed loop configuration with a full receiver front-end chain and an adaptive tuning algorithm would provide more insights on practical system implementation aspects, as well as an increased understanding of system performance and limitations.

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Paper I

Paper I

A Compensation Technique for Two-Stage Differential OTAs

Mohammed Abdulaziz, Markus Törmänen, Henrik Sjöland, “A Compensation Technique for Two-Stage Differential OTAs,” © 2014 IEEE, reprinted from *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 61, No. 8, pp. 594-598, 2014.

A Compensation Technique for Two-Stage Differential OTAs

Mohammed Abdulaziz, *Student Member, IEEE*, Markus Törmänen, *Senior Member, IEEE*, and Henrik Sjöland, *Senior Member, IEEE*

***Abstract*—In this brief, a frequency compensation method for operational transconductance amplifiers is proposed, which poses no power overhead compared to Miller compensation, while improving the 3-dB bandwidth, the unity gain frequency, and the slew rate. The technique employees positive feedback to introduce an extra left half plane zero to cancel a pole. The phase margin shows good robustness against process and temperature variations. The proposed technique poses no design constraints on the transconductance or capacitor values, which makes it attractive for low-power applications with low area overhead.**

***Index Terms*—Active filter, CMOS technology, low-pass filter, low-power electronics, operational amplifier, radio frequency receivers.**

I. Introduction

Wireless receivers use operational transconductance amplifiers (OTAs) extensively in the base band circuitry such as channel select filters (CSF) and analog to digital converters (ADCs). New communication standards offer higher data rates, resulting in increased channel bandwidth, which increases the bandwidth requirements of the OTAs. Since OTA-based designs are based on feedback, high DC gain is also required to secure enough loop gain.

OTAs with high DC gain can be designed by cascading several amplifying stages or by stacking transistors (cascoding). The second option is less attractive in modern CMOS technologies due to the reduced supply, and cascading just two amplifying stages provides enough gain for mobile receiver applications. Although cascading stages solves the problem, the resulting OTA has an insufficient phase margin. As this can result in unstable operation, the OTA must be compensated.

Various compensation techniques that alter the frequency response and stability properties of the OTA exist. The focus of this brief is on the widely used Miller compensation (also called pole splitting). The Miller compensation technique is based on reducing the first pole's frequency and increasing the frequency of the second, at the cost of reduced 3-dB bandwidth ($\mathrm{BW}_{3\,\mathrm{dB}}$) and gain bandwidth product (GBP). This is in contrast to the needs of more wide band OTAs for use in wireless receivers. In this brief, an enhanced phase compensation technique is therefore introduced, which achieves the required phase margin while having $\mathrm{BW}_{3\,\mathrm{dB}}$ and GBP only lightly affected compared to the OTA before compensation. This is achieved by introducing two zeros in the left half plane (LHP) that can be tuned to cancel the effect of two poles.

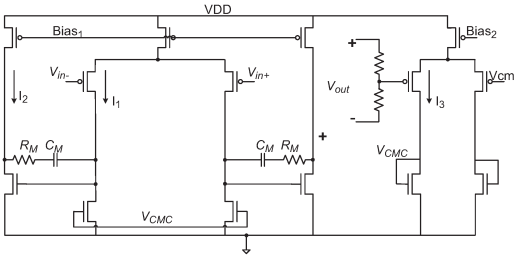

Fig. 1. Schematic of the OTA with Miller compensation.

The robustness of the technique is assessed by simulating active and passive device mismatches, as well as process and temperature variations in a 65-nm CMOS implementation. Robustness to load variation is also important, since the capacitor load can vary significantly when the OTA is used, e.g., in a base band circuit with reconfigurable bandwidth. To prove the effectiveness of the phase compensation in a real implementation a fifth order LTE CSF with reconfigurable bandwidth was fabricated and measured successfully [1].

In extension to [1] a detailed description and derivation of the mathematical model of the OTA using the proposed compensation technique with more robustness simulations is presented. This includes Monte-Carlo simulations with process and temperature simulations and load variation. The improvement to slew rate of the OTA is also presented in detail and simulation results are shown.

An introduction to conventional Miller compensation and a detailed description of the proposed enhanced method is presented in Section II. In Section III comparison with previous compensation techniques is presented. Finally, the conclusion is drawn in Section IV.

II. Amplifier Compensation

A. Miller Compensation

A conventional two-stage differential OTA is shown in Fig. 1, where the $R_M C_M$ links perform the Miller compensation. The small signal half circuit model for differential signals is found in many textbooks (e.g., [2]), if C_{par1} is the lumped parasitic

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Manuscript received April 10, 2014; revised May 14, 2014; accepted May 26, 2014. Date of publication May 30, 2014; date of current version August 4, 2014. The authors would like to thank the Swedish Foundation for Strategic Research (SSF) for funding the Digitally-Assisted Radio Evolution project, and ST-Microelectronics for fabrication of 65-nm CMOS circuits. This brief was recommended by Associate Editor E. Tlelo-Cuautle.

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Digital Object Identifier 10.1109/TCSII.2014.2327475

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capacitance at the input of the second stage, r_{o1} and r_{o2} the output resistances of the first and the second stage, respectively, g_{m1} and g_{m2} the transconductances of the first and second stage, and C_L the load. Then approximate expressions for the poles and zeros are shown as [2]

$$Z_{M1} \approx \left(\left(g_{m2}^{-1} - R_M\right) C_M\right)^{-1} \tag{1}$$

$$P_{M1} \approx -(g_{m2} r_{o2} r_{o1} C_M)^{-1} \tag{2}$$

$$P_{M2} \approx -g_{m2} \cdot C_L^{-1} \tag{3}$$

$$P_{M3} \approx -(C_{par1} R_M)^{-1}. \tag{4}$$

The first pole (P_{M1}) is at low frequency, which sets the $\mathrm{BW}_{3\,\mathrm{dB}}$. The frequency of the zero (Z_{M1}) can be tuned to cancel the second pole (P_{M2}) in the case of small and fixed load C_L. There is, however, a limitation in achievable phase margin improvement, since increasing R_M not only tunes the frequency of (Z_{M1}) but also reduces that of the third pole (P_{M3}). When the load C_L is not fixed, for instance in filter with programmable bandwidths and multi-mode ADCs, Miller compensation is configured to compensate for the highest load since that represents the worst case. This unfortunately reduces the maximum achievable bandwidth since larger load requires larger compensation capacitors. Another shortcoming is that Miller compensation is sensitive to process spread. For instance, in the Fast–Slow (FS) process corner, where the NMOS devices are fast and PMOS are slow, the frequency of the first pole (P_{M1}) increases while that of the second pole (P_{M2}) decreases, which results in reduced phase margin and may in the worst case lead to instability.

B. Enhanced Phase Compensation

It is evident that Miller (pole splitting) compensation achieves improved phase at the cost of significantly reduced $\mathrm{BW}_{3\,\mathrm{dB}}$ and GBP. Successful improvements in the $\mathrm{BW}_{3\,\mathrm{dB}}$ have been reported. However, GBP is not improved and the phase margin gets reduced as the poles become complex conjugate [3], [4].

In [4] positive feedback using a capacitor link proved useful in increasing the $\mathrm{BW}_{3\,\mathrm{dB}}$. Based on that, in this work we propose a phase-enhancement technique, shown in Fig. 2, where two zeros are introduced by using both negative and positive feedback resistor-capacitor links. At the same time a fourth pole, located above the transition frequency of the OTA, is introduced by the positive feedback.

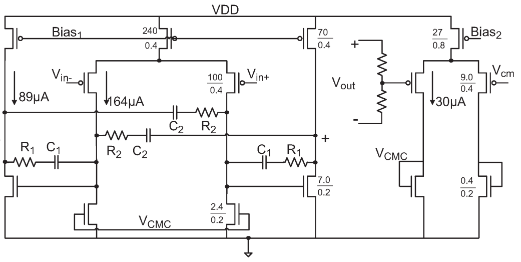


Fig. 2. Schematic of the OTA with enhanced phase compensation.

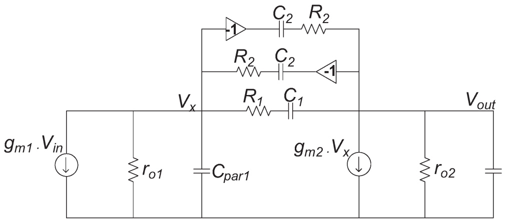


Fig. 3. Half circuit small signal model of the OTA with enhanced phase compensation.

The positive feedback RC-links are cross-coupled, which calls for care when using a half circuit model. Buffers with a gain of -1 are used to model signals coming from and going to opposite (180° phase shifted) half of the amplifier (see Fig. 3). The system transfer function is calculated based on this model, resulting in (5)–(8), shown at the bottom of the page. It is easily seen in Fig. 3 that the DC gain of the OTA is unchanged, since at DC the capacitors in the RC-links will represent open circuits. There are two left half-plane zeros that are mainly dependent on the values of the passive components and, depending on the OTA requirements, the values of these components can be chosen.

One recommended approach will result in high $\mathrm{BW}_{3\,\mathrm{dB}}$ and GBP is to choose equal capacitor sizes, i.e., $C_1 = C_2 = C$. The value of C should be chosen to be as small as possible. Choosing $C_1 = C_2$ removes the term $g_{m2} r_{o1} r_{o2}$ from (8), resulting in direct improvement of the $\mathrm{BW}_{3\,\mathrm{dB}}$. The values of R_1 and R_2 are chosen close enough to assume the term $g_{m2} r_{o1} r_{o2} C_1 C_2 (R_2 - R_1)$ in (7) negligible. By further

$$\frac{V_{out}}{V_{in}} = g_{m1} g_{m2} r_{o1} r_{o2} \frac{\left(g_{m2}^{-1}(C_1C_2R_1 - C_1C_2R_2) + R_1R_2C_1C_2\right) s^2 + \left(g_{m2}^{-1}(C_2 - C_1\right) + C_1R_1 + C_2R_2)s + 1}{(C_{par1}C_LC_1C_2r_{o1}r_{o2}R_1R_2)s^4 + D_1s^3 + D_2s^2 + D_3s + 1} \tag{5}$$

$$\begin{aligned} D_1 = {} & C_{par1}C_LC_1r_{o1}r_{o2}R_1 + C_{par1}C_LC_2r_{o1}r_{o2}R_2 + C_{par1}C_1C_2r_{o1}r_{o2}R_1 + C_LC_1C_2r_{o1}r_{o2}R_1 \\ & + C_{par1}C_1C_2r_{o1}r_{o2}R_2 + C_LC_1C_2r_{o1}r_{o2}R_2 + C_{par1}C_1C_2r_{o2}R_1R_2 + C_LC_1C_2r_{o2}R_1R_2 \end{aligned} \tag{6}$$

$$\begin{aligned} D_2 = {} & C_{par1}C_Lr_{o1}r_{o2} + C_{par1}C_1r_{o1}r_{o2} + C_LC_1r_{o1}r_{o2} + C_{par1}C_2r_{o1}r_{o2} + C_LC_2r_{o1}r_{o2} + C_{par1}C_1r_{o1}R_1 \\ & + C_LC_1r_{o2}R_1 + 4C_1C_2r_{o1}r_{o2} + C_{par1}C_2r_{o1}R_2 + C_LC_2r_{o2}R_2 + C_1C_2r_{o1}R_1 + C_1C_2r_{o2}R_1 \\ & + C_1C_2r_{o1}R_2 + C_1C_2r_{o2}R_2 + C_1C_2R_1R_2 + C_1C_2r_{o1}r_{o2}R_2g_{m2} - C_1C_2r_{o1}r_{o2}R_1g_{m2} \end{aligned} \tag{7}$$

$$D_3 = C_{par1}r_{o1} + C_Lr_{o2} + C_1r_{o1} + C_1r_{o2} + C_2r_{o1} + C_2r_{o2} + C_1R_1 + C_2R_2 + C_1g_{m2}r_{o1}r_{o2} - C_2g_{m2}r_{o1}r_{o2} \tag{8}$$

assuming that C_{par1} is negligible, very simplified equations for the zeros and poles can be derived as

$$Z_1 \approx -\frac{1}{C(R_1+R_2)} \tag{9}$$

$$Z_2 \approx -\frac{R_1+R_2}{C(R_1R_2)} \tag{10}$$

$$P_1 \approx -\frac{1}{(C_L+2C)r_{o2}+2Cr_{o1}} \tag{11}$$

$$P_2 \approx -\frac{(C_L+2C)r_{o2}+2Cr_{o1}}{2C_LCr_{o1}r_{o2}+C^2(4r_{o1}r_{o2})} \tag{12}$$

$$P_3 \approx -\frac{2C_L+4C}{C_LC(R_1+R_2)} \tag{13}$$

$$P_4 \approx -\frac{R_1+R_2}{C_{par1}R_1R_2}. \tag{14}$$

The first pole (P_1) is at high frequency compared to the pole-splitting compensation (2). Looking at (9), (10), and (13) we see that the frequencies of Z_1, Z_2, and P_3 are set by passive components and hence move in the same direction with process variation. The approximations are used assuming C_L and $C \gg C_{par1}$.

The pole-zero cancellation can be achieved easily since the frequencies of the zeros are fully determined by the values of the passive components [(9) and (10)]. The second pole (P_2) can be canceled by tuning the first zero (Z_1) with the sum of R_1 and R_2. The second zero (Z_2) can then be tuned to the frequency of the third pole, and we are left with the fourth pole that is located high in frequency since C_{par1} is small.

In more detail the compensation process can be done by first choosing a value for the compensation capacitors C. The value of C should be larger than C_{par1}. The sum $R_1 + R_2$ can then be calculated using that Z_1 should equal P_2, which yields (15). The second step is to find the ratio between R_1 and R_2 i.e., $R_2 = \alpha R_1$. Equating the third pole (P_3) with the second zero (Z_2) results in the relation given by (16) where α can be easily calculated as

$$R_1 + R_2 \approx \frac{2C_Lr_{o1}r_{o2}+4Cr_{o1}r_{o2}}{C_Lr_{o2}+2C(r_{o2}+r_{o1})} \tag{15}$$

$$\alpha/(1+\alpha)^2 \approx \frac{C_L}{2C_L+4C}. \tag{16}$$

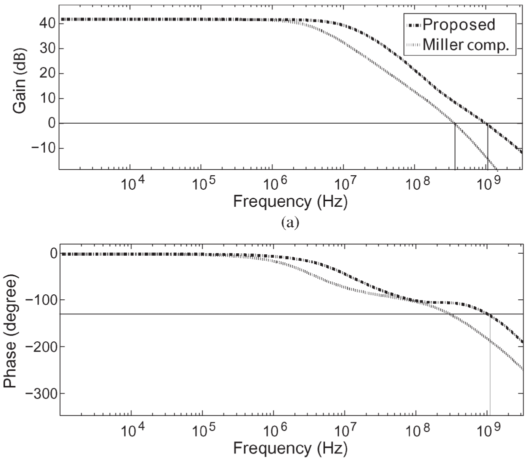
To have a feeling of the improvement we get in the frequency response, the $\mathrm{BW}_{3\,\mathrm{dB}}$ is compared by simply dividing the first pole frequency in the enhanced phase compensation by that of the first pole in the Miller compensated case (17). It is seen that the $\mathrm{BW}_{3\,\mathrm{dB}}$ improvement is large when C_L is small, as follows:

$$\mathrm{BW}_{ratio} \approx \frac{(C_L+C_M)r_{o2}+g_{m2}r_{o1}r_{o2}C_M}{(C_L+2C)r_{o2}+2Cr_{o1}+C(R_1+R_2)}. \tag{17}$$

Assuming compensation for the same phase margin, when the load C_L is variable and relatively small, the improvement in GBP when compared to Miller compensation is given in

$$\mathrm{GBP}_{ratio} \approx \frac{(R_1+R_2)C_L}{C_{par1}R_1R_2g_{m2}}. \tag{18}$$

For large loads (C_L) the dominant pole frequency decreases while the second and third pole frequencies (P2,P3) are less affected. This results in increased system stability at increased loads, as will be shown in Section II-C.



(a)

(b)

Fig. 4. Frequency response for the Miller compensation and the proposed compensation: (a) Gain and bandwidth and (b) Phase margin.

TABLE I
PERFORMANCES COMPARISON OF THE OTA ($C_L = 0.5$ pF)

	Miller Comp.	**Phase Enhancement**
$\mathrm{BW}_{3\mathrm{dB}}$ (MHz)	3.67	11.83
GBP (MHz)	378	1050
Phase Margin (°)	43.2	50.7
Power (mW)	0.68	0.68
Area (μm×μm)	53×60	54×60

C. *Amplifier Simulation*

The OTA used is optimized for noise with input transistors of size 100/0.4 and $g_{m1} = 2.8$ mS to reduce the noise. The output stage transconductance g_{m2} is only 1.4 mS with the output transistors of size 7/0.2, since bandwidth is less dependent on g_{m2} than for Miller compensation. The output resistance of the stages becomes $r_{o1} = 4.5$ kΩ and $r_{o2} \approx 10$ kΩ. Following the design procedure for the passive component values results in capacitance values of $C_1 = C_2 = C = 0.2$ pF, and resistances $R_1 =$ 3 kΩ and $R_2 = 3.5$ kΩ. The values used for the Miller compensated version are $R_M = 1.2$ kΩ and $C_M = 400$ fF, chosen based on the recommendations in [5]. The load capacitance C_L is 0.5 pF. A standard 65-nm CMOS process with silicided poly resistors and MIM capacitors was used to simulate the OTAs. The spectre simulator was used with BSIM4 transistor models.

1) Frequency Response: Simulations of the proposed compensation in comparison to the conventional Miller compensation show significant improvement in both the $\mathrm{BW}_{3\,\mathrm{dB}}$ and GBP, as shown in Fig. 4. Table I compares the simulated frequency properties of the OTA when Miller compensation is used and with the proposed compensation. The robustness to load capacitance variation can be seen in Fig. 5, where the load is varied from the nominal 0.5 pF to 8 pF while the compensation resistor capacitor values are kept constant for both cases. When using the proposed compensation technique the phase margin improves with the increasing load, while for the conventional Miller compensation case the phase margin instead decreases. Both techniques are designed to provide the same phase margin of about 50° at 0.5 pF load, at 1 pF and

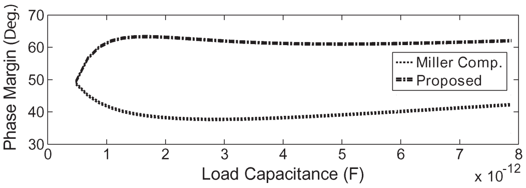


Fig. 5. OTA phase margin versus load capacitance for enhanced phase and Miller compensation.

TABLE II
CORNER SIMULATIONS OF THE OTA WITH ENHANCED PHASE TECHNIQUE ($C_L = 0.5$ pF)

Corner	FF	TT	SS	FS
$\mathrm{BW}_{3\mathrm{dB}}$ (MHz)	15.22	11.83	9.026	8.4
GBP (MHz)	1302	1050	703	530
Phase Margin (°)	52.8	50.7	53.5	63.5

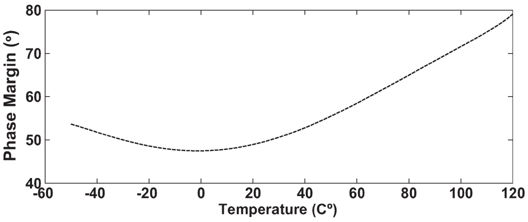


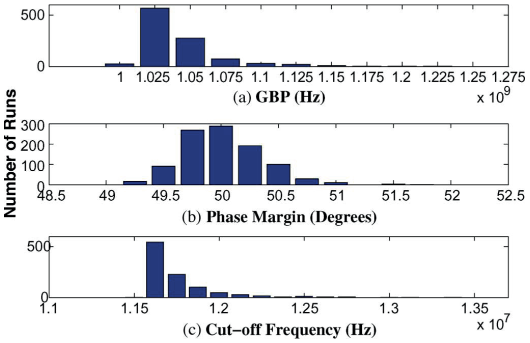
Fig. 6. OTA phase margin versus temperature with enhanced phase compensation.

above the phase margin differs by about 20° in favor of the proposed technique.

2) Compensation Robustness: To test the robustness to process variation different corners Typical–Typical (TT), Fast–Fast (FF), Slow–Slow (SS) and Fast–Slow (FS) were simulated, and the enhanced phase compensation shows good performance (see Table II). Temperature stability is another key measure of system robustness. The OTA was thus simulated with temperatures ranging from -50 °C to 120 °C (see Fig. 6). As can be seen the phase margin is actually improved at the temperature extremes. At high temperatures the frequency of the second pole in (P_2) increases as r_o of the MOS devices decreases. The gain also decreases which improves the phase margin. At low temperatures the second pole (P_2) decreases in frequency as r_o increases. Looking at Fig. 6, a very small decrease in the phase margin is due to the decrease in g_{ds} which results in increasing the gain. However, the decrease in g_{ds} is still in range for the pole-zero cancellation and so the phase margin remains unaffected.

To make the investigation complete, active and passive device mismatch must also be simulated to see if the pole-zero cancellation still holds. Monte-Carlo mismatch simulations were therefore performed in 1000 runs (see Fig. 7). It can be seen that for 95% of the runs the phase margin remains within $\pm 1^\circ$ of the average value. The values of R_1 and R_2 were changed to the maximum and minimum values of different corners and the same behavior was still achieved.

The enhanced phase technique introduces zeros to achieve pole cancellation, which makes it easier to increase the number of amplifying stages. The compensation can then be performed by first compensating the first two stages, and then compensating one stage further at a time using the enhanced phase technique, resulting in a structure resembling nested Miller [2].



(a) **GBP (Hz)**

(b) **Phase Margin (Degrees)**

(c) **Cut−off Frequency (Hz)**

Fig. 7. Mismatch simulation for (a) GBP variation (b) Phase margin and (c) $\mathrm{BW}_{3\,\mathrm{dB}}$.

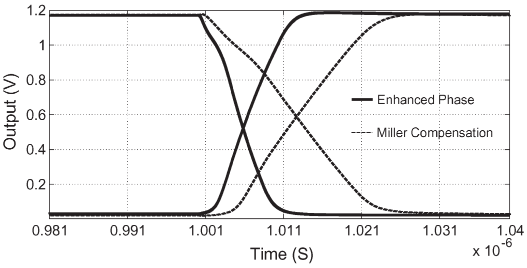


Fig. 8. Simulation of the positive and negative slew rate.

3) Slew Rate: Another important aspect is the slew rate performance of the OTA. In comparison to the Miller compensation, the proposed technique can improve the slew rate performance considerably. This is due to the fact that in the enhanced phase compensation the RC links conduct current with opposite phases. This effectively reduces the current that the input stage must supply to charge/discharge the compensation capacitors. In the case of equal compensation capacitor sizes, the slewing effect of the compensation capacitors is canceled.

For the OTA shown in Figs. 1 and 2 the bias current of the input stage is high since the OTA is optimized for low noise. To get more insight into the slew rate behavior the input stage current was therefore decreased and the output stage current was increased to have optimal slew rate as described in [5]. The input and output currents (I_1, I_2) are related by (19) [5].

$$I_2 \approx 2I_1(1 + C_L/C_M). \tag{19}$$

The capacitor values are given as $C_M = 2C = 0.6$ pF and $C_L = 1$ pF, which means that the output stage sees the same capacitance in both cases. The positive slew rate (SR^+) and the negative slow rate (SR^-) are shown in Fig. 8. The simulation results can also be seen in Table III. The improvement in both (SR^+) and (SR^-) is about two times thanks to the proposed compensation.

The two Figures of Merit (FoM) introduced in [6], [7] are given by $FoM_{SR} = SR_{diff} \cdot C_L/P_{diss}$ and $FoM_{Frequency} = GBP \cdot C_L/P_{diss}$, where GBP is in MHz, SR_{diff} differential slew rate in V/μS, C_L in pF, and P_{diss} in mW. It is clear

TABLE III
SLEW RATE SIMULATIONS OF THE OTA ($C_L = 1$ pF)

Compensation	Miller	Enhanced Phase
SR_{diff} (V/μs)	118.9	254
SR^+ (V/μs)	63.2	118.8
SR^- (V/μs)	53.6	128.9

that the FoM$_{SR}$ and FoM$_{Frequency}$ are proportional to SR_{diff} and GBP. The technique will thus improve both figures of merit, which can be used to achieve less power consumption on system level.

The simulations show that the enhanced phase compensation technique is useful in OTA compensation as it improves the frequency response parameters without any significant overhead or other compromise. The OTA performance is robust to process and temperature variations. Moreover, it is shown that OTA stability improves at large capacitive loads. Compared to Miller compensation, the slew rate of the OTA is also improved considerably as the effect of the compensation capacitors is canceled.

III. OTHER COMPENSATION TECHNIQUES

Since the proposed technique is an extension to the basic Miller compensation technique, the advantages of using enhanced phase compensation instead of Miller are presented in detail. However, other effective compensation techniques have been proposed to improve the speed of the OTA and overcome unwanted compensation effects such as the right half plane (RHP) zero, and large compensation capacitors. To mention a few, the no-capacitor feedforward (NCFF) technique [8] eliminates the Miller capacitances by feeding the signal forward to create a LHP zero for each feedforward path. Miller capacitance together with feedforward stages are used in the single Miller capacitor compensation technique (SMC) [9] to introduce LHP zeros and control the dominant pole location. In dual loop parallel compensation (DLPC) [10] fast signal paths are used to replace the feedback capacitors resulting in increased bandwidth. A compensation technique for large capacitive loads that uses passive components only is introduced in [11]. The effectiveness of the mentioned techniques, however, comes at the expense of complexity and power consumption overhead.

The advantage of using enhanced phase compensation is that, unlike other compensation techniques, there are no restrictions on the transconductance values (g_m). This makes the technique attractive in low-power applications and it also gives the designer one degree more of freedom. Added to that, the enhanced phase technique does not introduce any power overhead and can also easily be extended to more than two amplifying stages. The proposed technique is suitable for OTA's driving large loads since the dominant pole is

$$P_1 \approx \frac{-1}{C_L r_o} \tag{20}$$

for very large C_L.

A comparison with previously published works is shown in Table IV. It can be seen that although the OTA is designed to drive small loads, which results in smaller FoM, the performance of the proposed technique is still comparable to that of the previously published works designed to drive larger loads.

TABLE IV
COMPARISON WITH OTHER WORKS

Parameter	NCFF **[8]**	RFC **[12]**	FF **[13]**	GBCA **[14]**	SMC **[9]**	**This Work**
Techn. (nm)	500	180	180	180	500	**65**
Supply (V)	±1.25	1.2	1.8	1.8	2	**1.2**
Power (mW)	15.8	1.44	0.2	3.8	0.38	**0.75**
GBP (MHz)	300	134.2	1800	660	4.6	**780**
$\mathbf{C_L}$ (pF)	12	5.6	0.045	1	120	**1**
SR$(^{+,-})(\frac{\mathrm{V}}{\mu\mathrm{S}})$	NA	94.1	NA	800	3.28, 1.31	**119,** **129**
FoM$_{\mathbf{GBP}}(\frac{\mathbf{MHz \cdot pF}}{\mathbf{mW}})$	228	522	225	174	1453	**1040**
FoM$_{\mathbf{SR}}(\frac{\mathbf{(V/\mu S) \cdot pF}}{\mathbf{mW}})$	NA	366	NA	211	821	**344***

*differentially

IV. CONCLUSION

A new two-stage OTA compensation technique that improves the bandwidth of the amplifier while maintaining the required phase margin is presented. The compensation technique provides an improved BW$_{3\,\mathrm{dB}}$ and GBP compared to conventional Miller compensation. In addition, the proposed technique is robust against process and temperature variations. It can also be used to efficiently compensate OTAs with more than two amplifying stages, and OTAs with very large loads.

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Paper II

Paper II

A 3.4mW 65nm CMOS 5th Order Programmable Active-RC Channel Select Filter for LTE Receivers

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Mohammed Abdulaziz, Anders Nejdel, Markus Törmänen, Henrik Sjöland, “A 3.4mW 65nm CMOS 5^{th} Order Programmable Active-RC Channel Select Filter for LTE Receivers ,” © 2013 IEEE, reprinted from *Radio Frequency Integrated Circuits Symposium (RFIC)*, Seattle, USA, June 2013, pp. 217–220.

RMO4A-2

A 3.4mW 65nm CMOS 5^{th} Order Programmable Active-RC Channel Select Filter for LTE Receivers

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***Abstract*—In this work a low power 5^{th} order chebyshev active-RC low pass filter that meets Rel-8 LTE receiver requirements has been designed with programmable bandwidth and overshoot. Designed for a homodyne LTE receiver, filter bandwidths from 700kHz to 10MHz are supported. The bandwidth of the operational amplifiers is improved using a novel phase enhancement technique. The filter was implemented in 65nm CMOS technology with a core area of 0.29mm^2. Its total current consumption is 2.83mA from a 1.2V supply. The measured input referred noise is 39nV/$\sqrt{\mathrm{Hz}}$, the in-band IIP3 is 21.5dBm, at the band-edge the IIP3 is 20.7dBm, the out-of-band IIP3 is 20.6dBm, and the compression point is 0dBm.**

***Index Terms*—Active filters, low pass filters, low power electronics, CMOS technology, Operational Amplifiers.**

I. INTRODUCTION

Wireless communication standards such as LTE with high data rates require receivers with wide band channel select filters. Moreover, these filters must have high dynamic range to be able to reject strong interference while receiving weak signals. It is also required that different filter parameters like the bandwidth can be tuned digitally. Architectures of choice for such high performance filters for wireless applications is usually $\mathrm{g_m}$-C or active-RC.

Although $\mathrm{g_m}$-C filters have the advantage of high bandwidth and low noise, they suffer from poor linearity due to open loop operation, nonetheless they are superior for high frequency applications [1]. In contrast, active-RC filters have high dynamic range due to closed loop operation, but can not operate at as high frequencies as their $\mathrm{g_m}$-C counterparts. The reason is that the operational amplifiers (OPAMPs) must have a gain bandwidth product (GBP) that by far exceeds the filter cut-off frequency. They must also provide sufficient low frequency loop gain, and the demanding requirements result in high OPAMP power consumption [2].

In this paper a low power 5^{th} order low pass active-RC filter is presented. The power dissipated by the filter is reduced by using a new phase enhancement technique that improves both the 3-dB bandwidth and the GBP while controlling the phase margin. Also the common mode feedback (CMFB) stability is improved. The filter supports all Rel-8 LTE bands [3] with ± 40% of tuning range to counter process variations.

This paper will start by presenting the OPAMP architecture and compensation in Section II, and then the filter architecture in Section III. This is followed by measurement results and comparison with State-of-The-Art designs in Section IV, and conclusions in Section V.

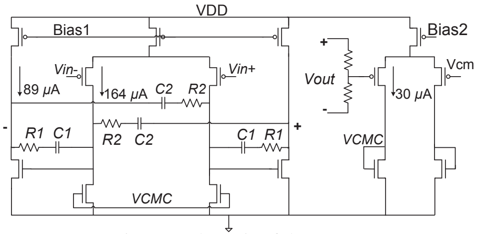

Fig. 1. Schematic of the OPAMP.

II. THE AMPLIFIER DESIGN

Representing the active part, the OPAMP is the main building block of the filter. We use the well-known differential two stage topology with CMFB, Fig. 1. The OPAMP consumes 0.56mA from a 1.2V supply. Of this 0.328mA is used in the input stage to improve the noise performance.

Using conventional multi-stage Miller pole splitting compensation, the 3-dB bandwidth and GBP get heavily decreased in order to improve the phase margin. Compensation improvement attempts have been reported successful in improving the 3-dB bandwidth, however, GBP is not improved and the phase margin gets reduced as the poles become complex conjugate[4], [5].

In this work we propose a phase enhancement technique (see Fig. 1), where two zeros are introduced in the numerator from the negative and positive feedback resistor-capacitor links. At the same time a forth pole that is located above the transition frequency of the OPAMP is introduced by the positive feedback.

The main idea is to use the two zeros to cancel two of the dominant poles. This leaves one dominant pole pushed high enough in frequency and another one that is outside the range of operation. Ultimately we get a two-stage single pole OPAMP, and as a result both the 3-dB bandwidth and the GBP increase significantly while having the required phase margin.

The small signal half circuit of the fully differential topology is shown in Fig. 2, where C_{par1} is the lumped parasitic capacitance at the input of the second stage, r_{o1} and r_{o2} the output resistances of the first and the second stage, respectively, g_m is the transconductance of the second stage, and C_L is the load.

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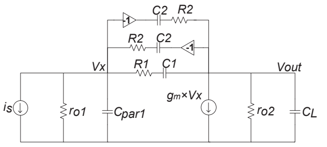
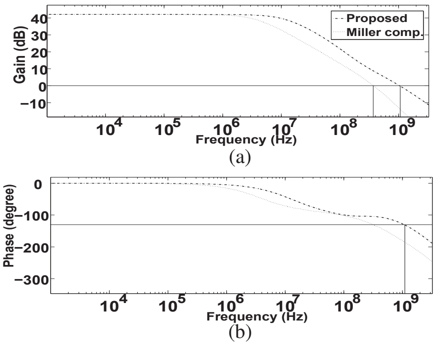


Fig. 2. A conceptual small signal model of the OPAMP.



(a)

(b)

Fig. 3. Frequency response for the Miller and the proposed compensation (a) gain and bandwidth and (b) Phase margin.

It is easy to see in Fig. 2 that the DC gain of the OPAMP is unchanged. The values of the passive components can be chosen in different ways. A recommended approach is to choose equal capacitor sizes $C_1 = C_2 = C$ to make the term $g_m r_{o1} r_{o2}$ disappear from the equation of the first pole. The capacitor value should be small to improve the slew rate and frequency performance and to minimize the area. As for the resistors we choose two values close enough to assume the term $(R_1 - R_2) g_m r_{o1} r_{o2}$ negligible in the second pole and push the pole higher in frequency. Under the mentioned assumptions very simplified equations for the zeros and poles of the OPAMP are shown in (1) to (6).

Looking at (3) we see that the first pole is located high in frequency compared to the conventional Miller compensation. The second pole (4) can be canceled by tuning the first zero (1) with R_1 and R_2. The second zero (2) can be equated with the third pole, and we are left with the forth pole that is located high in frequency since C_{par1} is small.

It must emphasized that the equations (1) to (6) are approximations and that more detailed equations must be used to find more accurate pole and zero positions. Unfortunately these equations are complicated and due to the limited space available the full equations can not be presented in this paper.

TABLE I
Performance of different OPAMP compensation techniques

	Miller Comp.	**Phase Enhancement**
3-dB Bandwidth (MHz)	3.67	11.83
GBP (MHz)	378	1050
Phase Margin (°)	43.2	50.7

TABLE II
Corner simulations of the OPAMP with phase enhancement

	FF	**TT**	**SS**	**FS**
3-dB Bandwidth (MHz)	15.22	11.83	9.026	8.4
GBP (MHz)	1302	1050	703	530
Phase Margin (°)	52.8	50.7	53.5	63.5

$$Z_1 \approx \frac{1}{C(R_1 + R_2)} \tag{1}$$

$$Z_2 \approx \frac{R_1 + R_2}{C(R_1 R_2)} \tag{2}$$

$$P_1 \approx \frac{1}{(C_L + 2C)ro2 + 2Cro1} \tag{3}$$

$$P_2 \approx \frac{(C_L + 2C)ro2 + 2Cro1}{2C_L Cro1ro2 + C^2(4ro1ro2)} \tag{4}$$

$$P_3 \approx \frac{2C_L + 4C}{C_L C(R_1 + R_2)} \tag{5}$$

$$P_4 \approx \frac{R_1 + R_2}{C_{par1} R_1 R_2} \tag{6}$$

Simulating the OPAMP using the conventional Miller compensation in comparison to the phase enhancement technique shows an improvement of more than three times in the 3-dB bandwidth and about three times in GBP for the same power consumption, see Table I and Fig. 3. At the same time the phase margin is 7° higher than when using Miller compensation, i.e. the improvement is even larger if we target the same phase margin. Moreover, simulations of different process corners, Fast-Fast (FF), Typical-Typical (TT), Slow-Slow (SS), and Fast-Slow (FS) show that the phase margin is maintained over process variations, Table II. Added to that, changing the temperature by ± 30 °C from room temperature changes the phase margin by no more than ± 5°. The proposed phase enhancement compensation is robust to process and temperature variations, since unlike Miller compensation the pole locations are independent of g_m. The phase margin is mainly determined by the compensation resistor-capacitor links and C_L. In Monte Carlo simulation (1000 runs) the phase margin is varying by just $\pm 1°$ for 95% of the runs, and also simulations of different corners with the values of R1 and R2 set to the maximum and minimum expected values indicate similar robustness. Furthermore, step response simulation of the complete filter at different corners indicates that the filter performance is not affected by the process corner.

It is concluded that the proposed compensation technique improves the overall OPAMP frequency response, and even silicon area, without any significant compromise. It is also very robust to temperature and process variations. All of this has major benefits in filter design, allowing power efficient high dynamic range filters with increased bandwidth to be designed.

III. Filter Design

A 5^{th} order low pass chebyshev filter was implemented to provide sufficient attenuation of out of band interference. The pass band ripple is 1.5dB worst case in the 10MHz bandwidth, below 1dB for the 7.5MHz bandwidth, and less than 0.4dB for the other bandwidths in use. The architecture of the filter is leapfrog (Fig. 4) which simulates the I-V relations of an LC filter prototype. The leapfrog architecture was chosen because it is robust against component spread (mismatch). It is also easy to tune parameters like filter bandwidth and gain as they have a linear relation to the resistor and capacitor values [2].

The filter supports all Rel-8 LTE bandwidths, namely, 10MHz, 7.5MHz, 5MHz, 2.5MHz, 1.5MHz and 0.7MHz. (The RF bandwidths are two times the filter bandwidths in a homodyne receiver). The switching between bandwidths is performed using a bank of switched capacitors. To account for process, voltage and temperature variations, 5-bit unit cell based resistor banks were used, providing a tuning range of ± 40%.

All of the capacitor and resistor bank switches were located at the input (virtual ground) side of the OPAMP. The associated parasitic capacitance reduces the frequency of the pole of the input node, decreasing the phase margin of the system, resulting in overshoot at the band edge [6]. Smaller switches would solve the problem, but the linearity performance would be severely harmed. To address the overshoot problem, the technique introduced in [6] (Q-Tuning) is instead used here, where a variable resistor bank is used in series with the capacitor bank, see Fig. 4.

The filter has a digital interface to control the operating bandwidth, the bandwidth fine tuning, and also the Q-tuning. This makes it possible to control the filter operation through a digital signal processor (DSP), which becomes more attractive as the technology scales down and DSP implementations become lower and lower in cost.

IV. Measurement Results

A filter prototype was designed and fabricated in 65nm CMOS technology, see chip photo in Fig. 5. The core area is 0.29mm^2, excluding the pads and output buffers. In all measurements the total filter current consumption is 2.83mA from a 1.2V supply.

The measurement setup is shown in Fig. 6, where the baluns (ZFSCJ-2-2) are used to enable usage of single-ended equipment. Low noise external buffers (B1, B2) are used to drive the 50Ω instrument. To drive these external buffers an on-chip OPAMP-based buffer (BUF) is used and its linearity degradation is de-embedded from the measurements.

TABLE III
Comparison with Other Works

Parameter	**[6]**	**[7]**	**[8]**	**This Work**
Technology (nm)	130	90	180	**65**
Filter Type	Cheb.	Butter.	Butter.	**Cheb.**
Area (mm^2)	0.2	0.239	0.23	**0.29**
Order	5^{th}	6^{th}	3^{rd}	$\mathbf{5^{\text{th}}}$
Supply (V)	1.5	1	1.2	**1.2**
Power (mW)	11.25	4.35	11.1	**3.4**
$\mathbf{f_{cutoff}}$ (MHz)	8.9,19.7	8.1,13.5	0.5,20	**0.44,14**
IIP3 (dBm)in- ,out-of-band	18.3 ,-	22.1 ,18.9	19 ,13	**21.5** **,20.6**
Noise (nV/$\sqrt{\text{Hz}}$)	30	75	12	**38.75**
SFDR	55.2	54.4	60.9	**56.8**
FoM (fJ)	0.35	0.268	0.15	**0.100**

The frequency response for each bandwidth is shown in Fig. 7. The losses of the test setup and the output buffers have been de-embedded. The gain variation over bandwidth tuning is about 1dB (approx. from 5.2dB to 4.2dB).

Q-tuning was implemented to control overshoot resulting from the parasitic pole at the input of the OPAMPs or from low temperature operation. Fig. 8 shows the Q-tuning steps which range from high overshoot to the over-compensated state to account for all possible environment conditions.

To estimate the dynamic range a two tone test (1MHz,1.1MHz tones for the in-band and 22.5MHz,40MHz for out-of-band) was performed to measure IIP3. The in-band-IIP3 is found to be 21.5dBm, the out-of-band is 20.6dBm, at the band edge the IIP3 is 20.7dBm and the achieved Compression Point (CP) is 0dBm. The measured average input referred noise floor is just 39nV/$\sqrt{\text{Hz}}$ and the integrated noise from 20Hz to 10MHz is $122\mu\text{V}_{\text{rms}}$. With these measurement results the commonly used Figure of Merit (FoM) shown in (7) can be calculated.

$$FoM = \frac{Power}{Order \cdot SFDR \cdot Bandwidth} \tag{7}$$

Where SFDR is the Spurious Free Dynamic Range and it is given by: $\frac{2}{3}(IIP_3 - P_{noise})$.

The performance summary and comparison with some previous works is shown in Table III. It can be seen that the power consumption is reduced compared to other works. The area is slightly larger, but this work supports much lower cut-off frequencies than the works[7], [6].

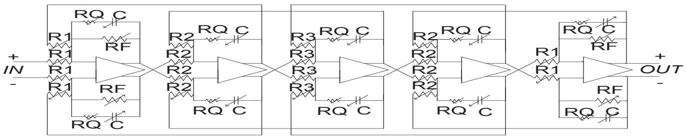
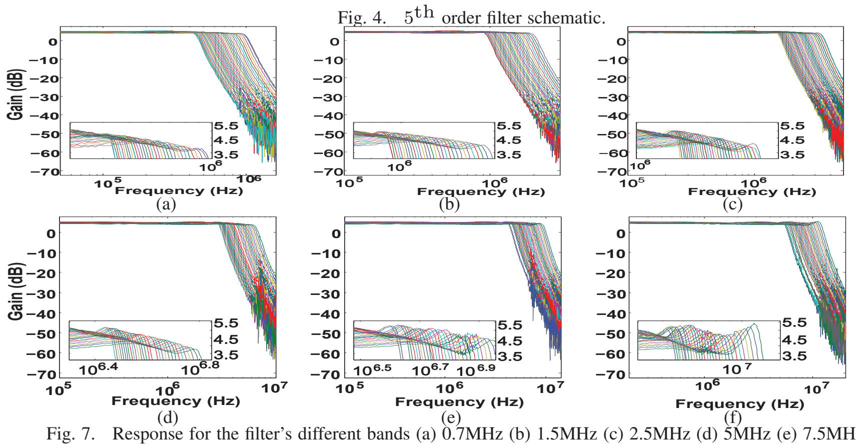


Fig. 4. $5^{\rm th}$ order filter schematic.



(a) (b) (c) (d) (e) (f)

Fig. 7. Response for the filter's different bands (a) 0.7MHz (b) 1.5MHz (c) 2.5MHz (d) 5MHz (e) 7.5MHz (f) 10MHz

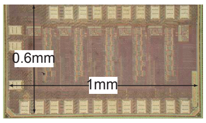


Fig. 5. Chip photo.

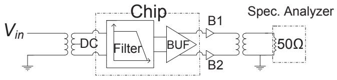


Fig. 6. Measurement setup.

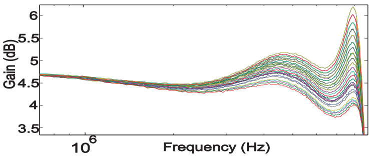


Fig. 8. Q-tuning different steps.

V. CONCLUSION

A low power $5^{\rm th}$ order active-RC filter for Rel-8 LTE receivers has been fabricated in 65nm CMOS and measured. The OPAMP in the filter benefits from a novel compensation technique that significantly improves its performance. Simulations and measurements prove the technique to be power efficient and robust to process and temperature variations. The filter measurement results show high dynamic range combined with wide range bandwidth tuning and Q-tuning to compensate for all possible operation scenarios.

ACKNOWLEDGMENT

The authors would like to thank Swedish Foundation for Strategic Research (SSF) for funding the Digitally-Assisted Radio Evolution (DARE) project, and ST-Microelectronics for fabrication of the chip.

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Paper III

Paper III

A 4^{th} Order Gm-C Filter with 10MHz Bandwidth and 39dBm IIP3 in 65nm CMOS

Mohammed Abdulaziz, Markus Törmänen, Henrik Sjöland, “A 4^{th} Order Gm-C Filter with 10MHz Bandwidth and 39dBm IIP3 in 65nm CMOS,” © 2014 IEEE, reprinted from *Proc. of IEEE ESSCIRC*, Venice, Italy, Sep. 2014, pp. 367–370.

A 4^{th} Order Gm-C Filter with 10MHz Bandwidth and 39dBm IIP3 in 65nm CMOS

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***Abstract*—Gm-C filters suffer from limited dynamic range due to a trade-off between noise and linearity in OTA design. This paper therefore presents a filter with a linearization technique to break this trade-off. This technique is demonstrated by a low power 4^{th} order 10MHz Butterworth Gm-C low pass filter. The filter was implemented in 65nm CMOS technology with a core area of 0.19mm^2 and a total current consumption of 3.5mA from a 1.2V supply. The measured input referred noise is $31\text{nV}/\sqrt{\text{Hz}}$, the maximum in-band IIP3 is 39dBm, the out-of-band IIP3 is 34dBm, and the compression point is 8.2dBm.**

***Keywords*—Active filters, CMOS technology, intermodulation distortion, low pass filters, low power electronics, operational transconductance amplifier.**

I. INTRODUCTION

Active channel select filters are key building blocks in direct-conversion receivers, and steep filters with stringent requirements on dynamic range are needed for cellular standards like LTE, to be able to receive weak signals in the presence of large interference. Two architectures are frequently used to implement such filters, active-RC and Gm-C. Technology scaling of digital CMOS is making operational amplifiers (OPAMPs) requirements increasingly difficult to meet, making Gm-C filters a more attractive choice in terms of power consumption. However, although Gm-C filters consume less current, they suffer from limited dynamic range since their operational transconductance amplifiers (OTAs) are used in open loop configuration, i.e. they are not linearized by feedback.

To improve the dynamic range of the Gm-C filter, linearization techniques can be applied to the OTAs. For this to be effective, however, the negative impact on noise must be limited. The limited voltage headroom in modern CMOS technologies unfortunately makes degeneration less attractive as the noise level is increased significantly. Nonlinearity cancellation approaches are more effective, since the noise performance is much less affected. In this paper we present a 4^{th} order Gm-C filter with a linearization technique proposed in [1] (simulation) that can achieve non-linearity cancellation without any increase of noise level, resulting in filters with high dynamic range and low power consumption.

The proposed OTA is described in detail in Section II. The filter architecture, measurement results and a comparison with state-of-the-art is presented in Section III. Conclusions are drawn in Section IV.

II. THE LINEARIZED OTA

The triode-transistor transconductor uses input transistors operating in the triode region [2]. For long channel devices if the drain-source voltage is kept constant using amplifiers, the output current will be linearly dependent on the input gate voltage [3], [4]. Unfortunately, reduced feature sizes and oxide thickness in new CMOS technologies results in effects like mobility degradation that make the devices nonlinear even when the drain-source voltage is kept constant.

When implemented in new technologies, the triode-transistor transconductor with constant drain-source voltage will thus suffer from limited linearity. The requirement on the amplifiers keeping the drain-source voltages constant are also substantial in terms of gain, bandwidth and noise, resulting in a significant power overhead.

The proposed OTA is a triode-transistor transconductor where the gates of the cascode devices are driven by attenuated signals from the input rather than by operational amplifiers, see schematic including common mode feedback (CMFB) in Fig. 1. Not only does this eliminate the noise and power consumption of the operational amplifiers, but the linearity can also be improved. As explained above even if the drain-source voltage of M_1 is kept perfectly constant with ideal feedback amplifiers, some nonlinearities of M_1 will remain unsuppressed. A more favorable situation is to not keep the drain-source constant, but to introduce a voltage attenuator consisting of capacitors C_1 and C_2, feeding part of the input signal to the gates of M_2. The drain-source voltage of M_1 is then equal to $v_{DS} = V_{DS} + \alpha \cdot v_{in}$, where α is the attenuation from the input to the drain terminal of M_1. When M_1 is operating in the triode region it performs a multiplication, as can be seen in the equation for the output current (1).

$$\begin{aligned} i_D = (a_0 + a_1 \cdot v_{in} + a_2 \cdot v_{in}^2 - a_3 \cdot v_{in}^3 \\ +...) \cdot (\mathrm{V_{DS}} + \alpha \cdot v_{in}) \end{aligned} \tag{1}$$

where the a_n coefficients model the non-linearity for a constant drain-source voltage equal to $\mathrm{V_{DS}}$.

The authors would like to acknowledge STMicroelectronics for chip fabrication and the Swedish Foundation for Strategic Research (SSF) for funding the Digitally-Assisted Radio Evolution (DARE) project.

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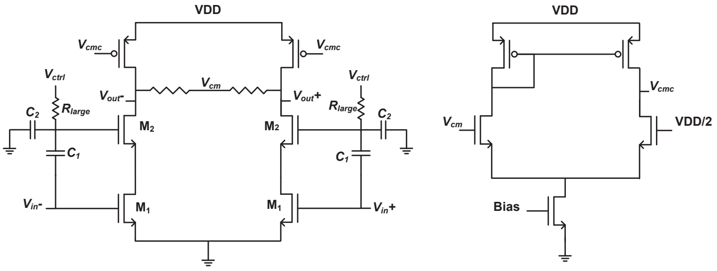


Fig. 1. Schematic of the proposed linearized OTA.

As the even order non-linearities are suppressed by the differential structure the third order non-linearity is dominant. It can be seen from (1) that if α is chosen such that $a_3 \cdot V_{DS} = a_2 \cdot \alpha$, the third order non-linearity will be canceled. In (1) the second order non-linearity is expanding, having a positive sign, and the third order is compressing, having a negative sign. This is the normal situation for a MOS-device, and cancellation will then occur for a positive value of α. Should, however, a device be used at a bias point where the second (a_2) and third order non-linearity (a_3) have the same sign, cancellation can still be achieved, using a negative α implemented by cross-coupling the capacitors C_1 in the differential circuit. The magnitude of α is controlled by the C_1/C_2 ratio and the transconductance (g_m) ratios of the M_1 to M_2 transistor pairs, the latter controlled through the control voltage (V_{ctrl}) that is fed to the gates of M_2 through a large resistor ($\mathrm{R}_{\mathrm{large}}$). The values of C_2 and $\mathrm{R}_{\mathrm{large}}$ are chosen large enough to push the resulting transfer function zero to a very low frequency. The capacitor ratio is chosen to minimize the third order non-linearities under nominal conditions, while V_{ctrl} is used to compensate for process and temperature variations. Since a single V_{ctrl} is used to tune all OTAs, careful filter layout is necessary to minimize device mismatches. A CMFB circuit sets the common-mode output voltage (v_{out}) to half the supply voltage.

III. MEASUREMENT RESULTS

To prove the concept a 4^{th} order Butterworth Gm-C filter, Fig. 3, was designed by cascading two biquads. Each biquad synthesizes two complex conjugate poles. The filter was implemented in a 65nm LP CMOS technology, using standard digital transistors without any extra options. MIM capacitors were used to implement the attenuators, where C_2 was fixed at 20pF for all OTAs.

Nonlinearity cancellation techniques can result in very high intercept points, in ideal case infinite. Mismatch and process variations, however, make the cancellation non-perfect. To investigate the robustness of the technique, a Monte-Carlo simulation of filter IIP3 was therefore performed with a fixed control voltage, i.e. the circuit was not tuned to counteract mismatch and process variations. The results in Fig. 2 show that high performance still holds. In fact, even in the worst cases of the Monte-Carlo simulation, state-of-the-art performance is achieved. Moreover, even higher linearity can be achieved by restoring the optimal cancellation by tuning the control voltage. It should also be noted that the large signal linearity, such as the 1dB compression point ($\mathrm{ICP}_{1\mathrm{dB}}$), is limited by the voltage headroom, and hence the relation $\mathrm{IIP3} \approx \mathrm{ICP}_{1\mathrm{dB}} + 10\mathrm{dB}$ does not hold, as IIP3 in this case is increased significantly.

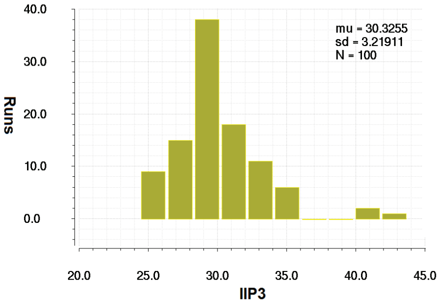


Fig. 2. Monte-Carlo simulation of filter IIP3 for fixed V_{ctrl}.

The filter is supplied by 1.2V and uses 3.5mA of current at the nominal V_{ctrl}. The filter transfer function is shown in Fig. 4, measured for different V_{ctrl} settings. The filter has a loss of about 2dB and a bandwidth of 10MHz. In this prototype V_{ctrl} is used for optimizing the dynamic range of the filter, however, switched capacitors can be used in combination with V_{ctrl} to enable independent tuning of bandwidth and dynamic range.

The test setup is shown in Fig. 5. The on-chip output buffer has two modes of operation to support linearity and noise measurements. In high linearity mode used to measure the intercept points the buffer has an attenuation

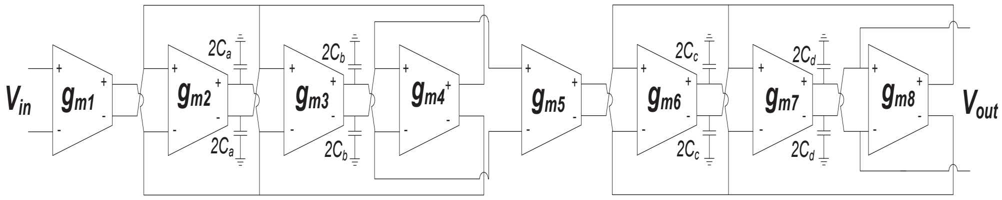


Fig. 3. Block schematic of the 4^{th} order Gm-C Butterworth filter.

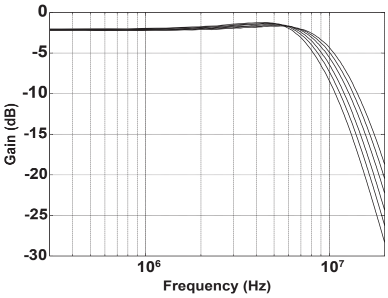


Fig. 4. Measured filter transfer function with different Gm settings.

of 20dB, and in low noise mode used to measure the noise performance, the gain is 0dB. The attenuation in the high linearity mode limits the maximum IIP3 that can be measured before the third order inter-modulation (IM3) term is hidden by noise. In our setup IIP3 up to 39dBm could be measured.

The linearity was measured using two-tone tests. For the in-band IIP3 tones at 1MHz and 1.1MHz were applied. The IIP3 versus V_{ctrl} is shown in Fig. 6 and 7. The roof seen in the figures is due to limitations in the measurement setup preventing higher IIP3 values from being measured. It can be seen that the filter can be tuned efficiently with a single control voltage towards an optimum performance. The out-of-band IIP3 was measured with two tones at 20MHz and 39MHz, with the filter tuned for maximum IIP3, yields a value of 34dBm. The $\text{ICP}_{1\text{dB}}$ is 8.2dBm, and the input referred noise (IRN) is $31\text{nV}/\sqrt{\text{Hz}}$. From the two tone tests and noise measurements, the in-band and out-of-band spurious free dynamic range (SFDR) are 70.9dB and 67.4dB, respectively.

To evaluate the linearization robustness to supply variations, the filter IIP3 was measured with supply voltage varied by $\pm 5\%$, see Fig. 6. It can be seen that the optimal control voltage deviation is below 20mV, but some tuning is required to maintain optimum performance. Robustness to temperature variations is evaluated by measuring the

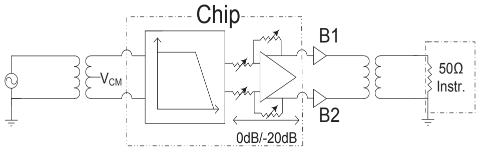
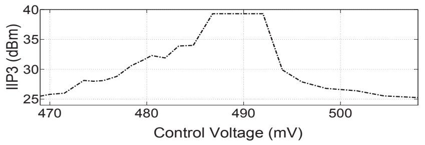
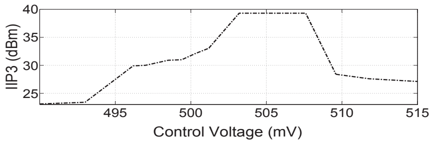


Fig. 5. Test setup for noise and linearity measurement.



(a) VDD+5%

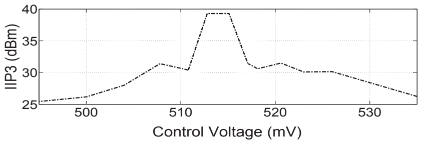


(b) VDD−5%

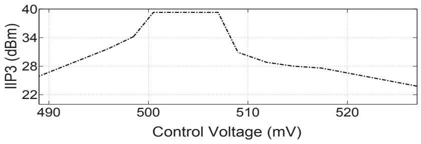
Fig. 6. Measured IIP3 vs. supply variation.

filter IIP3 at 0°C, 40°C and 80°C as shown in Fig. 7. It can be seen in Fig. 7 that even when the temperature is varied by 80°C the optimal control voltage IIP3 does not change considerably.

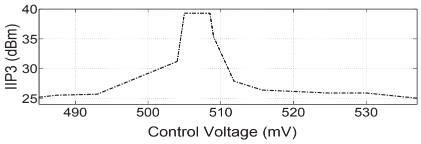
A comparison with recently published state-of-the-art designs is shown in Table I, where achieving a high SFDR requires a high supply voltage [5], or a discrete-time filter architecture [6]. Although being a completely time-continuous design operating at low supply voltage, due to the linearization technique the third order non-linearity is effectively canceled out and the present work achieves the highest reported in-band IIP3 and SFDR. The linearization technique does not pose any limit on the bias current to achieve cancellation, and the current is thus chosen to achieve the required noise performance. Furthermore, since the technique effectively cancels the third order non-linearity, a supply of 1.2V could be used for the filter while



(a) Temperature= 80°C



(b) Temperature= 40°C



(c) Temperature= 0°C

Fig. 7. Measured IIP3 vs. temperature variation.

achieving state-of-the-art performance, which makes the technique suitable for implementing low power and high performance analog filters in upcoming technology nodes.

It is evident that the proposed OTA offers a unique feature that allows tuning the filter to cancel the third order non-linearities. The tuning is achieved using just a single control voltage. While tuning control is still needed, however, having one tuning voltage considerably reduces the complexity of the tuning circuitry. High precision tuning is not needed, and finding the sweet spot can be achieved using a simple tuning algorithm. It can be implemented by first generating the third order non-linearity either in the digital or the analog domain. Digital implementation is favored over analog due to flexibility. Digital equalizers and correlators can then be used to measure the third order non-linearity at the filter output. Minimizing this power, the filter can then easily be tuned towards the optimal point through a DAC.

A chip photo is shown in Fig. 8, and the filter core occupies an area of $0.19\mathrm{mm}^2$. The capacitor banks include the supply decoupling and the capacitive attenuators.

IV. CONCLUSION

A 4^{th} order Gm-C filter with a linearized OTA was fabricated in 65nm CMOS. The filter achieves state-of-the-art IIP3 thanks to a OTA linearization technique. The technique does not increase the noise power of the OTA, resulting in a direct increase of the dynamic range of the filter. Measurements including supply and temperature variation prove the linearization to be robust as the optimal control voltage is not shifted significantly. The effectiveness of the linearization technique makes it attractive for implementing high dynamic range filters in advanced technology nodes.

TABLE I
COMPARISON WITH OTHER WORKS

Parameter	JSSC'10 **[5]**	ISSCC'12 **[6]**	JSSC'11 **[7]**	**This Work**
Tech. (nm)	90	90	90	**65**
Area (mm^2)	0.23	0.29	0.239	**0.19**
Order	4^{th}	4^{th}	6^{th}	**4^{th}**
Supply (V)	2.5	0.55-0.9	1	**1.2**
Power (mW)	1.26	2.9-19.1	4.35	**4.2**
Bandwidth (MHz)	2.8	7-30	13.5	**10**
IIP3 (dBm) $*$	10	-	22.1	**39.3**
IIP3 (dBm) $**$	36	-	18.9	**34**
Noise (nV/$\sqrt{\mathrm{Hz}}$)	19	23.7-32.8	75	**31.3**
SFDR (dB) $*$	58	67.6	53.4	**70.9**
SFDR (dB) $**$	75	-	51.4	**67.4**
FoM (dB) $*$	-157.5	-167.4	-156	**-170.8**
FoM (dB) $**$	-174	-	-154	**-167.2**

*In-band **Out-of-band

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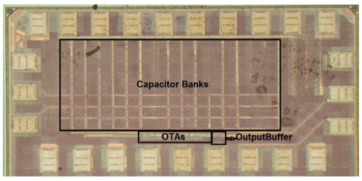

Fig. 8. Chip micrograph.

Paper IV

Paper IV

A Linearization Technique for Differential OTAs

Mohammed Abdulaziz, Waqas Ahmad, Markus Törmänen, Henrik Sjöland, "A Linearization Technique for Differential OTAs," submitted.

A Linearization Technique for Differential OTAs

Mohammed Abdulaziz, *Student Member, IEEE,* Waqas Ahmad, *Student Member, IEEE,* Markus Törmänen, *Senior Member, IEEE,* and Henrik Sjöland, *Senior Member, IEEE*

***Abstract*—This paper presents an OTA linearization technique that is applied to a low noise amplifier and an OTA-C filter. Simulations show the effectiveness of the proposed technique on the low noise amplifier, whose noise and gain performance remain unaffected while the linearity is significantly improved. Measurements of the 80MHz fourth order Butterworth OTA-C filter are also presented. It is implemented using six OTAs instead of eight, thus reducing the power consumption and area. The filter is implemented in 65nm low power CMOS, with a core area of 0.05mm^2 and consumes 12.6mA from 1.2V supply. The measured in-band noise voltage is below 42nV/$\sqrt{\text{Hz}}$, and the measured IIP3 improvement using OTA linearization is up to 17dB in-band and about 3dB out-of-band. Supply and temperature variation measurements on three samples show that the linearization is effective without need for bias adjustment.**

***Keywords*—CMOS technology, low power electronics, operational transconductance amplifier, linearization.**

I. Introduction

Modern wireless standards support a wide range of communication frequencies and high data rates, which implies large channel bandwidths and wide-band radio frequency (RF) amplifiers. Furthermore, in advanced communication standards such as LTE-A, carrier aggregation, where several carriers can be received concurrently by one device, is supported [1]. Therefore, wireless receivers need to support even higher bandwidths, increasing the need for wide bandwidth base-band circuits, including channel select filters (CSF).

Design of operational transconductance amplifiers (OTA) for low power, high performance handset transceivers is becoming more challenging. Advanced CMOS implementations are required to reduce the cost, leading to reduced voltage headroom and transistor intrinsic voltage gain. Moreover, stringent blocking scenarios with strong blockers close to the desired signal require OTAs with high linearity, which is particularly challenging when combined with wide bandwidth. In a receiver chain the signal is amplified before the CSF, relaxing its noise requirements. However, noise performance of RF low noise amplifiers (LNAs) is crucial.

High frequency OTA-C filters are power efficient, but they operate in an open loop configuration which impacts their linearity performance. Wide-band LNAs operate in open loop configuration as well, to achieve maximum possible amplification of weak received signals. Unfortunately strong interference (e.g. self-interference) is also amplified, which poses stringent linearity requirements on the LNA.

Several linearization techniques have been proposed to successfully improve the OTA linearity, e.g. in [2]-[4]. In [2], attenuation based pre-distortion is used to subject the input signal to the inverse of the expected nonlinearity. However, the current consumption is doubled and phase tuning is needed to improve the cancellation. In [3], two additional amplifiers are required for linear voltage-to-current conversion, increasing the power overhead. Furthermore, devices operate in weak inversion, limiting the maximum operating frequency.

In this paper, a linearization technique for high frequency OTAs is presented. It is simulated and analyzed for a wide-band LNA. The linearization is also implemented in a fourth order OTA-C filter with reduced number of OTAs. Measurements of the filter show significant linearity improvements. Measurements also show that the improvement in linearity is maintained across voltage and temperature variations without any trimming. Furthermore, no power or noise penalty is introduced due to the linearization technique, and the area overhead is minimal.

The proposed linearization technique is presented in Section II, while the LNA and Filter implementations and results are presented in Section III and Section IV. Filter measurement results are shown in Subsection IV-2, whereas, conclusions are provided in Section V.

II. Proposed Linearization Technique

At signal levels well below compression the MOS device current characteristic can be approximated by weakly nonlinear model with power series containing up to third order terms. If the body is connected to the source, then the drain current (i_D) nonlinearity is dominated by the gate-source (v_{gs}) and drain-source (v_{ds}) conductances [6], leading to the following characteristic equation:

$$\begin{aligned} i_D = \mathrm{I}_{\mathrm{DC}} &+ g_m \cdot v_{gs} + K_2^{g_m} \cdot v_{gs}^2 + K_3^{g_m} \cdot v_{gs}^3 \\ & g_o \cdot v_{ds} + K_2^{g_o} \cdot v_{ds}^2 + K_3^{g_o} \cdot v_{ds}^3 \\ & K_2^{g_m \delta g_o} \cdot v_{gs} \cdot v_{ds} + K_3^{g_m^2 \delta g_o} \cdot v_{gs}^2 \cdot v_{ds} \\ & K_3^{g_m \delta g_o^2} \cdot v_{gs} \cdot v_{ds}^2 \end{aligned} \tag{1}$$

where g_m and g_o are the device transconductance and drain-source conductance, respectively, and the memory elements (mainly capacitors) are ignored for simplicity. The third order term in (1) is given by

$$\begin{aligned} i_{D_3} =& K_3^{g_m} \cdot v_{gs}^3 + K_3^{g_o} \cdot v_{ds}^3 + K_3^{g_m^2 \delta g_o} \cdot v_{gs}^2 \cdot v_{ds} + \\ & K_3^{g_m \delta g_o^2} \cdot v_{gs} \cdot v_{ds}^2 \end{aligned} \tag{2}$$

The sign and value of the terms in (2) are dependent on the bias conditions of the device. Unfortunately, even with optimal bias, different terms in (2) dominate depending on the amplifier configuration and load impedance. This makes a

The authors would like to thank the Swedish Foundation for Strategic Research (SSF) for funding the Digitally-Assisted Radio Evolution project, and ST-Microelectronics for fabrication of 65nm CMOS circuits.

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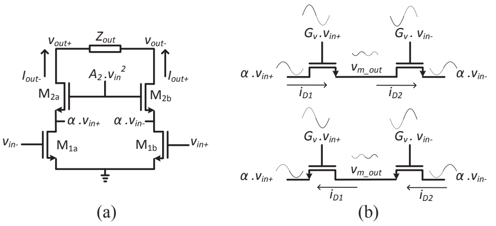


Fig. 1. (a) Linearized cascode amplifier , (b) second order generator .

general linearization scheme very difficult to apply on different OTA topologies.

Consider a simple common source (CS) with cascode amplifier shown in Fig. 1(a). Since the cascode devices M_2 have non-zero input impedance, a voltage $\alpha \cdot v_{in}$ is developed at the drain of M_1. Assuming that nonlinearity is dominated by devices M_1, seen in Fig. 1. Assuming further that the squared and amplified input voltage signal $(A_2 \cdot v_{in}^2)$ is applied to the gates of M_2, devices M_2 act as source followers with a voltage gain of approximately unity, so that the drain voltage of M_1 will also be equal to $A_2 \cdot v_{in}^2$ (plus bias). Replacing v_{gs} with v_{in} and v_{ds} with $\alpha \cdot v_{in} + A_2 \cdot v_{in}^2$ in (2), and under the mentioned conditions the third order term in (1) after linearization $i_{D_3\_modified}$ is

$$i_{D_3\_modified} = i_{D3} + A_2 \cdot K_2^{g_m \delta g_o} \cdot v_{in}^3 \tag{3}$$

For optimal third order linearity $i_{D_3\_modified} = 0$ the value of A_v is given by

$$A_{2\_optimal} = -\frac{i_{D3}}{K_2^{g_m \delta g_o} \cdot v_{in}^3} \tag{4}$$

The second order gate voltage is generated using two differentially excited MOS devices operating in triode region, as shown in Fig. 1(b). The triode devices should have small aspect ratios to avoid loading the circuit. Since the circuit is excited differentially, the DC current though the multiplier is zero, and the source and drain of the multiplier devices will therefore swap places depending on the input signal polarity. The output voltage could therefore be derived for one polarity without considering this issue. Furthermore, the symmetry of the circuit makes the output voltage for the other polarity.

The drain currents i_{D1} and i_{D2} can be calculated using the long channel MOS approximation in triode

$$\begin{aligned} i_{D1} =& K \cdot \frac{W}{L} \cdot ((V_{ov} + G_v \cdot v_{in+} - v_{m\_out}) \\ & \cdot (\alpha \cdot v_{in+} - v_{m\_out}) - \frac{(\alpha \cdot v_{in+} - v_{m\_out})^2}{2}) \end{aligned} \tag{5}$$

$$\begin{aligned} i_{D2} =& K \cdot \frac{W}{L} \cdot ((V_{ov} + G_v \cdot v_{in-} - \alpha \cdot v_{in-}) \\ & \cdot (v_{m\_out} - \alpha \cdot v_{in+}) - \frac{(v_{m\_out} - \alpha \cdot v_{in-})^2}{2}) \end{aligned} \tag{6}$$

where K is the MOS gain factor, W and L are the MOS channel width and length, and V_{ov} is the overdrive voltage $(V_{ov} = V_{GS} - V_t)$. Since $i_{D2} = i_{D1}$, the equation $i_{D2} - i_{D1} = 0$ is solved for v_{m_out}, and a quadratic equation is obtained with two solutions. The correct solution is found by observing that $v_{in} = 0$ must result in $v_{m\_out} = 0$, giving:

$$v_{m\_out} = V_{ov} - V_{ov} \sqrt{\frac{\alpha^2 \cdot v_{in+}^2 \cdot (1 - \frac{2 \cdot G_v}{\alpha})}{V_{ov}^2} + 1} \tag{7}$$

As this equation provides the same result for both positive and negative v_{in}, it can be used for both polarities without alterations using Taylor series expansion, (7) can be rewritten as:

$$\begin{aligned} v_{m\_out} = & -\frac{1}{2} \frac{\alpha^2 \cdot (1 - \frac{2 \cdot G_v}{\alpha}) \cdot v_{in+}^2}{V_{ov}} \\ & + \frac{1}{8} \frac{(\alpha^2 \cdot (1 - \frac{2 \cdot G_v}{\alpha}))^2 \cdot v_{in+}^4}{V_{ov}^3} \dots \end{aligned} \tag{8}$$

Due to the symmetry of the circuit (8) contains only even order terms, which has been verified in simulations. It can also be seen that the second order term has a coefficient of:

$$A_2 = -\frac{1}{2} \frac{\alpha^2 \cdot (1 - \frac{2 \cdot G_v}{\alpha})}{V_{ov}} \tag{9}$$

As seen in (9), the output voltage of the second order generator is independent on aspect ratio of the multiplier devices. This makes the triode multiplier very attractive as its size can be made small enough to avoid loading the amplifier, leading to negligible effect on the noise and gain performance. It can also be seen in (9) that the gate bias voltage can be used to tune the second order term for optimal i_{D3} cancellation.

Since the multiplier devices have small dimensions, effects of device mismatch is investigated. The multiplier device mismatch will result in a non-perfect cancellation of the odd order distortion products, which according to simulations are very small and have negligible effect on the performance. If device mismatch is modeled by using different values of the multiplier device's widths, W_1 and W_2, the second order term will be scaled by

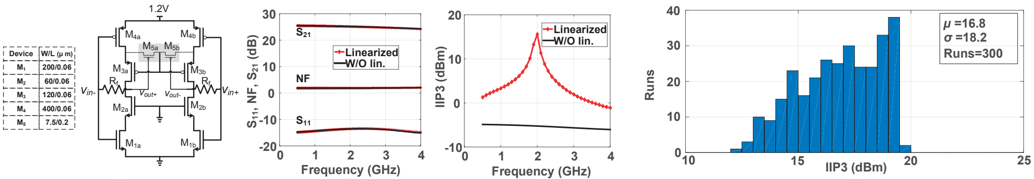
$$A_{2\_mismatch} = A_2 \cdot \frac{4 \cdot (W_1/W_2 - 1) + 4}{((W_1/W_2 - 1) + 2)^2} \tag{10}$$

For instance, a device mismatch of 10% (i.e. $W_1/W_2 = 1.1$) results in second order term gain error of only 0.23% compared to (9).

The triode multiplier is very attractive since it uses no DC current, which eliminates power overhead and gives immunity to flicker noise. The triode multiplier can also be used as a nonlinear impedance, that has higher resistance when an amplifier's output voltage is large, increasing the gain for large signals. The compression point and linearity will then increase at the expense of signal current drawn by the multiplier, resulting in a trade off between noise, gain and linearity. This is very useful for example in improving the compression point and IP3 of power amplifiers.

III. DIFFERENTIAL LNA

A differential LNA with shunt resistive feedback for wideband input matching was designed, see Fig. 2(a). Cascode


(a) (b) (c) (d)

Device	W/L (μ m)
M_1	200/0.06
M_2	60/0.06
M_3	120/0.06
M_4	400/0.06
M_5	7.5/0.2

Fig. 2. (a) LNA with proposed linearization (biasing omitted), (b) S_{11}, NF, and S_{21} simulation, (c) IIP3 simulation, and (d) IIP3 Monte-Carlo simulation.

devices were used for isolation. A complementary architecture was chosen to increase the current efficiency and eliminate the need for area consuming inductor loads. Both BSIMv4 and PSP transistor models were used in the simulations.

The proposed linearization technique is implemented in the shaded area of Fig. 2(a) (devices M_5). Only one multiplier is used, and its gain (A_2) is enlarged to account for the nonlinearity of not only the pMOS but also the nMOS devices.

The S-parameter and noise simulations shown in Fig. 2(b) indicate that the noise figure (NF), gain (S_{21}) and input match (S_{11}) remain unaffected. Two tone test simulations with a tone spacing of 10MHz show that the third order intercept point (IIP3) is improved by more than 20dB at 2GHz, Fig. 2(c). Due to capacitance at the output of the multiplier (mainly gate-source capacitance C_{gs} of M_{3a} and M_{3b}), frequency peaking in IIP3 is seen. Multiplier device gate bias and size can be used to optimize the linearity for the frequency in use, in Fig. 2(c) the performance was optimized for 2GHz. Nonetheless, an IIP3 improvement of more than 5dB was achieved throughout the frequency range (0.5GHz-4GHz).

An IIP3 Monte-Carlo simulation (with two tones placed at 2GHz and 2.01GHz) with 300 runs was performed to evaluate sensitivity to the process variations and mismatch, see Fig. 2(d). As can be seen the cancellation technique has good robustness.

IV. OTA-C FILTER

Cascading second order OTA-C biquads is frequently used to realize higher order filters. In this work a fourth order Butterworth filter is implemented in this way using two cascaded second order biquads.

Second order biquads are often realized using four OTAs as shown in Fig. 3. The first two OTAs form a lossy integrator, and the following two OTAs form a gyrator [7]. For high frequency applications, the OTAs must have a high transconductance (G_m) to output conductance (G_o) ratio, leading to increased power consumption. While using deep sub-micron CMOS technology is beneficial for the speed, it is unfortunately also associated with increased G_o and a limited voltage headroom leading to linearity degradation.

In this work we propose a three OTA biquad architecture instead of the conventional one with four OTAs. This biquad is realized by removing the second stage in Fig. 3 and using two relaxed G_o OTAs and one OTA with reduced G_o but relaxed linearity requirements, as shown in Fig. 4. The transfer function of the first biquad in Fig. 4 is given by

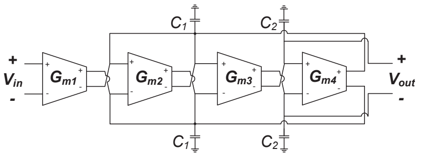


Fig. 3. Second order OTA-C biquad.

$$\frac{V_{out1}}{V_{in}} = \frac{G_{m1}G_{m2}}{C_1C_2s^2 + C_2(G_{o1}+G_{o3})s + G_{m2}G_{m3}} \tag{11}$$

The cut-off frequency ω_o and the Q-factor are given by

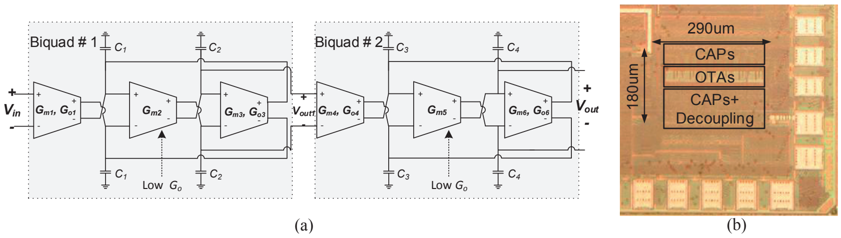
$$\omega_o \approx \frac{\sqrt{G_{m2}G_{m3}}}{\sqrt{C_1C_2}} \tag{12}$$

$$Q \approx \frac{\sqrt{G_{m2}G_{m3}}}{2.G_o}\sqrt{\frac{C_1}{C_2}} \tag{13}$$

As can be seen in (12,13), ω_o can be tuned by jointly varying capacitors C_1 and C_2 while Q is kept constant. For continuous G_m tuning it is known that for MOS devices, $g_o \propto I_D$ while $g_m \propto \sqrt{I_D}$. This limits the continuous tuning range of ω_o using g_m, as the value of Q starts to deviate from the desired value. Continuous wide tuning range filters can be achieved by e.g. diode connected loads which can track and counteract the effect of tuning on the Q-factor. High tuning range can also be achieved by using switched capacitors or varactors for coarse tuning and g_m tuning for fine frequency tuning. Wide tuning range was not, however, implemented in this prototype.

The topology is attractive since the ratio G_m/G_o is not required to be high, enabling low power implementation and use of scaled down transistors in advanced CMOS processes. Apart for the power and area savings, this topology is more linear compared to the conventional four OTA biquad. This is due to less voltage gain in the first OTA which operates in open loop.

1) OTA implementation: The OTA is based on the balanced OTA proposed in [8], designed and implemented in 65nm low power CMOS. Schematics of the reduced G_o (increased output resistance r_o) OTA is shown in Fig. 5, where cascodes are used to boost r_o (biasing is not shown). The cascode devices are removed in the other OTA's leading to significant G_o but increased voltage headroom. The proposed linearization is implemented using devices M_5



(a)

(b)

Fig. 4. (a) Schematic of the fourth order OTA-C filter and (b) die micrograph.

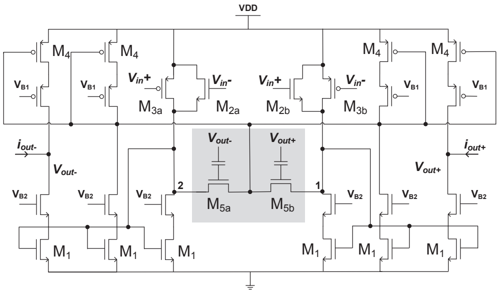


Fig. 5. Schematic of the low G_o OTA.

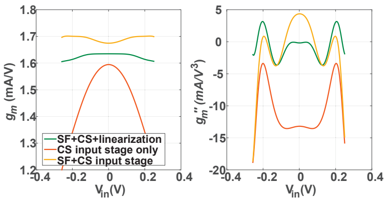


Fig. 6. Simulation of the OTA G_m and second derivative of G_m.

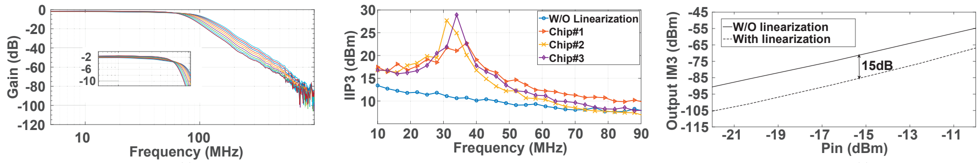
The input stage consists of devices M_3 forming a common source (CS) stage in parallel with devices M_2 forming source follower (SF) stage. This concept has recently been exploited in class-O power amplifiers [9]. Since the CS stage is inverting while the SF stage is non-inverting, the SF input signals are cross coupled. The SF operates in sub-threshold, resulting in partial third order nonlinearity cancellation, since the third order transconductance (g_{m3}) has opposite polarity in strong inversion and sub-threshold. The G_m tuning is performed using the SF DC bias voltage.

Fig. 6 shows simulation of the OTA G_m and second order derivative of G_m (g_m'') which resembles the third order transconductance. It is seen that parallel SF and CS input stage improves the linearity compared to having CS input only. Fig. 6 also shows significant improvement when the multiplier is used compared to no linearization, demonstrating the effectiveness of the proposed technique.

2) Filter Measurement Results: The filter was manufactured in an STM 65nm LP CMOS process and occupies just $0.05\,\mathrm{mm}^2$ of active chip area. The die micrograph is shown in Fig. 4. The chips were glued on an FR4 printed circuit board (PCB), to which all signals and bias voltages were wire bonded. An off-chip 100Ω resistor was used for differential input matching, and an on-chip open drain buffer was used to measure the output signals. A second identical buffer was also implemented on chip, whose frequency response was separately measured and carefully de-embedded from the filter measurement results. All measurements were performed using a 1.2V supply for the filter unless otherwise stated, whereas the supply voltage for the open drain thick oxide transistor buffer was 3.3V to make sure that the linearity measurements were not dominated by the buffer. The measured power consumption of the filter was 12.6mW at a bandwidth setting of 80MHz.

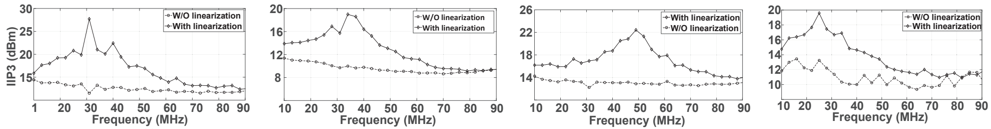
The input signal from the signal generator (R&S SMIQ-06B) was applied through a wide-band off-chip balun (Marki BAL-0006) and the output was measured with a spectrum analyzer (R&S FSU). The measured frequency response of the filter is shown in Fig.7(a). The bandwidth of the filter is continuously tunable between 67MHz and 95MHz by changing the transconductance using the input bias voltage. The nominal measured voltage signal loss of the filter is 2.1dB.

The linearity of the filter was measured using a two tone test. In-band IIP3 was measured across the pass-band of the filter by sweeping the frequency of two tones with a spacing of 1MHz between them. The measured IIP3 versus frequency from three samples is plotted in Fig.7(b). The IIP3 with linearization disabled is also plotted in the same figure from sample $\#1$. It is clear that the proposed linearization significantly improves the IIP3 at all frequencies, except at the band-edge where signal swings are high. Low frequency IIP3 also has lower improvement due to DC blocks in the multipliers, this can however be addressed by using level shifters instead of capacitors. Fig.7(c) shows the IM3 level versus 41MHz input power for both linearized and non-linearized case. It can be seen that the IM3 level is reduced by about 15dB up to high input power levels, further demonstrating the effectiveness of the linearization scheme. The out-of-band IIP3 is 17dBm, which was measured by applying two tones at 200MHz and 390MHz, respectively, compared to 14dBm without linearization. The measured averaged input referred noise is $42\mathrm{nV}/\sqrt{\mathrm{Hz}}$, whereas the input referred 1dB compression point is 5dBm. The spurious free dynamic range (SFDR) is between 44 and 56 dB and is calculated using $SFDR = \frac{2}{3}[IIP3 - P_{noise}]$, where P_{noise} is the integrated



(a) (b) (c)

Fig. 7. Measured (a) frequency response of the filter for different G_m settings, (b) Filter IIP3, and (c) IM3 vs. input power.



(a) (b) (c) (d)

Fig. 8. Measured IIP3 vs. frequency at (a) -20°C, (b) 60°C, (c) VDD+5% and (d) VDD-5%.

TABLE I
COMPARISON WITH OTHER WORKS IN CMOS

Parameter	**[10]**	**[11]**	**[2]**	**This Work**
Technology (nm)	65	130	130	**65**
Supply (V)	1.2	1.5	1.2	**1.2**
Power (mW)	60	21	20.8	**12.6**
Core area (mm^2)	0.35	0.12	0.5	**0.0522**
f_o (MHz)	200	70-280	200	**67-95**
IIP3 In-band$_{\mathbf{min,max}}$ (dBm)	10.3	17	14	**10-28**
Noise (nV/$\sqrt{Hz}$)	70	14	35.4	**42**
SFDR$_{\mathbf{min,max}}$ (dB)	38.25	51	44.7	**43.7-55.7**
FoM$_{\mathbf{min,max}}$* (dBJ)	-142	-159.3	-147.6	**$-$147.5, $-$159.5**

$$*FoM = \frac{Power}{Order \cdot SFDR \cdot f_o}$$

input noise power spectral density .

To evaluate the robustness of the proposed linearization, the IIP3 was measured with supply voltage varied by ±5%, see Fig.8(a,b). The measured results show that the linearization holds. The linearity of the filter was also measured at -20°C, 60°C and 80°C to evaluate the robustness against temperature variations, seen in Fig.8(c,d) (80°C measurement not shown for lack of space). The measurement at room temperature is already presented in Fig.7(b). It is clear that the linearization scheme is effective even under severe temperature variations. The linearization provides significant improvement in IIP3 without requiring any bias tuning in the presence of supply voltage or temperature variations. A comparison with recently published works is shown in TABLE I, which indicates that the performance is well in line with state-of-the-art. The core area is also very competitive.

V. CONCLUSION

A novel linearization technique that effectively cancels the third order nonlinearity is presented. The technique is implemented in a wide-band LNA and a fourth order 80MHz OTA-C filter. The filter was fabricated in 65nm low power CMOS and measures robust improved linearity performance under supply and temperature variations. The filter has a very competitive core area of just 0.05mm^2 and the measured performance is well in line with state-of-the-art. The proposed technique has negligible effect on the noise performance and poses no power overhead. Simulations and measurements confirm the effectiveness of the proposed technique.

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Paper V

Paper V

A Cellular Receiver Front-End with Blocker Sensing

Mohammed Abdulaziz, Waqas Ahmad, Anders Nejdel, Markus Törmänen, Henrik Sjöland, “A Cellular Receiver Front-End with Blocker Sensing,” © 2016 IEEE, *Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, USA, May 2016, Accepted.

A Cellular Receiver Front-End with Blocker Sensing

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***Abstract*— A receiver front-end supporting contiguous and non-contiguous intra-band carrier aggregation scenarios with a fully integrated spectrum sensor that can detect both in-gap and out-of-band blockers has been implemented in 65nm CMOS technology. An NF of 2.5dB is achieved using a noise canceling LNTA, and linearized OTAs are used to achieve an IIP3 improvement of up to 6.5dB in-band and 11dB at the filter band edge. The spectrum sensor can detect blocker levels in 22 steps of 9MHz between -100MHz and 100MHz IF. The system consumes between 36.6mA and 57.6mA from a 1.2V supply.**

***Index Terms*— Operational amplifier, linearization techniques, noise cancellation, receiver, active filter, carrier aggregation.**

I. INTRODUCTION

The increased data rates in advanced wireless communication standards pose significant challenges as the increased bandwidth (BW) reduces the relative frequency distance between the in-band wanted signal and the out-of-band interference. Further increasing the challenges, in LTE receivers (Rx) carrier aggregation is introduced to accommodate higher data rates [1]. Non-contiguous carrier aggregation (CA) with spacing of up to 70MHz is supported, introducing a new kind of blockers that are located in the gap between the wanted carriers. Duplexers are used to attenuate the transmitter power (Tx), however blockers at the band edge and close out-of-band remain amplified in the receiver chain. This increases the linearity requirement in-band and close out-of-band.

Different actions are required for different types of blockers. Strong close out-of-band blockers are best handled by reduction of the base band (BB) gain, while large out-of-band blockers instead require increase of the filtering capacitor at the output of the mixer, reduction of the RF gain may also be required in case of RF amplifier compression. In case of intra-band non-contiguous CA, narrow band strong in-gap blockers located at the image frequency require a high image rejection ratio (about 60dB)[1]. Alternatively, the local oscillator (LO) frequency can be shifted to move the blocker from the image frequency of the wanted carrier.

To achieve optimal Rx tuning, fast blocker detection is crucial and information about approximate blocker amplitude and offset from the carrier is required. Thus, spectrum sensing must be performed before the signal is digitized for two reasons: the detection time will otherwise be increased, and the out-of-band blockers are suppressed by the channel select filters (CSF).

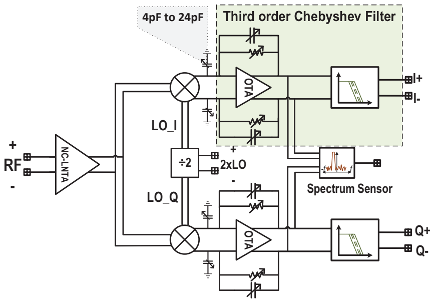


Fig. 1. Block diagram of the Rx-FE.

In this paper a highly configurable Rx front-end (Rx-FE) supporting contiguous and intra-band non-contiguous CA with a fully integrated spectrum sensor is proposed. The spectrum sensor is able to sense blockers and provide information about their frequency and amplitude. Measurements with LTE signals show that blocker sensing is crucial for efficiently improving the Rx-FE performance.

II. RECEIVER FRONT-END ARCHITECTURE

The Rx-FE block diagram is shown in Fig. 1. The RF signal is first amplified by a differential noise-canceling low-noise transconductance amplifier (NC-LNTA)[2], [3], then fed to current driven passive mixers to down convert the signal to BB. The mixer is driven by four quadrature 25% duty cycle LO signals. These are generated by a current mode logic (CML) divide-by-two circuit, where the input is a sinusoid at twice the LO frequency. At each mixer output a tunable capacitor is implemented (4pF to 24pF). Larger mixer capacitors sink more out-of-band blockers current, but unfortunately in-band linearity is then heavily degraded due to reduced transimpedance amplifier (TIA) loop gain BW, motivating spectrum sensing. Following the mixer is a TIA and a second order Tow-Thomas biquad, forming a third order Chebyshev filter. If they cannot be avoided, narrow band blockers located at the image frequency require high image rejection. Therefore, parallel high resistivity poly resistors are used in the resistor banks to enable separate fine tuning

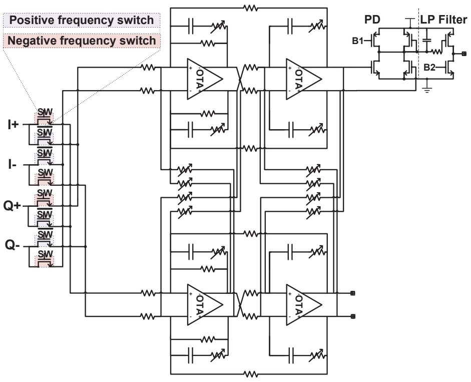


Fig. 2. Schematic of the spectrum sensing circuitry.

of amplitude and phase.

The spectrum sensor, illustrated in Fig. 2, consists of a fourth order complex band pass filter with tunable center frequency and a BW of 10MHz, followed by a power detector (PD) and a low pass filter [4]. The complex filter is configured to sweep positive and negative frequency offsets separately, using input switches to select between positive and negative frequency offsets as shown in Fig. 2. The second channel output of the complex filter is used for characterization and Q-tuning.

The implemented operational transconductance amplifier (OTA) is shown in Fig. 3. Since a high gain-BW product (GBP) is required for supporting large BB BWs, phase enhanced compensation is employed [5]. High linearity is also crucial, especially at the band edges in case of intra-band non-contiguous CA, and for this reason push-pull stages are used in the OTA. Furthermore, a linearization scheme is proposed (shown in the shaded area of Fig. 3), where devices operating in weak inversion are used in parallel with the main input devices. Since the input signal voltage of the TIA is reduced by feedback, the devices are excited by the output of the first stage, providing sufficient amplification of the effective transconductance to achieve linearization.

The LNTA shown in Fig. 4 has two modes of operation, one when the NC path is activated and the Rx noise figure (NF) is minimized, and one when the NC is disabled. NC is achieved since the noise at the output of stage-1 is fed back through R_f to the RF input, and then amplified in anti-phase to the output. Matching the gain of the main path (stage-1 and stage-2) to the gain of the NC-stage achieves NC [3]. The measured LNTA current consumption when NC is on and off is 14mA and 5.4mA, respectively.

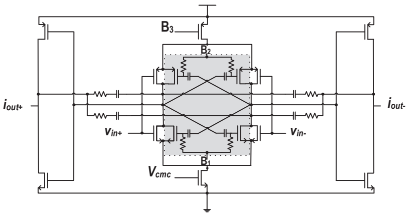


Fig. 3. Proposed OTA schematic.

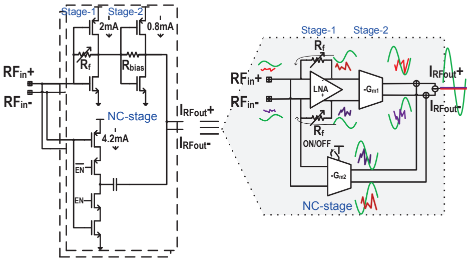


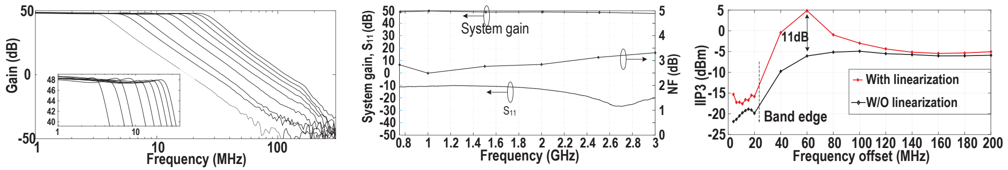
Fig. 4. Circuit details of the noise-canceling LNTA.

The spectrum sensing and Rx control algorithm can be performed by first disabling the input switches of the complex filter, and then measuring the spectrum sensor DC level. The frequency is then swept by activating the input switches and measuring the spectrum sensor output for each frequency step. After a full spectrum sweep, blocker levels are compared to stored threshold values, and when a decision is taken a digital control word is applied to the Rx-FE.

III. MEASUREMENT RESULTS

A prototype chip was fabricated in STM-65nm CMOS with a die area of $1.5\mathrm{mm}^2$ (die micrograph is shown in Fig. 6). Three samples were measured with similar performance, however, in all cases worst case performance is presented. The measurements were performed at maximum gain, a BB BW of 25MHz at LO of 2.5GHz, and a supply voltage of 1.2V (unless otherwise stated). Chips were wire bonded to FR-4 PCBs, and PCB losses were measured and de-embedded from the results. The current consumption of the complete circuit in low-noise mode at 3GHz LO is 57.6mA (see Fig. 6), and when the NC path is turned off and with an LO of 750MHz the current consumption reduces to 36.6mA. The measured NF penalty when turning off the NC path is 2 dB.

The system small signal gain measures 34.5dB and 49dB for the low and high BB gain settings, respectively. The CSF response has an in-band ripple of less than 0.5dB as can be seen in Fig. 5a. Also shown in Fig.5a, the CSF



(a) (b) (c)

Fig. 5. (a) Measured Rx-FE gain with different CSF BW settings, (b) Measured input matching (S_{11}), system gain, and NF and (c) Measured IIP3 with proposed OTA linearization on/off.

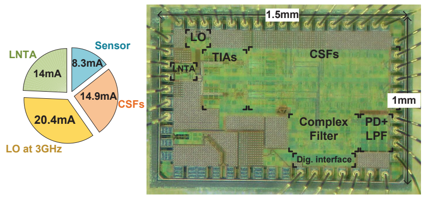


Fig. 6. Die micrograph (area $1.5\mathrm{mm} \times 1\mathrm{mm}$).

BW is coarsely tunable from 3MHz to 46MHz to support all LTE scenarios. Fine BW tuning is also implemented with 40% of tuning range.

The measured Rx-FE input matching (S_{11}), system gain and NF are shown in Fig. 5b. The input matching is better than -10dB over the entire frequency range from 750MHz to 3GHz, while the system gain variation is less than 2dB, and the NF is 2.5dB at 1GHz thanks to the NC feature of the LNTA.

The measured third order input referred intercept point (IIP3) in the Fig. 5c shows that the linearity is reduced in-band due to the high gain, and improves out-of-band where the gain rolls off. It can also be seen that the improvement of the in-band IIP3 due to the proposed OTA linearization is up to 6.5dB, and up to 11dB at the band edge. The out-of-band linearity is dominated by the RF part and it is thus not improved by the OTA linearization.

A four port vector network analyzer (R&S-ZVA67) was used to measure the differential IQ phase and amplitude imbalance. Tuning steps in phase and amplitude were also measured. The CSF achieves orthogonal phase and amplitude tuning with a worst case phase step of 0.15° and an amplitude step of 0.017dB at the band edge (BB BW was set to 46MHz), as shown in Fig. 7. Tuning the amplitude imbalance only (phase imbalance is not tuned) results in an image rejection ratio (IRR) of more than 50dB.

The spectrum sensor (Fig. 2) was measured by characterizing the complex filter first and manually de-embedding the TIA roll off from the output. The complex filter response is tunable up to 100MHz, thanks to the high speed OTA, in steps of approximately 9MHz, as can be seen in Fig. 8.

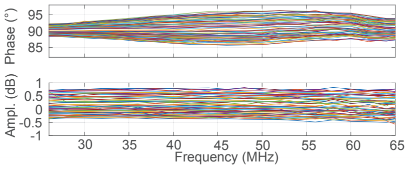


Fig. 7. IQ phase imbalance tuning (top) and amplitude imbalance tuning (bottom).

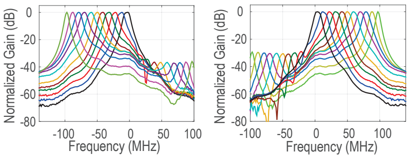
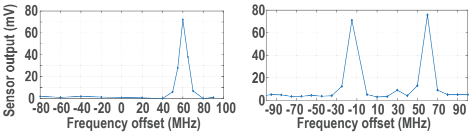


Fig. 8. Spectrum sensor's complex filter normalized response at (left) negative and (right) positive frequencies.

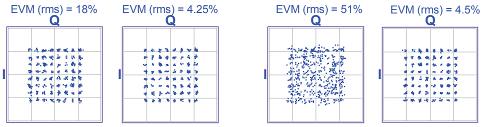


(a) (b)

Fig. 9. Spectrum sensor response to (a) single tone, (b) two tones.

A measurement of the spectrum sensor is also shown in Fig.9. A -39dBm tone at 60MHz offset from the LO was applied at the RF input. The spectrum sensor center frequency was then swept and in Fig. 9a it can be seen that the tone is well detected. In Fig. 9b a second tone at -15MHz offset was also applied. It can be seen the spectrum sensor provides accurate information about both blocker signals.

The Rx-FE was also tested with modulated signals. An LTE signal was generated using an Anritsu-MG3710A



(a) (b) (c) (d)

Fig. 10. Measured constellation of a 10MHz, 64-QAM LTE signal.

vector signal generator (VSG). The down converted I and Q signals from the circuit were combined using a second channel of the VSG and modulated to an intermediate frequency. The Anritsu-MS2830A vector signal analyzer (VSA) was used to demodulate the signal and measure the error vector magnitude (EVM). A modulated blocker was also introduced using an R&S-SMIQ VSG.

The performance of the Rx-FE with modulated signals was extensively evaluated, however, only performance in the presence of out-of-band blockers is reported due to limited space. The presented scenario includes a 10MHz BW 64-QAM LTE signal with level -60dBm centered at 40MHz offset from the LO, applied together with a blocker with 5MHz BW, QPSK modulation, and a level of -24dBm. The CSF BW was set to 46MHz, and the blocker frequency was changed based on the scenario with maximum gain settings.

First, when the blocker was placed at 100MHz offset, the measured EVM was 18.2% (see in Fig. 10.a) with the mixer capacitors set to minimum (4pF). Increasing the capacitor size to 24pF leads to a reduced EVM of 4.25% as depicted in Fig. 10.b. The blocker was then moved to 80MHz and the EVM increased to 50.9% for 4pF mixer capacitors (Fig. 10.c). Increasing the mixer capacitors did not reduce the EVM significantly (39%). However, BB gain reduction improves the EVM to 4.5% (Fig. 10.d). It is evident that accurate blocker information is highly beneficial in deciding the appropriate countermeasure.

The performance is summarized in TABLE I, where it is also compared to state-of-the-art CA Rx-FEs. The presented circuit has the highest system gain and the lowest NF. The IIP2 is comparable to [6] and better than [7] thanks to the fully differential structure. The IIP3 and compression point ($\mathrm{ICP}_{1\mathrm{dB}}$) are slightly lower due to the high system gain. However, the IIP3 at the band edge is highest thanks to the proposed OTA linearization technique. The RF range is also the largest, which increases the power consumption compared to [7]. However, only first order filtering is implemented and a single band is supported in [7].

TABLE I
COMPARISON WITH OTHER WORKS

	ISSCC'13 [6]	JSSC'15 [7]	This Work	Unit
Technology	65	45	**65**	nm
System gain	45	37	**49**	dB
CA scheme	Intra/Inter-band	Intra-band	**Intra-band**	
NF DSB	4.5	3.9	**2.5**	dB
IIP3	2.4	2.75	**-5**	dBm
IIP2	>58	40	**>57**	dBm
Supply	1.45	1	**1.2**	V
DC current	300 (1)	15(2)	**36.6-57.6**(3)	mA
RF range	0.7-2.7	2	**0.75-3**	GHz
RF input	Single	Single	**Differential**	
$\mathbf{ICP}_{1\mathrm{dB}}$	-15.5	NA	**-18.5**	dBm
Core area	14.8(1)	0.16(2)	**0.75**	mm^2

(1) Including PLLs, ADCs and digital BB. Three carrier reception is supported.
(2) Only LNA+LO+TIAs (no filters).
(3) Minimum current consumption when NC is off and LO is 750MHz.

IV. CONCLUSION

An Rx-FE with integrated spectrum sensing is presented. It has low noise figure thanks to a noise-canceling LNTA, and improved linearity thanks to a proposed OTA linearization scheme. The channel filters feature tuning of phase and amplitude imbalance. The spectrum sensor detects amplitude and frequency of signals up to ±100MHz offset. Measurements with LTE signals show that accurate spectrum sensing is required for optimal performance.

ACKNOWLEDGMENT

STMicroelectronics for chip fabrication, the Swedish Foundation for Strategic Research (SSF) for funding the Digitally-Assisted Radio Evolution (DARE) project, and Anritsu for lending the LTE signal instruments.

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