III-V Nanowire MOSFET High-Frequency Technology Platform

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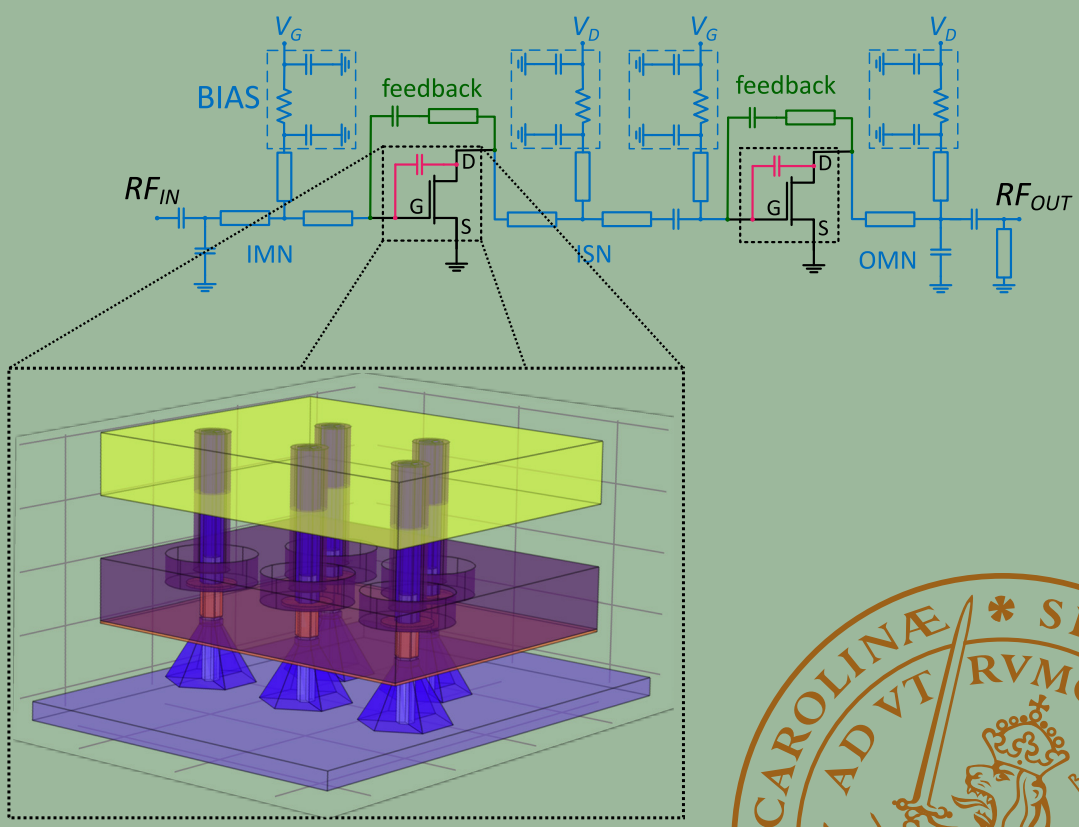

III-V Nanowire MOSFET High-Frequency Technology Platform

Doctoral Thesis

Stefan Andrić

LUND
UNIVERSITY

Department of Electrical and
Information Technology
Lund, May 2021

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Abstract:
This thesis addresses the main challenges in using III-V nanowire MOSFETs for high-frequency applications by building a III-V vertical nanowire MOSFET technology library. The initial device layout is designed, based on the assessment of the current III-V vertical nanowire MOSFET with state-of-the-art performance. The layout provides an option to scale device dimensions for the purpose of designing various high-frequency circuits. The nanowire MOSFET device is described using 1D transport theory, and modeled with a compact virtual source model. Device assessment is performed at high frequencies, where sidewall spacer overlaps have been identified and mitigated in subsequent design iterations. In the final stage of the design, the device is simulated with f_T > 500 GHz, and f_{max} > 700 GHz.
Alongside the III-V vertical nanowire device technology platform, a dedicated and adopted RF and mm-wave back-end-of-line (BEOL) has been developed. Investigation into the transmission line parameters reveals a line attenuation of 0.5 dB/mm at 50 GHz, corresponding to state-of-the-art values in many mm-wave integrated circuit technologies. Several key passive components have been characterized and modeled. The device interface module - an interconnect via stack, is one of the prominent components. Additionally, the approach is used to integrate ferroelectric MOS capacitors, in a unique setting where their ferroelectric behavior is captured at RF and mm-wave frequencies.
Finally, circuits have been designed. A proof-of-concept circuit, designed and fabricated with III-V lateral nanowire MOSFETs and mm-wave BEOL, validates the accuracy of the BEOL models, and the circuit design. The device scaling is shown to be reflected into circuit performance, in a unique device characterization through an amplifier noise-matched input stage. Furthermore, vertical-nanowire-MOSFET-based circuits have been designed with passive feedback components that resonate with the device gate-drain capacitance. The concept enables for device unilateralization and gain boosting. The designed low-noise amplifiers have matching points independent on the MOSFET gate length, based on capacitance balance between the intrinsic and extrinsic capacitance contributions, in a vertical geometry. The proposed technology platform offers flexibility in device and circuit design and provides novel III-V vertical nanowire MOSFET devices and circuits as a viable option to future wireless communication systems.

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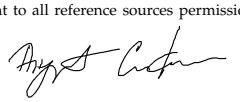
Signature: 

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To You,
Who Inspire Me.

- S

Abstract

This thesis addresses the main challenges in using III-V nanowire MOSFETs for high-frequency applications by building a III-V vertical nanowire MOSFET technology library. The initial device layout is designed, based on the assessment of the current III-V vertical nanowire MOSFET with state-of-the-art performance. The layout provides an option to scale device dimensions for the purpose of designing various high-frequency circuits. The nanowire MOSFET device is described using 1D transport theory, and modeled with a compact virtual source model. Device assessment is performed at high frequencies, where sidewall spacer overlaps have been identified and mitigated in subsequent design iterations. In the final stage of the design, the device is simulated with $f_T > 500$ GHz, and $f_{max} > 700$ GHz.

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Popular Science Summary

Have you ever wondered what is inside your electronic gadgets? Nowadays, we became used to the advanced functionality of mobile phones, the very fast internet in our homes and a great connectivity as we move. All this comes from decades of development in the field of information and computer technology (ICT). And the drive in the field is to make the experience for the users be as seamless as possible. Such end goal forces the ICT systems to be ever-more complex and to handle an increasing amount of data *instantly*. In the core of this data processing lie units that are widely known as *computer chips*.

Looking into those chips, we find something you can imagine as a highway for signals, but on many levels, and some ten thousand times narrower than a strand of hair. We would be observing nanoscale electronic circuits, the greatest engineering achievement of the modern world! Below this interconnect 'highway' lies a *nano*-engineered surface where tiny electronic transistors are embedded. They are the brain of the chip and they use the 'highway' of interconnections to make complex decisions. These electronic transistors are organized according to their functionality, which allows us to imagine the inside of a chip as an array of smaller blocks executing specific tasks. They are known as electronic circuits. Those that are interesting, from the aspect of this thesis, are those that enable us to communicate with the outside world. The electronic transistors used in these circuits handle radio signals landing onto antennas hidden in our phones, computers, or any other wireless devices.

The challenge in designing these communication systems lies in the internal design of the nano-scale electronic transistor, for the purpose of handling these radio signals. The traditional transistors are limited in their speed of operation, so a novel approach is needed. The transistor presented here has a design that would push this speed limit further. The transistor shape is rather unusual - it is a vertically-standing nanometer-scale wire, or a pillar, as opposed to the ones embedded in the surface of the chip. The choice of such *nanowire* structure is motivated by an increased performance due to a freedom to choose materials and the nanowire shape more easily. The goal is, much like with traditional embedded transistors, to create the same type of circuitry as in the dense computer chips used today.

This thesis ties the investigation of such nanowires to the implementation of specific materials, so that resulting devices perform better than the industry standard in some aspects. The core research is in the organization and efficiency of nanowire transistors, and in the building blocks that enable the nanowire electronic circuits, towards achieving the ever-advancing wireless communication systems. A way forward is created for nanowire transistors, with exploring limits in their design and functionality. This makes them compatible with building complex systems that exceed current wireless standards (up to 6 GHz), going towards the radar, and the very high-speed electronics (10s to 100s of GHz). Hence, the vertically-standing nanowires are an interesting option to investigate, since the future of our society will eventually use those 100s of GHz for the data transfer, and to support the increased inter-connectedness.

Acknowledgments

THIS pages are dedicated to all that have made this journey more enjoyable. I extend my greatest respect to my supervisors: *Lars-Erik Wernersson*, *Lars Ohlsson*, and *Erik Lind*. To *Lars-Erik*, I extend my gratitude for the given opportunity within the *Nanoelectronics* group. I looked into PhD studies only as a steppingstone in the carrier development, but it has now morphed into an ever-increasing wish to know more. I appreciate that spark that you managed to ignite during these years! And for making us all always see the bigger picture, and to look ahead! To *Lars*, I can only say thank you for the seemingly endless patience with my lack of knowledge that still is. You have thought me almost everything RF, and your critical sense have always made me take a closer look into things. And to *Erik*, I can proudly say that the most interesting course I have listened to in my long academic upbringing was given by you! I am grateful to the discussions and to be able to learn from you.

I am proud to be a part of the *Nanoelectronics* group over the last five years. Much has changed, but the experience will remain. I wish to thank *Johannes*, for always giving a nice word and for support in practical matters. To my fellow PhD students, I wish to acknowledge *Fredrik*, *Olli-Pekka*, and *Adam*, with whom I worked closely over the years and whom I greatly appreciate to have had as work colleagues. *Fredrik*, thank you for your enthusiasm, especially in the lab! *Olli-Pekka*, I thank you for the numerous samples (that I ruined) and for the close collaboration that pushed my research forward. *Adam*, I will always appreciate your humor, as well as your dedication to get the most out of your research. I acknowledge other group members, with whom I have shared (a portion of) my PhD experience: *Cezar*, *Elvedin*, *Karl-Magnus*, *Sebastian*, *Mattias*, *Abinaya*, *Heera*, *Lasse*, *Saketh*, *Gautham*, *Marcus*, *Anton*, *Navya*, *Robin*,

Patrik, *Zhongyunshen*, and *Andrea*. I greatly value the time we spent pushing boundaries. I appreciate your talent and expertise and I wish the best to all of you in your future endeavors.

Furthermore, I wish to thank the many administrative staff and department colleagues that have helped in making this a positive experience overall. During my time as a PhD student, I had an opportunity to work with *Thomas*, and *Arnulf*, from Fraunhofer Institute in Freiburg, Germany. I am most grateful to your guidance in the beginning of my PhD, a crucial time in my studies.

To combat PhD-induced stress, I thank *Jonas* and the entire team from Lunds Aikidoklubb. Over the last years, we have trained our body and mind together, in an array of the unforgettable experiences. I thank *Thalea*, *Moa*, *Simon*, *Jakob* for always being instructive and guiding me towards my inner calm, as well as *Sara*, *Will*, *Natalie*, *Sandra*, and many others, for their company and partnership in training. Also, to *Lars-Göran* (*Lasse*), I thank for unforgettable summers training Aikido up in Värmland! And to many other Aikidokas that I met from all corners of Sweden, you have made this experience a better one!

Finally, my cornerstone. You have made my final years that much more enjoyable, and with whom I wish to share my life with - thank you *Samuel*, for being my inspiration and for making me a better man! Eu amo, você é o amor da minha vida! I also thank my family that supported me all these years - Хвала вам на безусловној подршци: *Мама*, *Тата*, *Иване*, *Ивана*, *Саро*, *Лука* и *Андреје*. Без свих вас, цело ово искуство не би било потпуно! Without all of you, this experience would not be complete...

Стефан Андрић / Stefan Andrić
in Lund, May 2021.

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Preface

THIS thesis represents nearly five years of work in creating a suitable technology platform for design and simulation of III-V nanowire devices and circuits, at high frequencies. The work also represents a collaboration within the *Nanoelectronics* group at Lund University, supervised by Professor *Lars-Erik Wernersson*, Professor *Erik Lind*, and Dr. *Lars Ohlsson Fhager*.

STRUCTURE OF THE THESIS

The thesis is divided into several parts. First, a survey of the field is provided, conveying the message through discussion of circuit design strategies, ending with a performance benchmark for state-of-the-art device technologies. In the following section, a description of the III-V nanowire MOSFET technology platform is given. The focus lies in the device ballistic transport properties and compact modelling, as well as the layout organization of test vehicles, including the integration of structures for process monitoring. The third chapter describes the associated back-end-of-line. The most of the experimental work is presented in this chapter, through characterization of different passive components. The final chapter describes the usage of the technology platform and the device design to form a basis for the circuit design and realization, as well as benchmark against established technologies.

- **INTRODUCTION**
  The Introduction provides a comprehensive and more general view of the thesis topic. The major points are described in detail in the publications related to this thesis. It is written in a way to appeal to

broader audiences and attract interest of students and researchers in this specific field.

- **APPENDICES**

  A Optimum Matching Network Design
  Appendix A describes the optimum matching network design procedure, based on theoretical concepts that take into account transistor input and output quality factor and the set matching level, with the aim to maximize the available bandwidth. It forms a basis for circuit simulation and realization.

- **PAPERS**
  The papers, reproduced in the back of the thesis, are listed in the following. For some of the works, an input, weather as samples or model parameters, have been provided by Olli-Pekka Kilpi, Fredrik Lindelöw, Adam Jönsson, and Anton Persson.

INCLUDED PAPERS

The following papers form the structure of this thesis. These include journal papers and conference contributions, as well as works in a manuscript form. The respective papers and drafts are included in the back of this thesis.

Paper I: S. Andric, L. Ohlsson Fhager, F. Lindelöw, O.-P. Kilpi, and L.-E. Wernersson, "Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs", *Journal of Vacuum Science and technology* ***B***, vol. 37, art. no. 061204, Oct. 2019, doi: 10.1116/1.5121017.

▶ *I carried out standalone BEOL fabrication as well as the BEOL fabrication on top of test devices, performed device and test structures measurement and analyses, and wrote the paper.*

Paper II: S. Andric, L. Ohlsson, and L.-E. Wernersson, "Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III–V MOSFETs on Silicon", *92nd Microwave Measurement Conference (ARFTG)*, Orlando, FL, USA, pp. 1–4 Jan. 2019, doi: 10.1109/ARFTG.2019.8637222.

▶ *I designed BEOL layout, fabricated the BEOL with a TRL kit, performed measurements and data analyses, and wrote the paper.*

Paper III: S. Andrić, F. Lindelöw, L. Ohlsson Fhager, E. Lind, and L.-E. Wernersson, "High-Frequency Circuit-Level Characterization of Lateral III-V Nanowire MOSFETs", Manuscript submitted to *IEEE Transaction on Microwave Theory and Techniques*, Mar. 2021.

▶ *I designed BEOL models, simulated circuits, fabricated the BEOL on the sample, characterized passive components and circuits, carried out data analyses and modelling, and wrote the paper.*

Paper IV: S. Andrić, L. Ohlsson Fhager, and L.-E. Wernersson, "Design of III-V Vertical Nanowire MOSFETs for Near-Unilateral Millimeter-Wave Operation", *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, Utrecht, Netherlands, pp. 85–88, Jan. 2021.

▶ *I simulated the capacitor response, designed and simulated amplifiers, performed data analyses, and wrote the paper.*

Paper V: S. Andrić, L. Ohlsson Fhager, and L.-E. Wernersson, "Millimeter-Wave Vertical III-V Nanowire MOSFET Device-To-Circuit Co-Design", Manuscript submitted to *IEEE Transactions on Nanotechnology*, Jan. 2021.

▶ *I designed COMSOL models, wrote a Verilog-A code for the device model, carried out all simulations and analyses,and wrote the paper.*

Paper VI: A. E. O. Persson, S. Andrić, and L.-E. Wernersson, "MM-wave Capacitance Characterization of Ferroelectric MOSCAPs", Manuscript in preparation.

▶ *I designed the mm-wave MOS capacitor layout, as well as the on-chip calibration kit, helped fabricate and measure the sample, analyzed portion of the results, and helped in paper writing.*

RELATED WORK

The following publications are not included in the thesis. It represents the collaborative work within the *Nanoelectronics* group, that I contributed to.

Paper VII: K.-M. Persson, S. Andrić, S. Ram Mamidala, and L.-E. Wernersson, "Scaling Potential for Vertical ReRAM Crosspoint Arrays", Manuscript in preparation.

▶ *I designed COMSOL capacitance models, and helped writing the paper.*

Paper VIII: O. P. Kilpi, S. Andrić, J. Svensson, E. Lind, and L.-E. Wernersson, "High Breakdown Voltage in Vertical Heterostructure III-V Nanowire MOSFETs", Manuscript in preparation.
▶ *I analyzed device data, developed COMSOL model and simulated the field-plate response, and wrote part of the paper.*

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols, which are recurring throughout the thesis, are listed. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

BCB	Benzocyclobutene
BEOL	Back-End-Of-Line
CMOS	Complementary MOS
CPW	Co-Planar Waveguide
CV	Capacitance-Voltage
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DIM	Device Interface Module
FDSOI	Fully Depleted SOI
FEOL	Front-End-Of-Line
GAA	Gate-All-Around
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor

HSQ	Hydrogen Silsesquioxane
ILD	Interlayer Dielectric
LNA	Low-Noise Amplifier
LNW	Lateral Nanowire
LRRM	Line-Reflect-Reflect-Match
MIM	Metal-Insulator-Metal
***mm*-wave**	Millimeter Wave
MN	Matching Network
MOL	Middle(-End)-Of-Line
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide-Semiconductor
MOSCAP	MOS Capacitor
MOSFET	MOS Field-Effect Transistor
MS	Microstrip
mTRL	Multiline TRL
RF	Radio Frequency
SOI	Silicon-On-insulator
***s*-parameter**	Scattering Parameters
TEM	Transverse Electric-Magnetic
TFR	Thin-Film Resistor
TL	Transmission Line
TLM	Transmission Line Measurement
TRL	Thru-Reflect-Line
VNW	Vertical Nanowire
VS	Virtual Source
***y*-parameter**	Admittance Parameters

LATIN SYMBOLS

c		$\approx 3 \times 10^8$ m s^{-1},speed of light
C'	F m^{-1}	Distributed Line Capacitance
$C_{\mathrm{gx}}, C_{\mathrm{gx,p}}$	F,fF µm^{-1},aF/nw	Parasitic Gate Capacitance
$C_{\mathrm{gx,i}}$	F,fF µm^{-1}	Intrinsic Gate Capacitance
C_{inv}	F,aF nm^{-1}	Inversion Charge Capacitance
C_{via}	F	Interconnect Via Capacitance
D_{1D}	e V^{-1} cm^{-1}	1D Density-of-States
E_{G}	eV	Energy Band Gap
f_0	Hz	Cut-off Frequency Geometric Mean, Operating Frequency
f	Hz	Frequency
f_{FD}		Fermi-Dirac Distribution Function
FoM	Hz V^{-1}	Figure-of-Merit of the Transistor
f_{T}	Hz	Current Gain Transition Frequency
f_{max}	Hz	Maximum Oscillation Frequency
F_{s}		Saturation Factor
G, G_T, G_{max}	dB	Gain, Transducer Gain, Maximum Gain
g_d	S, mS µm^{-1}	Output Conductance
g_m	S, mS µm^{-1}	Transconductance
G'	S m^{-1}	Distributed Line Dielectric Conductance
GaN		Gallium Nitride
h		$\approx 6.626 \times 10^{-34}$ J s, Planck Constant
h	m	Dielectric Layer Height
HfZrO		Hafnium-Zirconium Oxide
I_{D}	A, mA µm^{-1}	Drain Current
InAs		Indium Arsenide
InGaAs		Indium-Gallium Arsenide
InP		Indium Phosphide

k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
L'	H m^{-1}	Distributed Line Inductance
L_eff	m	Effective (Reduced) Gate Length
L_fp	m	Field-Plate Length
L_G	m	Gate Length
L_via	H	Interconnect Via Inductance
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
m^*		Effective Mass
n_f		Number of Gate Fingers
n_w		Number of Nanowires
NF		Noise Figure
NF_min		Minimum Noise Figure
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
Q		Quality Factor
Q_x0	C, C m^{-2}	Channel Inversion Charge
R'	Ω m^{-1}	Distributed Line Resistance
R_ON	Ω, Ω µm	On-state resistance
$R_\mathrm{S/D}$	Ω, Ω µm	Terminal (Source/Drain) resistance
s		Signal-to-Ground Spacing
s_ij		Scattering Parameters
Si		Silicon
SiO_2		Silicon Dioxide
SiGe		Silicon-Germanium
T		Transmission
T	K	Temperature
t_b	m	Drain Underlap Height
t_S	m	Vertical Spacer Thickness
t_W	m	Gate Metal Thickness
v_{inj}	m s^{-1}	Injection Velocity, Thermal Velocity
V_B	V	Bias Voltage
V_DS	V	Drain-to-Source Voltage

V_{GS}	V	Gate-to-Source Voltage
V_{T}	V	Threshold Voltage
v_{x0}	$\mathrm{m\,s^{-1}}$	Virtual Source Velocity
w	m	Transmission Line Width
W_{G}	m	Gate Width
$y_{\mathrm{ij}}, Y_{\mathrm{ij}}$	S	Admittance Parameters
Z_0	Ω	Characteristic Impedance
Z_{opt}	Ω	Optimum-Noise Matching Impedance

GREEK SYMBOLS

α		Voltage Scaling Factor
α	$\mathrm{dB\,mm^{-1}}$	Transmission Line Attenuation
β		Saturation Factor Fitting Parameter
β	$\mathrm{rad\,mm^{-1}}$	Transmission Line Phase Constant
$\varepsilon_{(0)}$	e V	Top-Of-the-Barrier Energy
ε_0		$\approx 8.85 \times 10^{-12}\ \mathrm{F\,m^{-1}}$, Vacuum Permittivity
$\varepsilon_{\mathrm{eff}}$		Effective Dielectric Constant
ε_{r}		Relative Dielectric Constant
Γ		Reflection Coefficient
Γ_{opt}		Noise-Optimum Reflection Coefficient
κ		Relative Permittivity
λ	m	Mean-Free Path, Guided Wavelength
μ,μ_{e}	$\mathrm{m^2\,V^{-1}\,s^{-1}}$	Electron Mobility
ω	$\mathrm{rad\,s^{-1}}$	$= 2\pi f$, Angular Frequency
π		≈ 3.14159, Mathematical constant
γ	$\mathrm{m^{-1}}$	Propagation Constant

FUNCTIONS AND OPERATORS

$\mathrm{Im}(\cdot)$	Imaginary part
$\ln(\cdot)$	Natural Logarithm

INTRODUCTION

1

Fundamentals of RF Circuits

UR modern world is built around the fundamentals of communication using radio signals. Such communication systems enable us to transfer *a large amount* of information over vast distances. The system itself is built from circuits, electronic units with a specialized functionality. The first section of this chapter addresses the perspective of the design of radio signal-handling circuits using an electronic transistor, with a focus on frequency of operation. The next section dives into the core of many modern radio circuits out there - the nanoscale *Metal-Oxide-Semiconductor Field Effect Transistor* (MOSFET). Some of the basic properties are addressed, including transistor's nanoscale geometries. The chapter ends with a transistor state-of-the-art performance benchmark, which also provides a motivation for this thesis.

1.1 ABOUT CIRCUIT DESIGN

The electronic circuit represents a set of electronic components that can control electric impulses, or signals, which are a part of the electromagnetic spectrum, and are described as travelling waves. The spectrum of interest for electronic applications encompasses radio waves and microwaves, typically found at wavelengths between a few hundred km, down to a few µm, and correspond to frequencies ranging from a few kHz up to several hundred GHz. Various materials are used to capture specific properties of these waves, and to process them without distortion, or loss of the information they carry. These materials will, ultimately, build individual electronic components and with them, the electronic circuits and systems.

The core of these electronic circuits is an *active* component - an electronic transistor. Typically, it is made from a semiconducting material, and allows for transformation of the input electronic signals into the stronger, output signals. The effect is known as signal amplification. It revolutionized the world of electronics since this functionality proved to be an efficient way to transform signals and to manipulate them through integration of many transistor components. Electronic transistors are three- or four-terminal components, where one set of terminals is used as a controlling input, while others are used for the generated desired output. The electronic signals transistors manipulate are electrical current or voltage signals, or power waves at high frequencies. In essence, transistors are behaving like non-ideal current switches, and their non-idealities give rise to a range of effects that have been a subject of study for decades.

A representative circuit that utilizes electronic transistors will be designed differently based on the application for which the circuit is intended, or at which end of the frequency spectrum it operates. In principle, a combination of active components (electronic transistors), and various passive components (resistors, inductors, capacitors, transformers, and transmission lines), provide a specific functionality to the circuit. Fig. 1.1 shows some typical design examples of signal amplifiers for different frequency ranges, showcasing differences in design procedures at different operation frequencies. Fig. 1.1(a) illustrates the simplest case - a low frequency circuit, where the resistance values control the circuit operation. In the next stage (Fig. 1.1(b)), more reactive components will be needed to *suppress* the phase shift in the signal, which starts to

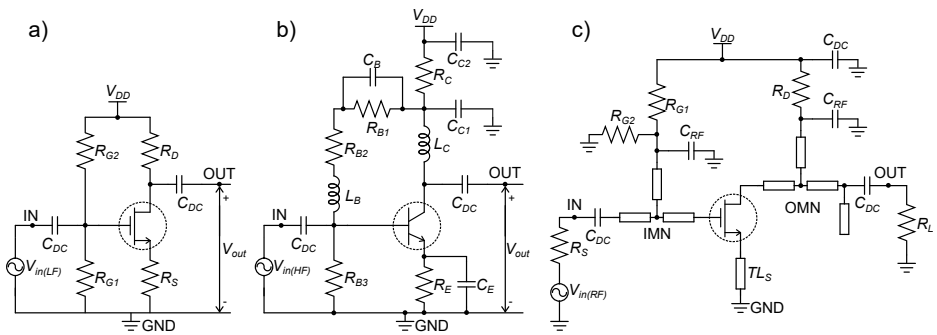

Figure 1.1: An example of various circuits with an electric transistor: a) low-frequency (kHz range), b) intermediate frequency (MHz range), and c) high frequency (GHz range) circuit. All circuits show arrangement of different components, to achieve signal amplification, with each version being more complex, ultimately resulting in distributed components (transmission line segments).

appear as the frequency of operation increases. Therefore, inductors are used. Additionally, an effort to stabilize and isolate the circuit is made, with added capacitors and a resistive feedback loop. Finally, the high-frequency design is the most interesting, and the most sensitive to the effects addressed in the Fig. 1.1(b). Here, distributed components are used, those that allow for amplitude and phase change along the dimensions of the component. Fig. 1.1(c) shows an implementation with distributed transmission line components. The distributed effects will be addressed in detail in the following chapters.

1.2 NANOSCALE MOSFET AS A RADIO DEVICE

At the core of many modern integrated radio circuits we find the nanoscale MOSFET, a device with some unique properties. Although the device concept was developed almost a century ago, it was brought to life only some 60 years ago with several discoveries following discrete transistor components [1–5]. An integrated version has been introduced to the world in '74, marking an important milestone for scaled devices and circuits, as well as for computing and signal processing [6, 7]. Following these first findings, an industrial development has followed hand-in-hand, enabling our modern society to benefit from the technology ever more. Particularly, mobile, or wireless communication development has come alive with the use of these integrated devices. The basic properties of modern nanoscale MOSFETs are given in the following subsections.

1.2.1 MOSFET BASIC DESIGN AND OPERATION

The nanoscale MOSFET is created by *nanoengineering* a device structure that contains three, or four terminals named *gate*, *source*, *drain*, and *bulk* (or *body*). In the device core is the semiconducting *channel*. The gate, and the body control the channel electrostatically, through capacitive coupling, and are considered input terminals. The output, that are the source and drain terminals, are resistively coupled, and conduct current based on the state of the input terminals. This significant difference in the coupling behavior of the input and output regions of the device results in a signal manipulation that is heavily based on the properties and dimensions the semiconductor material, as well as on how the material is integrated into a nanoscale device.

The MOSFET operation relies, among other things, on doping of the semiconductor by *impurities*. Introducing atoms of the specific elements into the semiconductor crystal will create an excess of charges that can

contribute to a reduced resistance. Source and drain terminals of the radio MOSFET are typically in excess of electrons, that participate in the electron transport in the device. Such devices are named *n-type* MOSFET, or nMOSFET for short. Fig. 1.2(a) shows such a MOSFET with doped regions integrated into the semiconductor. The capacitive coupling of the input terminals is achieved via a gate insulator, separating the channel and the gate electrode. An alternative approach is to integrate a metal electrode directly on the pure (undoped) semiconductor, creating an energy barrier, arising due to the difference in electron affinity between the materials (Schottky barrier). Both technology options exert an electric field over the channel and thereby control the channel conductivity by attracting or repulsing charges from the gate-semiconductor interface.

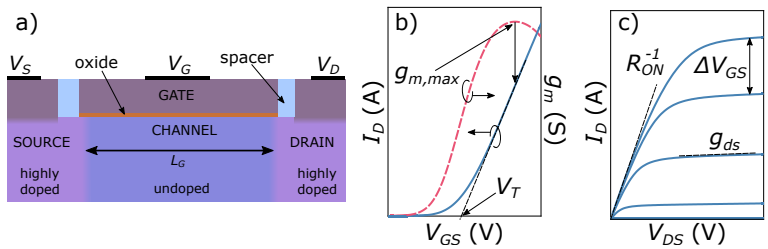

Figure 1.2: Overview of basic MOSFET design and operation: a) device illustration, showing highly doped drain and source region, channel, gate oxide and contact metals. b) Transfer plot of drain current and transconductance, and c) output plot of typical high-performance nanoscale MOSFET, with important parameters noted.

The current flow in the drain terminal, known as drain current I_D, is used to characterize the device operation. Fig. 1.2(b) depicts such a case, and it is known as a transfer plot, since it shows the dependency of I_D on the input gate-source voltage V_{GS}, for a set of drain-source voltage V_{DS} values. Two different states are identified: the off-state, where the current level is low and has an exponential behavior, and the on-state, where the current has a significant value and changes in a quadratic/linear relation. The border between these two states of operation is characterized by a threshold voltage, or V_T. The most important metric in radio device is the slope of I_D, or transconductance g_m. It is a derivative of the drain current with respect to the gate voltage, or $g_m = \partial I_d / \partial V_{gs}$, and is a measure of the amplification capabilities of radio signals in a MOSFET.

If I_D is measured at different V_{DS}, while V_{GS} remains constant, the output characteristics can be obtained, as shown in Fig. 1.2(c). Two distinct regions of operation are identified in this case as well. They

are named the triode (or resistive) region, and the saturation region. The resistive region is observed for small V_{DS}, where the current-voltage relationship is linear. The value of this resistance, the R_{ON}, is determined by the gate voltage, and its value will saturate as V_{GS} increases. In the case of higher V_{DS}, the current flattens out. The electric field on the drain side pinches off the conduction in the channel and creates a barrier that electrons cannot overcome, thus flattening the current. More prevalent nowadays, in devices with short gate-length, is that the channel pinch-off does not happen since the high electric field causes electrons to scatter in the channel, thus limiting their velocity (velocity saturation). The pinch-off occurs mostly for low V_{GS}. The ability for current to remain constant is a measure of the gate electrostatic control over the channel. The slope of the current in this region, known as output conductance, or $g_d = \partial I_d / \partial V_{ds}$, is also a measure of the quality of the device. The MOSFET intrinsic gain, or *self-gain* g_m/g_d, as well as transconductance efficiency, or g_m/I_D, are also important metrics in the analog and radio MOSFET, and determine the extent of the device operation.

1.2.2 SCALING OF RADIO MOSFETS

To improve on the MOSFET density and performance, reducing the device size is a proven method. The rules for device scaling are known as *Dennard scaling* rules [8]. Together with the now famous *Moore's law*, they formed a basis for defining scaling trends for future technology nodes, from an economic, as well as technological perspective [9]. According to Dennard scaling rules, the device dimensions and the operating voltages are scaled by a factor, effectively reducing the power consumption, while improving on the device performance [8]. However, the power density in the device would dramatically increase. Therefore, after almost two decades, this original rule has been replaced with an alternative approach that does not scale the device power density [10]. The optimization of the source/drain contacts, a gate insulator dielectric, and spacers was addressed instead. The electrostatic control of the channel is challenged in every iteration of gate length reduction, and eventually, the gate starts losing control over the channel potential due to penetrating electric field from the drain terminal, commonly known as a short-channel effect. This makes the device intrinsic gain, a crucial factor for analog operation, diminish.

In Fig. 1.3, geometry variations are depicted, showcasing considered approaches to solving scaling and performance bottlenecks of today. MOSFETs are illustrated with regions consisting of highly-doped semiconductor contacts, the intrinsic channel surrounded by a gate insulator (high-κ), and a patterned gate contact metal cover. Device spacers, drain/source

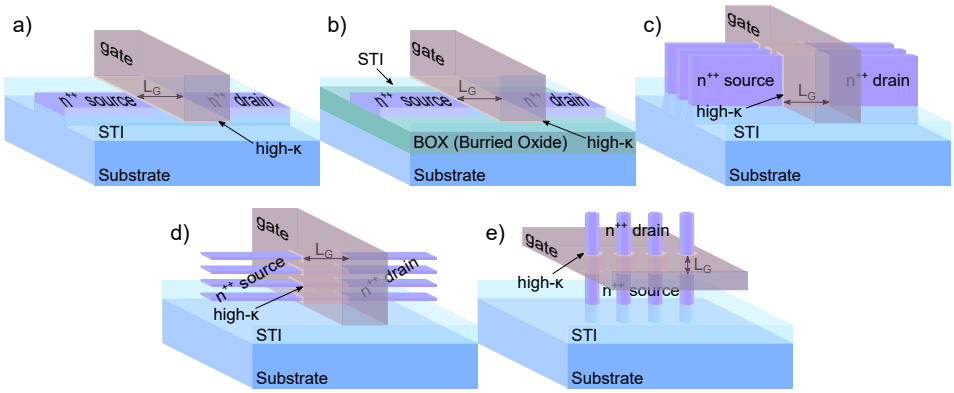

Figure 1.3: Illustration of nanoscale MOSFET structure, showing integrated transistor with relation to the substrate, consisting of n^+ contacts, intrinsic channel (marked with gate length L_G), high-κ insulator and gate metal, isolated with STI. MOSFETs are shown in various geometries: a) bulk, or planar, b) SOI MOSFET, c) FinFET, d) lateral GAA MOSFET, and e) vertical GAA, or nanowire MOSFET.

contact metals and enveloping low-κ dielectric (passivation) are omitted, for clarity. The two planar approaches, shown in Fig. 1.3(a-b), are bulk, and Si-On-Insulator (SOI) MOSFET geometry, respectively. They rely on semiconductor having a direct connection to the substrate, or are attached to the substrate with an insulating layer, known as a buried oxide, and isolated with a shallow-trench isolation (STI). The next stage in device geometric development are, among others, lateral devices, which utilize the existing planar technological solutions. They include the FinFET/tri-gate MOSFET (Fig. 1.3(c)), and lateral gate-all-around MOSFET (stacked nanosheets, Fig. 1.3(d)) [11,12]. The semiconductor channel is shaped as a very thin semiconductor *fin* and wrapped from more than one side with gate metal. The gate electrostatic control is then greatly improved, enabling further scaling. Recently, the FinFETs/tri-gate MOSFETs further show improvement in the high-frequency performance, which will be discussed in the next subsection.

Finally, the ultimate scaling trend leads to a semiconductor channel formed like a nanowire, possibly shaped from a thick semiconductor layer or grown as a wire on the semiconducting or insulating surface. They are known as vertical gate-all-around (GAA), or nanowire MOSFETs, and are shown in Fig. 1.3(e). The semiconductor material itself consists of a finite number of atoms, and the device operation has a strong influence of quantum effects that improve on performance. The vertical nanowires are

considered as the ultimate device scaling paradigm. They offer additional degrees of freedom, as the height does not limit the size of device contacts, which need to be restricted in planar and lateral device technologies. The vertical geometry should offer improved electrostatic control in extremely scaled devices, which should enable the state-of-the-art high-frequency devices as well. However, the exact path for device design is still under exploration and its performance limits are yet to be discovered. This thesis will consider a specific flavor of these devices and reveal some of their unique capabilities.

1.2.3 STATE-OF-THE-ART RADIO MOSFETS

The evaluation of high-frequency MOSFETs and other devices is compared by analyzing and comparing some specific quality-controlling metrics. Regarding the electrostatic control and the material quality, we discuss values of transconductance (g_m), output conductance (g_d), on-resistance (R_{on}), and on-current (I_{on}), among others. Additionally, some high-frequency metrics are considered as well, such as current-gain transition frequency (f_T), and maximum oscillation frequency (f_{max}). Details about derivation of these important metrics are given elsewhere [13, 14].

One figure of merit that is provided in most literature is the product of frequency and transconductance efficiency, $FoM = f_0 \cdot g_m / I_{on}$, and is given in THz/V. Here, the cut-off frequency geometric mean is taken, or $f_0 = \sqrt{f_T \cdot f_{max}}$, instead of individual cut-off frequency contributions. The transconductance efficiency allows for evaluation of the effectiveness of the charge transport in the semiconductor channel, while the cut-off frequencies reflect on device structural design. Fig. 1.4 shows a high quality gate control observed for Si-based materials, which exhibit some of the highest values. Heterojunction bipolar transistors (HBTs) are known for a having high transconductance as a measure of collector current (note that current gain, β is used as a metric in HBTs), hence they exceed all other devices in this particular metric. Their structural design allows them to minimize parasitic capacitances, and achieve high cut-off frequencies, representing the best FoM of nearly 10 THz/V. The RF-optimized Si MOSFET technologies show good FoM as well, going above 3 THz/V.

The III-V materials are very attractive for the transistor implementation, since heterostructure combinations provide flexibility in the device design. Among these, high electron mobility transistors (HEMTs) excel in their high-frequency performance, reaching cut-off frequency values above 1 THz. Their control of electrostatic coupling is not as good as in the Si-based transistors, but they benefit from III-V materials in another way - through high carrier velocity, giving them high currents and g_m values.

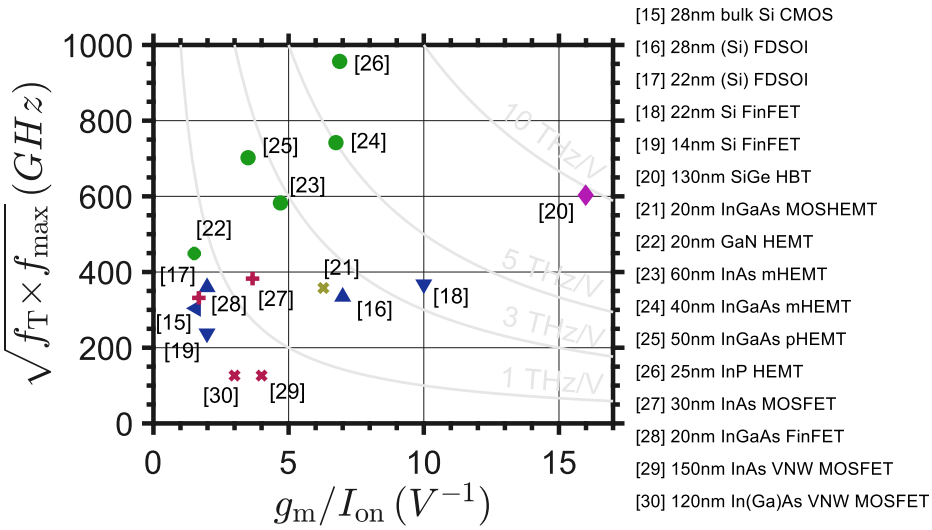

Figure 1.4: Different technologies high frequency quality measure - cut-off frequencies geometric mean w.r.t. device efficiency amplification for: Si technology [16–20], represented by blue '+' sign, the representative SiGe HBT technology [21], shown as pink diamond, a III-V MOSHEMT technology [22], shown as brown square, III-V HEMT technology [23–27], shown as green circles, and III-V MOSFET technology [28–31], represented by a red '×' sign. Thin grey lines show performance limit where figure of merit reaches 1, 3, 5, and 10 THz/V.

Therefore, their FoM is significant, even exceeding that of industrial-scale Si devices, with values well above 5 THz/V. Finally, III-V MOSFETs represent an experimental group of devices whose performance limits are yet to be assessed. These devices combine the Si MOSFET superior electrostatic control, with the III-V materials' transport properties and a structural engineering that enables high g_m and cut-off frequencies. Additionally, the III-V MOSFETs do not suffer from excessive gate leakage when scaled, like HEMTs, or from high DC power consumption, like HBTs. Therefore, a scaled III-V MOSFET is a viable candidate to compete with established technologies in terms of performance. The development of nanowire MOSFETs using III-V materials in scaled geometries have in fact resulted in some of the best individual performance metrics [15]. Their reported high-frequency performance currently is below 1 THz/V and it is challenging to optimize due to complicated device processing. Therefore, a structural optimization is needed to obtain all necessary performance metrics at the same time, and advance their high-frequency performance.

2

III-V NW MOSFET Technology Platform

The effort in creating a novel nanowire MOSFET technology platform requires many aspects of device design to be combined. The main contribution to such a platform is an accurate description the device structure. To support this effort, specific test structures need to be designed and evaluated separately. Such test structures we call *process monitor* structures. They are essentially semi-completed devices, with an added probing pad or similar, which provide evaluation of a specific device parameter. Typically, we need to know resistances in the source and drain access regions and separate them from the resistance in the MOSFET channel. Or we need an information about the gate metal resistance, in case we need to assess high-frequency data. This information then feeds into a MOSFET compact model, that is the core of the platform. The following chapter contains the description the nanowire MOSFET 1D channel transport and the compact model, as well as individual structures used in the III-V nanowire MOSFET technology platform.

2.1 NANOWIRE MOSFETS - III-V MATERIALS AND 1D TRANSPORT

The assessment and references from Chapter 1 introduce us to the world of the nanoscale MOSFETs. The interest in these structures has developed over about two decades, where the *International Roadmap for Devices and Systems* (IRDS) is establishing the future device development strategies [32]. The IRDS report states that device scaling can be maintained with nanowire technology and 3D integration of devices. This is motivated by the device electrostatic control, stemming from the GAA approach, as described in Chapter 1. Furthermore, IRDS states that such scaled

structure may be facilitated with alternative III-V materials [33,34]. These include compounds consisting of group III elements (Al, Ga, In), and group V elements (N, P, As, Sb) in the Mendeleev periodic table of elements.

The III-V compounds are attractive based on their electronic properties. A basic set of material parameters that are defined by the crystal structure and electron interactions within the crystal include the *effective mass* m^* and energy *band gap* E_g. From these, we derive other useful parameters, such as the *injection velocity* v_{inj}, the carrier *mobility* μ, and ultimately, the *mean-free-path* λ. The difference in injection velocity and mean-free-path for III-V materials is quite significant, when compared to more conventional materials with the same E_g, used in the large-scale industrial processes, such as group IV elements (Si, SiGe). This means that electrons are able to travel large distances in the crystal lattice without interacting with their surroundings (crystal lattice, impurities, other electrons). These material parameters are summarized in Table 2.1.

The presented values clearly show that III-V materials have an intrinsic advantage. Their low effective mass, coupled with a very high electron mobility, and more than twice of the injection velocity, makes them very attractive in electronic devices and circuits. The downside is the relatively low abundance of some materials (i.e. In is a scarce element), and their challenging implementation in industrial process schemes, since they are typically brittle materials. This does not prevent them from finding their place in niche applications, where conventional, Si-based technologies have

Table 2.1: Room temperature bulk material parameters for representative semiconductors and semiconductor compounds [35]. Note that these values represent theoretical values and are typically lower in fabricated devices.

Materials	Si	SiGe[a]	InAs	InGaAs[b]	InP	GaN[c]
Effective electron mass m^*/m_0	0.26	∼0.26	0.023	0.041	0.08	0.13
Energy band-gap E_g (eV)	1.12	1.005	0.354	0.74	1.344	3.2
Electron injection velocity v_{inj} ($\times 10^5$ m/s)	2.3	2.4	7.7	5.5	3.9	2.5
Electron mobility μ_e ($\mathrm{cm^2/V\,s}$)	1400	2600	40000	12000	5400	1000

[a]28% Ge [36]; [b]$In_{0.53}Ga_{0.47}As$; [c]zinc blende.

not yet shown sufficient performance (such as the high-frequency operation, see Fig. 1.4). Ultimately, one could think about integration, and aligning the III-V materials with a more conventional Si fabrication scheme. Such integration would benefit III-V materials as they rely on the Si platform for stability and large-scale integration, and it would benefit Si technology, on the other hand, by using the advantageous properties of the III-V materials.

2.1.1 PHYSICS OF NANOWIRE MOSFETS

We begin describing nanowire geometry with the evaluation of the channel structure, where we can assume that electrons can traverse without *scattering* with the crystal lattice, while the total amount of electrons participating in the transport is controlled by raising, or lowering the energy barrier with the gate potential. This effect is known as *ballistic transport*, and is illustrated in Fig. 2.1. Under such conditions, the drain

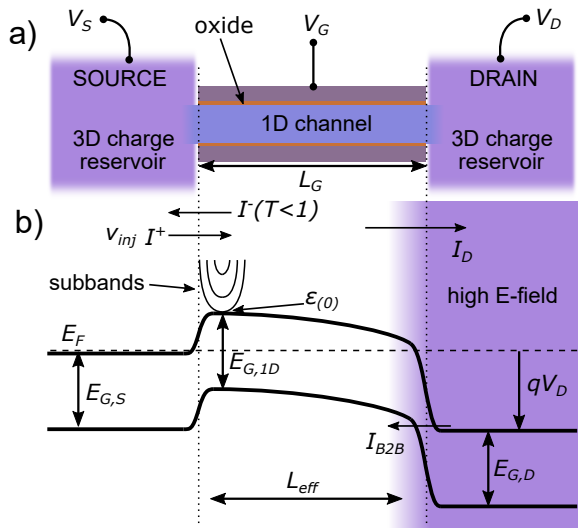

Figure 2.1: a) Schematic illustration of GAA nanowire MOSFET core, including 3D source and drain regions (electron reservoirs). The 1D channel is wrapped by an oxide and a gate metal. b) Energy landscape of source, drain, and channel regions, showing position of Fermi level E_F, conduction bands, and valence bands for all semiconductor regions, including the high electric field drain region penetrating the channel. Subband splitting is shown as well, together with top-of-the-barrier energy level $\varepsilon_{(0)}$. Drain current I_D is a combination of incident I^+ and reflected I^- current, due to finite transmission probability T. The band-to-band tunneling current I_{B2B} is shown as well, and can be suppressed with larger bandgap material on the drain side.

current of the *barrier-controlled device* can then be expressed as [13, 37]:

$$I_D = T(I^+ - I^-) = \frac{2q}{h}\int_E T(E)M(E)[f_{FD,s}(E) - f_{FD,d}(E)]\,dE, \quad (2.1)$$

where $f_{FD}(E)$ is the Fermi-Dirac distribution function of the source and drain regions, and q and h are physical constants. The term $T(E)$ is known as *transmission* and describes how ballistic the device is, and is directly related to the scattering rate. It depends on the carrier mean-free path λ, and is described by:

$$T = \frac{\lambda(E)}{\lambda(E) + L_{eff}} \quad (2.2a) \qquad \text{where } L_{eff} = \begin{cases} L_G, & \text{small } V_{DS} \\ \dfrac{k_B T}{qV_{DS}} L_G, & \text{large } V_{DS}. \end{cases} \quad (2.2b)$$

where L_{eff} is the gate length correction for high drain bias, and represents the portion of the channel where scattering reflection can still occur. The transmission changes with V_{DS} since electrons are not able to back-scatter under the presence of the high electric field in the channel region close to the drain area. Even if they scatter, they still constitute a current since they are not able to return to the source region, as shown by high electric field area and bent energy bands close to the drain reservoir, in Fig. 2.1. The mean-free-path will change as well, but is typically assumed as energy-independent. The transmission relation will be close to unity in a case where $\lambda >> L_{eff}$, while in quasi-ballistic devices, $\lambda \approx L_{eff}$, and transmission has values between 0.3 and 0.8.

The $M(E)$ term in (2.1) represents the number of available charge energy states that can participate in the transport, and is directly proportional to 1D *density of states* (DoS). It is given by [37, 38]:

$$M(E) = L_G \frac{h}{4} v_{inj} D_{1D}(E), \quad (2.3)$$

where L_G is the MOSFET gate length, and $D_{1D}(E)$ represents the 1D density-of-states (DoS), given as:

$$D_{1D}(E) = \frac{1}{\pi\hbar}\sqrt{\frac{2m^*}{E - \varepsilon_{(0)}}}, \quad (2.4)$$

where $\hbar = h/2\pi$ is the reduced Planck constant, and $\varepsilon_{(0)}$ is a lowest subband energy level or top of the barrier. From (2.3) and (2.4), $M(E)$ gives us 1 for a single occupied subband in a scaled nanowire (few nm

in diameter) at zero temperature, while for a typical nanowire (10s of nm), the bands are positioned closer together, and smeared in values due to temperature dependence of the Fermi-Dirac distribution function, thus making this number larger. Note that the expression (2.4) is based on parabolic band approximation, which is typically correct only for a small energies and wave vectors. A more rigorous treatment of these expressions would include corrections or even numerical solutions, but it is outside of the scope of this thesis.

2.1.2 COMPACT MODELLING OF NANOWIRE MOSFETS

For the purpose of device evaluation and circuit design, a device compact model is developed, instead of rigorously evaluating MOSFET operation based on physical expressions. The strategy behind compact modelling should always be to enable use of a device model in a variety of simulation environments. It needs to represent the semiconductor behavior in a sufficiently accurate manner, as well as to account for the environment surrounding the device. Furthermore, the compact models are verified in circuit design and implementation, where feedback is provided to both device design and to the compact modelling. There are many models that consider the physical aspects of device behavior, and they rely on many parameters to describe this behavior accurately (i.e. SPICE models). Therefore, the selection of compact modelling environment is essential in understanding the device operation and should be related to the physical device description.

The compact model used to describe nanowire MOSFETs in this thesis is based on physical parameters described in the previous subsection. It takes into account all the aspects of the ballistic transport as well as dimensioning the device channel, and is known in the literature as *virtual-source model* (VS model) [39–42]. The current description is similar to the relation (2.1):

$$I_D = W_G Q_{ix0}(V_{GS}, V_{DS}) v_{x0} F_s, \tag{2.5}$$

where W_G is gate width, Q_{ix0} is total voltage-dependent channel inversion charge, v_{x0} is the carrier velocity at the 'virtual source', and F_s is the smoothing transition function from linear region to saturation region. Comparing (2.1) to (2.5), we can easily come to the conclusion that the virtual source velocity is the injection velocity, v_{inj}, scaled by the transmission factor T, while channel inversion charge will be given as:

$$Q_{ix0} = -q \int_E D_{1D}(E) f_{FD}(E)\, dE \approx n C_{inv} (V_{GS} - V_T)^{\alpha}, \tag{2.6}$$

where n is a subthreshold slope dependent parameter, C_{inv} is on-state (strong inversion) gate capacitance, and α is a parameter that has value close to 1 in device on-state, in case of most short-channel devices. The channel inversion charge Q_{ix0} depends on V_{DS}, through threshold voltage, $V_T = V_{T0} - DIBL \cdot V_{DS}$. Finally, the smoothing function F_s is a saturation- and mobility-dependent function that describes transition between different regimes of operation:

$$F_s = \frac{V_{DS}^{'}/V_{Dsat}}{(1 + (V_{DS}^{'}/V_{Dsat})^{\beta})^{1/\beta}}, \tag{2.7}$$

where $V_{Dsat} \sim v_{x0}L_G/\mu$ is a gate length and mobility dependent function that scales the saturation velocity. Here, the mobility μ is not related to the material-based parameter μ_e, as in a classical diffusive transport, but should be seen as a fitting parameter. The voltage $V_{DS}^{'}$ is intrinsic drain-source voltage, excluding the device access resistances ($V_{DS}^{'} = V_{DS} - I_D \cdot (R_S + R_D)$), while β is another fitting factor that sets the shape of the device output characteristic. Using these simple expressions, the device complex characteristics are easily described, using only a few fitting parameters. Such a model implementation in circuit environment becomes rather straightforward.

2.2 LAYOUT OF NANOWIRE MOSFET

A very important segment in building the technology platform, aside from the compact modelling of the device, is the layout design of the device itself. A standalone device layout with electrical contacts is known as front-end-of-line (FEOL), while the interconnect stack that is used to realize circuit functionality is named back-end-of-line (BEOL). The smart use, and scaling of these layouts has always been an advantage of Si CMOS process. [43,44]. The density rules are introduced, to limit device variability and increase yield. However, these density rules drive the reduction in the contact area in FEOL, and increased parasitics in scaled BEOL, which may negatively impact the device high-frequency performance. High-frequency MOSFETs therefore require less stringent density rules to achieve optimum high-frequency operation. Here, a specific process flow and layout of III-V vertical nanowire (VNW) MOSFETs is discussed, being a rather unique approach to device design.

The III-V VNW MOSFET process flow starts with an epitaxial growth facilitated by a catalyst (Au). The intrinsic nanowire segment grows from underneath the Au island, while the catalyst size determines the diameter

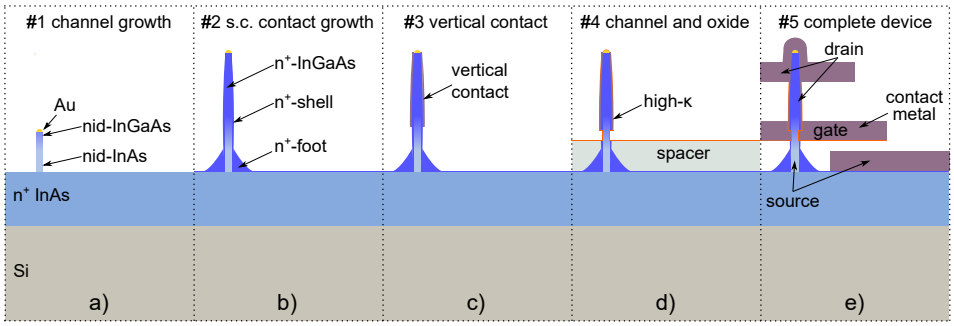

Figure 2.2: A general process flow of III-V VNW MOSFETs: a) formation of InAs and graded InAs/InGaAs segment, b) semiconductor contact overgrowth (Sn-doped InGaAs) - formation of the shell and nanowire foot, c) deposition of vertical contact (improved contact resistance), d) removal of highly-doped shell from channel region and gate dielectric deposition, and e) metallization, and complete outlook of device with terminal contacts.

of the nanowire, as shown in Fig. 2.2(a). Initially, InAs segment is grown, while subsequently Ga is incorporated, to achieve channel grading from InAs to InGaAs. Following the grading, a Sn-doped InGaAs segment is grown. At the same time, the material overgrows the nanowire sidewalls, creating a core-shell structure, as shown in Fig. 2.2(b). The overgrowth of the doped semiconductor forms low-access-resistance drain/source regions. A protective mask is defined, and the top portion of the wire is covered in metal, followed by a selective etching step that removes the metal from the planar surface. This leaves metal on the nanowire sidewall only, forming a large drain contact area. The vertical contact is illustrated in Fig. 2.2(c). In the next step, a spacer is defined, and the area between the spacer and the vertical contact is oxidized, after which a selective etching of the III-V oxide is performed, to remove the highly-doped shell and expose the intrinsic nanowire channel (Fig. 2.2(d)). The area is covered in a high-κ gate dielectric, to separate the gate electrode from the semiconductor channel. In the final step, metal terminals are formed, thus finalizing the device fabrication (Fig. 2.2(e)). A more complete process description can be found in [45].

These crucial steps help in understanding some advantages in the vertical nanowire devices. The vertical placement of device terminals allows for decoupling of the device contact regions from the device footprint, as opposed to any laterally oriented device. Additionally, metals are routed on three different heights and have to be separated and supported by dielectrics. This provides circuit designers with the opportunity to create

interconnects using only FEOL layout layers, thus reducing the total amount of necessary BEOL layers. Furthermore, the nanowires are grown on top of the highly-doped InAs buffer layer, grown on a high-resistivity Si substrate. Shaping this buffer layer into an island (mesa) enables a fully isolated device. A layout depiction of the III-V VNW MOSFET is shown in Fig. 2.3.

Fig. 2.3(a) shows typical two-gate-finger III-V VNW MOSFET, intended for RF and mm-wave operation. The most standard way of fabricating RF devices is by patterning the gate metal into finger structures. In planar technologies, gate fingers are used to create a compact device layout and reduce the gate resistance. Additionally, in VNW MOSFETs, each gate finger will contain two rows of equidistant nanowires, with 200 nm spacing between nanowires (Fig. 2.3(b)). In this way, an equal amount of material is available for each nanowire during growth, and the spread in the nanowire height and diameter is minimized. Finally, Fig. 2.3(c) shows a 200 nm × 250 nm nanowire unit cell, typically with 28 nm nanowire core placed in the right third of the unit cell. The unit cell is symmetric, to allow for easy device routing. The dimensions are relaxed to enable low gate resistance, while minimizing parasitic parallel-plate capacitance.

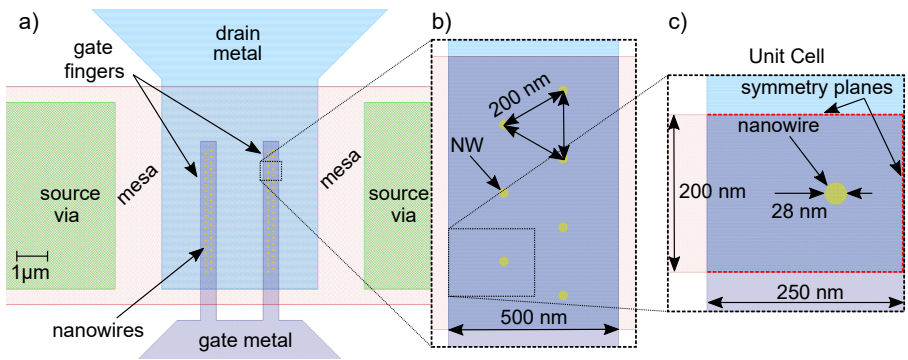

Figure 2.3: a) Layout of high-frequency VNW MOSFET with a mesa island on which the source contact vias are placed, a gate metal with a finger-like shape, and a drain metal pad cover. The overlaps are reduced to minimize parasitics. b) A zoomed-in view of a single gate finger, showing two parallel columns of nanowires ordered in an equidistant manner (200 nm spacing). The gate finger width is 500 nm. c) An enlarged symmetric unit cell, sized as 200 nm×250 nm. showing symmetry planes, as well as the 28 nm nanowire position. The gate metal is wide, to enable the device high-frequency operation.

2.3 PROCESS MONITOR STRUCTURE DESIGN

During the development of the nanowire MOSFET technology platform, the specific device properties need to be assessed separately. To achieve this, process monitor structures are designed. In essence, these structures represent a portion of the nanowire MOSFET, used for evaluation of a particular device functionality. The parameters obtained with process monitor structures typically include contact resistances, or channel capacitances. The key is to integrate such structures into the main process flow.

The first such evaluation structure is a transmission-line measurement (TLM) kit. It is used for the evaluation of the vertical (drain) contact. Fig. 2.4 shows key process steps that enable fabrication of the TLM kit alongside the VNW MOSFETs. Initially, the vertical contact height is defined using an electron-beam exposure-sensitive layer, known as hydrogen silsesquioxane (HSQ) [46]. The delivered electron-beam dose affects the resulting HSQ height (Fig. 2.4(a)). Note that the critical dimension becomes the mask layer height, not the width, which is a paradigm change, when compared to planar technologies.

From this point on, the process flow splits into two parallel branches. In both cases, another HSQ exposure step is used. In case of the III-V VNW MOSFETs, a low electron-beam dose is delivered to the layer, thus opening the MOSFET channel region, as depicted in Fig. 2.4(b). Such process flow branch has been successfully implemented in a gate-length scaling study, demonstrating an exceptional performance [47]. The other process flow branch yields the TLM kit process monitor structures, shown in Fig. 2.4(c). A high electron-beam dose is delivered to the HSQ layer, nearly covering the nanowire. The vertical contact and the HSQ prevent the selective etching of the nanowire. The uncovered part is subsequently metallized, completing the two-terminal structure (InAs mesa is used as

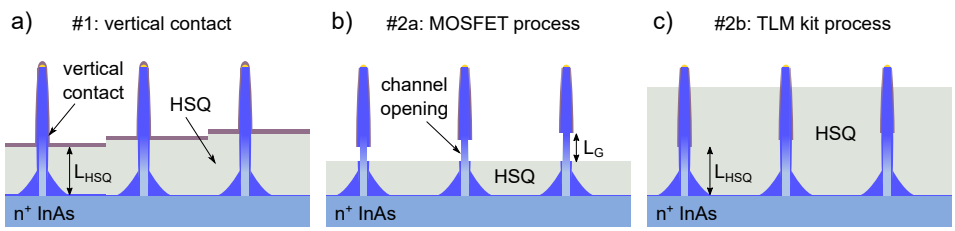

Figure 2.4: A part of the VNW MOSFET process flow: a) vertical contact formation with varying HSQ height (electron-beam dose), b) thin HSQ layer allows for a MOSFET channel opening, c) thick HSQ layer nearly covers the nanowire and protects the semiconductor from etching.

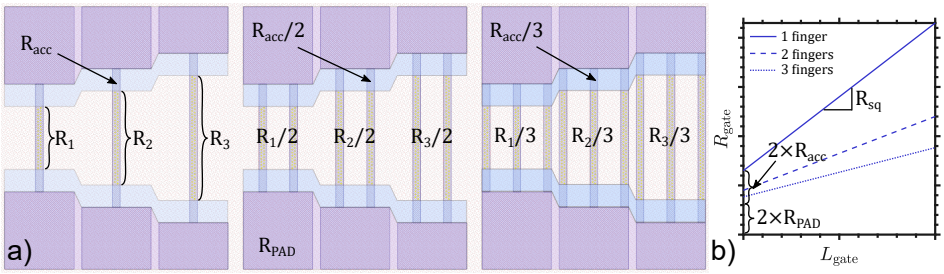

Figure 2.5: a) A layout of the gate metal process monitor structures, marking different resistance contributions. b) A typical resistance VS finger length measurement, with different contributions to the gate resistance clearly marked.

a second terminal). The highly-doped shell remains intact and can be characterized via the TLM measurement. Therefore, in a single mask step, both the VNW MOSFET and the vertical contact TLM are integrated.

In a similar manner, the device gate metal resistance can be evaluated. The gate resistance is essential in the evaluation of the MOSFET RF performance, where it is deembeded from the high-frequency admittance parameters (y-parameters). The gate process monitor structure is depicted in Fig. 2.5(a). Three separate contributions to the gate resistance are identified: a gate pad resistance R_{PAD}, a gate finger access resistance R_{acc}, and a gate finger resistance R_{sq}. The R_{PAD} and R_{acc} contributions to the gate resistance is typically small, since they represents the resistance in the metal pad and the short finger access line. The largest contribution is the R_{sq}, as it represents the portion of the gate metal that is perforated with nanowires, which increases its resistance value. The resulting measurements from such structures are depicted in Fig. 2.5(b). If scaling of the finger length and the number of fingers is provided, the individual contributions can be evaluated and layout optimized for low-gate-resistance high-frequency VNW MOSFETs.

Finally, capacitance evaluation is needed as well. Capacitance-voltage (CV) measurements are typically used to assess charge density in the channel and the frequency dispersion in the gate oxide. The CV process monitor structures are intended to be fabricated alongside the RF MOSFETs, therefore their layout designs are similar. The structures contain an isolated device mesa and the gate fingers, while the difference is visible in the layout of the source and drain terminals. For CV process monitor structures, the source/drain terminals are connected, making the CV structure a two-terminal structure. Fig. 2.6 depicts an example RF VNW MOSFET and an example CV VNW process monitor structure. The 180

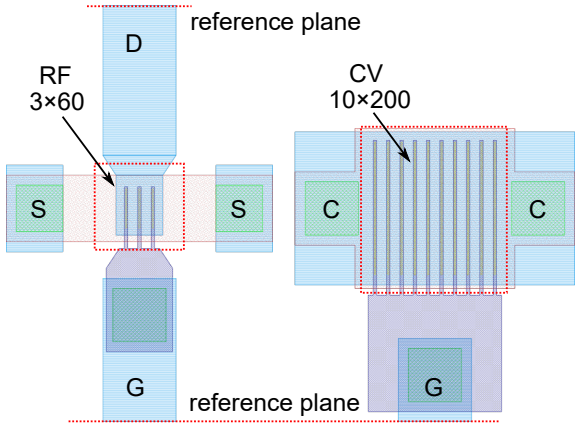

Figure 2.6: Comparison between 3×60 RF VNW MOSFET and 10×200 CV vertical nanowire process monitor structure. The increase in the device size allows for an accurate capacitance evaluation.

wires in the RF VNW MOSFET are sufficient to evaluate the the device RF performance. On the other hand, the CV VNW process monitor structure typically consists of a large array of nanowires (the example shown in the figure contains 2000 wires). The total device capacitance will be large, allowing the low-frequency-measurement instruments to accurately assess the gate capacitance, as well as the dispersion in the gate oxide. Following the optimization of the device high-frequency operation, such process monitor structure becomes an essential tool in understanding the capacitance bottleneck in an RF device. Using this, and the other process monitor structures, the entire process flow can be monitored and the individual blocks of the vertical nanowire MOSFETs can be optimized for increased performance.

3

High-Frequency BEOL for III-V NW MOSFETs

The nanowire (NW) MOSFETs described in the previous chapter represent the FEOL part of the integrated circuit design. This chapter provides insights into a custom BEOL, developed to assist in the III-V NW MOSFET optimization, and performance evaluation. A specific focus is given to the high-frequency design, revolving around transmission line design and integration. Furthermore, a great deal of effort is dedicated to developing a suitable BEOL environment for high-frequency signal propagation. To complete the story, an overview of passive components is provided. A unique take on the BEOL performance assessment is showcased, through an integration with novel materials, such as thin ferroelectric films.

3.1 TRANSMISSION LINE THEORY

To understand how circuit design using BEOL can be done, a discussion is provided about the realization of the transmission line environment. It is an essential part of high-frequency circuits, ranging from inductors and transformers in a dense RF CMOS process, to the long line segments used in impedance transformation in III-V mm-wave integrated circuits (MMICs), which are also the focus of this thesis. Before discussing the circuit realization, however, a basic description of the transmission line environment is provided.

Each transmission line (TL) segment can be represented with its distributed circuit parameters. They are referred to as distributed line inductance $L^{'}$, capacitance $C^{'}$, resistance $R^{'}$, and conductance $G^{'}$. They model electromagnetic fields that exist, or are terminated within the

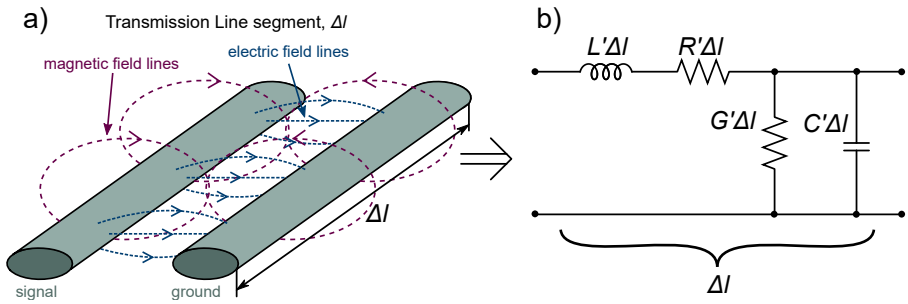

Figure 3.1: a) An illustration of the transmission line (TL) segment (Δl) with depicted electric and magnetic field lines. b) Equivalent circuit of the TL segment.

space between signal and ground metal segments, as depicted in Fig. 3.1. Important to note is that both signal lines and ground planes conduct high-frequency currents, and therefore, the geometry of the signal line and the ground plane will determine their field coupling. Together with material properties (metal resistivity, skin effect, dielectric permittivity), they define the TL distributed parameters.

Investigating the relation between TL distributed parameters for a given line length l, the relation between input voltage wave to input current wave will give the following relationship:

$$Z_0 = \frac{v_+}{i_+} = \frac{v_-}{i_-} = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \approx \sqrt{\frac{L'}{C'}}, \tag{3.1}$$

where $v_{+/-}$ and $i_{+/-}$ are incident and reflected voltage and current waves, respectively. The resulting impedance, Z_0, is called the characteristic impedance, and it represents the approximate relationship between line inductance and the signal-to-ground line capacitance, in the case of low-loss TLs. The standard Z_0 value in most microwave designs is 50 Ω, a historical value of matched radio systems, representing a balance between insertion loss and power handling capabilities in printed circuit board transmission lines [48].

The differential equation describing the current-voltage relationship at the position x on a transmission line is given by telegrapher's equations [49]:

$$\frac{\partial V(x)}{\partial x} = -(R^{'} + j\omega L^{'})I(x), \text{ and } \frac{\partial I(x)}{\partial x} = -(G^{'} + j\omega C^{'})V(x); \tag{3.2}$$

$$\frac{\partial^2 V(x)}{\partial x^2} = \gamma^2 V(x), \text{ and } \frac{\partial^2 I(x)}{\partial x^2} = \gamma^2 I(x), \tag{3.3}$$

where $V(x)$ and $I(x)$ are the instantaneous current and voltage at the position x. The parameter γ is the complex propagation constant of the transmission line:

$$\gamma = \alpha + j\beta = \sqrt{(R' + j\omega L')(G' + j\omega C')}, \tag{3.4}$$

where α is the line attenuation, and β is the phase constant. The assessment of the TL performance is established through assessment of propagation parameters α and β, and reveals the TL performance limit, as well as any network and passive component built with TLs. Additionally, the phase constant is a direct measure of transmission line guided wavelength, or $\beta = 2\pi/\lambda$, where λ is the wavelength, given as $\lambda = f/c\sqrt{\varepsilon_{eff}}$, where f is the frequency of the electromagnetic wave, c is the speed of light, and ε_{eff} is the effective dielectric constant that depends on the material and the geometry of the transmission line.

When a (voltage/current/power) wave is excited on the transmission line, a reflected wave may appear. The relationship between the reflected wave and the incident wave is named the reflection coefficient Γ. The reflection coefficient is a direct way of probing the impedance seen in the specific part of the circuit, and is used for matching different segments of the circuit to each other [50]. The relation between a given impedance Z, and the reflection coefficient Γ is given as:

$$\Gamma = \frac{v_-}{v_+} = \frac{i_-}{i_+} = \frac{Z - Z_0}{Z + Z_0}. \tag{3.5}$$

This relationship is bilinear, and allows for normalization of the impedance to a unity circle in the complex plane. Such mapping of impedances through their reflection coefficients is known as the *Smith chart*. Since TLs transform the reflection coefficient based on the line length and γ, given in (3.4), the reflection coefficient along the transmission line will be transformed as $\Gamma_l = \Gamma e^{\gamma l}$, thus allowing rotation in the complex plane and consequently, an impedance transformation. This line property is used heavily in matching networks, where usually an arbitrary impedance transformation is required.

3.2 BEOL FOR III-V NANOWIRE MOSFET

The multi-layer metal stack that is inherent to III-V VNW MOSFET, as described in Chapter 2, allows for the possibility for utilizing the FEOL metal stack in BEOL as well. Such a concept has been already attempted in the realization of a nanowire-based mixer circuit [51]. In this thesis, an effort is made to generalize these concepts and build a BEOL stack that would include a library of passive components and TLs, as the integral part of the technology platform. The following subsections provide insights into the realization of the TLs and passive components, and the utilization of the *low-κ dielectric layers* (materials with low relative permittivity ε_r), stemming from various BEOL stacks considered for integration into the III-V VNW MOSFET technology platform. An attempt is made to route TLs on different metal layers, which affects the performance of the TLs and integrated passive components, as well as the complexity in the circuit design.

3.2.1 TRANSMISSION LINE REALIZATIONS

Considering the principles of the TL operation, two flavors of the TL realization are considered: co-planar waveguide (CPW), and microstrip (MS) TL segments. Both are depicted in Fig. 3.2. The CPW lines (Fig. 3.2(a)) are realized in a single metal layer, denoted as *MET1*. The CPW line consists of a signal line of width w, with a very wide ground plane on each side, separated by a clearance s. The electromagnetic (EM) field coupling for transverse-electric-magnetic (TEM) wave propagation are illustrated as well. A portion of the field-lines couples in air, while another portion couples within the substrate. This results in ε_{eff}, γ, and Z_0 values depending on the geometry of the CPW line, as well as supporting substrate's ε_r. These key parameters are typically determined numerically, or semi-empirically [52, 53].

The second flavor of the TL realization is the MS line (Fig. 3.2(b)). It represents a more traditional, Si-CMOS-like approach to BEOL design, using a multi-layer metal stack. Both the signal line, and the ground plane are realized in raised *MET2* and *MET3* layers, respectively. The EM field-lines are isolated from the underlying substrate and limited to the signal-to-ground dielectric separator and the surrounding air, rather than penetrating into the often lossy substrate. Compared to CPW, the MS lines have an advantage due to independent selection of the supporting dielectric layer thickness. This low-κ dielectric, together with the signal line width, sets the key TL properties, which are also determined semi-empirically [54, 55].

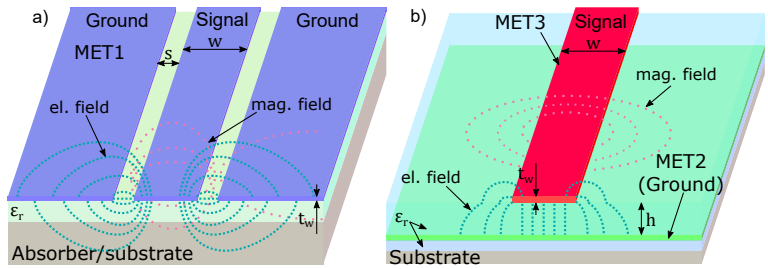

Figure 3.2: a) Schematic illustration of a co-planar waveguide (CPW), including the signal line of width w, clearance s, and wide ground planes, realized in BEOL *MET1* layer. The EM field-lines illustrate denser electric field coupling in the underlying dielectric/substrate. b) Schematic illustration of a microstrip (MS) line, including a wide ground plane, realized in BEOL *MET2* layer, separated from the substrate with a low-κ interlayer dielectric. Another low-κ dielectric layer of height h, supports the signal line of width w, realized in BEOL *MET3* layer. The EM field-lines show broken electric field lines as they cross from air into the dielectric.

3.2.2 CO-INTEGRATED RF BEOL

Utilizing the CPW lines alongside the III-V VNW MOSFETs, a co-integration is realized. Key passive and active components are implemented using available FEOL layers, minimizing the amount of added BEOL layers. The schematic illustration of the FEOL-BEOL co-integration is shown in Fig. 3.3. A low-κ interlayer dielectric is used as a planarization layer that supports the MOSFET contacts, as well as the CPW lines, realized in *MET1* layer. The CPW ground planes are connected via an *underpass*, a metal layer routed on Si substrate, instead of a bridge, routed above the CPW line. Line bends, crosses and tees use the underpass layer to connect various ground plane sections, ensuring the same potential level in each ground plane section, and preventing unwanted reflections in the TEM wave propagation. The combined height of the III-V VNW MOSFET and the source mesa island result in a sufficient CPW-to-underpass separation, which exhibits low parasitic capacitance.

The capacitors are realized in several ways. Fig. 3.3 depicts a case where the gate metal and the CPW line are used to realize a low-capacitance-density metal-oxide-metal (MOM) capacitor [43, 44]. A high-capacitance-density metal-insulator-metal (MIM) capacitors are realized using an additional high-κ dielectric layer, sandwiched in between the drain contact metal and the CPW line. In an another MIM capacitor version, the source mesa contact layer is used as an electrode, while the MOSFET gate high-κ is used as the capacitor dielectric. Furthermore, a

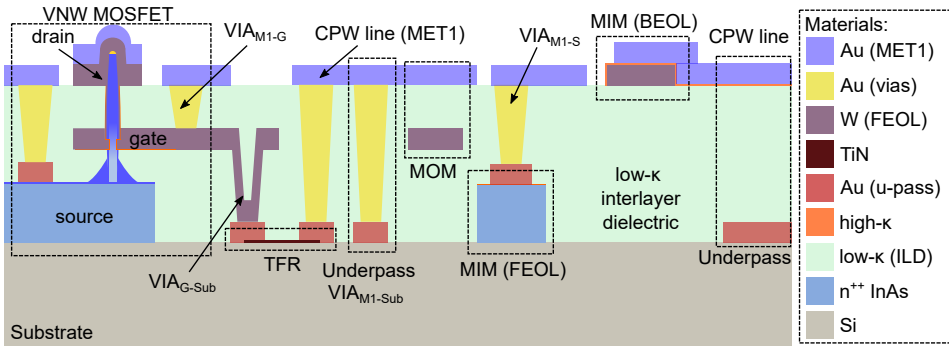

Figure 3.3: Schematic illustration of the III-V VNW MOSFET, co-integrated with BEOL components, including thin-film resistors (TFR), MIM/MOM capacitors, underpasses, CPW lines, and various interconnect vias. Materials used in realization of the FEOL/BEOL layers are listed as well.

thin-film-resistor (*TFR*) layer is routed on Si substrate. The *TFR* layer is primarily intended for use in a DC biasing circuit, or to stabilize the VNW MOSFETs, together with BEOL capacitors. Finally, low-loss interconnect vias are realized on different levels, connecting various components into circuits.

3.2.3 MILLIMETER-WAVE BEOL

While the co-integrated BEOL adds functionality using a minimum amount of added lithography steps, the BEOL components are restricted in their design and realization. A front-side BEOL layer stack, as illustrated in Fig. 3.4, removes this limitation. The first aspect of this BEOL is the use of a first interlayer dielectric *ILD1*. The layer is thick enough to efficiently planarize tall structures such as III-V VNW MOSFETs, while simultaneously isolating mm-wave signals from reaching the substrate. If the *ILD1* layer is too thick, however, the interconnect via parasitics would be large, so a good balance was found at 2 µm layer thickness. The *ILD1* layer supports a *MET2* ground-plane layer. The dielectric layer supporting the RF and mm-wave signal propagation is denoted as *ILD2*. The thickness of this layer is also a careful balance of interconnect via parasitics and the MS line performance.

Since the substrate needs to be isolated to reduce losses, the strategy is to reduce openings in the ground plane. Therefore, all passive components are routed in the RF environment. Since interconnect vias are not needed for connecting these passive components, aside from ground vias, their parasitics are also minimized. A *TFR* layer is deposited on the *ILD2* and

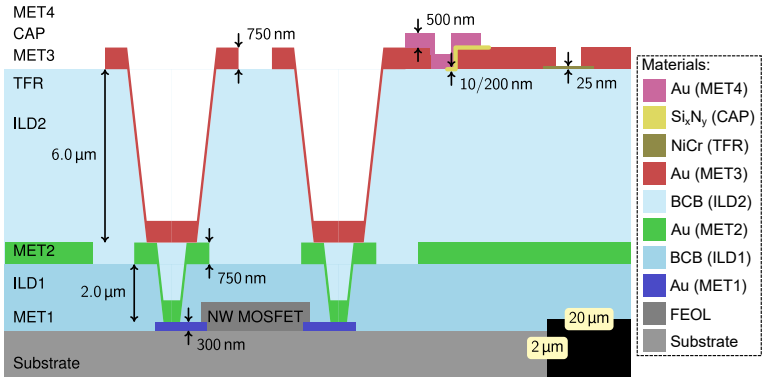

Figure 3.4: Schematic illustration of a mm-wave front-side BEOL layer stack, with two dielectric interlayers (*ILD1-2*), four metal layers (*MET1-4*), *TFR*, MIM capacitor layers (*CAP*), and interconnect vias. Layer thickness values and materials used in the realization of this BEOL, are marked as well.

contacted with the *MET3* layer, while capacitor layers are patterned with different thickness values, to enable both high- and low-capacitance-density films. An additional metal layer (*MET4*) will create the second capacitor electrode, forming a high quality MIM capacitor. This way, a complete component set is provided for the design of high performance mm-wave circuits.

3.3 BEOL PERFORMANCE EVALUATION

When realizing the BEOL layer stack, the important point to consider is materials used for BEOL fabrication. In Fig. 3.3-3.4, some of the essential materials are listed. Among them, the low-κ interlayer dielectric is the most important. It supports TL segments, and serves as a medium where EM field-lines will propagate. Therefore, properties of this layer are crucial in establishing the TL performance. In this thesis, all BEOL interlayers are realized with benzocyclobutene (BCB) - a spin-on organosilane compound with excellent planarization properties [56, 57]. Its low dielectric constant of $\varepsilon_{BCB} \approx 2.8$ extends well into mm-wave frequencies, where the dielectric has been evaluated up to 1 THz [58].

In addition, as passive components and interconnect vias measure tens of µm in size, there needs to exist a way to characterize them at high frequencies without measuring cables, connectors, probing equipment, and various instrument inaccuracies [59]. Therefore, a on-wafer-measurement *calibration kit* is developed. The simplest one, relying solely on TL

segments, known as the *Thru-Reflect-Line* (TRL) calibration kit, is implemented and characterized, allowing for line performance evaluation.

3.3.1 TRL CALIBRATION AND TRANSMISSION LINE PROPERTIES

The TRL kit is a simple TL-based instrument measurement-error correction kit. Much like every other calibration kit, TRL is comprised of several calibration standards. There is always a *THRU* standard - two measurement ports connected to each other, where amplitude and phase relation between the ports is obtained. The *REFLECT* (*OPEN* type, or *SHORT* type) standards are those that exhibit $\Gamma \approx \pm 1$, and are used primarily for setting the individual port phase offset, as well as defining the amplitude in the polar plane. Finally, the *LINE* standard is used to establish a delay between the calibration reference planes. The TRL kit typically comes with many lines, and is named a multiline TRL, or mTRL. The TLs are designed in a specific way in order to have a specific set of time delays with each line set. This allows for a wideband calibration, with minimal error propagating at the band edges. A typical recommendation is to design a line that has length equal to $\lambda/4$ at the desired frequency, and a three times longer line, to extend the calibrated bandwidth [60].

The core difference of mTRL, as compared to other calibration kits, is in the use of the line Z_0 as the normalization impedance [60–65]. In comparison, other available calibration standards, such as Line-Reflect-Reflect-Match (LRRM), or Thru-Match-Reflect-Reflect (TMRR), rely on measurement of a high-precision 50 Ω *MATCH* for the system impedance normalization. [66–71]. The value of Z_0 must be fully known for the mTRL calibration to be applicable. Since Z_0 cannot be properly determined sometimes (i.e. due to complex line geometry), the line capacitance model can be used, which, in combination with the measured standards, can yield the line characteristic impedance [72]. Additionally, a separate evaluation of the line propagation constant can yield results as well [73]. Measurements on many lines, as well as several *REFLECT* standards removes measurement uncertainty, so mTRL is often a good choice for high-frequency (RF and mm-wave) calibration.

Optical micrographs of the implemented TRL kit with CPW lines, and with MS lines, are shown in Fig. 3.5. The calibration kits are realized keeping in mind that an evanescent mode, alongside a quasi-TEM mode, is launched from the probe tip onto a landing pad, and it needs to be allowed to diminish before reaching the set reference plane. Therefore, in addition a probe landing pad, each calibration standard contains a *line access segment*, that shifts the reference plane away from the probe landing pad. The CPW-based probing pads do not contain any vias (Fig. 3.5(a)), due to

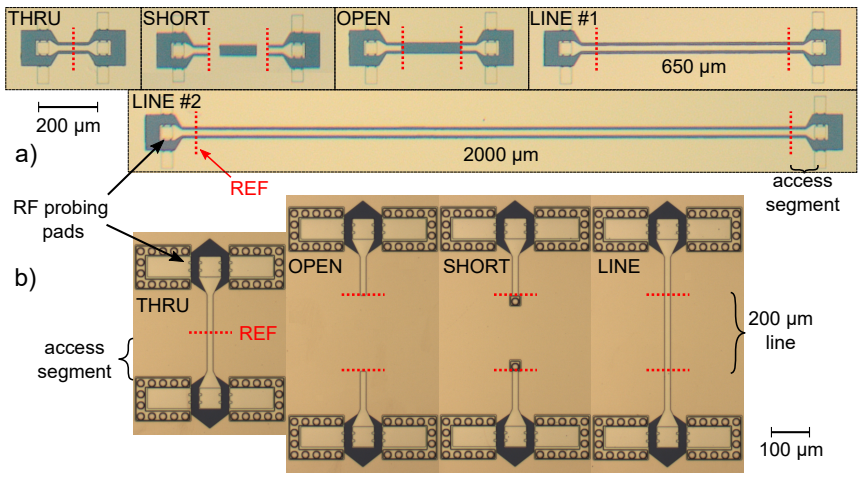

Figure 3.5: Optical micrographs of TRL kits, realized in BEOL as: a) CPW structures for RF BEOL: *THRU*, *OPEN*, *SHORT*, and *LINE*; b) MS line structures for mm-wave BEOL: *THRU*, *OPEN*, *SHORT*, and *LINE*. The CPW lines are realized in *MET1* BEOL layer, while the MS lines are realized in *MET3*, with the underlying ground plane realized in *MET2* BEOL layer and vias that connect landing pads for ground connection.

both signal line and ground plane being realized in the same *MET1* layer. The MS-based probing pads, however, have their ground pads connected to the *MET2* ground plane with interconnect vias, while signal line is routed in the *MET3* layer (Fig. 3.5(b)). The line access segment length is 50 µm and 100 µm, in case of CPW-based and MS-based TRL kits, respectively. An example TL segments are shown in Fig. 3.5(a), where CPW-based mTRL kit contains 650 µm and 2 mm line, for 5-90 GHz calibration range. The MS-line-based mTRL kit (Fig. 3.5(b)),with its 200 µm line, covers the W-band (75 GHz to 110 GHz).

Evaluating the mTRL calibration, we obtain essential line properties. Fig. 3.6(a) shows measured and simulated attenuation of the CPW line, a TL parameter typically used as a benchmark value. In case of a 500-nm-thick *MET1* layer, we obtain $\alpha \approx 0.6$ dB/mm at 50 GHz. The simulated data is obtained using line models developed in Keysight Advanced Design Systems (ADS). Describing line geometry and material parameters in ADS, the TL behavior is reproduced in simulation, as demonstrated in Fig. 3.6(b). Regarding MS line evaluation, Fig. 3.6(c) shows that groundplane cover isolates the underlying substrate from the RF environment, as no significant substrate effect in the measured line attenuation is observed. Furthermore, the attenuation value for a 50 Ω

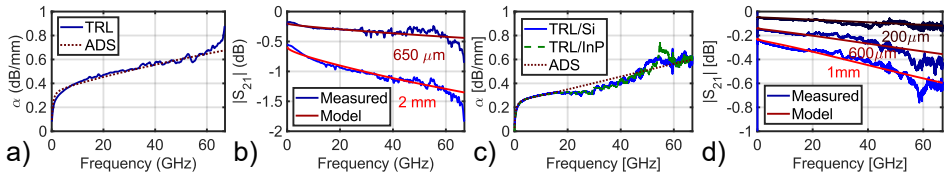

Figure 3.6: Measured and simulated CPW line properties: a) attenuation α, and b) line loss ($|s_{21}|$) VS. frequency, for 50 Ω CPW lines of different lengths. c) Measured and simulated MS line attenuation on III-V (InP) and on Si substrate, showing efficient groundplane isolation. d) Measured and simulated line loss versus frequency for different 50 Ω MS line lengths.

MS line is $\alpha \approx 0.5$ dB/mm at 50 GHz, a state-of-the-art value, when compared to both the RF CMOS and MMIC design kits [58, 74]. Finally, Fig. 3.6(d) demonstrates the fit between measured and modelled MS lines where, much like for CPW lines, the behavior can be accurately predicted.

3.3.2 RF BEOL COMPONENTS - FERROELECTRIC MOS CAPACITORS

Extending the BEOL component evaluation past the TL sections, the evaluation of thin ferroelectric films, an emerging material that promises steep-slope MOSFETs, among other applications, is attempted at high frequencies [75–78]. The RF BEOL process yields ferroelectric MOS capacitors (MOSCAPs), a MIM capacitor variety presented in Subsection 3.2.2. In a modified process, a non-intentionally-doped InAs layer grown on a high-resistivity Si substrate is used, as compared to the highly-doped InAs buffer, used for conventional MOSFETs [79,80]. This allows for capacitance modulation of the MOSCAP structure, with the aim to capture this effect in the RF environment as well.

Fig. 3.7(a) depicts a ferroelectric MOSCAP structure. The structure is designed to have minimal extension from the calibration reference plane, so that distributed effects associated with the structure can be neglected at RF frequencies. The capacitor area is approximately 30 µm^2, and is accessed through an interconnect via from the *MET1* layer down to the metal electrode. The InAs mesa structure is routed to the ground plane on both ends, thus reducing the mesa resistance by a factor of two. In a similar design, a *TFR* layer is patterned, to realize the 50 Ω *MATCH* standard is realized, so that a LRRM calibration can be performed.

Three different thicknesses of a ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ film were measured. For 15nm, to 10nm, and 6nm, all three films show distinct ferroelectric peaks when voltage is swept in either direction. Fig. 3.7(b-d) shows measurement results. Each point on the plot is a result of

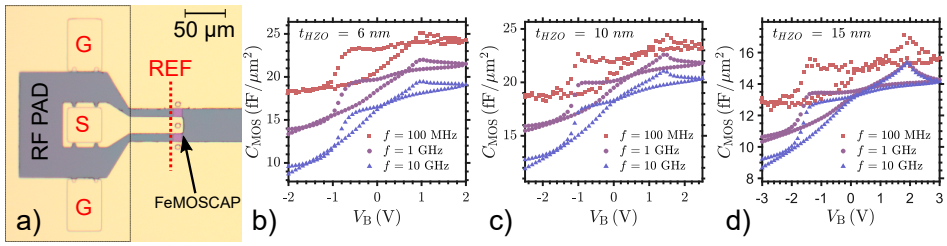

Figure 3.7: a) Optical micrograph of a test structure for the assessment of a ferroelectric MOSCAP. The structure is relatively small compared to the incoming signal wavelength. Plots show capacitance-voltage measurements of ferroelectric MOSCAPs, for the layer thickness values of: b) 6 nm, c) 10 nm, and d) 15 nm $Hf_{0.5}Zr_{0.5}O_2$. Distinct ferroelectric peaks appear at frequencies in the measurement range from 100 MHz, up to 10 GHz, demonstrating the highest recorded characterization frequency for $Hf_{0.5}Zr_{0.5}O_2$ film.

continuous wave (CW) excitation from the vector network analyzer, for a fixed bias voltage V_B. The ferroelectric film retains its polarization during the measurement, as seen through the measured capacitance. Moreover, the frequency dispersion in capacitance value is evident, with previously observed trends extending into the RF frequencies [79, 80]. The measurement results serve as a proof-of-concept for capturing material properties in the RF domain. This initial step lays foundation for RF analysis of ferroelectric MOSFETs [81].

3.3.3 MILLIMETER-WAVE BEOL COMPONENTS

For the mm-wave BEOL kit, it is essential to evaluate the MS line performance, but the parasitic contribution of the interconnect vias has to be considered as well. Their behavior is characterized in order for the model to predict the combined FEOL and BEOL contribution [82]. An interconnect via stack is used to connect to FEOL, primarily to MOSFETs, as illustrated in Fig. 3.8(a). Each interconnect via will have an inductance L_{via}, and a capacitance C_{via}. In case the interconnect vias are used to connect to a multi-port structure (i.e MOSFETs), there will be a cross-talk contribution as well, seen as inter-via capacitance C_{inter}. These lumped components form a parasitic shell that needs to be included in the MOSFET model. The interface between the FEOL and the BEOL is therefore named *device interface module* (DIM).

Fig. 3.8(b) shows optical micrographs of measured structures. The measurement structure is a two-port access structure, with a common ground, consisting of landing probe pads and access structures, which

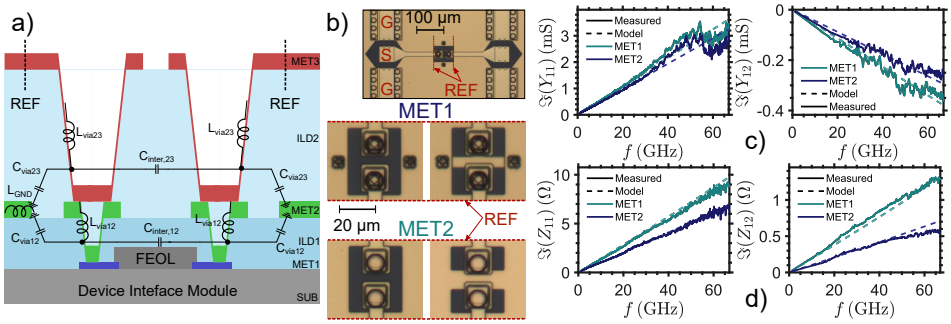

Figure 3.8: a) Schematic illustration of a device interface module (DIM), with via inductance and capacitance contributions. b) Optical micrographs of the DIM measurement structures, where insets are different via stack structures: *OPEN* and *SHORT* standards, terminating either on the *MET1*, or on the *MET2* layer. c) An *OPEN*-terminated DIM structure parasitic admittance (imaginary part→capacitance). d) A *SHORT*-terminated DIM structure parasitic impedance (imaginary part→inductance).

are removed in the mTRL calibration, leaving only the interconnect via stack contribution. The vias are realized with either OPEN, or SHORT termination, allowing for either capacitance, or inductance to be assessed, respectively. Furthermore, they are realized in between the *MET3* and *MET2* layers, or they are descending from the *MET3* layer down to the *MET1* layer on the substrate, as a stacked via. This separation allows for the exact evaluation of the individual contributions from both vias. Fig. 3.8(c-d) depicts measured and modelled structures, demonstrating a clear distinction between port reflections, as well as the coupling between ports. The model captures the cross-talk between the ports, which is essential in using the DIM in combination with various FEOL.

Aside from the DIM characterization, MIM capacitors are evaluated as well. Fig. 3.9(a) shows the capacitor realization either as a series capacitor, or as a capacitor-to-ground (with symmetric or asymmetric vias). For capacitor dielectrics, silicon nitride ($\varepsilon_r \approx 8.5$) is used. The size of the mm-wave MIM capacitors is small, and they require minimum routing, in order to reduce unwanted distributed effects. As these MIM capacitors are intended for use in the matching networks, such distributed effects deteriorate the capacitor performance. Their measured response (Fig. 3.9(b)) demonstrates capacitor components with a high *quality factor* (Q) value, determined primarily by the quality of the capacitor dielectric layer. Thicker layers enable low capacitance density, with measured values corresponding to the capacitance of 50 fF, both for the parallel and the

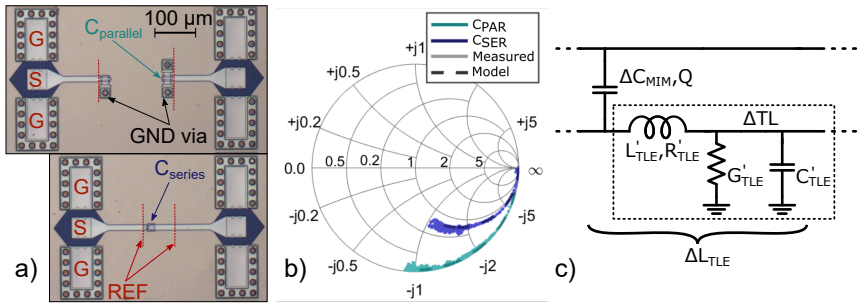

Figure 3.9: a) Optical micrographs of mm-wave MIM capacitors, connected in parallel (with a ground via), and in series (with an added TL segment). The mTRL reference plane is marked with a dashed line. b) Measured and modelled s-parameter capacitor response. c) A capacitor model unit cell, consisting of a portion of the finite-Q MIM-capacitance and TL segment of length ΔL_{TLE}, represented with distributed $RLGC$ elements.

series capacitor structure. Furthermore, a capacitor model is established, consisting of unit cells, as shown in Fig. 3.9(c). The unit cell contains a capacitor element with a portion of the total capacitance, and the associated Q value. The distributed effects are modelled with a TL segment, which corresponds to the portion of the MS line. The MS line is represented by scalable RLGC parameters, thus improving the model accuracy.

Many other models for passive components have been built, including additional BEOL line sections, resistors, and probe-tip lumped components. They all are included in the BEOL portion of the technology library. Such a complete model library, with layout designs, allows for the design of the high-frequency circuits. Circuit design is described in the next chapter, as a use case for the III-V nanowire MOSFET technology library. Details about the processing of the BEOL can be found in Paper I, while more information about the MS line performance, using mTRL calibration, is given in Paper II. Finally, the RF characterization of the ferroelectric MOSCAPs, including the LRRM calibration kit, is presented in Paper VI.

4

III-V NW MOSFET mm-Wave Devices and Circuits

This chapter will be this work's summarizing chapter. It starts of with the BEOL integration with III-V *lateral* nanowire (LNW) MOSFETs, a technology option with nanowires parallel to the substrate surface. The result is an amplifier input stage, whose properties will be used for the MOSFET evaluation. It marks an important step in the evaluation of the nanowire MOSFET technology library.

The following section will primarily analyze high-frequency performance of the III-V VNW MOSFETs. The III-V VNW MOSFET technology library, as proposed in Chapter 2, is evaluated, primarily for the parasitic capacitance contributions. The nanowire vertical contact alignment is addressed, providing valuable insights into the RF and mm-wave properties of III-V VNW MOSFETs. A demonstrator circuit reveals the design and the performance benefits of the III-V VNW MOSFET technology. In the following section, the specific features of the vertical geometry are utilized for improving the high-power characteristics of the RF III-V VNW MOSFET. Finally, device benchmarking are revisited, now including a circuit performance benchmarking as well.

4.1 LATERAL NANOWIRE MOSFET 60 GHZ LNA INPUT STAGE

The high-frequency circuit design starts with the evaluation of the MOSFET performance. The main interest lies within specific device properties: maximum stable/available gain MSG/MAG, optimum noise matching point Γ_{opt}/Z_{opt}, device stability factor K, and DC current I_D, among many. During the development of the MOSFET technology platform, the focus is typically on the standalone MOSFET, while the BEOL stack is evaluated

separately. In the following step, they are integrated into a single process. This has been implemented in the case of III-V LNW MOSFETs, a lateral-nanowire, or tri-gate-based MOS transistor platform [29,83–91]. The device model is analyzed, and an optimum matching network has been designed, considering both the FEOL performance and the DIM parasitics. More details on the optimum matching network design procedure are provided in Appendix A.

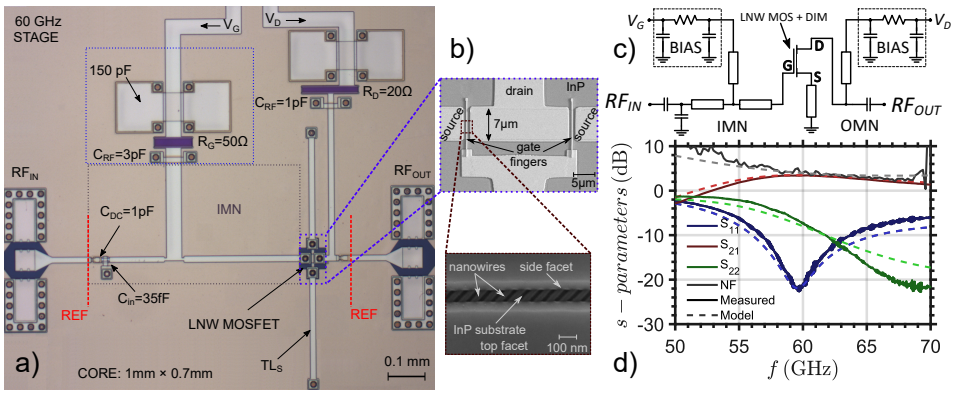

Figure 4.1: a) Optical micrograph of III-V LNW MOSFET LNA input stage. The circuit consists of biasing, IMN, output inductive peaking and source stabilization stubs. The LNA area, excluding the access structures, is 0.7 mm^2. b) Micrograph of the III-V LNW RF MOSFET, consisting of 2×7 μm gate fingers, making a total of 2×100 nanowires ($W_G = 8\ \mu m$). The inset shows lateral nanowire array with overgrown contacts. c) The LNA input stage circuit schematic model, illustrating the relevant matching components, including the biasing network. d) Measured and simulated s-parameters and noise for the LNA input stage The LNA exhibits $G \approx 3.4$ dB, and $NF \approx 2.5$ dB. The LNA is biased at $V_G = 0.8$ V, and $V_D = 1$ V, and consumes a total of $I_D = 6.4$ mA. The MOSFET gate length is $L_G = 80$ nm.

The resulting circuit is a low-noise amplifier (LNA) input stage, whose micrographs are shown in Fig. 4.1(a-b). It consists of one III-V LNW MOSFET with a four-port DIM, which, when combined, constitute the circuit-level III-V LNW MOSFET. The device is stabilized for operation at 60 GHz, using inductive source degeneration. Additionally, a $\lambda/4$ TL section is placed in the device input, in order to transform the matching network's neighbouring inductance into the DIM capacitance, using Kuroda identities [92]. In this way, interconnect vias become a part of the matching, without increasing the number of network elements. The output matching network (OMN) uses an inductive peaking technique, that minimizes OMN size and insertion loss, while improving the device power matching [93]. A bias stub, shorter than $\lambda/4$, is used to achieve this

matching inductance. The circuit is finalized with an access line structure, RF probe landing pads and bias circuitry through which the DC bias is supplied. Accounting only for the area between the mTRL reference planes, the LNA input stage size is 1 mm × 0.7 mm, determined primarily by the long input lines and the stabilization stubs. The inset (Fig. 4.1(b)) shows 2×7 µm active MOSFET area, with the underlying array of 2×100 lateral nanowires, which are the main part of the circuit.

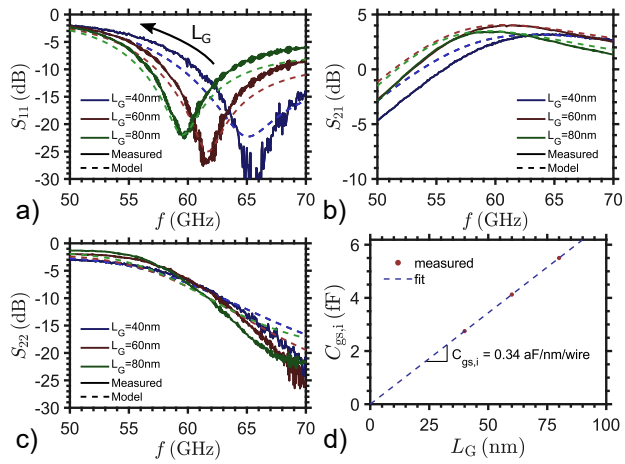

Figure 4.2: Assessment of L_G scaling on the circuit performance. Measured and simulated s-parameter response of the LNA input stage: a) s_{11}, b) s_{21}, and c) s_{22}, for L_G = 40, 60, and 80 nm. d) Modelling of the intrinsic (quantum) capacitance $C_{gs,i}$ of the III-V LNW MOSFET, normalized as aF per nm gate length, per nanowire.

The LNA input stage circuit schematic is illustrated in Fig. 4.1(c), containing three TL sections in the IMN, a matching 35 fF capacitor-to-ground, and a series DC-block capacitor. The OMN contains the DC-block capacitor as well, and a TL section, also used as a bias line. The bias circuit is an RC network that ensures the bias and the low-frequency stability. The LNA input stage performance for L_G = 80 nm III-V LNW MOSFET is shown in Fig. 4.1(d). The circuit is biased at V_G = 0.8 V, and V_D = 1 V, and spends a total current of I_D = 6.4 mA. The LNA input stage exhibits gain of $G \approx$ 3.4 dB, noise figure value of $NF \approx$ 2.5 dB, and a 60-GHz-matched input reflection s_{11} < -10 dB. The noise figure measurement is the first circuit-level noise measurement of the III-V LNW MOSFET, demonstrating a good fit to the modelled device noise [87]. Moreover, the measured data is accurately predicted by circuit simulations, demonstrating the ability of using the MOSFET technology library with

the BEOL models, with the intention of designing and realizing complete mm-wave circuits and systems.

The interesting option that the circuit implementation provides, is in the gate-length-scaling study. The LNA input stage is implemented on III-V LNW MOSFETs with 40, 60, and 80 nm gate lengths. Their s-parameter response is shown in Fig. 4.2(a-c). A clear frequency shift in s_{11} and s_{21} is directly related to the change in the intrinsic gate capacitance $C_{gs,i}$. The parasitic values remain fairly constant, as no significant frequency shift occurs in the circuit output reflection, or s_{22}. Considering resistance, conductance, and capacitance values in the device small-signal model (Fig. 8d in Paper III), an intrinsic capacitance scaling is obtained, as shown in Fig. 4.2(d). The value corresponds to a theoretical gate capacitance value, when MOSFET operates under the quasi-ballistic regime. The obtained $C_{gs,i}$ demonstrates the ability of the technology library to assist in the device assessment through circuit realization. Additional interesting aspects of the LNA input stages, and lateral nanowire MOSFETs can be found in Paper III.

4.2 VERTICAL NANOWIRE MOSFET MM-WAVE DESIGN

The design of III-V VNW MOSFETs is based on the heterostructure epitaxial process discussed in Section 2.2. Such RF-optimized III-V VNW MOSFETs have already been implemented for long gate lengths. The results from this 130-GHz III-V VNW MOSFET are given in [31], while the detailed small-signal model is developed in [94]. The model includes the separation of an extrinsic parasitic, and an intrinsic gate capacitances. The device contains 180 wires organized into 3 gate fingers, according to the layout template provided in Section 2.2. The parasitic gate overlap capacitances are $C_{gs,p}$ = 20 fF, and $C_{gd,p}$ = 6 fF, while the intrinsic capacitances are $C_{gs,i}$ = 6 fF, and $C_{gd,i}$ = 1 fF, for L_G = 120 nm. Approximately 73% of the total device capacitance is attributed to external parasitics, and this percentage increases as L_G is scaled. These high parasitic capacitances are attributed in part to the highly-doped shell, and in part to the overlap of the vertical (drain) contact and the gate metal. The initial analysis of the III-V VNW MOSFET establishes two separate layout-based contributions:

$$C_{gx,p} = C_{gx,MOL} + n_w * C_{gx}, \tag{4.1}$$

where $C_{gx,MOL}$ (x={s,d}) is a Middle(-End)-Of-Line (MOL) capacitance contribution, originating from routing of the device metal access segments on the FEOL level. The nanowire extrinsic parasitic overlap capacitance

contribution, denoted as C_{gx}, is scaling with the number of wires n_w, or with the gate width W_G, and are denoted either as aF/wire, or as fF/µm, respectively.

4.2.1 VERTICAL NANOWIRE MOSFET MOL DESIGN

The RF operation of the III-V VNW MOSFET is tied to the metal routing that connects FEOL device with the BEOL interconnect via stack. This MOL structure consists of routed metal segments on different heights, supported by a low-κ dielectric, with the interconnect vias that connect them to the BEOL *MET1* layer (see Fig. 3.3). The major parasitic contribution from the MOL structure is the parasitic capacitance of these metal segments, and it is considered separately from the III-V VNW MOSFET active area. Both the aforementioned HSQ, and BCB layers are considered, having a similar dielectric constant of $\varepsilon_r \approx 3$.

Since the VNW MOSFET is essentially a 3D structure, it is visualized and analyzed using COMSOL Multiphysics. An electrostatic simulation is used to obtain the MOL capacitance values, assigned between the MOSFET terminals (gate, source, and drain). The gate metal is placed at a 100 nm height from the source mesa, and it is considered planar, i.e. the spacer layer is planarized over the mesa edge. Similarly, the drain metal is separated from the gate metal by a planarized 100-nm-thick low-κ

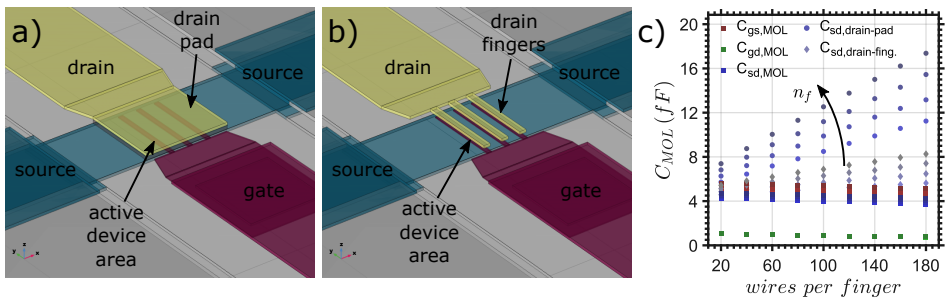

Figure 4.3: COMSOL Multiphysics model used for evaluation of the MOL parasitics, using: a) drain pad metal, and b) drain metal fingers extending into the active VNW MOSFET area. c) Simulated MOL capacitance between different MOSFET terminals (gate, drain, source), for different widths of the active area, represented as number of nanowires per gate finger. The total parasitic C_{sd} increases with drain pad metal extending into the active area, while a significant reduction in capacitance is observed when drain fingers are implemented. All MOL capacitance contributions increase in values when number of gate fingers n_f increases.

layer. The height placement of different metal layers is motivated by the nanowire design, and the MOSFET fabrication procedure. Furthermore, two varieties of the drain metal are considered: a drain pad, covering the entire active area, and drain fingers, routed only on top of the nanowires, as illustrated in Fig. 4.3(a-b). The source-drain capacitance contribution is a combination of the MOL parasitic capacitance $C_{sd,MOL}$, and the active area overlap capacitance $C_{sd,drain}$, and does not depend on the design of the vertical nanowires.

The simulated MOL capacitance contributions are plotted in Fig. 4.3(c). The simulated $C_{gs,MOL}$ and $C_{gd,MOL}$ have values in the range of 4.5 fF to 5.1 fF, and 0.7 fF to 1 fF, respectively. Higher values are associated with a larger number of gate fingers n_f. The capacitances represent the parasitic fringing capacitances (excluding the gate finger in the active device area). Regarding the source-drain capacitance, the MOL fringing capacitance $C_{sd,MOL}$ has values between 3.7 fF and 4.7 fF. Adding the drain pad, the source-drain capacitance has values up to $C_{sd,drain-pad} = 17.4$ fF. This value can be controlled by patterning the drain pad into drain fingers, thus removing the excess parasitic source-drain overlap in the active device area. The parasitic capacitance values increase up to $C_{sd,drain-fing.} = 8.3$ fF, a substantial decrease in the device output parasitics. After evaluating the device MOL parasitics, the active device extrinsic parasitic capacitances are still required, to complete the parasitic network for the III-V VNW MOSFETs.

4.2.2 OPTIMIZATION OF VNW MOSFET PARASITIC CAPACITANCE

When the MOL parasitic capacitance contribution is compared to the measured device data from [31], it constitutes less than 20% of the total device parasitic capacitance. The major parasitic contribution in the III-V VNW MOSFET is therefore in the scalable active device area. Note that the MOL design and its parasitics are only relevant for large nanowire arrays. Cases of a single (or a few) nanowire device are not considered in this thesis. The reason why a large parasitic capacitance contribution is expected in the device active area is a consequence of the proximity of the gate metal to the doped semiconductor and the metal contacts. Such overlaps are illustrated in Fig. 4.4(a). The device contacts are optimized for the state-of-the-art DC performance in III-V VNW MOSFETs, and should be retained in the RF process as well [15, 45, 47, 95].

Analyzing the the vertical nanowire unit cell, two contributions to the parasitic capacitance are identified: the parallel-plate capacitance $C_{gx,ILD}$, and the extrinsic parasitic overlap capacitance $C_{gx,ext}$. For the 100-nm-thick low-κ interlayer, the parallel-plate capacitance has a value of

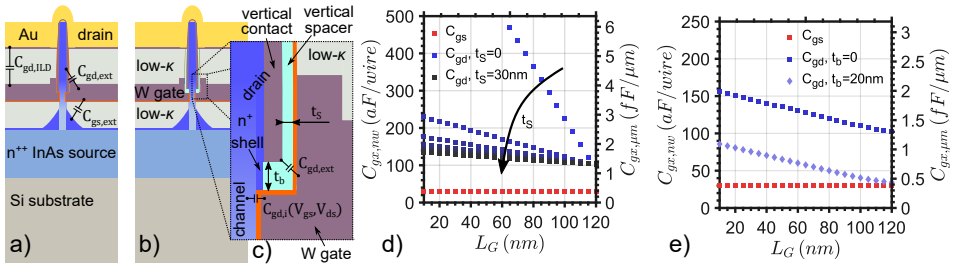

Figure 4.4: a) A schematic illustration of the III-V VNW MOSFET, including the gate metal, a vertical contact, the drain metal, and b) a case with a vertical spacer implementation in the gate-drain overlap area. The gate-drain external parasitic capacitance $C_{gd,ext}$ and the gate-drain parallel plate capacitance $C_{gd,ILD}$ are shown. c) The inset shows the gate-drain overlap area in detail, with the vertical spacer sidewall thickness t_S, and the drain underlap height t_b. d) COMSOL-simulated values for the total gate-source parasitic capacitance C_{gs}, and the gate-drain parasitic capacitance C_{gd}, for various L_G and gate-drain overlap designs, in a case where t_S is varying from 0 to 30 nm, while $t_b = 0$. e) Simulated influence of t_b, showing C_{gd} values for $t_b = 0$ and $t_b = 20$ nm, while $t_S = 15$ nm. In all cases, C_{gs} remains L_G-independent.

$C_{gx,ILD} \approx 5$ aF/wire (63 aF/μm). Hence, the value of C_{gx} is primarily set by the value of $C_{gx,ext}$. First, a thin highly-doped shell in the vicinity of the channel contributes to a large portion of $C_{gx,ext}$. For the gate-source capacitance $C_{gs,ext}$, the shape of the nanowire foot, as formed by the epitaxial growth, is optimal for the capacitance minimization, where $C_{gs} \approx 31$ aF/wire (0.4 fF/μm), and is L_G-independent. The gate-drain capacitance $C_{gd,ext}$, however, contains an additional contribution from the gate metal and the vertical (drain) contact MIM capacitance. When L_G is scaled, this overlap will increase, resulting in a large C_{gd}. Given that the value of C_{gd} should be as low as possible, an alternative approach is selected. As shown in Fig. 4.4(b), a vertical spacer is inserted in between the gate metal and the vertical contact, to control the C_{gd} value. The vertical spacer is preferably a conformal-covering low-κ spacer, for instance SiO_2 ($\varepsilon_{SiO} \approx 4$). The inset (Fig. 4.4(c)) provides details on the III-V VNW MOSFET gate-to-drain overlap region.

In COMSOL, a 2D axisymetric model is used to describe the nanowire unit cell. It is a simplified geometry that provides the capacitance value of the equivalent 3D structure. In Fig. 4.4(d), it is indicated that when no vertical spacer is present, $C_{gd} \approx 800$ aF/wire (10.2 fF/μm) for scaled L_G. This large capacitance value is mitigated by the vertical spacer. Increasing the spacer thickness to $t_S = 30$ nm, limits the C_{gd}

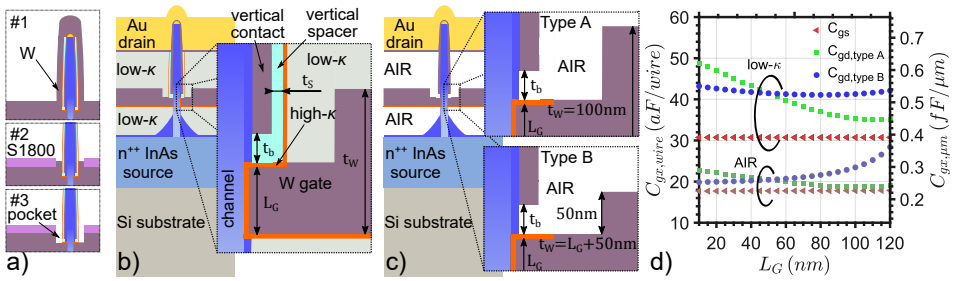

Figure 4.5: a) Schematic illustration of the Γ-gate development: gate metal deposition (#1); selective removal of the gate metal using a thin mask layer (#2); an alternative process, where a pocked is formed (#3). b) A III-V VNW MOSFET illustration, with a Γ-gate. The inset shows increased spacing between the gate metal and the vertical contact. c) A III-V VNW MOSFET illustration with air spacers. The insets show an air gap between the gate metal and the vertical contact, and two options for the gate metal thickness scaling: type A - the gate metal height fixed to $t_W = 100$ nm, and type B - the gate metal extension is fixed ($t_W = L_G$+50 nm). d) Comparison between capacitance contributions for both spacer solutions and device types.

to 130 aF/wire (1.65 fF/µm). For $L_G = 120$ nm, the capacitance value of approx. 100 aF/wire (1.3 fF/µm) does not correspond to the modelled $C_{gd} \approx 33$ aF/wire (0.42 fF/µm), suggesting a drain underlap [94]. Therefore, the vertical contact retraction (drain underlap) in implemented in COMSOL as well. Fig. 4.4(e) shows the C_{gd} values for $t_S = 15$ nm. For the underlap width of $t_b = 20$ nm, the value of C_{gd} is reduced by approximately a factor of 2, exhibiting a value of approx. 80 aF/wire (1 fF/µm) for scaled L_G, and a matching C_{gd} value for 120-nm MOSFET.

The large overlap between the gate metal and the vertical contact is primarily driven by the gate metal resistance optimization. As described in Section 2.3, the gate finger is perforated with nanowires, substantially increasing the gate resistance R_G. Therefore, the gate metal thickness is set to $t_W = 100$ nm, which increases the C_{gd} value. A workaround for this issue is illustrated in Fig. 4.5(a). A mask layer protects the planar surface and allows for the removal of the gate metal from the nanowire sidewall, leaving a residual overlap area. In an alternative process, a pocket would be created as well, resulting in a Γ-shaped gate metal (Γ-gate), as shown in Fig. 4.5(b). The use of the vertical spacer and the Γ-gate creates a structure similar to planar HEMTs, but applied to the vertical geometry. Furthermore, the parasitics can be lowered further by removing the spacer layers. Using drain fingers in the active device area,

for instance, the dielectric layers can be isotropically removed. Fig. 4.5(c) shows the resulting air gap between the gate metal and the drain contact.

To study the influence of the Γ-gate, two device types are considered: a device with a fixed total gate metal height of $t_W = 100$ nm (type A), and a device with a fixed gate metal overlap on the vertical contact, as $t_W = L_G + 50$ nm (type B). Their respective capacitance contributions, shown in Fig. 4.5(d), are simulated in COMSOL. The evaluation of the MOSFET with the Γ-gate and spacer layers reveals the parasitic C_{gx} values of 30-60 aF/wire (0.4-0.6 fF/µm). When L_G is scaled, an approximately 25% increase in the parasitic C_{gd} is expected in the type A device, while the value remains nearly constant for the type B device. A similar trend is observed for the MOSFET with air spacers. The parasitic C_{gx} values are in the order of 15-25 aF/wire (0.2-0.3 fF/µm), which are typical values for the III-V HEMTs. Additionally, these parasitics are reproduced in previous works in vertical InAs nanowire MOSFETs [30, 96].

4.2.3 III-V VNW MOSFET MM-WAVE PERFORMANCE

Following the optimization of the device parasitics, a mm-wave III-V VNW MOSFET can be modelled. In Subsection 2.1.2 a compact VS model is established, used to describe the current-voltage relationship. The model is implemented as a Verilog-A code, a hardware description language that allows building of complex analog modules [97]. The L_G is coupled to the virtual-source (injection) velocity v_{x0}, through the transmission factor T. Using the measured device data, key III-V VNW MOSFET model parameters are obtained [98]. The modelling reveals the mean-free-path value of $\lambda \approx 35$ nm ($T \approx 0.7$), for the 20-nm VNW MOSFET showing 70% ballistic transport. Furthermore, the obtained contact resistance values $R_S = 70$ Ω·µm, and $R_D = 170$ Ω·µm, signify the importance of the vertical contact and the highly-doped shell. The drain underlap contribution to the access resistance is considered as well [99]. The transfer characteristics of the III-V VNW MOSFET for $L_G = 100/50/20$ nm, are shown in Fig. 4.6(a). The transconductance value of $g_m \approx 3.1$ mS/µm, at $V_{DS} = 0.5$ V, corresponds to the previously published device results [15].

The III-V VNW MOSFET compact model is extended to include parasitic capacitances. The channel inversion charge Q_{ix0} is partitioned between the source and drain terminals, resulting in intrinsic MOSFET capacitances $C_{gx,i}$ [40, 41]. Furthermore, external parasitic capacitances $C_{gx,p}$ are added as well, as described in Subsection 4.2.2. The C_{gx} values considered for the mm-wave MOSFET, all include Γ-gate implementation, with the vertical spacers (Fig. 4.5(b)), as well as the air spacers (Fig. 4.5(c)). The different Γ-gate types are considered also. The mm-

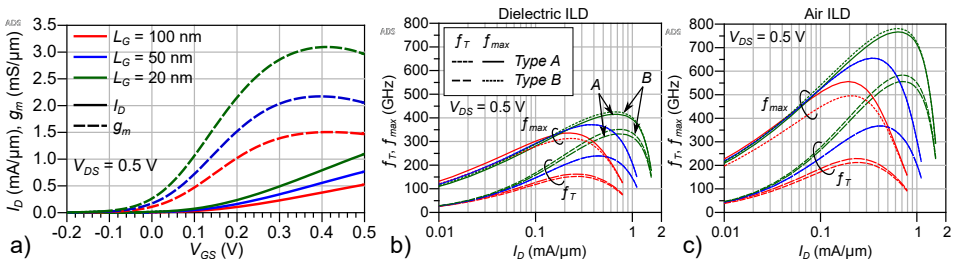

Figure 4.6: a) III-V VNW MOSFET compact VS model DC response for L_G = 100/50/20 nm, at V_{DS} = 0.5 V. b) The mm-wave cut-off frequency (f_T, f_{max}) response versus drain current, for the III-V VNW MOSFET with the vertical spacers, and c) the air spacers. The mm-wave performance is evaluated at different L_G: 100, 50, and 20 nm, for both Γ-gate types.

wave III-V VNW MOSFET, used in the performance assesment, contains 300 nanowires organized into five gate fingers, where the total active area is 12 µm×8 µm.

The device f_T and f_{max} are evaluated with respect to the drain current I_D. Fig. 4.6(b) illustrates the case where the vertical spacers are implemented. For L_G = 20 nm, the f_T > 300 GHz and f_{max} > 400 GHz, demonstrate the vertical nanowire MOSFET performance comparable to the state-of-the art Si-based devices [17–19]. Even for L_G = 100 nm, the f_{max} > 300 GHz is predicted, due to the reduced parasitic C_{gd} and the high intrinsic gain, inherent to the III-V VNW MOSFET. In Fig. 4.6(c), the air-spacer III-V VNW MOSFETs are evaluated. The f_T and f_{max} reach values above 500 GHz, and 700 GHz, respectively, with peak $f_T \approx$ 580 GHz, and $f_{max} \approx$ 780 GHz, for L_G = 20 nm. Such high f_T/f_{max} make III-V VNW MOSFETs comparable in performance to III-V HEMTs. The discrepancies in different Γ-gate types has little impact, demonstrating that the devices are limited primarily by the parasitic capacitances, rather than the gate resistance. A further optimization on the nanowire diameter, MOSFET gate-length, the highly-doped shell, and the carrier mean-free-path, would enable mm-wave performance boost past the 1 THz limit.

4.2.4 III-V VNW MOSFET DEVICE-TO-CIRCUIT CO-DESIGN

An unique aspect of III-V VNW MOSFETs is their parasitic capacitance scaling behavior. The linear dependence of the C_{gd} on the value of L_G allows for the exploration of a different circuit design approach using such devices. The Γ-gate extension can be designed in such a way that the increase in C_{gd} (and subsequently, the $C_{gd,p}$), due to L_G scaling, is compensated by a decrease in total intrinsic gate capacitance $C_{gg,i}$. Such a MOSFET would have a L_G-independent response, for which a resonant network can be designed, to match the MOSFET's mm-wave response across different gate-lengths.

The example network that resonates with the $C_{gd,p}$ is depicted in Fig. 4.7(a). It is a LC feedback network, where the feedback inductance L_F resonates with the MOSFET $C_{gd,p}$. The feedback capacitance C_F prevents gate-to-drain DC leakage, but also sets the frequency of the resonant poles, together with L_F. The imaginary part of the feedback admittance $\mathrm{Im}\{y_{12}\}$, for the III-V VNW MOSFET and the feedback network is:

$$\mathrm{Im}\{y_{12}\} = -\,\mathrm{Im}\{y_{gd} + y_F\} \approx -\omega \left(C_{gd,p} - \frac{C_F}{1 - \omega^2 L_F C_F} \right), \qquad (4.2)$$

where y_{gd} is the MOSFET gate-drain (feedback) admittance, y_F is the resonant feedback network admittance, and $\omega = 2\pi f$ is the angular frequency. The expression is more complex, since the inductance L_F is realized as a TL segment. Furthermore, the gate-drain capacitance that is resonating with the feedback network also contains MOL and DIM capacitance contributions, which are L_G-independent. The simulation of this feedback structure is done in D-band (110-170 GHz), with the selected

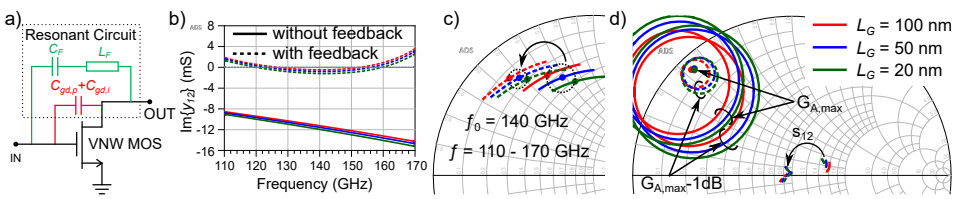

Figure 4.7: a) Schematic representation of the resonant feedback design with the III-V VNW MOSFET. b) Imaginary part of the feedback admittance y_{12}, before (solid) and after (dashed) feedback implementation, for different gate lengths. c) Optimum noise matching point Γ_{opt}, shifting with the feedback implementation. d) Available gain circles, at the center frequency $f_0 = 140$ GHz, showing MOSFET unconditional stability. Feedback gain (isolation, s_{12}) shifts to the center of the Smith chart as well, indicating MOSFET unilateralization.

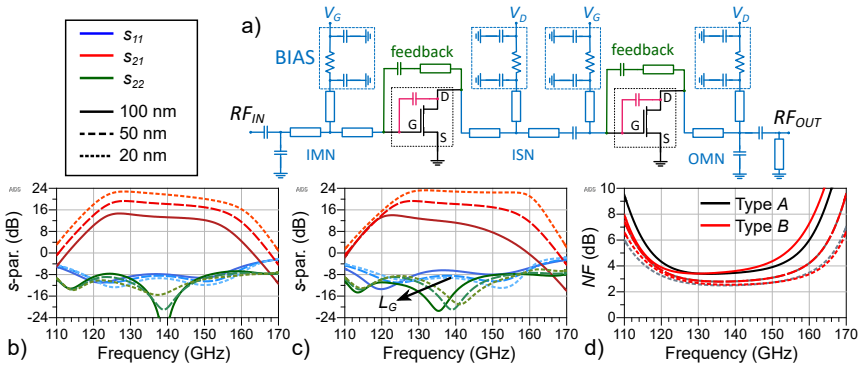

Figure 4.8: a) Schematic illustration of the III-V VNW MOSFET-based LNA, with the resonant feedback network, showing the input, interstage, and the output matching network. Simulated s-parameters, for the gate length of L_G = 100, 50, and 20 nm, in D-band: b) for device Γ-gate type A, and c) device type B. d) Noise figure comparison for device Γ-gate type A, and B, respectively.

design frequency of f_0 = 140 GHz. Since high device f_T and f_{max} are necessary to perform circuit design in D-band, the III-V VNW MOSFET model with air spacers is used.

Fig. 4.7(b) shows the $\mathrm{Im}\{y_{12}\}$ in the case of a circuit-level MOSFET (with DIM), without, and with the resonant feedback network applied. While the circuit-level MOSFET exhibits $\mathrm{Im}\{y_{12}\} \approx 8$ mS at 140 GHz, the total $\mathrm{Im}\{y_{12}\}$ swings around zero, making the III-V VNW MOSFET effectively unilateralized in the frequency range of interest [100]. To understand how this added admittance reflects on the device matching point in the frequency range of interest, the optimum noise reflection coefficient Γ_{opt}, and available gain circles G_A are presented in Fig. 4.7(c-d). Both the Γ_{opt}, and the G_A shift towards lower impedance values (higher Q-values), and have very similar values for different L_G. The G_A values are also limited to the Smith chart unity circle, indicating that the MOSFETs are unconditionally stable. The feedback gain s_{12} shifts towards the center of the Smith chart, which is expected, since the contribution of the feedback capacitance, which causes instability, is drastically reduced.

To evaluate the full device performance, a two-stage LNA is designed and simulated. The matching networks are designed according to Appendix A. The implemented interstage matching network (ISN) is a second-order network, which reduces the total number of elements and the insertion loss between the two active stages. The LNA schematic is illustrated in Fig. 4.8(a), while the LNA response, for both Γ-gate types, is presented in Fig. 4.8(b-d). The type-A-based LNAs confirm the assumption that the

L_G scaling results in a constant capacitance value. This is confirmed by the resonant peaks in the LNA input reflection and gain, s_{11} and s_{21}, respectively. The type-B-based LNAs demonstrate the opposite capacitance scaling trend, where a clear shift in the resonant peaks in s_{11}, as well as the s_{21} deformation, is evident. The LNA design with $L_G = 20$ nm predicts gain of $G \approx 24$ dB. The benefits of the unilateral design are clearly visible in the very high gain value for the two-stage LNA. The NF values, shown in Fig. 4.8(d), for both Γ-gate types, are very similar, with the minimum niose figure value of $NF \approx 2.5$ dB, for $L_G = 20$ nm. The selected co-design strategy allows for a careful examination of the III-V VNW MOSFETs as high-performance mm-wave devices, capable of delivering high drive currents and having high transconductance efficiency at scaled gate lengths. Additional circuit design benefits are unveiled in Paper V.

4.3 VERTICAL NANOWIRE MOSFETS LARGE-SIGNAL DESIGN

A specific flavor of RF devices are those that operate under high power density conditions. The III-V compounds are interesting for high-power applications, from the aspect of amplification, transfer and handling of high-power signals in the communication systems. Signal fidelity, modulation scheme and density of information being transferred depends heavily on the device parameters, as well as the applicable voltage range [101]. The main physical breakdown mechanisms in III-V MOSFETs are band-to-band tunneling (BTBT, see Fig. 2.1), and impact ionization. Under high electric field on the drain side, carriers are tunnelling from the drain conduction band to the channel valence band. The accumulated charge causes a potential shift in the channel, which lowers the top of the barrier and creates a positive feedback loop that would ultimately break the device [102]. To prevent the MOSFET from breaking under high voltage operation, the electric field needs to be spread across the drain region.

The *screening* of the electric field in the drain region is achieved with a weak gate coupling over the area between the channel and the drain. Such region is known as a field-plate region, and a III-V VNW MOSFET with the field-plate is illustrated in Fig. 4.9(a-b). The vertical spacer is adjusted for use as a field plate oxide, to moderate the high electric field within the drain region. In Fig. 4.9(c), the energy band diagrams, simulated using COMSOL semiconductor module, reveal the effect that the field-plate has on the energy bands. This is applicable if the region is not intentionally doped. For doped segments, starting from the nanowire height of 200 nm, the energy band moderation will not be possible, as is evident for devices

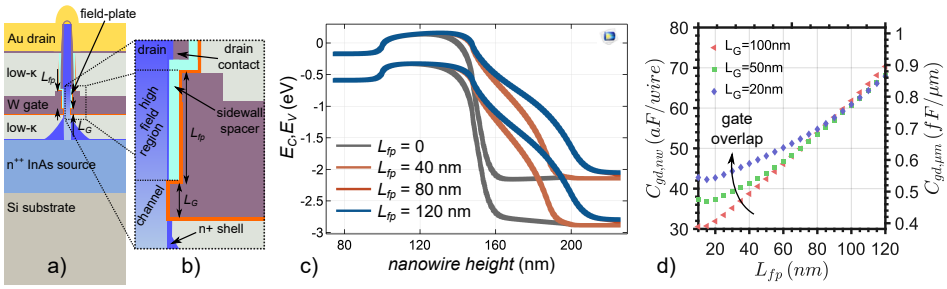

Figure 4.9: a) Schematic illustration of the III-V VNW MOSFET, with a field-plate region. b) The inset illustrates the field-plate region separating the drain and the channel in the nanowire. c) Energy band diagram of III-V VNW MOSFET, taken alongside the length of the nanowire, showing increased separation of the energy bands with increased field-plate length L_{fp}. d) A COMSOL-simulated parasitic C_{gd}, including the field-plate (MOS) capacitance, for L_G = 100/50/20 nm. The influence of the Γ-gate is seen only at low L_{fp}.

with field-plate lengths of L_{fp} = 80 nm and 120 nm, where a similar energy band diagram is observed. Furthermore, the COMSOL simulation of the parasitic C_{gd} for different L_G, and L_{fp} has been done, as depicted in Fig. 4.9(d). Although the Γ-gate overlap causes the C_{gd} increase for short L_{fp} (as described in Subsection 4.2.3), the C_{gd} values are dominated by the field-plate capacitance contribution for long L_{fp}. The estimated capacitance density in the field-plate region is approx. 2 aF per nm field-plate, per nanowire.

When describing the field-plate in the III-V VNW MOSFET compact model, the transmission factor is scaled, to account for the increased total effective gate length. A portion of the length of the field plate region contributes to this value, depending on the applied drain electric field. Additionally, the contribution to the access resistance needs to be included as well. These two contributions are modelled separately, since transmission affects the g_m peak, while the increased access resistance shapes the g_m roll-off at high V_{GS}. Fig. 4.10(a) shows the model response for different L_{fp}, demonstrating approximately 40% reduction in peak g_m, for L_{fp} = 120 nm. Regarding the III-V VNW MOSFET mm-wave performance, lower g_m and higher $C_{gd,p}$ result in lower simulated cut-off frequencies. Fig. 4.10(b-c) shows f_T and f_{max} values versus I_D, for the III-V VNW MOSFET with the field-plate. When L_{fp} = 0, the estimated cut-off frequencies are above 350 and 400 GHz, for 50 and 20 nm gate length, respectively. When L_{fp} = 120 nm, the breakdown voltage is expect to increase to V_{BD} = 2V, while the cut-off-frequencies remain

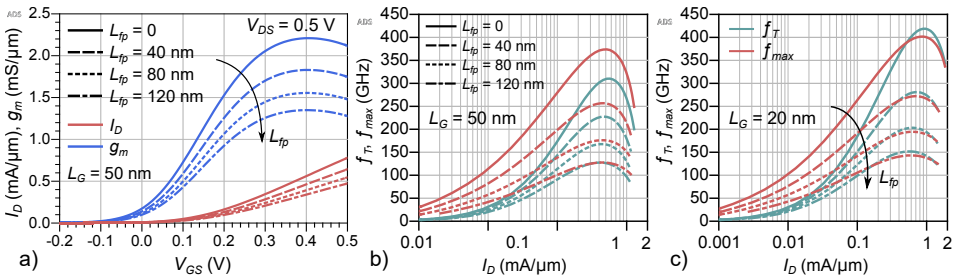

Figure 4.10: a) Transfer characteristics for the III-V VNW MOSFET with field-plate, at V_{DS} = 0.5 V, showing I_D and g_m reduction with increasing L_{fp}. b) High frequency response of III-V VNW MOSFETs with L_{fp} scaled from 0 to 120 nm (corresponding to an evaluated breakdown voltage from 0.8 V to 2 V), for L_G = 50 nm, and c) L_G = 20 nm. The reduction in f_T and f_{max} arises due to increased gate-drain overlap capacitance, dominated by the field-plate capacitance.

above 120 GHz. Therefore, the field-plate implementation in the III-V VNW MOSFETs extends their design capabilities into high-power RF and mm-wave circuits.

4.4 DEVICE AND CIRCUIT BENCHMARKING

Subsequent to the design and the performance evaluation of the LNAs, is the benchmark analysis of the circuits. The benchmarking helps in establishing the comparison between different design approaches, as well as technology implementations. From literature, the technologies which have been used in D-band are included in Table 4.1. These are 22 nm fully-depleted SOI (FDSOI) CMOS, 90 nm SiGe HBT, 50 nm InGaAs HEMT, and 40 nm GaN HEMT. The respective device technologies vary in cut-off frequencies, and are represented in Fig. 1.4. For this analysis, the device benchmark properties are the cut-off frequencies and the drain current. In general, the III-V technologies demonstrate higher speed than Si-based technologies. The 50 nm InGaAs HEMTs have significant f_T and f_{max} values, while the 35 nm version exhibits $f_{max} > 1$ THz [107]. GaN HEMTs are known for their high-power properties, but can also exhibit high frequency of operation. The III-V VNW MOSFETs benefit from shorter gate lengths and InAs source, allowing them to exhibit higher carrier injection velocities and higher drain currents. Consequently, the high g_m value will translate into the mm-wave performance, as presented in Subsection 4.2.3. Fig. 4.11 outlines the performance of mm-wave-optimized III-V VNW MOSFET,

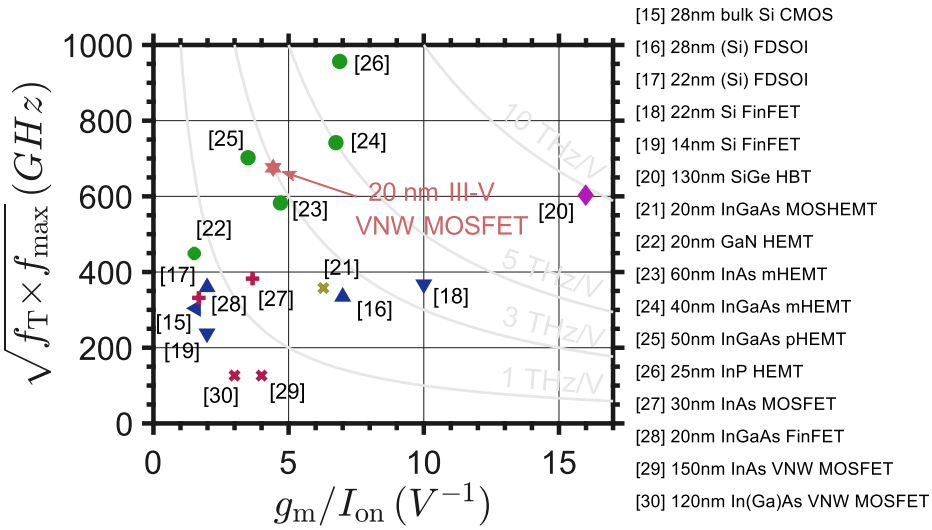

Figure 4.11: An addition to Fig. 1.4: the 20 nm III-V VNW MOSFET optimized for mm-wave operation, showing $\sqrt{f_T \times f_{max}} = 675$ GHz, and the total $FoM \approx 3$ THz/V.

with the figure-of-metrit value of $FoM \approx 3$ THz/V, a value comparable to state-of-the-art Si-based and III-V-based technologies.

For the D-band LNAs, parameters such as gain, noise figure, bandwidth and power consumption are essential. Here, Si-based technologies show comparable gain to III-V technologies, but in general, their noise properties are not as good. In this case, In-based channel material will have an advantage, due to its low effective mass and DoS. The III-V VNW MOSFETs present a favourable balance of the high gain and low noise figure, in an optimized process that enables high operation frequency and a circuit design option that allows for a very low power consumption (approximately four times less than Si-based technologies). Such prospect places III-V VNW MOSFETs at the forefront for the mm-wave circuits and systems design.

Table 4.1: Device and circuit performance comparison for representative technologies, which also include the published D-band LNA evaluation.

Technology	20 nm[a] III-V VNW MOSFET [This work]	22 nm FDSOI CMOS [103]	90 nm SiGe HBT [104]	50 nm InGaAs HEMT [105]	40 nm GaN HEMT [106]
f_T (GHz)	360[b]	240[b]	300	380	>200
f_{max} (GHz)	720[b]	230[b]	350	670	>400
I_D (mA/µm)	0.5	0.3	0.85[d]	0.3	0.26
Topology	2×CS	4×CC[c]	3×CC	3×CC	6×CC
G_T (dB)	23	16	30	30.8	>25
G_T/stage (dB)	11.5	4	10	10.3	4-5
BW (GHz)	30	40	28	67	>60
NF (dB)	2.5	8.5	6.2	3	6
P_{DC} (mW)	11.4	44	45	57.6	225

[a]simulated device and circuit performance only;
[b]circuit-level performance;
[c]mA/µm^2;
[d]differential design.

5

Conclusions and Outlook

Over the span of this thesis work, a comprehensive *technology library* is created, with the hope that it can serve those who inherit it to build their custom devices and circuits, stemming from the knowledge and experiences accumulated over time. A considerable effort is placed on the implementation of the mm-wave BEOL, whose development took the major portion of the experimental work in the thesis, contributing to every publication in this thesis. The mm-wave BEOL forms a base from which the technology library is launched, together with the lateral, and vertical nanowire MOSFETs that have been experimentally verified, and now implemented in a scalable compact model. This thesis attempts to address those issues, but also left a room for improvement. The thesis work can be divided into three significant topics, summarized below.

BEOL library and mm-wave circuit verification [Paper I-III]: The effort in the integration of III-V lateral nanowire MOSFETs with the mm-wave BEOL resulted in the realization of the LNA input stage. The LNA implementation was preceded by an extensive investigation into the optimum design of the standalone BEOL. From it, the mm-wave passive components were designed, fabricated and characterized, including capacitors, resistors and interconnect via structures. An addition to the existing BEOL would be a *MET5* layer, used as a secondary coil in a mm-wave transformer, which would expand the mm-wave BEOL towards the differential circuit design, mostly used in circuit design in a Si-based technology platform. Furthermore, a complete multi-stage lateral-nanowire-based amplifier could be realized, since both the FEOL and BEOL have already been successfully integrated, and demonstrated that the technology can be applied in mm-wave circuit design.

III-V VNW MOSFET technology library [Paper V-VI]: This topic covers the realization of the III-V VNW MOSFET compact model and associated process monitor kit. As such, these components are valuable in establishing a process flow and characterizing specific MOSFET parameters, although they have not been published in their true form. Instead, they are rooted in other works. From this library, the co-integrated RF BEOL is derived, a simplified option for the circuit design that uses vertical nanowire MOSFET 3D structure. The characterization of this BEOL has been performed in the same way as for the mm-wave BEOL, evaluating the mTRL kit and passive components. A MOSCAP structure with a thin ferroelectric dielectric layer is fabricated and characterized at high frequencies. The concept of unifying basic material research with the more complicated processing scheme, such as RF BEOL allowed for new characterization possibilities to be established. Furthermore, it motivates the integration of III-V ferroelectric VNW MOSFETs. Finally, the key part of the technology library is the III-V VNW MOSFET, integrated on the Si substrate. The experience gained in performance evaluation of the vertical nanowire heterostructure design, guided the optimization of the mm-wave III-V VNW MOSFET. The resulting cut-off frequencies are comparable to III-V HEMT values. Additionally, the device large-signal performance is modelled, including a field-plate structure.

III-V VNW MOSFET mm-wave circuits [Paper IV-V]: A mm-wave BEOL is combined with the vertical nanowire MOSFETs. A concept of unilateralization using features of III-V VNW MOSFET design allowed for the state-of-the-art simulated LNA performance. The device parasitic capacitances have demonstrated unique scaling capabilities, which result in a circuit design that is mostly gate-length independent. To date, this feature is established for III-V vertical nanowire MOSFETs only. The circuit design could be expanded into the large-signal domain, where device power-handling capabilities could be explored. A specific power amplifier would yield valuable insights into linearity of III-V vertical nanowire MOSFETs. The technology library with device and circuit models represents a complete set, capable of generating high-performance state-of-the-art mm-wave devices and circuits.

For the most part, the results are summarized in the attached papers, while some specifics are left to be examined in this thesis. Therefore, this *Introduction* contains valuable information that could not be included in the scientific publications, but establishes the foundation for the final result. The author hopes to inspire the reader into embarking onto a scientific path, where many unexplored niches are waiting. The contribution of this thesis is simply a steppingstone into a world ready to be discovered.

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APPENDICES

A

Optimum matching network design

In this appendix, the path from device design to circuit implementation is presented. As it is an essential part of the circuit design effort presented in this thesis, it should be elaborated in more detail. The described procedure includes the device treatment, matching point selection and matching network generation and transformation.

A.1 RF DEVICE IN CIRCUIT DESIGN ENVIRONMENT

In the *Introduction*, a description of the III-V VNW MOSFET is provided. The device behavior is subsequently captured in the compact model, which is used in the circuit design. Prior to designing the matching network (MN), the device size and the bias point need to be selected. Furthermore, parameters such as f_T/f_{max}, the maximum gain G_{max}, the minimum noise figure NF_{min}, the stability factor K, and input/output impedance $Z_{in/out}$, are essential in understanding the device performance. In an iterative process, the device operating point and dimensions are tuned, so that selected RF parameters are reaching their optimum value, needed for the successful matching network, and circuit design.

In this thesis, the III-V nanowire MOSFET is analyzed for LNA operation, so the device is optimized for NF_{min} and the value of the noise-optimum matching point Γ_{opt} (Z_{opt}). Fig. A.1(a) shows the bias-dependent G_{max} and NF_{min} for a standalone 5×60 ($W_G \approx 23.5$ µm) 20-nm III-V VNW MOSFET at $f_0 = 140$ GHz. As device G_{max} and NF_{min} are changing very little in a voltage span of ±0.15 V around the g_m peak, the chosen bias point is $V_{GS} = 0.3$ V, which gives $I_D = 0.5$ mA/µm and $g_m = 2.8$ mS/µm, which spends 40% less power, as compared to

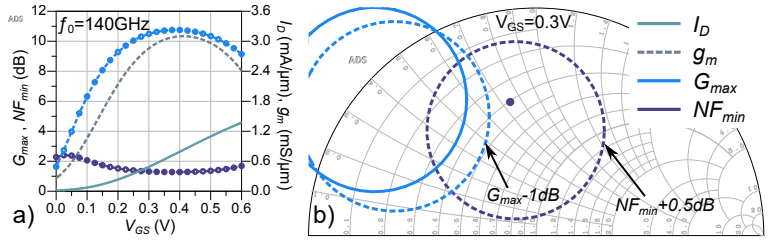

Figure A.1: III-V VNW MOSFET gate-source voltage-dependent maximum gain and minimum noise figure at $f_0 = 140$ GHz. The right y-axis shows the MOSFET DC parameters: I_D and g_m. b) Gain and noise circles, at $V_{GS} = 0.3$ V, and $f_0 = 140$ GHz. The gain circles show that the device is potentially unstable.

the peak g_m point. The device gain and noise circles are illustrated in Fig. A.1(b). The noise parabola is wide, and NF increases by 0.7 dB for 50 Ω impedance. The device is conditionally stable, however, since gain circles are partially outside the Smith chart. As described in Subsection 4.2.4, device is embedded in the mm-wave BEOL, and stabilized with the resonant feedback network, which shifts the gain and noise matching points (illustrated in Fig. 4.7(c-d)). The resulting noise-optimum matching impedance $Z_{opt} = R_{opt} + 1/j\omega C_{opt}$ is then used for matching network design.

A.2 OPTIMUM MATCHING NETWORK TRANSFORMATIONS

The initial investigations into MN design have been presented in [108], while the theory is developed further in [109, 110]. The concept of *Bode-Fano limit* originates from these works, and relates the impedance, and the selected matching level, to the network's available frequency bandwidth, as:

$$ln\left(\frac{1}{|\Gamma|}\right) \leq \frac{\pi}{2R\omega C} = \frac{\pi}{2Q}, \tag{A.1}$$

where R and C represent the matching impedance, Q is the corresponding (device input/output) quality factor, and Γ is the selected matching level. Therefore, the value of Γ depends on the device properties, which are reflected in the matching impedance. From this fundamental expression, an analytical model that determines the value of each matching element is developed [111–113].

The analytical models are used to derive coefficients for a Chebyshev low-pass prototype filter, from the obtained device Z_{opt}. Limitations are placed depending on the network order and the terminating impedance.

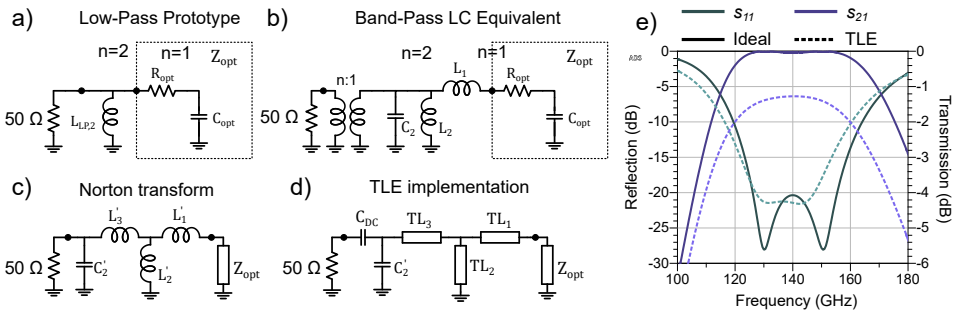

Figure A.2: An optimum (input) matching network realization: a) a second-order low-pass prototype network; b) band-pass equivalent LC network, with a impedance transformation; c) transformer absorption into the matching network (Norton transform); d) replacement of ideal components with real TL segments and finite-Q capacitors. e) Ideal, and TL-based (mm-wave BEOL) MN response.

Fig. A.2(a) illustrates the second order low-pass prototype network that matches Z_{opt} to Z_0 =50 Ω. Note that the device reactive component is also the part of the network, so only one additional element is needed. Since the input reactance is capacitive, the second-order element is therefore inductive. This low-pass prototype is scaled to its band-pass equivalent (Fig. A.2(b)), where to each element a resonant equivalent is added. Their values are scaled so that they resonate at the design frequency. Additionally, an ideal n:1 transformer is needed to convert device R_{opt} to 50 Ω, and is subsequently absorbed by the matching network in the next step. In Fig. A.2(c), transformation of inductors into a T-network will generate a 1:n transformer, which annihilates with the transformer. This procedure is known as Norton transformation [114, 115]. Additionally, the network's capacitance value is transformed, as transformers are moved through the network.

The ideal inductor-to-ground is replaced with a shorted stub, series inductors are replaced by TL sections, while capacitors are replaced with their finite-Q models (Fig. A.2(d)). A DC-block capacitor is added as well, to isolate the DC current path from the RF source. Additionally, the network is completed by replacing ideal ground of the shorted stub with a bias network capable of supplying DC bias for the active device, while still acting as an RF-short at high frequencies (not shown). This is typically achieved by placing a bypass capacitor instead of a short. The simulated response of the designed input (optimum) MN is shown in Fig. A.2(e). The second-order ideal network will have two poles, while the matching level for this design has been selected as $|\Gamma| = 0.1$ (-20 dB). The TL-based

network, realized in mm-wave BEOL, exhibits similar matching level, but with an insertion loss of approx. 1.3 dB at 140 GHz, due to MS line loss.

Similar to the input MN, an interstage and an output MN can be implemented. The network order will vary based on Γ, and $Z_{in/out}$. The LNA, shown in Fig. 4.8, has all three MN types implemented. Alternatively, the input MN for III-V LNW MOSFETs employs additional tricks to optimize the network response. More interesting examples of the design of matching networks are provided in [116, 117]. The references provided in this Appendix and in Papers should guide the reader towards understanding the basic MN implementation, while the actual MN design always depends on the active device, but also on the circuit designer.

PAPERS

Paper I

Paper I

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S. Andric, L. Ohlsson Fagher, F. Lindelöw, O.-P. Kilpi, and L.-E. Wernersson, "Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs," *Journal of Vacuum Science and technology* ***B***, vol. 37, art. no. 061204, Oct 2019, doi: 10.1116/1.5121017.

Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs

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We present a low-temperature processing scheme for the integration of either lateral or vertical nanowire (NW) transistors with a multilayer back-end-of-line interconnect stack. The nanowire device temperature budget has been addressed, and materials for the interconnect fabrication have been selected accordingly. A benzocyclobutene (BCB) polymer is used as an interlayer dielectric, with interconnect vias formed by reactive ion etching. A study on via etching conditions for multiple interlayer dielectric thicknesses reveals that the sidewall slope can be engineered. An optimal reactive ion etch is identified at 250 mTorr chamber pressure and power of 160 W, using an SF_6 to O_2 gas mix of 4%. This results in a low via resistance, even for scaled structures. The BCB dielectric etch rate and dielectric-to-soft mask etch selectivity are quantified. Electrical measurements on lateral and vertical III-V NW transistors, before and after the back-end-of-line process, are presented. No performance degradation is observed, only minor differences that are attributed to contact annealing and threshold voltage shift. *Published by the AVS.* https://doi.org/10.1116/1.5121017

I. INTRODUCTION

As traditional silicon complementary metal-oxide-semiconductor (CMOS) technology nodes reach their scaling limits, there is a transition to silicon-on-insulator (SOI) technology and nonplanar structures, e.g., FinFETs.[1] A potential next step on the roadmap is transistor implementations either as lateral or vertical nanowires (NWs).[1] Their specific one-dimensional transport is already thoroughly examined.[2,3] The exploration of III-V materials for NW MOSFET implementation has been investigated as well,[4,5] with the particular focus on high-frequency applications. Exceptionally high intrinsic transconductance ($g_m > 3$ mS/μm) and cutoff frequency[6,7] make III-V NW transistors ideal for radio frequency (RF) and millimeter-wave (mm-wave) applications. However, further efforts on a suitable RF back-end-of-line (BEOL), which enables large-scale circuit functionality, are still necessary.

A typical multilayer BEOL for RF applications consists of interconnects on different heights, separated by a low-κ dielectric and a variety of passive components (resistors, capacitors). The BEOL is also used for on-chip calibration[8] and deembedding[9] structures that aid accurate RF characterization of devices. Modern silicon CMOS device technologies employ specific design kits for RF applications,[10] which allow implementation of functional mm-wave circuits.[11] However, the lossy silicon substrate and high-density design rules[12–14] are limiting the RF circuit performance. Additionally, a typical Si CMOS BEOL process has a temperature budget of about 450 °C.[15,16] This is too high for III-V MOS structures[17] and NW MOSFETs, thereby require an alternative RF BEOL.

BEOL implementations utilizing benzocyclobutene (BCB),[18] as an interlayer dielectric material, show excellent high-frequency performance[19] and are commonly used for III-V technology. BCB is a spin-on dielectric, which can be cured at as low as 250 °C, with excellent planarization and step coverage, eliminating the need for chemical-mechanical polishing (CMP) in the multilayer BEOL.[18] This low curing temperature in combination with excellent dielectric properties gives BCB an advantage over materials such as spin-on-glass[20,21] or hydrogen silsesquioxane.[22] Furthermore, BCB offers mechanical stability needed for a successful via opening and metallization deposition that allows for high-quality, low-resistance interconnects to be formed.

In cases where the via metallization process relies on sputtering or evaporation, a suitably positive via sidewall slope formation is critical and should be engineered with optimum etching conditions. For BCB dry etching, typically a fluorine-based (SF_6) compound is used in combination with oxygen, allowing for efficient via etching and sidewall passivation.[23] To that end, SF_6 concentration was varied from 100% to as low as 5%,[23–25] showing that the vertical-to-lateral etch rate can be engineered with the choice of the correct SF_6 concentration. Etch selectivity and isotropy can be efficiently engineered as well, by tuning the chamber pressure.[26] However, SF_6 concentrations below 5% have not been explored, so optimum pressure and power should be derived in these cases as well.

In this paper, we establish processing techniques for the BEOL implementation on both lateral[6,7] and vertical[27,28] III-V NW MOSFETs to achieve RF circuit functionality. Dry etching of interlayer dielectric via openings is critical in this process. Reactive ion etching of BCB through a soft mask is studied in detail, with special attention to the resulting via profile, to identify a suitable process condition. The developed BEOL is also successfully integrated with in-house fabricated lateral and vertical NW MOSFETs and verified by electrical measurements.

The paper is structured as follows. Section II presents a brief analysis of the temperature budget for NW MOSFETs. Section III deals with the BEOL implementation, where for the most part via etching and metallization is being addressed,

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as they are the most crucial parts of the BEOL fabrication. Finally, in Sec. IV, integration with front-end-of-line (FEOL)—NW MOSFETs has been demonstrated and discussed.

II. III-V NW MOSFET TEMPERATURE BUDGET

The front-end-of-line (FEOL) processing descriptions in this section have a specific focus on the overall temperature budget. More details on the fabrication of NW MOSFETs are available elsewhere.[6,7,27,28] There are a few general temperature limitations during the NW MOSFET processing, primarily in the NW growth, gate oxide deposition, and contact formation. The process temperatures also depend on which NW configuration is utilized, lateral or vertical. Moreover, there may be alternatives to this fabrication approach, but they are not considered here.

A. Lateral NW MOSFETs

Regarding lateral NW MOSFETs, an InGaAs NW layer is typically grown at 600 °C by means of selective area epitaxy.[29] Furthermore, raised source/drain contacts are regrown at 500 °C, which is much lower temperature than 600–800 °C, commonly used for the deposition of SiGe contacts in the strained Si process.[30]

After Al_2O_3/HfO_2 bilayer high-κ gate dielectric is deposited, typically at 300 °C,[31] processing temperature budget is further reduced. An annealing study of metal-oxide-semiconductor capacitors shows that the performance degradation of the HfO_2-InGaAs interface occurs after 350 °C.[17] Finally, contact deposition is usually not a limiting factor in lateral NW MOSFET performance, although no detailed contact annealing study has been investigated yet.

B. Vertical NW MOSFETs

For vertical NW MOSFETs, however, the temperature budget is more restrictive. Although InAs/InGaAs heterostructure[27] NWs are grown from an Au seed particle at temperatures as high as 500 °C[32] utilizing the vapor-liquid-solid (VLS) growth method, it has been shown that the subsequent temperature increase above 350 °C will decompose the nanowire through the seed particle.[33] Such a temperature budget is more restrictive than that of lateral NW MOSFETs. However, with processing techniques similar to that of lateral NW MOSFETs, it is possible to process vertical NW MOSFETs, in spite of these temperature restrictions.

In general, vertical NW MOSFETs are considered for future applications due to their ability to decouple gate length and contact length from the footprint, which allows tighter packing. VLS growth further allows straightforward integration of III-V materials on Si. These devices rely on spacer technology to separate contacts, and therefore, an accurate control of the spacer thicknesses is needed. With stacking of different layers, properties including thermal expansion, stability, and delamination of spacers are some of the main concerns for the overall performance of the vertical NW MOSFET technology.

III. BEOL FABRICATION

Reviewing the III-V NW MOSFET processing in Sec. II A, we find that a suitable temperature budget for the BEOL is less than 300 °C. This temperature limit defines the selection of BEOL interlayer dielectric materials. In this work, we chose BCB as an interlayer dielectric. It is a spin-on dielectric with a curing temperature as low as 250 °C, which is compatible with our temperature budget.[18]

A. BEOL overview

Using a simple processing scheme, BCB layers can be deposited as thick interlayers that simultaneously planarize the sample and provide a platform for routing. Here, vertical or lateral NW MOSFET is covered uniformly, thanks to the excellent planarization properties and thickness of BCB. Moreover, the fabrication of interconnect vias, where the main part is via etching, is explored. Finally, metallization itself is not temperature-critical, as it relies on evaporation and lift-off process, with temperature steps up to 100 °C only. The complete BEOL stack is shown in Fig. 1.

A simple BEOL developed for NW MOSFETs consists of four metal layers (MET1-4), two interlayer dielectrics (ILD1-2), one thin-film resistive layer (TFR), and one capacitor dielectric layer (CAP), so that RF circuit functionality can be implemented. With the TFR layer, resistors can be implemented, while with a selected thickness of the CAP layer, sandwiched between metal contacts, a specific capacitance density metal-insulator-metal (MIM) capacitor can be realized. The interlayer dielectric (ILD) layers support routing of metal lines and interconnect vias. The thickness of ILD and MET layers has been selected to satisfy specific requirements for RF and mm-wave operation, for which III-V NW MOSFETs and the BEOL are intended.

B. BCB-based BEOL fabrication technology

The BEOL process described below begins with the completion of the FEOL process.[6,27] In order to build the interconnect layer stack, Cyclotene 3022 series electronic resin is spun onto $10 \times 10\,mm^2$ sample piece and cured into BCB

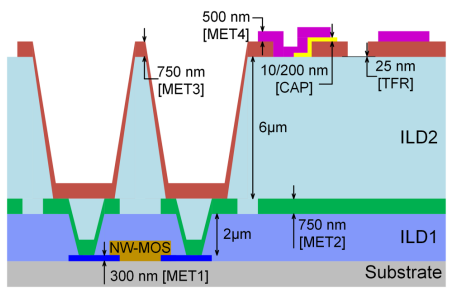

FIG. 1. Schematic BEOL dummy cross section, showing metal (MET), interlayer (ILD), capacitor (CAP), and resistor (TFR) layers, including via structures to an NW MOSFET.

polymer layer. Then, ma-N 400 series negative tone photoresist soft mask is spun, exposed through a UV contact aligner lithography system. Unexposed areas are developed, thus creating desired pattern. Vias are opened through a pattern-transfer technique in O_2/SF_6 plasma, where both BCB and ma-N photoresist are etched simultaneously. The ma-N 400 series photoresist is also used as a lift-off mask in the metal evaporation process, with different exposure/development conditions. Finally, the resistor layer is fabricated in the evaporation/lift-off process as well, while the capacitor dielectric is deposited through plasma-enhanced chemical-vapor deposition (PE-CVD) and patterned with the etch-back process.

The spinning speed and time in spin-coating determine the final BCB layer thickness. Our chemicals used to synthesize BCB polymer include Cyclotene 3022-46 and Cyclotene 3022-57, all spun according to spin curves provided by Dow Chemicals. After the layer has been cured at 250 °C in an N_2 atmosphere, the obtained BCB layer thicknesses are 2 and 6 μm for Cyclotene 3022-46 and 3022-57, respectively.

Layer thickness and surface roughness has been evaluated using profilometer scans, by measuring the etched via height or the flat surface of the BCB layer. The profilometer measurements reveal surface roughness in the order of 5 to 10 nm at the 0.5 mm scanning range. The good planarization properties of BCB monomer layer, including step coverage, provide a surface on which interconnects can be deposited without the need for CMP, allowing for planar metal line deposition.

C. Via etching considerations

In order to establish interconnect vias, a soft mask is fabricated on top of the cured BCB layer. For this purpose, an ma-N 400 series photosensitive resist, from Micro-Resist Technology, has been applied. As for BCB, the final thickness of the photo resist depends on the spinning speed and time. Targeted resist thicknesses have been 3 and 7 μm, obtained from ma-N 440 and ma-N 490 photoresists, respectively. The photoresist is then exposed using a contact aligner and developed with an ma-D 532/S developer, from Micro-Resist Technology.

The resulting structure is shown in Fig. 2. Development time has been adjusted so that mask opening at the bottom is smaller than at the top, thus allowing for a positive sidewall slope. Target dimensions for the mask openings are $5\times5\,\mu m^2$ and $10\times10\,\mu m^2$, for 2 and 6 μm thick BCB layers, respectively. Additionally, a scaling study has been performed for these layers, and a minimum size of $2\times2\,\mu m^2$ vias has been fabricated and measured. This size is limited by contact aligner's resolution. On the other hand, our interest lies in low-resistance vias, whose size should be larger than $2\times2\,\mu m^2$, since smaller vias negatively affect the RF performance due to the increase in resistance.

Via etching has been performed in a reactive ion etcher (RIE), from TRION. The process has been optimized to engineer the sidewall slope for metal evaporation, while maintaining rather short total etch time. This has been achieved through a high pressure and high-power plasma etch process, with a specific ratio of SF_6 to O_2. The selected ratio is 4%,

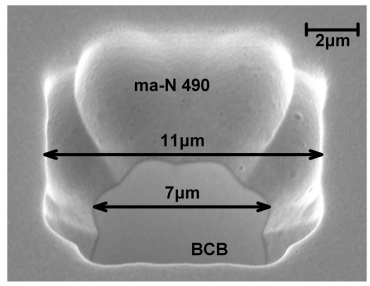

FIG. 2. SEM 30° tilted-view micrograph of a 7.5 μm-thick ma-N490 photoresist used as soft mask for BCB dry etching, with defined opening of 10 μm, showing well-behaving sidewalls and marked size of the opening at the top and the bottom of the ma-N490 layer. The structure is fabricated on top of the 6 μm-thick BCB layer, which rests on the Si substrate.

which corresponds to the total ratio of Si in fully-cured BCB, and may result in full utilization of SF_6 in the etching process. As SF_6 will only etch Si from the BCB polymer backbone, a high concentration of SF_6 will adversely affect the etch rate and will not contribute to chemical etching process.[25,26] Therefore, only the chamber pressure and power have been varied, in observation of the etch rate, etch selectivity, and final via shape, while the gas composition and total gas flow have been kept at specified values. After the BCB layer has been etched, the layer thickness has been measured with a Dektak Stylus Profilometer, from which etch rate and etch selectivity are calculated.

Metallization has, in this case, been done through metal evaporation and a lift-off process. As most metals do not adhere to the fully-cured BCB, a 5-nm-thick Ti layer is initially evaporated, to provide the necessary adhesion to the BCB, followed by a subsequent evaporation of 750 nm Au. The lift-off mask utilizes an ma-N 440 photoresist. In the case of evaporation, the photoresist development time has been adjusted so that the sidewalls generate a negative slope, opposite to the one needed for etching (Fig. 2), thus preventing flake formation on the edges of the metal layers, which can happen as a result of metal deposition on to the sidewalls of the photoresist mask.

D. Lumped passive components

To enable passive component functionality in the BEOL layer stack, two additional layers are deposited. Prior to MET3 deposition step, a 25-nm-thick NiCr TFR layer is deposited by the metal evaporation and the lift-off process. It is the equivalent process used for metal line evaporation and patterning. After MET3 evaporation, a capacitor dielectric is deposited by plasma-enhanced chemical-vapor deposition (PE-CVD). Here, the plasma-enhanced process enables a high-quality layer deposition at reduced temperatures. We use 200 °C as the deposition temperature, to deposit either 15 nm- or 200 nm-thick Si_3N_4 layers, used for high-quality MIM capacitors, where the capacitance

density is determined by the layer thickness. This layer is patterned by an etch-back process, using SF_6-based plasma in RIE. Finally, a 500 nm Au MET4 layer, which represents the top electrode for the MIM-capacitors, is evaporated through a lift-off mask, completing the entire BEOL stack.

IV. RESULTS AND DISCUSSION

A. BCB etching

A matrix of via cross sections for a 6-μm-thick BCB layer on Si is shown in Fig. 3. Here, a thin Au layer was sputtered to ensure proper contrast in the scanning electron microscope (SEM) so that the sidewalls can be clearly visualized. Each sample was processed with different RIE chamber pressures and RF powers.

Selected RIE chamber pressures are 200, 250, and 300 mTorr, while the selected RIE RF powers are defined as 140, 160, and 180 W. From the observed data, we conclude that for a very high chamber pressure, the etching dependence on the RF power diminishes. The sidewall slope is very steep, and thus not optimal for metal evaporation. Additionally, vias are very wide, suggesting significant mask erosion. The via widening due to mask erosion during the etching process is described elsewhere.[23]

The contour plot in Fig. 4 shows BCB etch rate dependence, with respect to RF power and chamber pressure. The etch rate is calculated with height data obtained with profilometer measurements, while an interferometric end-point detection system, available in RIE, is used to monitor the etching time. An interesting dependence occurs at a lower chamber pressure, where the selected RF power shapes the via sidewall slope. In general, a lower power implies that there will be more chemical etching than physical, while a low chamber pressure ensures proper control on the amount of etching. In Fig. 4, we notice that the etch rate is reduced at lower powers, as expected but also at higher pressures. Here, the efficient decomposition of reactive gasses is inhibited by

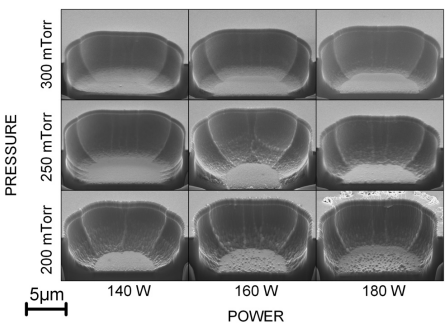

FIG. 3. SEM 52° tilted-view images, showing cross sections of etched 6 μm vias with the RIE chamber pressure variation from 200 to 300 mTorr (bottom to top row), while the power was swept from 140 W to 180 W (left to right column), for the total gas flow of 78 sccm and 4% SF_6 in the gas mix. Vias are opened with focused ion beam (FIB), available in SEM.

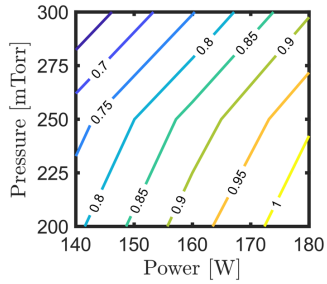

FIG. 4. Interpolated contour plot of BCB etch rate dependence, in μm/min, on the RIE chamber pressure and RF power for 4% SF_6 in the O_2/SF_6 gas mix. Numbers marked on the lines show the contour where the specific etch rate can be obtained.

molecule interaction in the chamber, therefore reducing reactant availability, and finally, the etch rate.

On the other hand, more chemical etching will inevitably ensure reaction of O_2 plasma with the photoresist mask, which will, in turn, change the selectivity between the ma-N 400 photoresist and the BCB, in favor of BCB. The contour plot in Fig. 5 shows etch selectivity of BCB to the ma-N400 photoresist mask. Etch selectivity increases when the chamber pressure is lower, which might imply more efficient decomposition of reactant gases. Also, the obtained selectivity is close to 1, suggesting that BCB and photoresist have similar etch rates under selected chamber conditions. Therefore, we conclude that careful selection of chamber pressure and power, in combination with the photomask thickness, is required to obtain an optimal sidewall slope of 45° from the underlying substrate.

Finally, all processing is established with the choice of 160 W RIE RF power, and 250 mTorr chamber pressure, as reference etching conditions, giving the desired via sidewall slope with the acceptable etch rate and etch selectivity. As a result, sidewalls can be uniformly covered with evaporation through a lift-off mask, which enables good quality

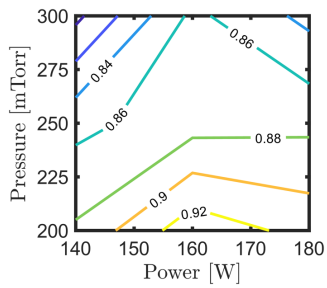

FIG. 5. Interpolated contour plot of ma-N 490 photoresist to BCB etch selectivity (unitless), with dependence on RIE chamber pressure and RF power for 4% SF_6 in O_2/SF_6 gas mix. Numbers marked on the lines show the contour where the specific etch selectivity can be obtained.

interconnect via, suitable for low-loss RF and mm-wave signal propagation.

B. BEOL interconnect stack evaluation

BCB etching is just one of many steps included in the full BEOL process. In Fig. 6, a via interconnect stack is shown. It starts with the FEOL metal layer (MET1), allowing for NW MOSFET characterization prior to the BEOL ILD layers deposition. After MET1 layer, ILD1 layer is spun and cured to 2 μm final thickness. Then, vias are etched via the pattern-transfer technique from the ma-N 400 series photoresist, followed by an angled via metal evaporation and a 0° tilt evaporation of the rest of the line structures.

MET2 layer is evaporated in a similar way to MET1. Subsequently, a 6 μm-thick interlayer dielectric (ILD2) has been spun after MET2 metallization, followed by the same procedure for etching and via and line evaporation. Additionally, layers that define resistors and capacitors can be deposited before and after MET3 layer, respectively. MIM-capacitor layers are connected by evaporating MET4 layer as final fabrication step. This brings the complete circuit functionality into the sample, all together with NW transistors.

The via sizes have to be optimal for connecting the MOSFETs, while still manufacturable on complicated stacked structures, like vertical NW transistors. For this reason, a basic scaling study has been performed. ILD1 via openings have been defined in the range from 2 μm to 5 μm, in steps of 1 μm, while ILD2 openings have been defined as 5, 6, and 7 μm. The final size of the etched vias will, however, be larger, due to mask erosion in the RIE process.[23] Via size can be directly transferred through anisotropic etching in the RIE process, but that will hinder sidewall slope metallization. Instead, etching conditions that ensure metal coverage of via sidewalls are targeted, yielding an increase in the via size, as compared to the developed etch mask.

To be able to measure the accurate value of via resistance, a four-point Kelvin measurement[34] is performed on an array of vias. The averaged via resistance measurement results, for different runs, are shown in Fig. 7. Values for via sizes are

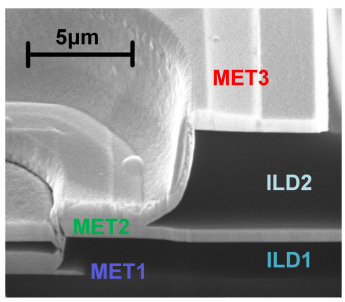

FIG. 6. SEM 52° tilted-view of a via cross section profile from the substrate to the top metal layer, showing various interlayer dielectrics and metal layers. Vias are opened with FIB, available in SEM.

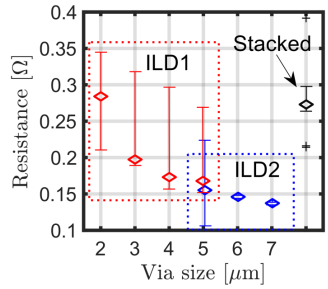

FIG. 7. Measured DC via resistance as a function of via size. Measured vias include ILD1 and ILD2 vias, as well as stacked (ILD1 + ILD2) via. Variation in resistance values is measured throughout 1 × 1 cm sample, on several fabrication runs. Diamonds (◊) represent median values, while limit lines define 99% range of values. Values marked with cross (+) are the outliers, appearing less than 1% of the cases.

defined openings in the mask. For the majority of values, there is a trend where with a reduction in via dimensions, the total metal width is reduced, thus giving a rise in resistance. In general, the values are several orders of magnitude lower than the typical transistor on-resistance, which will be discussed in Sec. IV C. Vias should not, therefore, influence the total current of the MOSFET, thus enabling low-resistance connection from FEOL to the BEOL, which is essential in retaining DC and RF-performance.

The stacked via (ILD1 + ILD2 via) total resistance amounts to approximately 0.27 Ω, and is not significantly influenced by the variation of processing conditions. The reason why the resistance of 7 μm ILD2 via and 2 μm ILD1 via do not add up in stacked via structure is that more metal is evaporated in the ILD1 via, thus reducing the ILD1 via resistance further. The stacked via resistance should be added to the gate parasitic resistance, or drain contact resistance in the NW MOSFET, while the source contact in NW MOSFET, generally consists only of ILD1 via.

C. BEOL cointegration with NW MOSFETs

The final verification is to fabricate BEOL on top of NW MOSFETs, both in lateral and vertical configurations. For this purpose, BEOL test layouts have been developed and the structures subsequently fabricated. To provide an example of such BEOL test structures, BEOL contacts have been fabricated on top of vertical III-V NW MOSFETs.

An optical micrograph containing the structure is shown in Fig. 8. The structure shown includes one BCB interlayer dielectric deposition and via etching, in addition to the metallization step, where contacting pads are evaporated through a lift-off mask. Via metallization has been done in a separate evaporation step, ensuring low via resistance values. Cointegration of lateral III-V NW MOSFETs with the BEOL has been completed as well, with a structure similar to the one shown in Fig. 8.

To evaluate the MOSFET performance, a DC characterization and comparison between the FEOL and BEOL

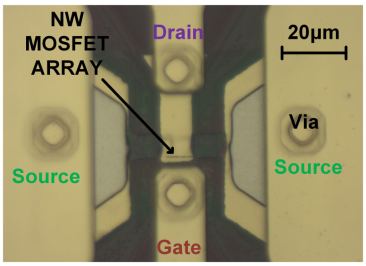

FIG. 8. Optical micrograph of the first interconnect layer on vertical NW MOSFETs, showing top view of the vertical NW MOSFET structure of top of which one BCB and one metal layer have been deposited, with separate via metallization layers visible.

measurements have been made as well, on both lateral and vertical NW MOSFETs. Lateral III-V NW MOSFETs have 200 wires, with a gate length of 70 nm.[6] Wires are 10 nm high and 30 nm wide. The channel material is not intentionally doped InGaAs, while the contacts consist of regrown InGaAs n^+-layers. Two such lateral III-V NW MOSFETs have been fabricated and measured. The first is measured on the FEOL level, while the second is measured after BEOL is applied. Vertical NW MOSFET has 280 heterostructure InAs/InGaAs wires, with an average diameter of 28 nm.[27]

Figures 9 and 10 show the comparison between the MOSFET performances. The BEOL measurements have been done through the full BEOL stack, as shown in Fig. 7. Note that, for lateral NW MOSFETs, the transistors in FEOL and in BEOL are not the exact same device, but rather neighboring devices fabricated at the same time, on the same die, due to processing restrictions. The vertical NW MOSFET is the same device measured before and after BEOL. Figure 9 shows the transfer characteristics, together with transconductance values, while Fig. 10 shows the output characteristics.

For transfer curves, both MOSFETs source-drain voltage was set to $V_{DS} = 0.5$ V, and the current dependence on gate-source voltage, V_{GS}, is measured. From Fig. 9, it can be seen that the transistor exhibits similar current-voltage behavior. When looking into peak g_m, we examine a V_T shift, which may be a result of curing the gate dielectric, as

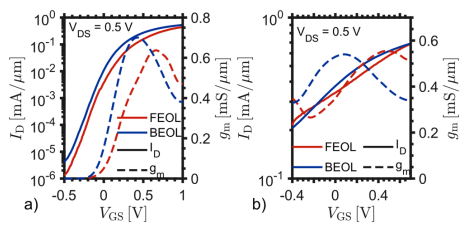

FIG. 9. Transfer characteristics of (a) lateral, and (b) vertical NW MOSFETs, showing current measurements at the FEOL and on BEOL level, normalized to the gate width. The MOSFET transconductance (g_m) has also been included (dashed line).

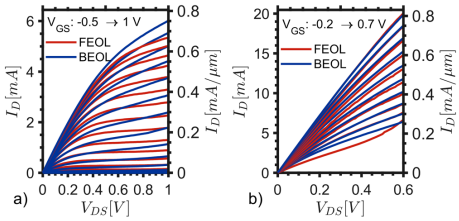

FIG. 10. Output characteristics of (a) lateral, and (b) vertical NW MOSFETs, measured at the FEOL, and on the BEOL level.

well as the contacts. Contact annealing may explain the improved peak g_m. Additionally, lateral NW MOSFETs have good off-state current ($I_{off} < 10$ nA/μm) and subthreshold slope ($SS_{min} = 120$ mV/dec.), which is retained after the BEOL process.

In Fig. 10, we see that the MOSFET on-resistance is approximately 100 Ω for lateral and 25 Ω for vertical NW MOSFET. Comparing to 0.27 Ω for a single stacked via, we conclude that the effect of adding interconnect vias does not significantly influence the overall performance of the NW MOSFET. Again, the only observable difference is V_T shift, which we can also derive from transfer curve measurements. In the case of vertical NW MOSFETs, this is clearly visible in the output characteristic as well, when the MOSFET has a negative gate bias, experiencing different current levels for the same V_{DS}.

V. SUMMARY AND CONCLUSIONS

We have developed a BEOL technology compatible with III-V NW MOSFETs in both lateral and vertical configurations. The aspects of device temperature budget, contact formation, and spacers have been identified as crucial for pushing NW technology from the device level to the circuit level. In line with these considerations, BCB is selected as the interlayer dielectric that will support different BEOL metal structures routed on top of the FEOL transistors. A study on via etching was performed and metallization shows that the total via resistance is in the order of 0.27 Ω, a very low value compared to the MOSFET's on-resistance. Additionally, the BEOL has been applied to III-V NW MOSFETs. Electrical characterization of both lateral and vertical NW devices shows that the performance is maintained during the BEOL process, retaining the current, as well as on-resistance. A threshold voltage shift is observed, but further studies are required to clearly identify its cause. These results show that this BEOL process is promising for future complex circuit implementations.

ACKNOWLEDGMENTS

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Paper II

Paper II

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S. Andric, L. Ohlsson, and L.-E. Wernersson, "Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III–V MOSFETs on Silicon," *92nd Microwave Measurement Conference (ARFTG)*, Orlando, FL, USA, pp. 1–4 Jan. 2019, doi: 10.1109/ARFTG.2019.8637222..

Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III–V MOSFETs on Silicon

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***Abstract* — A multiline Thru-Reflect-Line (mTRL) calibration and parasitic pad removal kit is presented, intended for mm-wave III-V nanowire MOSFET characterization. Multiline TRL is implemented in a low-temperature BEOL process with substrate decoupled microstrip transmission lines. The transmission line characteristic impedance needed for accurate mTRL calibration is modelled. Simulated transmission line parameters show a good fit with measured transmission line data, including line characteristic impedance variation. Line loss less than 0.5 dB/mm up to 50 GHz is obtained. Finally, interconnect via section is calibrated and modelled, showing mTRL's ability to obtain small parasitic parameters.**

***Index Terms* — Back-End-Of-Line (BEOL), Benzocyclobutene (BCB), Microstrip Transmission Line, Nanowire MOSFET, On-wafer Calibration, Thru-Reflect-Line (TRL)**

I. Introduction

Characterization of intrinsic transistor performance at radio (RF) and millimeter-wave (mm-wave) frequencies poses a significant challenge [1]. Complications are related to instrument calibration and on-wafer deembedding techniques, where probing pad parasitics are removed from measured data. Device parasitics are easily misjudged due to non-ideal definition of reference standards in the complex environment of a monolithic circuit. In addition, most standards will deviate from ideal behavior with increasing frequency [2].

To address future transistor performance needs, III-V nanowire (NW) MOSFETs integrated on silicon (Si) are a promising candidate [3-4]. On the front-end-of-line (FEOL) level, their device contacts are typically defined on multiple levels in a dielectric environment. Even if thoroughly characterized at the FEOL level, RF circuit design takes place on the back-end-of-line (BEOL) level.

A device access structure, consisting of metallized vias, must be used to interface between FEOL devices and BEOL circuit environment. To provide maximum device performance at the circuit level, this access structure is required to provide low loss and minimal reactive parasitics. It must also support a well-defined calibration reference plane at BEOL level to yield data useful in circuit design. Furthermore, knowledge of the parasitic structure in the interface module connecting FEOL and BEOL allows for direct translation of performance between the two levels, accelerating the design cycle. Therefore, to maintain integrity and performance of scaled III–V NW MOSFETs, the BEOL must be fabricated at a limited thermal budget.

In this paper, we demonstrate the implementation of an RF BEOL compatible with the low thermal budget required by III–V NW MOSFET technology. Microstrip transmission line technology is utilized to implement a set of multiline thru-reflect-line (mTRL) calibration kits [5-7]. It offers high accuracy over a defined bandwidth, while maintaining simplicity in structural design. Initial modelling of the device interface module, connecting between FEOL and BEOL, is also evaluated.

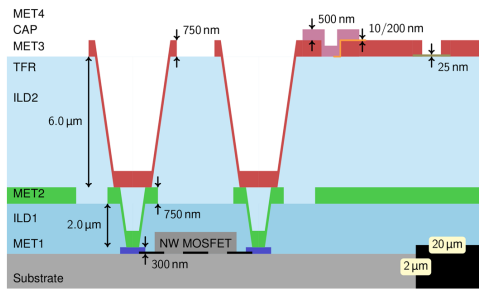

Fig. 1. Schematic BEOL dummy cross-section, showing metal (MET), interlayer (ILD), capacitor (CAP) and resistor (TFR) layers, including via structures to a NW MOSFET.

II. BEOL Fabrication and TRL Overview

A schematic cross-section of the implemented BEOL is shown in Fig. 1. It contains two interlayer dielectric (ILD) layers, four metal (MET) layers, one thin film resistive (TFR) layer, and one thin capacitive (CAP) layer. This front-side only RF BEOL is intended for co-integration on FEOL technologies utilizing III–V nanowire MOSFETs. The first interlayer dielectric provides separation between the device contacts (MET1) and the RF groundplane (MET2). A thicker interlayer dielectric (ILD2) supports microstrip transmission lines and passive devices formed in the top layers (TFR, MET3, CAP, and MET4), facilitating RF signal propagation, matching, and stabilization.

The interlayer dielectrics are realized by Dow Cyclotene™ spin coating and curing into benzocyclobutene (BCB), which has low relative dielectric permittivity, $\varepsilon_r = 2.7$. The layers

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are cured in nitrogen ambient at only 250°C to preserve the III-V nanowire MOSFET technology. Interconnect vias are dry etched in O_2/SF_6 based RIE through a soft mask. All metal layers are deposited by thermal evaporation of Ti/Au through a lift-off mask. The thin film resistive layer is NiCr with a sheet resistance of 100 Ω/□, patterned by lithography and thermal evaporation in a lift-off process. Capacitors, deposited by means of low temperature ICP-PECVD and liftoff, are formed by sandwiching SiO_2 between the topmost metal layers. All lithography steps utilize soft UV exposures.

This simplistic fabrication scheme with a low temperature budget is compatible with our in-house III-V NW MOSFET technologies. It also allows co-integration on, e.g. high-density Si CMOS technologies enabling digitally-assisted mm-wave circuits with access to a low loss RF BEOL.

A. TRL Kit Description

The microstrip transmission line environment is ideal for front-side BEOL implementation. It decouples the RF signals from substrate effects (loss and mode coupling) by means of the groundplane. Transmission lines and discrete passive components are placed on the topmost BCB layer (ILD2). The groundplane is only opened at via positions to the substrate level and at 100 µm pitch RF probe pads. A tapered transition and a 100 µm line section is used to feed the calibration reference plane. This allows for evanescent mode decay and establishes well behaved quasi-TEM propagation.

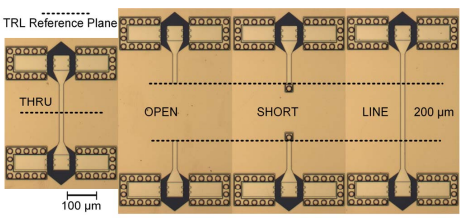

Fig. 2. Optical micrograph showing different TRL standards: THRU, OPEN, SHORT and 200µm long LINE standard, shown left to right, respectively, with marked calibration reference plane

A calibration kit with structures that support on-wafer mTRL has been fabricated, as shown in Fig. 2. The mTRL calibration procedure is based on a few basic structures. They consist of a "THRU" standard, where RF pads and access structures are connected back-to-back. By contrast, the individual reference planes of the "REFLECT" standards ("OPEN" and "SHORT") are separated by 200 µm to minimize crosstalk. Multiple "LINE" standards have also been fabricated. Their lengths yield the valid frequency band of the mTRL routine, loosely defined by the propagation phase range from 20° through 160°. Fabricated microstrip line lengths are 200 µm, 600 µm and 1mm, which, considering the approximate microstrip mode effective dielectric permittivity $\varepsilon_{eff} = 2.3$, corresponds to the bandwidth 10–440 GHz.

The mTRL calibration routine requires the characteristic impedance (Z_0) of the transmission line to be known per frequency. An incorrect impedance assumption leads to improper s-parameters scaling and deteriorated calibration accuracy. In general terms, the line impedance is

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}}, \tag{1}$$

where R', L', G', and C' are resistance, inductance, conductance, and capacitance per unit length, respectively, while $\omega = 2\pi f$ denotes angular frequency. These frequency dependent line parameters are found during calibration, under the assumption of a characteristic impedance, determined separately. We use values calculated by Keysight ADS for the specific geometry utilized, together with line DC resistivity measurement. Additionally, the line and dielectric parameters determine the propagation constant

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta, \tag{2}$$

where α is the attenuation and β is the phase constant. It is derived from TRL measurements directly and only assumes invariant error boxes connecting to the reference plane.

B. Measurement Procedure

The fabricated structures are measured up to 67 GHz using Cascade i67 100µm-pitch GSG probes, and a Rohde&Schwarz ZVA67 vector network analyzer. The first-tier LRRM instrument calibration is done using a Cascade impedance standard substrate (ISS 109-101C). A second-tier mTRL calibration is then performed, which sets the reference plane shown in Fig. 2. The probing setup is then ready for the circuit level device measurements. Device research typically includes further deembedding measurements, providing access to intrinsic FEOL device data, excluding the interface structure parasitics. All measurement data is processed in Cascade WinCal 4.6.

The first-tier calibration is performed initially in order to evaluate performance of on-wafer standards, prior to second-tier calibration. After the first-tier instrument calibration with the off-wafer calibration kit, the on-wafer mTRL kit is measured in a specific order: THRU, OPEN, SHORT, LINE1, LINE2, and LINE3, as a part of a second-tier calibration. For successive standards, the distance between probes has to be changed. This is a drawback of the TRL calibration, where any change of the distance between probes changes cross-talk terms in the error box. Increased redundancy compensates for possible crosstalk errors due to spacing variation between probes, providing robustness. To enable this, the dual REFLECT standards (OPEN and SHORT), and several LINE standards with different lengths are utilized in mTRL.

III. Results And Discussion

A. Transmission Line Parameters

A microstrip transmission line cross-section with all relevant dimensions is shown in Fig. 3(a). The line width is set to 16 µm, which corresponds to the characteristic impedance of approximately 50Ω. This is a line design in one of the mTRL calibration kits. The mTRL kits were fabricated on both semi-insulating InP and high-resistivity Si substrates to verify the effectiveness of the microstrip groundplane. As shown in the measured data in Fig. 3(b), no significant contribution from substrate is present in attenuation. Fig 3(b) also shows that the transmission line model generated by ADS gives a good fit to the measured data, using a dielectric loss tangent, $\tan\delta_{BCB} = 10^{-2}$ for the BCB. The resulting attenuation constant of 0.5 dB/mm at 50 GHz is comparable to other BCB-based processes in use today [8-9].

The attenuation at low frequency is governed by metal loss, as expected. However, the measured attenuation exhibits a slope transition, approximately above 30 GHz. This can be attributed to Debye-type dielectric relaxation centered at frequencies far above the measurement range, dominating over the total loss at high frequencies. One possible explanation is the low BCB curing temperature which can result in the polymerization rate less than 100% [10]. Additionally, groundplane opening beneath probe pads could cause complex behavior in attenuation. However, as seen from Fig. 3b, there is no significant substrate effect present. Therefore, further investigation is needed to determine the loss mechanism. Finally, we attribute the periodic ripple to cable movements during TRL measurements, while deviations around 55 GHz correspond to probe placement variability on the measurement pads.

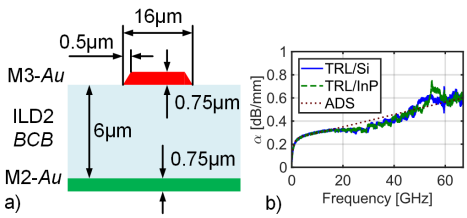

Fig. 3. a) A 50Ω microstrip line cross-section (not to scale) showing line (red) and groundplane (green), separated by the thick interlayer dielectric (blue) layer and b) measured and simulated attenuation constant for microstrip lines on Si and InP substrates.

A range of line impedances are necessary in RF and mm-wave circuit design. To evaluate the implemented design environment further, TRL kits with line width variation were fabricated. Fig. 4(a-b) shows measured and modelled components of the propagation constant for line widths of 8µm, 16µm, and 43µm, which correspond to approximately 75Ω, 50Ω, and 25Ω, respectively. The agreement between measured and simulated data shows that the ADS model can be applied to a wide range of line dimensions, and that measured line parameters are acceptably captured by the model used. Distributed line parameters are also found in reasonable agreement, as shown in Fig 4(c-f), which follows from assuming the characteristic impedance from ADS for the TRL data. We attribute the deviations in distributed resistance and especially the complex behavior of the conductance at low frequency to limited models of skin effect and dielectric loss.

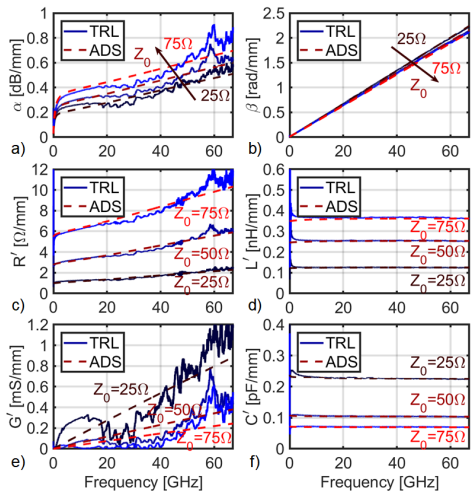

Fig. 4. a) Measured and simulated line attenuation constant, and b) phase constant vs frequency, with respect to the characteristic impedance Z_0 = 25Ω, 50Ω, and 75Ω; c) Measured and simulated line distributed resistance, d) inductance, e) conductance, and f) capacitance per unit length; with respect to the characteristic impedance Z_0 = 25Ω, 50Ω, and 75Ω

B. Component Calibration and Deembedding

The second-tier mTRL calibration establishes a microstrip reference plane on-wafer. Effectively, the RF probing pads, signal line tapering, and access microstrip line are calibrated out. This enables precise circuit level parameter derivation in the frequency band of interest for BEOL design. However, device studies also require deembedding of the stacked-via interface structure between BEOL and FEOL.

A scanning electron microscope (SEM) image of a measured stacked via structure on Si substrate is shown in Fig. 5(a). It illustrates how the metal layers contact from MET3 by MET2 down to MET1 layer. The structure has been fabricated and measured with RF probing pads and access lines, which are then effectively removed with the mTRL calibration. A calibrated measurement to simulation

comparison of a "MET1-OPEN" deembed structure is shown in Fig. 5(b). It describes the response of two stacked vias with an underlying, non-connected MET1 pad, which would be used as part of a standard two-step deembedding technique [11].

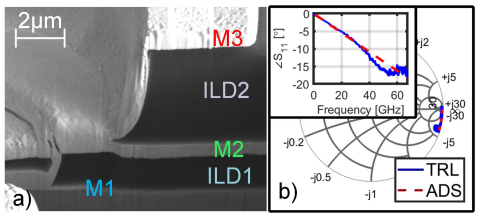

Fig. 5. a) SEM image of via structure connecting MET3, MET2 and MET1 layer; b) Simulated and measured reflection coefficient (s_{11}) and phase (inset) vs frequency, of stacked via structure terminated with "MET1-OPEN" standard

Modelling the structure, via resistance is estimated with DC measurements. For a total capacitance estimation, individual via capacitance is separately calculated, as well as capacitance between all neighboring segments, which are not belonging to individual vias. Self-inductance of individual metal segments have also been considered [12]. This quasi-physical model, consisting of lumped components implemented in ADS, shows good agreement to the measurements. The effective capacitance seen from the reference plane is $C_{via} = 8fF$, a relatively low value. We, once again, attribute parts of the deviations about 55 GHz to probe placement, but also to the complex mode matching problem; a transition from BEOL quasi-TEM microstrip mode to FEOL point contacts. This second-order effect needs to be evaluated further.

IV. Conclusion

An mTRL calibration kit has been presented using a simple BEOL design with low-temperature processing scheme. As part of the mTRL calibration kit, microstrip transmission line parameters were measured and a model has been implemented to simulate the line performance. Microstrip lines show less than 0.5 dB/mm loss at measured frequencies up to 50 GHz, while simulations are able to predict line behavior when line width is varied. The implemented RF BEOL was also verified to not depend in the underlying substrate. This promises successful integration on a variety of FEOL technology platforms. As proof-of-concept, small interconnect vias were measured and corrected with mTRL, showing good fit to a physical model used to describe via behavior. This low loss RF and mm-wave environment is henceforth universally available for future circuit design, as well as complex device and circuit characterization, such as III-V nanowire MOSFETs on Si.

Acknowledgement

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Paper III

Paper III

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S. Andrić, F. Lindelöw, L. Ohlsson Fhager, E. Lind, and L.-E. Wernersson, "High-Frequency Circuit-Level Characterization of Lateral III-V Nanowire MOSFETs," *Manuscript submitted to IEEE Transaction on Microwave Theory and Techniques*, Mar. 2021.

High-Frequency Circuit-Level Characterization of Lateral III-V Nanowire MOSFETs

Stefan Andrić, Fredrik Lindelöw, Lars Ohlsson Fhager, Erik Lind, Lars-Erik Wernersson

***Abstract*—Lateral nanowire MOSFETs are a promising candidate for high-frequency electronics. However, their circuit performance is not yet assessed. Here, we demonstrate a path to establish and understand lateral nanowires integration into the circuit environment. Devices are fabricated in a simple scheme with a DC transconductance of up to 1.3 mS/μm, on-resistance down to 265 Ω·μm, and cut-off frequency up to 250 GHz. The circuit model estimates 25% device parasitic capacitance increase due to back-end-of-line dielectric cladding. Interconnect vias contribute with additional capacitance of 8 fF, a value comparable to device parasitics. A low-noise amplifier input stage is designed with optimum network design for a noise matched input, and an inductive peaking output. The input stage shows 3.5 dB gain and 2.5 dB noise figure, at 60 GHz. Moreover, a device scaling study in the circuit environment has been performed. The amplifier response reveals a clear shift in input reflection, which is directly related to the intrinsic device performance. The device parasitic capacitance is estimated to be 6.5±0.5 fF for a 2×7μm (200 nanowires) device. The obtained intrinsic capacitance has a value of 0.34 aF per nm gate length per nanowire, which is comparable to the theoretical capacitance value. The characterization method shows the benefit in integrating MOSFETs into a circuit environment, with enhanced process stability as well as the possibility to evaluate device gate-length scaling properties on the circuit level.**

***Index Terms*—Lateral, Nanowire, FEOL, BEOL, III-V, InGaAs, LNA, Capacitance modelling, Nanowire circuits.**

I. Introduction

NANOWIRE (NW) MOSFETs have gained attention in recent years due to their opportunity as a candidate for future device scaling [1]. Geometries and materials are explored to support the need for high-performance devices and circuits in modern communication systems. Their benefits are related to the use of In-rich III-V materials, and in their low material volume at scaled geometries [5]. In-rich materials show excellent properties in high-performance high electron mobility transistor (HEMT) and MOSHEMT planar structures and are attractive for quantum applications due to weak interaction of electrons with the crystal lattice [10].

III-V materials offer superior transport properties such as electron mobility, mean free path, and high injection velocity [6]. Epitaxially-grown composite substrates have been used for high-performance III-V HEMTs, with cut-off frequencies above 1 THz [9]. The basis for this outstanding performance is the efficient heterostructure engineering that is easily achievable with different III-V material compositions. This allows for electron confinement and formation of two-dimensional electron gas (2DEG) which is transported quasi-ballistically along the channel. However, the gate-length scaling in HEMTs scales the Schottky barrier, thus deteriorating the channel control.

In III-V nanowire MOSFETs, a superior gate control is obtainable even for extremely scaled devices [11]. The high surface-to-volume ratio in these structures implies that surface effects will dominate device operation [12]. However, improvement in short-channel effects, such as drain-induced barrier lowering (DIBL) and impact ionization, outweigh the drawbacks. Additionally, III-V nanowire MOSFETs have shown state-of-the-art transport properties, including a very high transconductance, even when integrated on a Si platform [13]. III-V lateral nanowire (LNW) /tri-gate/ MOSFETs have shown exceptional performance as well, having reported mean-free-path of 140 nm, and transconductance of 3.3 mS/μm, for 8-nm-thick $In_{0.85}Ga_{0.15}As$ channels [11]. The electrostatic control of these devices is exceptional, with slopes close to the theoretical limit and suppressed short-channel effects [14],[15].

Regarding III-V lateral nanowire MOSFET high-frequency performance, cut-off frequencies of about 400 GHz have been reported [16][17]. This is attributed, much like in HEMTs, to a low effective mass, and combined with a high injection velocity, III-V LNW MOSFETs exhibit some of the highest drive currents. Moreover, their intrinsic channel capacitances are low, so the device performance is mainly limited by parasitic capacitances and access resistances. With improved control of these parasitics, as characterized in this paper, an improved high-frequency performance is expected. Therefore, the III-V LNW MOSFETs are an interesting option for high-frequency circuit design.

To establish a III-V LNW MOSFET circuit design platform, the integration of III-V LNW MOSFETs into a circuit environment is essential. Development and integration of back-

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end-of-line (BEOL) is needed, especially for radio-frequency and millimeter-wave (RF and mm-wave) applications. Additionally, characterization of these devices on the circuit level and as part of a circuit block would provide information about their application space, as well as understanding their intrinsic properties. It will enable further mm-wave integrated circuit (MMIC) design and characterization

In this work, we present a III-V LNW MOSEFT technology platform, consisting of LNW RF devices, combined with RF BEOL, circuit design, and implementation. Section II provides description of the technology platform, including the integration of nanowire devices into the BEOL, and the circuit design strategies. In Section III, a characterization of required circuit passive components is performed, while Section IV addresses fabricated LNA input stage performance, as compared to the design. Finally, the benefits of the technology platform are demonstrated through gate-length scaled circuit characterization, with the MSOFET intrinsic properties derived directly from circuit measurements.

II. III-V Lateral Nanowire MOSFET Technology Platform

The technology platform for III-V LNW MOSFETs consists of fabrication of lateral-nanowire-based devices and circuits, and device and circuit design using established models. Initially, both front-end-of-line (FEOL), and BEOL are fabricated and characterized separately, to build the component library necessary for design and integration of RF devices into circuits. Keysight's Advanced Design Systems (ADS) is used to establish a model library, design an LNA input stage, and generate lithography masks used for the circuit fabrication. Key features of the technology platform are described below.

A. Overview of FEOL and BEOL

The III-V LNW MOSEFTs are processed with the epitaxial growth of InGaAs layers on Fe-doped semi-insulating InP substrate, according to the processing scheme described in [16]. Both the nanowire channel and the contact layers are grown selectively using metal-organic vapor phase epitaxy (MOVPE) system and thin patterned hydrogen silsesquioxane (HSQ) [18]. Following the contact growth, a sacrificial InP layer is grown as well. The nanowire layer is 35 nm wide, has 8 nm thickness, with sloping facets, and it constitutes the MOSFET channel region. The contact layer is approximately 25 nm thick. A facet growth enables these layers to slope outwards from the channel region [18]. In this process the width of the HSQ dummy gate determines the MOSFET gate length, L_G. Values used in this work are L_G = 40 nm, 60 nm, and 80 nm. The micrograph of as grown layers is shown in Fig. 1a.

The process continues with patterning of 7-µm-wide mesa islands, which contain 200 wires organized into two gate-fingers. The device is completed by an atomic-layer deposition (ALD) of the Al_2O_3/HfO_2 bi-layer high-κ, followed by the gate and contact metal deposition. The excess gate metal overlap is reduced by the sacrificial InP removal. Fig. 1b shows the schematic illustration of the complete III-V LNW MSOFET, while the micrograph of the complete device is shown in Fig. 1c. The nanowire gated circumference is approximately 40 nm, corresponding to a total gate width of W_G = 8 µm.

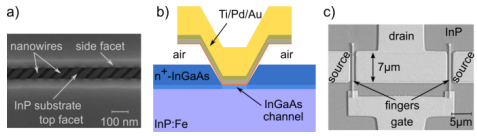

Fig. 1. a) SEM micrograph of as-grown nanowires, contact, and sacrificial layers. b) Schematic illustration of the III-V LNW MOSFET , showing the nanowire channel, the n+ InGaAs contact with sloping facets, high-κ and metal gate. c) SEM micrograph of a complete 2×7µm (2×100 wires) RF device.

The full BEOL layer stack is described in detail in [19]. It consists of four metal layers (MET1-4), two interlayer dielectric layers (ILD1-2), one resistive layer (TFR) and capacitive layer (CAP). MET1 provides connection to the FEOL layer, while ILD1 separates the RF signal propagation from the substrate. On this layer, MET2 (groundplane) layer is resting. MET3 provides RF routing and connects passive components together with MET4. The TFR layer is used for high-precision load resistors, while the CAP layer is used for metal-insulator-metal (MIM) capacitor structures. Both resistors and capacitors are placed on the ILD2 layer, allowing simple routing via RF lines, thus minimizing parasitic routing losses.

The interlayer dielectric material selected here is benzocyclobutene (BCB), a spin-on dielectric that enables planarization and metal routing. Additionally, BCB has a low dielectric constant ($\varepsilon_r \approx 2.8$), which allows for low-loss RF and mm-wave signal propagation [20]. Metal lines are evaporated Au ($\sigma_{Au} \approx 4.2 \cdot 10^{-7}$ S/m), while resistor lines are evaporated NiCr, with measured sheet resistance of 50Ω/□. Finally, for capacitor dielectric, a low-temperature plasma-enhanced chemical vapor deposition (PECVD) Si_xN_y ($\varepsilon_r \approx 8.5$) layer is used. The layer is deposited as a cover and later patterned and etched back. In two subsequent deposition and patterning steps, both *fF*-type (200nm Si_xN_y), and *pF*-type (15nm Si_xN_y) capacitors are fabricated. The RF environment is facilitated with microstrip lines routed in MET3.

To remove the effect of measurement pad parasitics on the BEOL level, the on-wafer thru-reflect-line (TRL) calibration kit is developed [21]. Using the TRL kit, the microstrip transmission lines are measured to have 0.5 dB/mm loss at 50 GHz, a value comparable to state-of-the-art MMIC BEOL [22]. The TRL kit eliminates the effect of the probing pads, as well as the 100 µm access line segment, allowing the quasi-TEM wave to settle before reaching the device, or circuit area. With such TRL design, a reference plane is established, and later used for the assessment of RF circuits.

B. III-V LNW MOSFET in BEOL Environment

To connect the III-V LNW MOSFET from the FEOL MET1 layer to the BEOL MET3 layer, a via stack is used, as depicted in Fig. 2. The presence of the BEOL via stack influences the FEOL devices in different ways. First, since the FEOL MOSFET is still uncladded with an interlayer dielectric (Fig. 1a), introducing it will increase a portion of the MOSFET parasitic capacitance by a factor of κ_{BCB} (Fig. 2a). An estimated

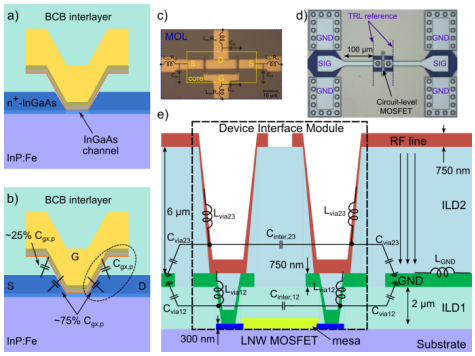

Fig. 2. Integration of III-V LNW MOSFET into the RF BEOL environment: a) device cladded with BCB interlayer, as the first BEOL step, and b) parasitic capacitance outlook in the BCB environment, with estimated 25% of the parasitic capacitance increase by a factor of κ_{BCB}. c) Optical micrograph of core LNW RF MOSFET with access lines represented by their parasitic LC branches. d) BEOL-level access structure (probe pads, access line) for measurement of III-V LNW MOSFET at circuit level, with marked TRL reference plane for on-wafer calibration. e) Schematic illustration of device interface module (DIM), showing stacked via structure, as well as vias LC contributions, including the capacitive cross-talk.

25% of the total parasitic capacitance is affected by dielectric cladding, as depicted in Fig. 2b. The largest contribution (75%) to parasitic capacitance is placed in between the gate metal and the highly-doped contact region.

The second contribution, besides the BCB cladding, are the parasitics of the routing metal segments and vias that connect the MOSFET up to the circuit level, as shown in Fig. 2c-d. The metal segments and the BEOL via stack cannot be treated as a transmission line element, due to the complex EM-field coupling. Instead, this device interface module (DIM), is assessed separately, and modelled with lumped components [23]. The schematic representation of the DIM and its major parasitic contributions is shown in Fig. 2e. The DIM contains individual via resistance (R_{via}), inductance (L_{via}), capacitance (C_{via}), and cross-talk terms (C_{inter}). Such DIM model can be used in the circuit design.

C. *Amplifier design using III-V LNW MOSFETs*

After establishing models for both FEOL – the III-V lateral NW MOSFET, and for its interface module (DIM), the models are used in conjunction to estimate device circuit-level response. The amplifier design described here focuses on device input matching for minimum noise. An elaborate device input matching yields a significant insight into the intrinsic device parameters as well. These are typically difficult to access due to limited design space at the FEOL level. Such matching network should also utilize maximum available bandwidth, and the frequency range should be selected so that the gate-length scaling properties can be observed.

The selected design frequency is 60 GHz, a center frequency in V-band (55 to 75 GHz). To first stabilize the device, an inductive source degeneration is used. This technique enables sufficient gain and an unconditionally stable MOSFET

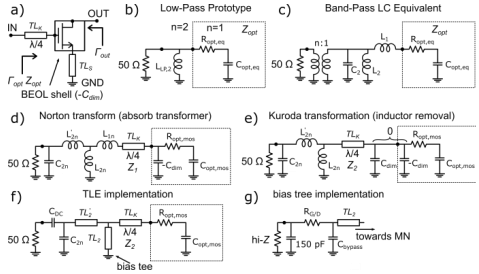

Fig. 3. Input matching network design procedure: a) MOSFET with BEOL shell, with removed shell capacitive contributions ($-C_{dim}$), source inductive degeneration, and λ/4 input low-Z0 transmission line; b) low pass network prototype for the equivalent Z_{opt}; c) band-pass ideal LC equivalent and transformer network; d) transformer absorption into the matching network (Norton transform); e) Kuroda transformation of series inductor into parallel capacitor, with changing λ/4 line characteristic impedance; the aim is to generate a C_{dim} capacitance that is absorbed into the via stack; f) replacement of ideal components with real microstrip elements and finite-Q inductors; g) the outlook of bias circuit from hi-Z DC probe to MN's shorted stub; implementation with different values of resistor and RF-short capacitor.

operation. The device response is altered by removing parasitic shell capacitances on the MOSFET gate and placing a quarter-wavelength (λ/4) low-Z_0 transmission line, as depicted in Fig. 3a. These components will be used in obtaining the input matching network (IMN).

After establishing such device description, we identify the noise optimum matching reflection coefficient, Γ_{opt} (Z_{opt}), from small signal modelling. This impedance value is used to generate a two-stage low-pass LC prototype network, according to [24]. Fig. 3b shows such prototype network, where matching $Z_{opt} = R_{opt,eq} + 1/j\omega C_{opt,eq}$. As displayed in Fig. 3c, the network is transformed into its band-pass equivalent and values are adjusted so that they correspond to the matching impedance levels in the frequency band of interest. This leaves the network with ideal LC components and an ideal transformer.

A series of network transformations are used, as depicted in Fig. 3d-f. The aim is to reduce the number of components by applying several circuit transformations. First, a Norton transform is applied on the L_1-L_2 inductors, leaving a transformer with *1:n* ratio [25]. This transformer reduces the value of the C_2 capacitor and absorbs the existing *n:1* transformer. Moreover, the remaining L_{1n} series inductor is transformed into a parallel capacitor according to Kuroda transformation rules [26]. When values of the matching level and bandwidth are adjusted in the correct manner, the resulting capacitance should be equal to the removed C_{dim}, allowing us to absorb the capacitance with DIM via stack [27]. Subsequently, the characteristic impedance of the λ/4 line increases as well, preferably to a value close to 50 Ω.

In the final stage, the remaining inductors are replaced with the transmission line sections, while the capacitors are replaced with their finite-Q versions. A DC-block capacitor is added as well. The resulting matching network include the λ/4 line, a short stub, and an additional line, followed by two capacitors. The short stub is capacitively coupled to ground and a bias voltage is supplied through a series of capacitors and limiting

resistors, as shown in Fig. 3g. A similar bias tee is used on the output of the MOSFET as well, with the addition of another DC block capacitor. The shorted stub has length less than λ/4, so it participates in the device output matching, the technique known as inductive peaking [28]. The reduced number of elements in the output network allows for increased total input stage gain, an important parameter in determining circuit properties.

III. Characterization of Circuit Components

The III-V LNW MOSFET technology platform has already been partially fabricated and characterized, with results shown elsewhere [21][29]. This includes active devices, the III-V LNW MOSFETs, but also the RF transmission lines, realized as microstrip components. Therefore, the focus of this work is on characterizing and modelling of the remaining, passive components, including the DIM and capacitors. Furthermore, an LNA input stage is fabricated and characterized as well, following the design procedure described above.

The high-frequency measurements are performed using Rohde&Schwarz ZVA67 vector network analyzer (VNA), alongside Keithley 2602B source measurement unit (SMU), for DC biasing. On-wafer probing was realized through Cascade i67 RF probe tips, landing on integrated probe pads, while a Picoprobe MCW is used to provide DC bias to the circuits. The system is calibrated using on-wafer multiline Thru-Reflect-Line (mTRL) calibration kit, described in [21]. The mTRL line lengths are set to correspond to the V-band frequency range [30]. For the noise figure measurements, an internal noise figure measurement routine of ZVA67 is used [31]. The system is noise-calibrated using an on-wafer 50 Ω impedance standard.

The total parasitic parameters of the vias were measured and evaluated from a typical two-port via structure either terminated on substrate (MET1) or on the first BCB layer (MET2). The type of termination is either capacitive (OPEN), or inductive (SHORT). The structure optical micrographs are shown in Fig. 4a-c. Measuring one of these four structures, we obtain the open admittance parameters, or short impedance parameters,

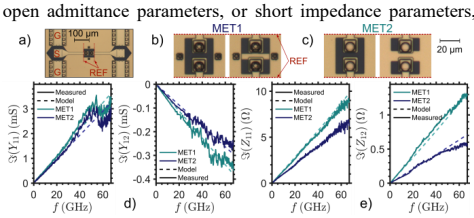

Fig. 4. Optical micrographs of a) DIM characterization structure, b-c) OPEN- and SHORT-terminated terminated via stack ending on MET1 and MET2 layer, respectively. d) OPEN-terminated via stack *y*-parameters, and e) SHORT-terminated via stack *z*-parameters, ending on MET1 on MET2 layer, to estimate parasitic capacitance, and inductance, respectively.

TABLE I
DIM Parasitics Estimated From Measurements

Parameter	C_{via} (fF)	$C_{inter,11}$ (fF)	$C_{inter,12}$ (fF)	L_{via} (pH)	L_{GND} (pH)	R_{via} (Ω)
VIA 1-2	0.7	0	0.2	2[1]	0	0.05
VIA 2-3	6	1	0.7	6	5.5	0.15

[1]Includes MOL inductance

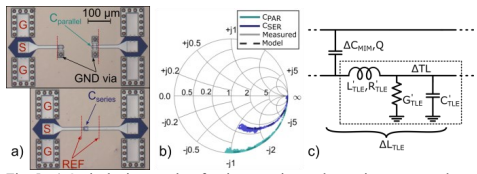

Fig. 5. a) Optical micrographs of series capacitor and capacitor-to-ground test structure. Dashed lines depict the TRL calibration reference planes. b) *s*-parameter plot of capacitor response, and c) capacitor model unit cell consisting of a portion of the MIM-capacitance and portion of transmission line represented with distributed RLGC elements.

which yield via capacitances, or inductances, respectively. The plot shows measured values compared with the model (dashed lines) values. The high frequency discrepancy between measurements and model is attributed to measurement accuracy. The detailed summary of the via LC values is shown in Table I. The measurement and modelling show that total port capacitance is approximately $C_P \approx 8$fF, while port inductance is $L_P \approx 13$ pH. The capacitance value is comparable to the device parasitic capacitance, which suggests that the DIM will alter the device behavior significantly.

To assess the capacitance structures needed for matching networks, both series capacitors, as well as capacitors-to-ground have been fabricated. The via structure parasitic model resembles the via model used in DIM evaluation, excluding the groundplane delay (L_{GND}). An optical micrograph of the structures is depicted in Fig. 5a, while Fig. 5b displays measured and modeled *s*-parameter response of the capacitor structure. The capacitance density is 0.37 fF/µm^2, and the target capacitance value of 50 fF is achieved in both cases. The model response is depicted as well. The model consists of unit cells, as shown in Fig. 5c, where each segment contains a portion of capacitance and delay/phase change due to underlying transmission line environment. Aside from the low capacitance density layers, high capacitance density layers have been evaluated and the resulting capacitance density is 4.9 fF/µm^2, which allowed for fabrication of 150 pF capacitors for the stabilization of the DC bias lines.

IV. III-V LNW MOSFET LNA Input Stage

To verify the established models that are derived from measurements of the individual MOSFET, microstrip lines, interface modules, and the passive components, a single-stage LNA circuit is built. The aim is to verify that the established models can accurately predict the performance of the resulting LNA. Furthermore, the investigation into the intrinsic device performance is carried out, as a part of the effort to understand the circuit-level performance of the III-V LNW MSOFETs. The device gain and noise models used are derived from available device-level noise measurements, shown in [32].

The circuit optical micrograph is shown in Fig. 6a, while the corresponding schematic is depicted in Fig. 6b. The central part of the circuit is the input matching network, whose design is described in Section II.C. Also, great attention has been given to biasing, which improves circuit low frequency stability. As mentioned earlier, the output matching consists only of a DC

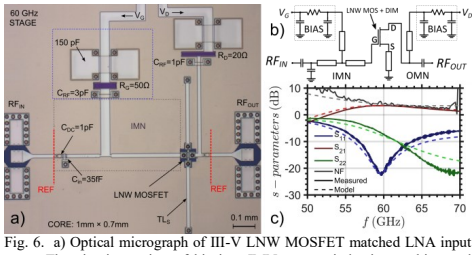

Fig. 6. a) Optical micrograph of III-V LNW MOSFET matched LNA input stage. The circuit consists of biasing, IMN, output inductive peaking and stabilization stubs. The core area is 0.7 mm^2. b) Circuit schematic of LNA input stage. c) Measured s-parameters and noise figure for 80 nm III-V LNW MOSFET, measure ad V_G = 0.8 V, V_D = 1V, with I_D = 6.3 mA.

block capacitor and *l*<λ/4 inductive peaking stub, to boost single-stage LNA gain. The LNA stage core area is 1mm × 0.7 mm, mainly due to the size of the IMN λ/4 line. The *s*-parameter response is shown in Fig. 6c. The input stage is biased at V_G = 0.8 V and V_D = 1 V, giving the total current of I_D = 6.3 mA for the gate length of L_G = 80 nm. This LNA input stage exhibits 3.5 dB gain at 59 GHz, while both input and output reflection are below -10 dB, demonstrating a well-matched circuit.

To enable the accurate noise figure (*NF*) measurements, a VNA direct-receiver access is used [31]. In the VNA receiver path, a V-band LNA, from Low Noise Factory, is inserted. This LNA improves the noise measurement accuracy by suppressing the receiver noise figure. The discrepancies seen at frequencies lower than 55 GHz are mainly due to insufficient gain of the single-stage LNA, while the discrepancies above 67 GHz correspond to the external LNA bandwidth limit. The measured minimum value of the noise figure (*NF*) is between 2.5 dB and 3 dB, while an in-band value in between 2.5 and 6 dB. This measurement is the first observed circuit-level noise behavior of lateral nanowire MOSFETs and represents the confirmation of the predicted device RF noise properties. The technology shows potential for implementation of multi-stage LNAs in future high-frequency low power RF and mm-wave circuits and systems.

To verify the circuit design approach, a transistor gate-length scaling study was included among the amplifiers. Three amplifier input stages were fabricated, for gate lengths of 40, 60, and 80 nm. Before the stages *s*-parameters were measured, the individual transistors were characterized by DC sweeps. The results are shown in Fig. 7a-c, while the equivalent circuit schematic is depicted in Fig. 7e. The supply voltage was swept from 0 to 1V and the output curves were obtained by subtracting the voltage drop on R_D = 10 Ω – an external resistor used in the LNA biasing. The corrected values of MOSFET on-resistance, R_{ON}, are shown as well, reaching values down to 265 Ω·μm for a 40 nm MOSFET.

Fig. 7d shows the measured transconductance value of g_m = 1.2-1.3 mS/μm, as evaluated form the output curves, at V_{DD} = 1 V. Moreover, in Fig. 7f, the R_{ON} versus L_G is plotted, revealing scaling of lateral nanowire channel resistance. Source and drain contacts are estimated to contribute to R_{ON} with the contact resistance of R_C = 98 Ω·μm each. The value is

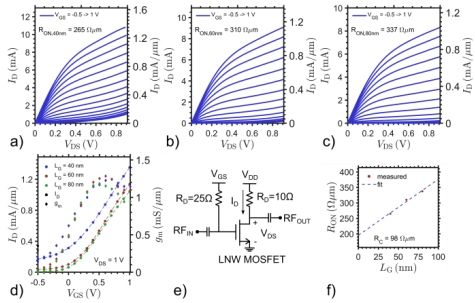

Fig. 7. a)-c) Output plot of amplifier stage coupled devices. Device output was measured until V_{DD} = 1V and V_{DS} was recalculated, considering R_D = 10 Ω. d) Extrapolated g_m from and I_D from output curves. e) Schematic DC circuit for device analysis. e) R_{ON} versus L_G showcasing contact resistance of R_C = 98 Ω·μm per contact.

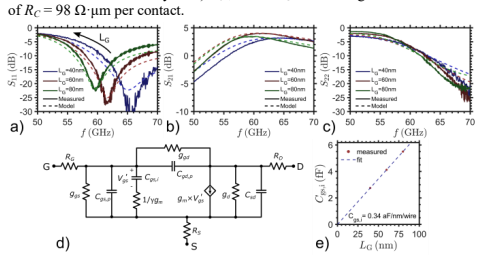

Fig. 8. LNA input stage *s*-parameter plots: a) s_{11}, b) s_{21}, and c) s_{22}, versus frequency of interest, for L_G = 40 , 60, and 80 nm gate length. Solid lines represent measured data, while dashed lines are circuit models. d) III-V LNW MOSFET small signal model used to fit device data. e) Intrinsic capacitance fit showing slope of 0.34 aF per nm gate length, per nanowire.

comparable to previously reported results for LNW MOSFETs [11]. The device scalability is evident from measurement on the BEOL level, with well behaving characteristics. The 40 nm MOSFET exhibits larger off-state current, explained primarily by a parasitic hole conduction in the channel, as well as somewhat larger nanowire width (35 nm) [33].

The scalability study continues with the evaluation of the device RF response. The LNA stage *s*-parameter plots for three different gate lengths are shown in Fig. 8. The input reflection (s_{11}, Fig. 8a) matching peak has a clear shifts in frequency, which we can attribute to the changing intrinsic device capacitance. The frequency shifts are also evident in the gain peak (s_{21}, Fig. 8b), while the peak gain value reflects on changing device transconductance. The gain value peaks for 60 nm gate length, having value of 4 dB at 60 GHz, while 40 nm gate length device delivers 3.2 dB at 64 GHz, a smaller value due to poorer device gain. The output (s_{22}, Fig. 8c) remains nearly constant, since C_{SD} and C_{GD} typically are only represented with their parasitic values and are nearly constant.

Table II lists the main MOSFET small-signal model (SSM) parameters for different gate lengths, that is used to model the LNAs response, shown in Fig. 8d. The gate length scaling allowed for confirmation and extrapolation of crucial device data. The parasitic overlap capacitances are $C_{gx,p}$ = 6.5 ± 0.5 fF (x={s, d}), where 0.5 fF is considered the accuracy limit of the modelling and fitting approach. The source-drain capacitance is

TABLE II
MOSFET* SSM PARAMETERS FROM LNA MEASUREMENTS

Parameter	L_G = 40 nm	L_G = 60 nm	L_G = 80 nm
R_G (Ω)	9	5	1
$R_{S/D}$ (Ω)	10	10	10
$C_{gx,p}$ (fF)	6	6.5	7
C_{SD} (fF)	10	8	6
$C_{gs,i}$ (fF)	2.75	4.125	5.5
$G_{m,RF}$ (mS)	22	26	20
$g_{m,DC}$ (mS/μm)	1.24	1.28	1.18
$g_{m,RF}$ (mS/μm)	2.75	3.25	2.5
G_m/G_d	4	4.5	5
$g_{gs/gd}$ (μS)	1	1	1
NFmin @ 60 GHz (dB)	1.54	1.36	1.47
MSG @ 60 GHz (dB)	8.6	8.7	7.7
f_T / f_{max} (GHz)	240 / 200	215 / 255	152 / 259

*All devices are 2×7μm wide, with W_G = 8μm (200 nanowires)

scaling as the gate length is reduced, due to a decreasing distance between the contacts. We can see the effect of this scaling in alteration of the s_{22} curve (Fig. 8c). The R_G value, alongside an intrinsic channel resistance ($1/\gamma g_m$), forms the total gate resistance, and is a part of the gain, or s_{21}, response. The contact resistance value $R_{S/D}$ is L_G-independent.

The device scaling influences the transconductance values as well. Using SSM, we obtain the intrinsic $g_{m,RF}$, then derive the extrinsic values, and compare them to the DC values shown in Fig. 7d. The LNA modelling results for intrinsic RF transconductance are given in Table II, from which the extrinsic g_m is obtained according to $g_m = g_{m,i}/(1 + g_{m,i} \cdot R_S + g_d \cdot (R_S + R_D))$. The estimated extrinsic g_m from the small signal model is 2.1, 2.38, and 1.95 mS/μm, for 40,60, and 80 nm, respectively, which are substantial improvement in comparison with the obtained DC values below 1.3 mS/μm. The intrinsic values achieve even higher values, up to 3.25 mS/μm, demonstrating the benefit of using III-V materials in the channel of the scaled MOSFET. Additionally, the device NF_{min} values down to 1.36 dB, *MSG* values up to 8.6 dB at 60 GHz, and estimated cut-off frequencies up to 240/260 GHz, demonstrate the LNW potential in the mm-wave circuit design.

The frequency shift in the matching peaks in s_{11} are governed by changing of the intrinsic device capacitance, denoted as $C_{gs,i}$ in Table II. This capacitance estimates the total inversion charge capacitance (or total gate capacitance) during the device operation. As shown in Fig. 8e, the obtained intrinsic capacitance is $C_{gs,i}$ = 0.34 aF per nm gate-length per nanowire. To accurately model the capacitance contributions, we investigate the quasi-ballistic transport theory in nanoscale FETs. In general, the gate capacitance is a series connection of the oxide capacitance and a channel quantum capacitance, or ${C_{gs,i}}^{-1} = {C_{ox}}^{-1} + {C_q}^{-1} + {C_C}^{-1}$, where C_{ox} is oxide capacitance, C_q is semiconductor (quantum) 2D capacitance, and C_c is charge centroid capacitance [34],[35]. The calculated capacitances are:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r W_{nw}}{t_{ox}} + 1.116\varepsilon_0\varepsilon_r,\ C_q = \frac{q^2 m^*}{2\pi\hbar^2},\ \text{and}\ C_C = \frac{\varepsilon_0 \varepsilon_S}{0.28 t_W}, \quad (3)$$

where ε_r and ε_s are relative dielectric constants of the gate oxide and semiconductor, respectively, t_{ox} and t_W are oxide and semiconductor thickness, respectively, W_{nw} is nanowire circumference (tri-gate geometry), q is elementary charge, and $\hbar$ is reduced Planck constant. The material effective mass m^*, value is corrected based on empirical calculations provided in [35]. Calculated values are 1.4, 0.74, and 2.11 aF/nm(L_G)/nanowire for C_{ox}, C_q, and C_C, respectively. The total intrinsic gate capacitance is $C_{gs,i}$ = 0.39 aF/nm(L_G)/nanowire, which is in close agreement with values obtained by measurements. The described experiment shows the ability to obtain essential device data from circuit evaluation and can be used as a powerful tool in technology platform building.

The proposed lateral nanowire technology platform allows for circuit-level investigation into individual BEOL components, as well as MOSFETs, using an on-wafer mTRL calibration kit. It also enables an efficient circuit design and characterization, such as small signal gain and noise figure. The integration of different processes is successfully implemented, harmonizing the behavior of the FEOL and BEOL components. The obtained intrinsic capacitance fits the theoretical value and serves as a proof-of-concept for the technology platform capabilities, thus simplifying future design and fabrication efforts. It is an important cornerstone in the development of III-V lateral nanowire MOSFETs towards a fully integrated technology platform for implementation into complex RF and mm-wave circuits and systems.

V. CONCLUSION

We present a III-V lateral nanowire MOSFET technology platform, consisting of III-V LNW MOSFET RF devices and a conventional BEOL adapted for nanowire technology. The device process is established based on previous research, while new standalone passive components are fabricated and characterized. Data obtained from the interface module and passive components suggest a high-quality realization with low parasitic values. The components are used to design and implement an LNA input-stage, where part of the device interface module parasitics are absorbed into the matching network. The LNA single stage is designed using optimum matching network design approach that maximizes the available bandwidth, with the addition of a Norton transform, to absorb the network's transformer, and Kuroda transform, to eliminate excess network inductance.

The assessment of the device behavior reveals III-V LNW MOSFET DC transconductance of 1.2-1.3 mS/μm for varying gate lengths. The obtained contact resistance is 98 Ω·μm, suggesting good device behavior. The LNA input stage exhibits up to 4 dB gain and down to 2.5 dB noise figure in V-band. Moreover, the evaluation of the same LNA design on different MOSFET gate lengths allow for establishing an accurate device model. The RF extrinsic transconductance is estimated up to 2.6 mS/μm, doubling the DC value, while the intrinsic transconductance values reach up to 3.25 mS/μm. The input reflection matching a frequency shift sets constant parasitic gate capacitances to $C_{gx,p}$ = 6.5 ± 0.5 fF across all gate lengths, while the shift is carried out by scaling the intrinsic gate capacitances, resulting in $C_{gs,i}$ = 0.34 aF/nm(L_G)/nanowire. By carefully considering the nanowire quantum capacitance contributions, we obtain the theoretical value for $C_{gs,i}$ of 0.39 aF/nm(L_G)/nanowire, which is in close agreement with the value obtained by measurements. The proposed proof-of-concept design and measurements reveal potential for more

complex III-V LNW MOSFET circuits. The achieved accuracy between the measured and modelled data, and the theoretical predictions demonstrate a complete technology platform, suitable for high-performance RF and mm-wave circuits and systems design.

ACKNOWLEDGMENT

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Paper IV

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Design of III-V Vertical Nanowire MOSFETs for Near-Unilateral Millimeter-Wave Operation

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***Abstract* — Vertical nanowire MOSFETs exhibit asymmetric gate capacitances, allowing for their independent engineering to improve device high frequency performance. Minimizing gate-drain parasitic capacitance with the use of a vertical sidewall spacer enables universal feedback neutralization and a unilateral circuit design. For vertical spacer thickness above 20 nm, the gate-drain capacitance variability is reduced. Device technology is verified by simulation of 60 GHz three-stage low-noise amplifier. The amplifier exhibits 10 dB gain and 6.9 dB noise figure. The noise figure can be further reduced to 5.9 dB by combining several feedback techniques. The use of capacitance minimization reduces circuit sensitivity to device variation, demonstrating the potential of this technology in implementation of mm-wave communication and sensing systems.**

***Keywords* — Nanowires, MOSFET, capacitance, millimeter-wave integrated circuits, feedback, low-noise amplifiers.**

I. Introduction

III-V vertical nanowire (NW) transistor architecture is one candidate for future computational devices [1]. Studies of an optimum III-V channel MOSFET device geometry reveal superior device performance at scaled gate lengths [2], [3]. Furthermore, radio frequency (RF) characterization shows that the asymmetric structure of III-V vertical NW MOSFETs, and in particular the spacer layers, introduces asymmetric gate capacitances [4]. This allows a high degree of freedom to engineer the device RF operation, as compared to lateral devices. Therefore, these transistors allow for application of a unique RF circuit design that leverages device asymmetry.

The low effective mass in III-V materials is beneficial not only for charge transport in MOSFETs, but the associated low density of states provides a low fixed charge density during device operation, and in turn, a resulting low intrinsic device capacitance. In general, III-V MOSFETs are limited by the extrinsic, parasitic capacitances, which mainly depend on device geometry and the processing technology. If the parasitic capacitances can be designed, independent of the MOSFET gate length, the subsequent feedback neutralization circuit will remain unchanged. This provides a unilateral device module for use in RF circuit design [5].

In case of high cut-off frequency devices, parasitic gate-drain capacitance is a dominant factor. For III-V vertical NW MOSFETs, a trade-off between gate resistance and the gate-drain capacitance sets the maximum oscillation frequency. A thicker gate metal provides low gate resistance, but also a large gate-drain extrinsic capacitance, due to gate-drain metal overlap. Addressing this problem would allow vertical NW MOSFETs to extend the operation into sub millimeter wave frequencies as well, following lateral nanowire MOSFETs, which have already demonstrated performance exceeding that of Si CMOS and SOI technologies [6].

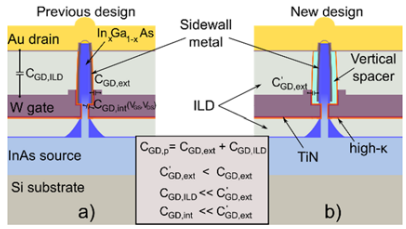

Fig. 1. a) Schematic illustration of a vertical nanowire MOSFET with different gate-drain capacitances included. b) Vertical NW MOSFET with a vertical spacer for minimization of the extrinsic gate-drain capacitance. The inset shows relations between different CGD contributions.

In this paper, a study of the gate-drain parasitic capacitance minimization is performed. Furthermore, feedback circuits for such device are explored, giving insight into possible circuit techniques suitable for vertical NW MOSFET operation in the 60 GHz ISM band [7]. A special focus is given to device unilateralization, utilizing extrinsic gate-drain capacitance, which is shown to improve device overall performance [8]. Finally, the device technology is accessed through design of multi-stage low-noise amplifiers (LNAs).

II. III-V Vertical Nanowire MOSFETs

The studied III-V vertical NW MOSFET, illustrated in Fig. 1a, is based on processing and performance described elsewhere [3]. This device has a large overlap between the gate and drain contacts due to sidewall contact formation on the device drain side and a thick gate metal, which will result in large extrinsic gate-drain capacitance, $C_{GD,ext}$. A total parasitic gate-drain capacitance, $C_{GD,p}$, also contains a plate capacitance contribution from contact routing, $C_{GD,ILD}$, but that capacitance is much smaller than the extrinsic gate-drain capacitance, as noted in the inset in Fig 1.

A possible way for reduction in $C_{GD,p}$ is illustrated in Fig 1b. Here, a spacer is introduced on the sidewall of the nanowire, effectively separating the gate metal from the drain sidewall metal. With this adaptation, the largest contribution to the gate-drain capacitance, $C_{GD,ext}$, can be reduced to a low value. Such

a process may include a separation of the contacts from the bottom side as well. This, however, forms an ungated region, which increases the drain access resistance. The resistance change has not been included in this study, and it is assumed that a very small separation will not significantly affect the device performance.

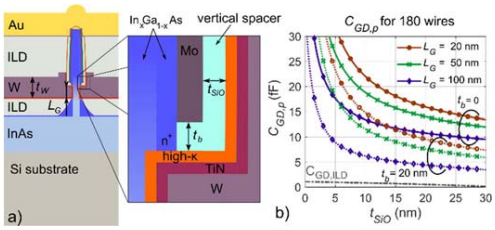

Fig. 2. a) Schematic illustration of the vertical NW MOSFET with vertical spacer, with specific spacer dimensions noted; b) $C_{GD,p}$ values for different t_{SiO} and different gate lengths, for a total of 180 nanowires. The values are plotted for bottom separation $t_b = 0$ (full line) and $t_b = 20$ nm (dotted line).

A detailed illustration of the gate-drain overlap region is shown in Fig 2a. In this study, we assume total gate metal thickness of t_W = 120 nm, while a vertical spacer dielectric constant is assumed to be that of a common material, such as SiO_2 ($\varepsilon_r = 3.9$). Two distinct dimensions are defined in this case: the separation between the bottom side of drain Mo contact, t_b, and the sidewall separation between Mo drain contact and W/TiN gate metal, t_{SiO}. An accurate small-signal RF device model is presented elsewhere [4]. This device contains 180 nanowires organized in 3 gate fingers, i.e. 60 wires per finger, while the gate length is L_G = 120 nm. The device total extrinsic capacitance is modelled to a value of $C_{GD,p} \approx 6$ fF.

The simulated values for the parasitic gate-drain capacitance, $C_{GD,p}$ are shown in Fig. 2b. Here, the contribution of $C_{GD,ILD}$ is low, showing that total capacitance lies almost exclusively within $C_{GD,ext}$. Three gate lengths are considered: 100 nm, 50 nm, and 20 nm. If a vertical spacer is not included, the metal separation is limited to a thin high-κ layer, making the total capacitance larger than 50 fF. Introducing a vertical spacer with $t_{SiO} > 20$ nm, will reduce $C_{GD,p}$ to below 15 fF. This, however, is still larger than the desired value. To achieve values around 6 fF even at scaled gate lengths, an additional, lateral spacer is necessary. If $t_b = 20$ nm, the total gate capacitance is nearly halved for $t_{SiO} > 20$ nm. Additionally, the dependence of $C_{GD,p}$ on the variation in sidewall spacer thickness is very small (less than 1aF/nm at $t_{SiO} > 20$ nm), thus reducing sensitivity in the circuit design to device variations.

III. Vertical NW MOSFET Feedback Design

A. Vertical NW MOSFET RF response

To integrate III-V vertical NW MOSFETs, a custom designed RF back-end-of-line (BEOL) is used [9]. The BEOL contains metal layers for integration of passive components, and a microstrip transmission line environment for RF signal routing [11]. The active device small-signal RF model includes a transconductance-frequency dispersion, which influences the device unilateral gain and is important in the feedback design [9]. The passive and active component library used is built and simulated in Keysight ADS.

To achieve a suitable output impedance in the frequency range of interest, the device size is adapted to 360 wires organized into 6 fingers, giving a total device width of 6 × 5.6 µm, and a total parasitic gate-drain capacitance of $C_{GD,p} \approx 12$ fF. The MOSFET is biased in common-source (CS) configuration, with V_{GS} = 0.4V, and V_{DS} = 0.5V, giving total drain current I_D = 10.8 mA. The device has a maximum stable gain MSG = 7.4 dB at 60 GHz, while the stability factor is lower than 1, so the device is potentially unstable. Minimum noise figure is NF_{MIN} = 2.9 dB, and isolation (S_{12}) is -14dB.

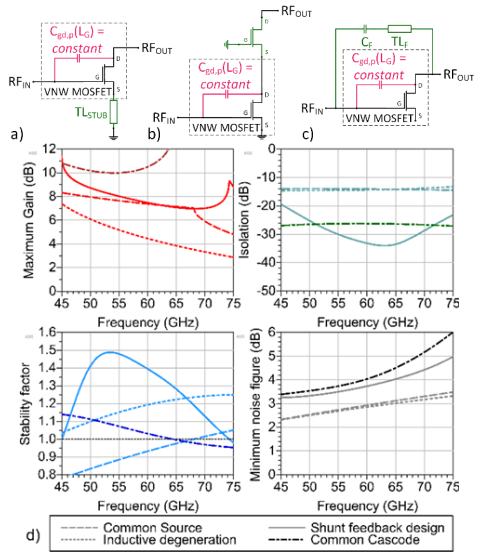

Fig. 3. a) Circuit diagram of vertical NW MOSFET with series feedback (inductive source degeneration), b) cascode, and c) shunt (LC) feedback. d) Comparison of maximum gain, isolation (S_{12}), stability factor (µ), and minimum noise figure for different feedback implementations.

Unilateralization of the device is investigated with several different feedback designs. Fig. 3a shows a series inductive (series L) feedback, with inductive degeneration in the source. Cascode (CC) design is shown in Fig 3b, where the feedback is a device in common-gate (CG) configuration. A transmission line is routed in between devices, to match the output impedance of the CS stage to the noise optimum impedance (Z_{OPT}) of the CG stage. The schematic of inductive (LC) feedback structure is shown in Fig 3c, and it consists of an inductor (transmission line) and a tuning capacitor, C_F, that also prevents DC current in the feedback path. Devices with various feedback frequency responses are shown in Fig. 3d.

The series L feedback achieves unconditional stability by reducing the gain of the device to 4.4 dB at 60 GHz. Here, only device gain is affected, as isolation in this case does not improve,

as compared to the standard, CS configuration, showing a continuing strong influence of $C_{GD,p}$. The CC configuration, on the other hand, neutralizes $C_{GD,p}$ with added CG MOSFET stage, increasing available gain to 10.5 dB at 60 GHz. Additionally, isolation is improved to less than -25 dB, showing efficient feedback neutralization. This implementation, however, doubles DC power consumption, and increases device NF_{MIN} from 2.8 dB to 4dB at 60 GHz.

B. Shunt LC Unilateralization

The shunt LC feedback presents an optimum solution that maximizing RF performance, while preserving gain and DC power consumption, and improving stability and isolation. Fig. 3d shows shunt LC plots in solid lines, where the stability factor is larger than 1 in the frequency band of interest, and available device gain larger than CS *MSG* values. This is the condition to regard the NW MOSFET as unilateralized. Isolation for this configuration has the lowest value at the design frequency, reaching below -30 dB. This feedback configuration avoids the trade-off between available gain and stability but relies on a clearly defined C_{GD} value. Additionally, NF_{MIN} increases from 2.8 dB to 3.7 dB.

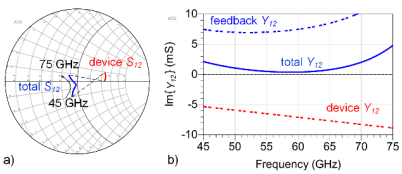

Fig. 4. a) Zoomed-in Smith chart showing isolation (S_{12}) of a standalone device, and device with feedback. b) Imaginary part of feedback admittance y_{12} for a standalone device, the feedback structure and the total y_{12}.

A further analysis reveals that the shunt LC feedback network itself has a resonant behavior outside of circuit design frequency band. Simplifying the internal reactive feedback of the vertical NW MOSFET with an equivalent gate-drain capacitance, $C_{GD,p}$, upon adding shunt LC feedback, the imaginary part of the total admittance, Y_{12}, will be:

$$Im\{Y_{12}\} = -Im\{Y_{GD} + Y_F\} \approx -\omega\left(C_{GD,p} - \frac{C_F}{\omega^2 L_F C_F - 1}\right) \quad (1)$$

where C_F is a feedback network capacitance, L_F is a feedback network equivalent inductance, and ω is the angular frequency. The shunt LC feedback circuit acts as an impedance inverter, neutralizing the total reactance in the device feedback path. $Im\{Y_F\}$ has a minimum that is mismatched to the design frequency, and two resonant peaks that are outside of the band of interest. The minimum is determined by feedback network loss, while distance between resonant peaks is directly controlled by C_F. Altogether, the total feedback susceptance is close to zero at the design frequency.

The normalized value of the device isolation before and after feedback implementation, is shown in Fig 4a. Its shape suggests impedance-matched circuit behavior, over a specified bandwidth. Plotting the magnitude of Y_{12} for the NW MOSFET, the shunt LC feedback, as well as for MOSFET with the shunt LC feedback network, as shown in Fig 4b, it is noted that $Im\{Y_{12}\}$ is indeed minimized, confirming capacitance neutralization at the design frequency.

IV. Low-Noise Amplifier Demonstrator

In order to utilize the available bandwidth given by the NW MOSFET and the feedback structure, an optimum matching networks have been designed, according to [12]. Matching networks are derived as optimum Chebyshev band-pass filters, where the bandwidth depends on device input/output quality factor, and gain response is limited to the specified bandwidth only. Ideal LC elements of the network are replaced with realistic transmission lines, stubs, and finite-Q metal-insulator-metal (MIM) capacitors [13]. The schematic implementation of the LNA is shown in Fig. 5a. A total of three amplifier stages were considered, with the focus on circuit area, power consumption, as well as resulting gain and noise figure. Simulation results are shown in Fig 5b-d, as well as Fig. 6, and they are summarized in Table I.

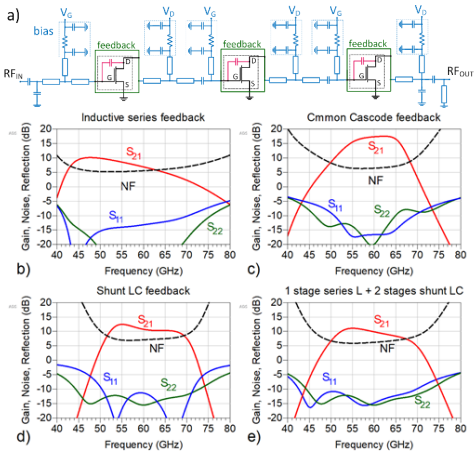

Fig. 5. a) Schematic illustration of three-stage LNA, including input, two interstage and an output matching networks, together with biasing circuit for low-frequency stability. b) S-parameters and noise figure plot for three-stage LNA with series L implementation, c) common cascode implementation, d) shunt LC implementation, and e) shunt LC implementation where the first stage is implemented with a series L feedback.

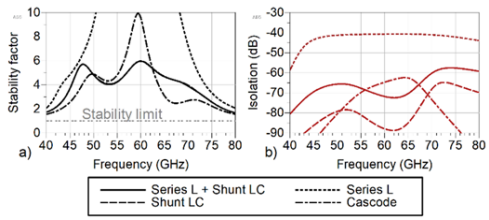

Fig. 6. a) Stability factor for different LNA implementations. b) Isolation (S_{12}) for different LNA implementations.

Table 1. Three-stage 60 GHz LNA performance summary

Design	LNA Performance Overview				
	G [dB]	NF_{MIN} [dB]	BW_{3dB} [GHz]	P_{DC} [mW]	S_{12} [dB]
Series L (SL)	6.9	**5.2**	16	16.2	-40.7
Cascode (CC)	**17.3**	6.3	12	32.4	-64.7
Shunt LC (SLC)	10.7	6.9	**16**	16.2	**-87.9**
1 SL + 2 SLC	9.8	5.9	15	**16.2**	-71.8

The simulation results for each implementation are shown in Fig 5b-d. Fig. 5e shows a special case where the first stage was implemented with a series L feedback, while the remaining stages are implemented using shunt LC feedback. In Fig 5b, the inherent low available gain and steep gain curve of the series L feedback implementation give rise to poor gain performance of the LNA, demonstrating a value below 7 dB at 60 GHz, while the 10 dB gain peak is located at 44 GHz. The cascode design, shown in Fig 5c, exhibits higher gain, reaching 17.3 dB at 60 GHz. A large portion of device intrinsic gain is used to compensate matching networks' insertion loss, due to BEOL implementation restrictions, which makes this design suboptimal, especially considering the power consumption, which doubles for cascode-connected MOSFETs.

The LNA with the series L implementation exhibits the lowest noise figure of 5.2 dB, while cascode implementation noise figure is 6.3 dB. Shunt LC design shows the highest noise figure due to feedback transmission line loss and the insertion loss of the input matching network. Replacing the first stage of the shunt LC LNA with a series L stage lowers the noise figure to 5.9 dB, while keeping the circuit gain to 10 dB, over a 15 GHz bandwidth, as shown in Fig 5e.

Finally, LNA stability and feedback analysis are shown in Fig 6. In Fig 6a, the stability factor is very large for series L implementation mainly due to high output matching level (S_{22}) achieved in the circuit. The shunt LC implementation exhibits reasonable stability value over the entire frequency band of interest, making it a balanced design. The difference in isolation for different implementations, as shown in Fig 6b, shows the largest discrepancy. Although the shunt LC implementation exhibits less than -80 dB in isolation, it will be difficult to access this isolation level with sufficient accuracy in most measurement systems, mainly due to instrument calibration inaccuracy. The simulation, however, shows a clear advantage of the feedback neutralization.

The designs presented in this paper show a possible use-case for vertical NW MOSFETs in a circuit environment. Generally, the design should be robust and less prone to variability on the device level. Setting a proper value of $C_{GD,p}$ has a great impact not only on device performance, but also on subsequent circuit performance. Therefore, a sensitivity analysis of the overall device variability should be of interest from the circuit design aspect. In this work, a set of fixed model parameters is used, but it would be advantageous to investigate for example, the total power consumption increases due to increased drain access resistance, since $t_b > 0$. The tradeoff between $C_{GD,p}$ and drain access resistance gives insight into technology performance. This topic, however, deserves a separate investigation.

V. Conclusion

Careful engineering of the vertical NW MOSFET gate-drain parasitic capacitance shows potential in achieving a constant value when device gate length is scaled. Selecting a specific value allows for a unique feedback circuit implementation that will simplify circuit design selection procedure. Several feedback designs have been implemented, where shunt LC feedback network showed the most stable design, reducing the feedback admittance in the frequency band of interest. Devices with implemented feedback are used in a 3-stage LNA design using optimum matching networks. The LNA simulation results show that a design with first stage series L feedback device, in combination with shunt LC second and third stage has a good balance of gain, bandwidth, power consumption, while keeping isolation levels well below -70 dB. Therefore, the feedback implementation in combination with optimum circuit design can prove beneficial in future mm-wave circuit design.

Acknowledgment

This work is supported in part by Swedish Foundation for Strategic Research (SSF), Swedish Research Council (VR), as well as European Union H2020 programs INSIGHT (Grant 688784), and SEQUENCE (Grant 871764). The authors thank Olli-Pekka Kilpi and Markus Hellebrand for fabricating and modelling of vertical NW MOSFET, respectively.

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Paper V

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Millimeter-Wave Vertical III-V Nanowire MOSFET Device-To-Circuit Co-Design

Stefan Andrić, Lars Ohlsson Fhager, Lars-Erik Wernersson

***Abstract*—Vertical III-V nanowire MOSFETs show potential towards the ultimate transistor scaling. A high transconductance and current density are achieved based on the gate-all-around architecture. This work presents a high-frequency design of such devices, achieving more than 600 GHz cut-off frequencies (f_T, f_{max}), at 20 nm gate length. Furthermore, capacitance design and scaling trends, supported by COMSOL Multiphysics simulations derive state-of-the-art parasitics magnitudes for vertical devices in general, reaching gate-drain capacitance values of 17 aF/wire, corresponding to 0.2 fF/µm. A unique co-designed feedback resonant circuit makes the device unilateral, exhibiting up to 15 dB gain in D-band at 0.5 V supply, and with a current density of 0.5 mA/µm. Finally, a 2-stage low noise amplifier is designed using an optimum matching concept to utilize the full available bandwidth. The resulting circuit performance is independent of transistor gate length, since any decrease in device intrinsic capacitance is assisted by an increase in device overlap capacitances in a setting unique to a current implementation of vertical nanowire MOSFETs. With this approach, amplifiers are designed with more than 20 dB gain and minimum noise figure of 2.5 dB in a simulation environment at 140 GHz. The proposed technology and design platform show a great potential in future low-power communication systems.**

***Index Terms*— III-V MOSFETs, Vertical MOSFETs, Circuits, Feedback, Unilateral, LNA, Noise, RF, mm-wave, Communication**

I. Introduction

The vertical III-V gate-all-around (GAA) nanowire (NW) device architecture is one candidate for future computational devices, supporting further device scaling [1]. GAA exhibit superior electrostatic control over the channel potential through wrapping of the gate around the semiconductor channel. Such III-V devices have been studied in detail and offer superior transport properties [2-5]. The ballistic transport in III-V MOSFETs provides high transconductance, achievable at relaxed gate lengths and reduced supply voltages, enabling attractive high-frequency operation [6,7]. Combining narrow band-gap III-V materials with GAA architecture enables further scaling of device performance while minimizing short-channel effects. Additionally, the small nanowire dimensions facilitate the integration of III-V materials on Si substrates and allow for novel heterostructure device architectures [8,9]. For instance, they offer high breakdown voltage in combination with high transconductance [10].

The current work on high-frequency vertical III-V NW MOSFET devices show encouraging results with potential for further development [11,12]. Cut-off frequencies up to 150 GHz have been reported, with a new option for asymmetry between parasitic gate-source and gate-drain capacitances, due to a low access resistance provided by advanced heterostructures. As a result, a possibility to independently tune these parasitic capacitances would allow for the engineering of the device radio-frequency, or millimeter-wave (RF or mm-wave) operation with an additional degree of freedom [11]. These features open a path with potential to use vertical III-V NW MOSFETs in large-scale integration, low-power communication systems [13].

From a circuit design perspective, devices such as vertical III-V NW MOSFETs exhibit large intrinsic gain, allowing for a single-ended design, resembling that of a III-V mm-wave integrated circuit (MMIC) design [14]. However, due to efficient scalability and the use of CMOS-like processing of vertical III-V NW MSOFETs, a standard RF CMOS design could be achieved as well. Such design utilizes differential cross-coupled stages with transformer-based matching networks, realized in a multilayer back-end-of-line (BEOL) [15]. Both concepts offer attractive solutions in terms of design strategies, while being fine-tuned for either III-V high electron mobility transistors (HEMTs) or Si RF CMOS, respectively.

Novel RF devices could provide benefits for operation in communication systems with large data rate, with an ever-increasing operation frequency. One frequency range attractive for short-range communication is D-band, spanning a range from 110 GHz to 170 GHz, a bandwidth where large data-rate can occur at low latency. At these frequencies it is challenging to simultaneously achieve a combination of high circuit gain with low noise figure, high output power, linearity and bandwidth, while still providing high integration density on the device level. High-performance amplifiers have been designed, showing that it is challenging to achieve desired circuit performance [14-20]. While Si RF CMOS offers high integration density and process uniformity, the challenge is to achieve a sufficient gain and noise performance as such high frequencies. III-V HEMTs provide the performance but integration is challenging. Therefore, other solutions are needed

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to achieve both the performance and integration requirements, where a different technology platform would be necessary.

In this work, we present a concept of mm-wave design using vertical III-V NW MOSFETs, primarily by engineering the gate-drain capacitance and enabling parasitics-independent gate-length scaling, for D-band circuit operation. This concept is verified by comparing two different device design strategies. A unique feedback structure that resonates with gate-drain capacitance of vertical III-V NW MOSFET is utilized for the circuit design, providing device unilateralization [21]. For the transistor implementation, a large signal model is developed to capture transport properties and parasitics scaling. The implementation of D-band low-noise amplifiers (LNAs) is used as an assessment of possible technology limits. Investigation rests upon modelled parasitic external capacitances, which are identified as key metric in vertical NW MOSFET RF design.

II. Vertical III-V Nanowire MOSFET

The complete schematic structure of the vertical III-V NW MOSFET is shown in Fig 1a. In general, the InAs/InGaAs nanowire heterostructure is grown using metal organic vapor phase epitaxy (MOVPE). The nanowire design enables modulation doped semiconductor access regions. Additionally, an axial heterostructure with increased bandgap towards the drain contact is introduced [10]. This InGaAs segment suppresses the off-state leakage current, mitigates short-channel effects and increases device breakdown voltage. On the other hand, the narrower bandgap InAs source provides large injection velocity and an increased on-state current. Device fabrication and characterization is described in detail elsewhere [22,23].

The drain contact is essential in obtaining low contact resistance for vertical NW MOSFET, and is realized through metallization of the nanowire sidewall, as shown in Fig 1. Since the external parasitic gate-drain capacitance needs to be minimized in a mm-wave MOSFET design, a 20 nm separation between gate and drain contact is introduced. The self-aligned contact and access segment formation are enabled by utilizing vertical spacers, as well as low-κ planarization layers [24]. As the spacer dielectric constant limits vertical NW MOSFET mm-wave performance, it would be beneficial to remove these layers, as shown in Fig 1a. Such concept has been utilized before, by patterning gate and drain metal into finger structures, and enables very low capacitance values [11].

To mitigate the large gate resistance which would arise because of gate metal thickness scaling, this work addresses the possibility to introduce a gate metal segment that overlaps the drain contact area. Fig. 1b-c shows two distinct cases of gate metal thickness (t_W) scaling. Device type *A* has a constant gate metal thickness, here taken as $t_W = 100$ nm, as shown in Fig. 1b. This approach gives constant gate resistance. Alternatively, device type *B* has a constant gate metal overlap on the drain sidewall, given as $t_W = L_G + 100$ nm, where L_G is MOSFET gate length, as depicted in Fig. 1c. Here, a balance between gate resistance and gate-drain capacitance is achieved. The unique Γ-shaped gate metal resembles that of a T-gate in modern high-frequency III-V HEMTs. Both device design approaches are investigated in further sections.

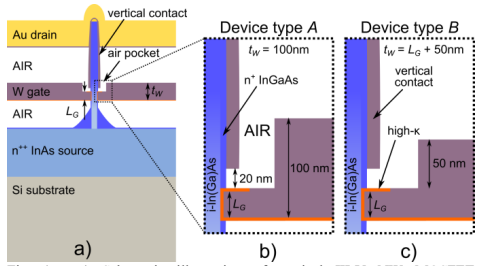

Fig. 1. a) Schematic illustration of vertical III-V NW MOSFET heterostructure, showing vertically stacked source, gate and drain contact metallization, with gate metal recess for capacitance minimization and air spacers. Detailed outlook of the gate-drain overlap area showing vertical drain contact metal, nanowire heterostructure and Γ-gate with: b) gate metal thickness fixed to $t_W = 100$ nm, corresponding to device type *A*, and c) gate metal constant overlap on the drain area, where gate metal thickness of $t_W = L_G + 50$ nm, corresponding to device type *B*.

A. Vertical III-V Nanowire MOSFET Large Signal Properties

To evaluate the device performance, a large signal model is developed and implemented in Keysight Advanced Design Systems (ADS). The device transport properties are captured using virtual source modelling with ballistic transport, assuming a finite transmission probability in quasi-ballistic devices [22,25-27]. Furthermore, the model is extended to capture the intrinsic capacitances of the channel, channel noise properties, as well as scalable external parasitic components, in order to establish a first-order approximation of the measured device data in a simulation environment [28].

Regarding vertical III-V NW MOSFET contact evaluation, a modulation-doped nanowire segment provides low access resistance. The total drain contact access resistance is evaluated to 150 Ω·µm, normalized to device width, including the 20 nm segment that separates drain contact metal from the gate metal. The source contact, on the other hand, inherently has low access resistance, approximately 70 Ω·µm, due to the presence of a nanowire foot with modulation doping in the source region. The resistance values are derived from the vertical contact evaluation, as shown elsewhere [29].

Fig. 2 shows vertical III-V NW MOSFET transfer characteristics for gate lengths of $L_G = 100$, 50, and 20 nm. Device dimensions also include a 25-nm-diameter channel core, with a 10-nm-thick modulation doped InGaAs contact, giving the contact resistance as described above. Note that even lower experimental contact resistances have been reported, opening for even further improvements in the device performance [4]. For $L_G = 20$ nm, the modelled vertical III-V NW MOSFET exhibits close to 65% transmission, which results in a peak $g_m \approx 3.1$ mS/µm at drain current density of $I_D \approx 0.76$ mA/µm, for the supply voltage of $V_{DS} = 0.5$V, which corresponds well to reported performance [4]. The gate length scaling is visible in current density, but especially in transconductance, attributed to the increased transmission probability, and modelled through an increased injection (virtual source) velocity.

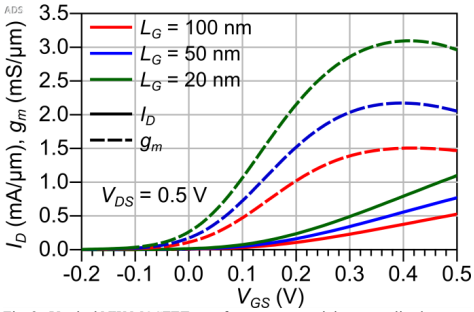

Fig. 2. Vertical NW MOSFET transfer curves, containing normalized current and transconductance, demonstrating gate-length scaling capabilities of the large signal model, as well as performance of vertical III-V GAA structures.

B. Vertical III-V Nanowire MOSFET mm-wave Design

The vertical III-V NW MOSFET layout decouples the contact area from the nanowire footprint, allowing for tall 3D-stacked contacts with thick planarization layers as spacers, as shown in Fig. 1a. Therefore, the external parasitic capacitances typically do not originate from laterally routed metal layers, but rather the overlap between the gate metal and the highly doped semiconductor shell. Additionally, proximity of the drain contact metal to the gate area introduces a large metal-insulator-metal (MIM) capacitance. As the geometry of these overlaps is complex, a 3D physics-based model is necessary to evaluate these external parasitic capacitances.

For this purpose, COMSOL Multiphysics is used to evaluate the external parasitic capacitance on the source side, as well as different contributions, which originate in different gate-drain metal overlaps. A full 3D structure is depicted in Fig. 3a, while the simplified 2D axisymmetric model is used to obtain capacitance data. As depicted in Fig. 1, the drain contact is separated from the gate area on the bottom by a fixed 20 nm, while the gate metal on the sidewall is forming a Γ-shape. In this study we use electrostatic simulation to obtain electric field distribution, and capacitance values are derived using built-in distributed capacitance models for metal-dielectric-semiconductor capacitors. The gate length is varied from 110 nm down to 10 nm.

Fig. 3b depicts extrinsic parasitic capacitance values, $C_{gx,p}$, normalized either to a single nanowire (aF/wire), or to the device gate width (fF/μm), for reference. The parasitic gate-source overlap capacitance, $C_{gs,p}$, is kept constant in this work, as device L_G scaling affects the drain overlap only. As depicted in Section II, the parasitic gate-drain overlap capacitances, $C_{gd,p}$, is evaluated for two distinct device architectures. For the type *A* device, $C_{gd,p}$ increases with decreasing L_G due to increasing overlap region in between gate metal and the sidewall drain contact metal. The increase is linear since added sections correspond to cylindrical MIM capacitance.

On the other hand, type *B* device gives lower $C_{gd,p}$ values at scaled gate lengths, but there may be an added penalty of

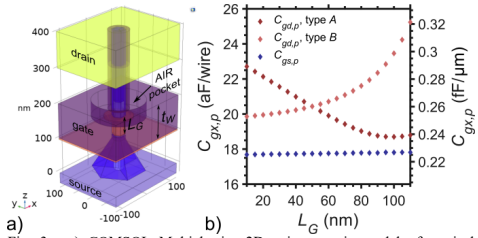

Fig. 3. a) COMSOL Multiphysics 2D axisymmetric model of vertical structure designed for C_{gs} and C_{gd} evaluation. b) Obtained parasitic capacitance values versus gate length: parasitic C_{gs} and two types of parasitic C_{gd}, depending on gate metal thickness – type *A* corresponds to a fixed gate metal height (t_W = 100 nm), whereas type *B* corresponds to a 50 nm gate metal overlap on the drain sidewall ($t_W = L_G + 50$ nm).

increased gate resistance, R_G, as mentioned earlier. A high R_G impedes device high-frequency performance, specifically maximum oscillation frequency (f_{max}). Additionally, long devices will have higher $C_{gd,p}$ due to proximity of gate metal to the lateral drain contact. Simulations show a total change in $C_{gd,p}$ of about 20% as L_G is scaled, for both device types. Finally, the device designs overlap for L_G = 50 nm, thus providing a reference point for the subsequent circuit design.

The extrinsic parasitic capacitance scaling is a unique characteristic of vertical nanowire GAA structure. In general, we have the total gate-drain capacitance as $C_{gd,t} = C_{gd,i} + C_{gd,p}$. Scaling of intrinsic gate-drain capacitance, $C_{gd,i}$, depends on L_G and bias conditions, whereas typically $C_{gd,p}$ is set by processing of device spacers on which device performance depends heavily. The vertical device architecture provides an additional degree of freedom in setting $C_{gd,p}$ while retaining device performance. This paves the way towards a L_G-independent $C_{gd,t}$, that can be used in many feedback circuits. Additionally, the influence of the process spread in L_G is reduced as well.

To address the R_G-C_{gd} balance in maximizing high-frequency gain, it is necessary to evaluate the complete device structure at specific gate lengths. The vertical III-V NW MOSFET used in this assessment contains 300 nanowires organized into 6 gate fingers. The 3D contact stacking of vertical III-V NW MOSFET enables arbitrary number of gate fingers, independent of the BEOL routing, allowing for additional degree of freedom in device selection. Each gate finger contains two rows of 25 equidistant nanowires, 200 nm apart, to ensure nanowire height and diameter uniformity. The total device gate width is $W_G \approx 23.5$ μm, while the total gate metal length is 30 μm (6 × 5μm), while gate metal width is 500 nm per finger [12]. Considering the finger spacing of 2μm, the device active area is only 5μm × 10.5 μm.

The high-frequency response of III-V NW mm-wave MOSFETs is depicted in Fig. 4a, for a bias voltage of V_{GS} = 0.3 V, and V_{DS} = 0.5 V, showing current gain (h_{21}) and maximum stable/available gain (*MSG*/*MAG*), for three representative gate lengths, L_G = 100 nm, 50 nm, and 20 nm. Devices are biased for obtaining maximum gain and minimum noise figure, while reducing total power consumption. Moreover, two different device types are shown, as per

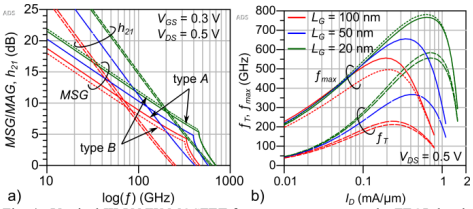

Fig. 4. Vertical III-V NW MOSFET frequency response on the FEOL level, for specific gate lengths (L_G = 100/50/20 nm), for both type *A* and type *B* device architectures. Device consists of 300 nanowires placed in 6 gate fingers ($W_G \approx 6\times3.9$ μm). a) Power gain (*MSG*/*MAG*, solid and dotted lines) and current gain (h_{21}, long- and short-dashed lines) for gate bias V_{GS} = 0.3 V, and drain bias V_{DS} = 0.5 V, and two device types. b) f_T and f_{max} versus drain current density for 0.5 V drain bias and specific gate lengths and device types.

COMSOL simulated data. From device high-frequency performance simulation, we see that even when the gate metal thickness reduces, the total R_G contribution to f_{max} degradation is not significant, as compared to a $C_{gd,p}$ contribution.

A more intuitive representation of the device cut-off frequencies is given in Fig 4b, where their dependence on I_D is shown. Even at L_G = 100 nm, type *A* devices exhibit f_T = 230 GHz and f_{max} = 550 GHz, whereas a slight drop in f_{max} to 500 GHz is observed for type *B* devices, suggesting that both approaches should be taken under consideration in circuit design. The reference design, with L_G = 50 nm, exhibits f_T = 370 GHz and f_{max} = 650 GHz. Ultimately, for L_G = 20 nm, a f_T/f_{max} up to 580/780 GHz is simulated, placing vertical III-V NW MOSFETs as a contender among the traditional high-frequency technologies, such as III-V HEMTs, yet they are integrated on a Si platform [30].

III. Co-Design Of C_{GD} Resonant Network and Vertical III-V NW MOSFET Unilateralization

Precise engineering of $C_{gd,p}$ in vertical III-V NW MOSFETs enables high-performance vertical mm-wave devices. Additionally, our approach is to mitigate the change in $C_{gd,p}$ when scaling L_G by scaling $C_{gd,i}$. This enables an L_G-independent total gate-drain capacitance. The concept is evaluated by creating a unique resonant circuit that will suppress the feedback effect of $C_{gd,t}$. This L_G-independent unilateral circuit is given in Fig. 5a. The feedback circuit consists of an inductive element (transmission line), and a bandwidth-setting feedback capacitor, C_F, that serves as a DC-block as well [31]. The transmission line and capacitor are implemented using in-house BEOL with characteristics comparable to state-of-the-art, developed and characterized for the purpose to be used with vertical nanowire MOSFETs [32,33].

The width of the matching window is determined by a resonant pole-setting capacitor C_F, which determines the Q-factor of the entire feedback resonant circuit, thus opening a frequency window where matching can be obtained. The resulting suppression of the total $C_{gd,t}$ for different NW MOSFET gate-lengths (100, 50, and 20 nm), is represented by the *Y*-parameters shown in Fig 5b. ADS simulations using the

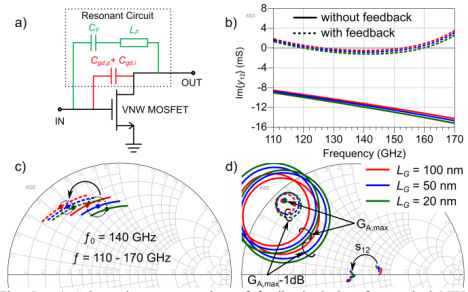

Fig. 5. a) Schematic representation of feedback design for vertical NW MOSFET; b) Feedback admittance imaginary part, before (solid) and after (dashed) feedback implementation, for different gate lengths. c) Optimum noise matching point, Γ_{opt} shift with feedback implementation. d) Available gain circles showing maximum available gain independent of MOSFET gate length at center frequency (f_0 = 140 GHz), as well as shift of feedback gain (isolation, s_{12}) to the center of the Smith Chart - a device resonant behavior.

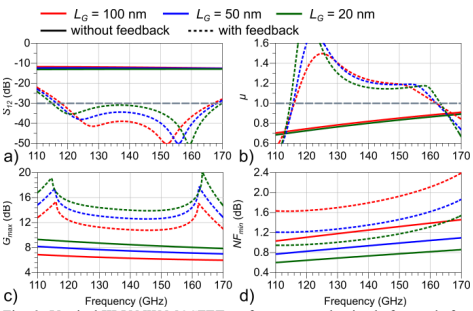

Fig. 6. Vertical III-V NW MOSFET performance evaluation before and after feedback implementation, for gate-length values of L_G = 100/50/20 nm, in D-band: a) feedback gain / device isolation (s_{12}), b) stability factor (*K*), c) maximum gain (*MAG*, G_{max}), and d) minimum noise figure (NF_{min}).

transistor models described in section II show that the total imaginary part of y_{12}, which represents the feedback capacitance, swings around zero in the D-band. The transmission line has the electrical length of approx. 3λ/8, where λ is the guided wavelength, while the resonant capacitor value has been set to C_F = 13 fF, to cover most of the D-band.

Fig. 5c-d shows the optimum noise reflection (Γ_{opt}) and maximum available gain ($G_{A,max}$) values in the D-band. The Γ_{opt} values shift towards $G_{A,max}$ with implementation of resonant feedback. The optimum noise match impedance this way becomes a maximum gain matching impedance as well. At the same time, Fig 5d shows that the $G_{A,max}$ matching point is very similar across all gate lengths, as well as that stability improves for the target frequency. As an additional measure, s_{12} (feedback gain / isolation) also shifts towards the lower magnitude in the frequency band of interest.

The effect of the resonant feedback influences not only the matching impedances, but the overall device behavior as well. Fig. 6a shows s_{12} in the D-band, which maintains a value less than -30 dB across the bandwidth of interest, for all gate lengths, and shows two resonant poles. Moreover, the available

bandwidth increases as L_G is reduced, due to a change in the MOSFET Q-factor. A similar behavior is reflected in the stability factor K, shown in Fig. 6b. Overall, K is well above 1, a measure of unconditional stability. Fig. 6c-d show the available gain and minimum noise figure for vertical III-V NW MOSFETs with and without the feedback structure, respectively. The above-MSG values suggest a unilateral device behavior, exhibiting gain values of 10, 13, and 14 dB for 100, 50, and 20 nm, at 140 GHz, respectively. Observed gain variability in 120-160 GHz band is less than 1dB. On the other hand, the minimum noise figure (NF_{MIN}) exhibits a slight increase due to the feedback resonant network insertion loss (~0.5 dB), with values of 1.79, 1.35, and 1.1 dB at 140 GHz.

IV. L_G-Independent LNA Design

The concept of device unilateralization has been used to design a low noise amplifier (LNA) in the D-band. The LNA has been designed using vertical III-V NW MOSFET with L_G = 50 nm, where both type A and type B devices exhibit equal performance. The device with the implemented feedback network is used for the LNA design. The circuit design has been performed by determining the optimum noise matching point, Γ_{opt}, and designing an optimum matching network for noise input matching. The matching network is generated based on the device Q-factor, which determines the available network bandwidth and a matching level, according to the Bode-Fano limit [34]. A low-pass ideal prototype LC network is generated and later transformed into a band-pass network, using the optimum design procedure that gives an ideal Chebyshev filter response [35].

In the subsequent steps, the Norton transform is used to absorb ideal transformers into the L- and C-network elements [36]. Finally, ideal elements are replaced with lossy microstrip transmission lines and finite-Q capacitors, as part of the BEOL. This approach has been implemented before and shows full utilization of the frequency band, as well as achieving gain flatness [37,38]. Additionally, the design filters the device resonant peaks appearing at 115 GHz, and at 165 GHz, as shown in Fig. 6c. The schematic illustration of the designed LNA is shown in Fig. 7a. Aside from two MOSFETs with feedback resonant network, input (IMN), interstage (ISN), and output matching networks (OMN) are used to realize a full 2-stage amplifier. Each matching network generates an insertion loss of $IL \approx$ 1-2 dB. The same network design is applied to other gate lengths, and both device types.

Fig. 7b-d shows the summary of the LNA performance for two vertical NW MOSFET types, for L_G = 100/50/20 nm, as depicted above. Fig. 7b-c show LNA performance in the case of L_G scaling of the device type A and type B, respectively. The resonant pole in LNA input/output reflection (s_{11}, s_{22}) for two distinct device types reveal the intrinsic and extrinsic capacitance change as the gate length changes. Type A devices exhibit an increase in $C_{gd,p}$, while simultaneously decreasing $C_{gd,i}$, thus keeping $C_{gd,t}$ nearly constant. This is evident in Fig 7b, where resonant poles do not shift in frequency as device gate length is changed. On the other hand, Fig. 7c shows a clear shift of the resonant poles in the input/output reflection, since

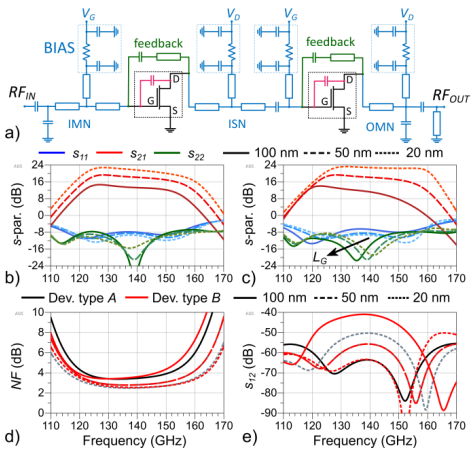

Fig. 7. a) Schematic illustration of vertical III-V NW MOSFET-based LNA, showing input, interstage, and output matching network, combined with feedback structure as well as MOSFET with gate-drain capacitance. Performance evaluation, for gate length values of L_G = 100/50/20 nm, in D-band: S-parameters for b) device type A, and c) device type B. d) Noise figure and e) circuit isolation (s_{12}) comparison for device type A and B, respectively.

both $C_{gd,p}$ and $C_{gd,i}$ decrease simultaneously as L_G is scaled.

In both cases, the LNAs exhibit a peak gain of 14, 19 and 23 dB at 128 GHz, for gate lengths of 100, 50, and 20 nm, respectively. The bandwidth remains constant at 30 GHz, for the type A devices, while for type B devices, it scales from 23 to 36 GHz. The reflection parameters (s_{11}, s_{22}) reach values below -10 dB, suggesting sufficient matching is present on the LNA input and output. The concept of replacing a reduction in intrinsic gate-drain capacitance with the overlap parasitic gate-drain capacitance can be translated from the device level all the way to the circuit level. Consequently, device and circuit designs are less sensitive to the exact height and position of the gate metal, thus reducing the processing constraints. This robust design is beneficial in a challenging process, such as vertical III-V NW mm-wave MOSFETs.

Regarding the LNA noise performance, Fig. 7d depicts noise figure for both device types and for all three gate lengths. There is a slight shift in noise performance for 100 nm devices, but minimum noise figure values remain the same for both device types. The noise figure values achieved with this design are 3.4, 2.8, and 2.5 dB for L_G = 100, 50, and 20 nm, respectively. A very low noise figure value is attributed to the very low device noise, due to III-V channel's low density of states and high cutoff frequencies [39]. Furthermore, the obtained values of the noise figure suggest that the MOSFET noise performance is less susceptible to changes in $C_{gd,t}$, as seen in Fig. 5c. Finally, Fig. 7e shows circuit isolation (s_{12}) values, which are generally well below -40 dB, suggesting suppression of unwanted feedback that causes circuit instability, as a result of the device feedback implementation.

TABLE I
140 GHz LNA Performance Comparison

Technology	This work, 20 nm V-NW	22nm FDSOI CMOS [15]	90nm SiGe HBT [16]	50nm InGaAs HEMT [14]	40nm GaN HEMT [19]
f_T [GHz]	360[1]	240[1]	300	380	>200
f_{max} [GHz]	720[1]	230[1]	350	670	>400
I_D [mA/μm]	0.5	0.3	0.85[2]	0.3	0.26
Topology	2×CS	4×CC[3]	3×CC	3×CC	6×CS
G_T [dB]	23	16	30	30.8	>25
G_T/stage [dB]	11.5	4	10	10.3	4-5
BW [GHz]	30	40	28	67	>60
NF [dB]	2.5	8.5	6.2	3	6
P_{DC} [mW]	11.4	44	45	57.6	225

[1]Circuit-level performance
[2]mA/μm^2
[3]Differential design

V. Discussion

A summary of key parameters of this work, as well as benchmarking with state-of-the-art reported in literature, for D-band (140 GHz) LNA operation, is given in Table I. The included technologies are 22 nm FDSOI CMOS process, 90 nm SiGe heterojunction bipolar transistor (HBT), 50 nm InGaAs HEMT, and finally 40 nm GaN HEMT, representing a variety of state-of-the-art technologies. The technologies vary in cut-off frequencies, where InGaAs HEMTs provide an extended frequency operation range, next to which vertical III-V NW MOSFETs would be similar in performance. A crucial benefit for MOSFETs, as compared to HEMTs, is the lower leakage current level, allowing for superior gate control at reduced gate lengths, enabling further channel scaling. Scaling is reflected in current density as well, with vertical III-V NW MSOFETs exhibiting 0.5 mA/μm at 20 nm, while 50 nm InGaAs HEMTs and 22nm FDSOI CMOS have comparable current density to 50 nm NW MOSFETs. SiGe HBTs, however, exhibit much larger current densities inherent to the device design.

Regarding the LNA performance, gain values vary significantly, from 4-5 dB/stage, in case of FDSOI and GaN HEMTs, up to 11 dB/stage, for HBTs, InGaAs HEMTS and NW MOSFETs. Besides, the LNA noise properties are superior in case of InGaAs-based devices, while for other technologies, a typical 6 dB is reported. The bandwidth is very design-dependent and is either adapted for broadband design (HEMTs) or solely dependent on device Q-factor (FDSOI, SiGe HBT). In case of our new III-V NW MOSFET design, the resulting bandwidth is a direct consequence of the feedback network implementation, which limits available bandwidth, and would require different feedback design for each stage. Finally, DC power consumption is the lowest for III-V NW MOSFETs, due to reduced operating voltage (V_D = 0.5V), while a typical state-of-the-art LNA would consume up to 5× more power.

Given the performance metrics stated in Table I, the performance of III-V NW MOSFETs shows comparable performance to other state-of-the-art technologies. This interoperability makes III-V NW MSOEFTs a platform for integration of key functionality aspects needed for low-power, high performance IoT circuits and systems, as part of 5G/6G mobile communication system. The performance of the designed LNA demonstrates the possibilities of such low-power, high-performance design.

VI. Conclusion

This work presents a device-to-circuit co-design strategy for vertical III-V NW MOSFETs on a Si substrate, summarizing device performance and designing an LNA as a technology benchmark. Simulated vertical III-V NW MOSFETs down to 20 nm gate length exhibit normalized g_m up to 3.1 mS/μm in agreement with experimental data, and a cut-off frequencies up to 780 GHz. The transistor layout utilizes 3D stacking of gate and drain fingers, and air pockets to minimize parasitic capacitances. An overlap between gate and drain area is considered crucial in maintaining high f_T/f_{max}. Furthermore, the concept of parasitic capacitance scaling is utilized in designing a resonant feedback structure that neutralizes the total device C_{gd}. The device performance is accessed with a 2-stage LNA, providing 23 dB gain and 2.5 dB noise figure. The LNA performance is benchmarked with state-of-the-art technologies, revealing that low-power, high-frequency circuit design in III-V NW MOSFET technology would allow for potential use in high-performance, low-power IoT systems that rely on 5G/6G mobile communication standards. These simulations show a prospect for implementation of vertical III-V NW MOSFETs in a physical circuit environment.

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Paper VI

Paper VI

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Millimeter-Wave Characterization of Ferroelectric MOS Capacitors

Anton E. O. Persson, Stefan Andrić, and Lars-Erik Wernersson

***Abstract*—In this paper, we present frequency-dependent capacitance characterization of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films, spanning over six orders of magnitude. Using a bi-directional capacitance-voltage measurement on the scaled ferroelectric metal-oxide-semiconductor capacitors, for the first time the ferroelectricity is captured at high-frequencies, demonstrating ferroelectric behavior up to 10 GHz. The obtained frequency span allows for an accurate prediction of the capacitance frequency dispersion, with extrapolated values up to 100 GHz. The proposed dispersion function demonstrates steady-state dielectric behavior of the HZO film, operating in the mm-wave frequency range. Changing the measurement to a preset-pulsing scheme, a reconfigurable capacitor is obtained with up to 25% tunability, demonstrating the ferroelectric film application in non-volatile reconfigurable electronics.**

***Index Terms*— Ferroelectric, Hafnium, Zirconium, HZO, RF, mm-wave, on-chip calibration, III-V, InAs.**

I. Introduction

Ferroelectric HfO_2 has attracted considerable attention for memory, neuromorphic, and steep-slope transistor applications [1],[2]. So far, the millimeter wave (30-300 GHz) characteristics of HfO_2-based ferroelectrics have not been extensively treated although it, for decades, has been an active field of research for ferroelectric perovskites [3]. An appealing feature of ferroelectric materials is the field dependent permittivity that have enabled their usage in varactors, i.e., capacitors whose capacitance is voltage-controlled. A varactor is an important microwave component widely used in amplifiers, filters, phase shifters, and voltage-controlled oscillators [3].

Generally, varactor applications of ferroelectric films assume that they are based on perovskite materials in the paraelectric phase i.e., quantum paraelectric or above the Curie temperature [3]. The Curie temperature of the polar ferroelectric HfO_2 is expected to be >250°C [4][5]. Therefore, the proposed varactor applications have mainly focused on using the capacitance tunability of the ferroelectric response in the sub-coercive voltage region, where domain switching can be neglected [4][6]. This allows for a capacitance tunability of a couple of tens of percent that with simulated filters have shown promising results. However, there is a need to characterize the varactors at mm-wave frequencies to validate the approach.

The ferroelectric films also allow for an increased tuning range, as well as compatibility with the conventional process flows. The usage of a reconfigurable capacitance has previously been suggested for overcoming mismatch problems in digital-to-analog and analog-to-digital converters, non-volatile memories, and programmable filters [7][8]. From the obtained results, those varactor-type capacitors are expected to be implementable, to operate at mm-wave frequencies, as compared to the low frequency ferroelectric capacitors for memory applications. More importantly, the reconfigurable capacitor is tuned at very low bias voltages which would enable their use in power efficient circuits.

Here, a ferroelectric hafnium-zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, or HZO) MOS capacitor (MOSCAP) with a signal routing that extends the device characterization into the radio-frequency (RF) and millimeter-wave (mm-wave) frequency range. A complementary on-chip calibration is fabricated alongside the MOSCAPs. We show that the capacitance modulation originating from the ferroelectric HZO films is retained at mm-wave frequencies. By using the semiconductor capacitance modulation induced by the polarization state, we further show that the MOSCAP's capacitance can be continuously reconfigured over the entirety of the explored frequency range. The method provides the first experimental verification of HfO_2-based ferroelectric films at high frequencies.

II. Device Fabrication

The fabrication of the structure is illustrated in Fig. 1. It includes co-integration of the MOSCAP device with the signal routing for an on-wafer RF/mm-wave calibration and measurements. The methods described below are expected to be entirely transferrable to metal-insulator-metal (MIM) capacitors by exchanging the semiconductor InAs mesa with a metal bottom film etched to similar lateral dimensions.

The MOSCAP fabrication starts by growing a 250-nm-thick Sn-doped InAs layer ($\sim 5\times10^{19}$ cm^{-3}) capped with a 50-nm-thick unintentionally doped InAs layer ($\sim 3\times10^{18}$ cm^{-3}), on a high-resistivity (>15000 Ω·cm) Si substrate using Metalorganic Vapor Phase Epitaxy (MOVPE) [9]. The device

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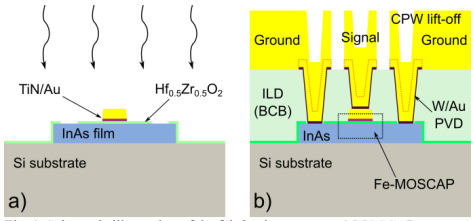

Fig. 1. Schematic illustration of the fabrication process: a) MOSCAP structure for RTP annealing, consisting of a ferroelectric HZO film, sandwiched between an isolated InAs mesa and a TiN/Au metal, and b) complete structure, including the BCB planarization layer, interconnect vias, and CPW lines.

is isolated by wet etching of mesas defined by soft UV lithography. The InAs native oxide was removed using $HCl:H_2O$ (1:10) mixture, followed by the immediate atomic layer deposition (ALD) of thin HZO layer. Three different thicknesses (6 nm, 10 nm, and 15 nm) were deposited at 200 °C in a thermal reactor with a 1:1 alternation between Tetrakis(dimethylamido)hafnium (TDMAHf) and Tetrakis(ethylmethylamido)zirconium (TEMAZr) precursors. In two subsequent sputtering steps, a 30-nm TiN thin-film-resistor (TFR), and 10nm/100nm TiN/Au MOSCAP contact layer are formed. The capacitor area is 30 μm^2. Vias through the HZO to the InAs were defined by UV lithography and etched using buffered-oxide etch (1:10), after which the samples were annealed at 600°C in a rapid thermal process (RTP) for 30s. The illustration of such a structure is shown in Fig. 1a.

Following the formation of the ferroelectric film, the sample is planarized by spinning, and subsequently curing Cyclotene 3022-35 electronic resin into a ~1 µm benzocyclobutene (BCB) polymer film. The BCB is a low permittivity dielectric ($\varepsilon_r \approx 2.8$) used for high-frequency integrated circuits, which is here also used as a passivation layer [10][12]. Aside from planarization, the BCB layer improves isolation of the RF/mm-wave propagation from the lossy Si substrate. The BCB layer was thinned to 550 nm using Reactive Ion Etching (RIE) and interconnect vias were defined by UV lithography and dry etched in SF_6-based plasma by RIE [13][14]. Metal contacts to the MOSACPs are defined by UV lithography and etching of a sputtered 20 nm/150 nm W/Au layer using a KI-based Au wet etch and a RIE W dry-etch. The vias were sputtered to ensure good connection between layers. Finally, coplanar waveguides (CPW) were deposited by a UV lithography defined e-beam evaporation and lift-off of 5 nm/500 nm Ti/Au layer.

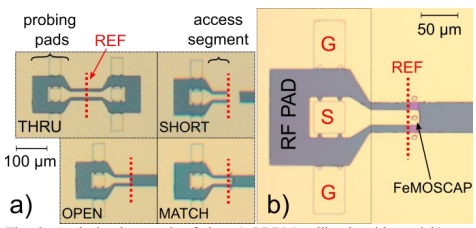

Fig. 2. Optical micrograph of the: a) LRRM calibration kit, and b) test measurement structure for evaluation of the MOSCAP. Dashed lines show the calibrated reference planes.

The CPW lines are utilized for the realization of the Line-Reflect-Reflect-Match (LRRM) calibration kit. Optical micrographs of the realized calibration kit structures are shown in Fig. 2a. While the THRU, OPEN, and SHORT standards are limited to the CPW metal layer, the 50-Ω MATCH standard is realized with the patterned TFR on substrate, accessed through interconnect vias, in a similar manner as the ferroelectric MOSCAPs. The on-chip standards are probed through probe landing pads, suitable for ground-signal-ground (GSG) probes. To minimize the interference of the evanescent modes, that are launched from the RF probe, a 50-µm-long CPW line access segment is included as well [15]. Therefore, the reference plane is shifted inwards, illustrated with a dashed line in Fig. 2b. The MOSCAP structure is placed on the other end of the reference plane and is much smaller than the RF signal wavelength λ, minimizing the distributed effects. Furthermore, the InAs mesa island is routed to both ends of the ground plane, which reduces the parasitic resistance of the layer by a factor of two.

III. Device Characterization

The electrical characterization was performed on a MPI TS2000-SE wafer probing system. Using a Keysight B1500A Parameter Analyzer with a B1530A waveform generator module, a conventional positive-up-negative-down (PUND) measurements were performed. The measurement result in shown in Fig. 3a), indicating clear ferroelectric hysteresis loops with polarization values ranging 18-22 $\mu C/cm^2$ for all thicknesses in line with previous InAs/HZO integrations [16][17]. Prior to the PUND measurements, the devices were pulsed 1000 times using a square wave with an amplitude corresponding to the highest voltage of each PUND measurement, to wake up the ferroelectric film

For the RF characterization, MPI TITAN 100µm pitch GSG high frequency probes and a Rohde&Schwarz ZVA67 vector network analyzer (VNA) are used, supporting the 10 MHz-67 GHz frequency range. The capacitors are biased through the internal bias tee of the VNA, using a Keithley 2912A source-measure unit (SMU). The system is calibrated with the on-chip LRRM kit in the specific order: thru, open, short, and match. The error terms are obtained using the Cascade WinCal 4.6, where a custom LRRM description is implemented [18][20]. The terms are then applied on the VNA, which removes the effect of the probing pad and access line segment, leaving only the RF-compatible MOSCAP contribution, see Fig 2b.

The MOSCAP characterization frequency range is extended using an Agilent 4294A Impedance Analyzer, which has a measurement range from 40 Hz to 110 MHz. The measurement is performed on a Lake Shore CRX 4K cryogenic probe station using ZN50R high-frequency probes. The impedance analyzer internal biasing system is used as a voltage supply to the MOSCAPs. The measurement of the OPEN calibration standard is performed prior to the measurement of the HZO MOSCAP device. The excess capacitance, originating from the probing pad and the CPW line access segment, is obtained, and removed from the final capacitance value. The capacitance-voltage (CV) curves, shown in Fig. 3b-d, are measured by

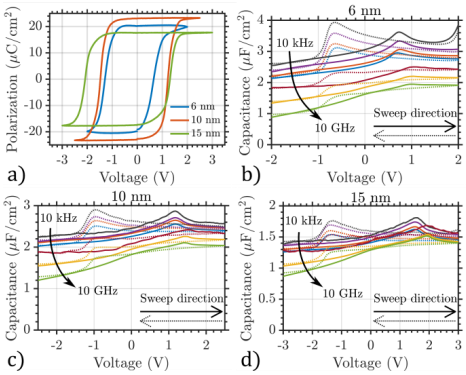

Fig. 3. (a) PUND measurements of the films with 6, 10, and 15 nm thickness, respectively. (b-d) Capacitance characterization of the different thicknesses of the HZO film: b) 6 nm, c) 10 nm, and d) 15 nm. The CV curves are captured using the impedance analyzed for the 10 kHz-10 MHz range, while VNA is used in the 100 MHz-10 GHz range. For the 6-nm film, measurements below 100 MHz are performed on a large MOSCAP instead of the RF MOSCAP.

supplying the bias voltage, while sweeping the frequency of the continuous-wave (CW) RF signal. From measured scattering parameters (*s*-parameters), or input impedance, the capacitance values at a specific bias voltage are obtained, such as in more conventional CV profiling methods.

By using the bidirectional CV method, i.e., stepping the bias voltage beyond the positive and negative coercive field, the measurements in Fig. 3b-d provide results comparable to previous studies on ferroelectric HZO/InAs MOSCAPs [21]. Here, however, the characterization is extended into the mm-wave frequency range. However, using the VNA at frequencies above 20 GHz, the error in obtained capacitance values becomes very large, as the large capacitive values result in very small imaginary part of the input impedance, Im(Z_{in}), making the accurate capacitance derivation challenging. Similarly, the capacitance values become unreliable below 100 MHz, due to high noise levels. This makes the quantitative VNA frequency range 100 MHz-20 GHz. The measurements using impedance analyzer have similar issues, making values above 10 MHz unreliable due to the lack of the accurate calibration, and measurements below 10 kHz noisy due to the small device capacitance. As shown in Fig. 3b-d), there is a slight mismatch in capacitance values due to different measurement systems and the use of a very large MOSCAP, in case of the 6-nm HZO film (7850 μm^2). The overall CV shapes show that the ferroelectric behavior up to 10 GHz.

The measurement error for mm wave VNA measurements is illustrated in Fig. 4a. Due to very high characterization frequency, the smallest fabricated capacitors have a very large capacitance. Therefore, an attempt to predict the capacitance dispersive behavior further into the mm-wave regime is made. The capacitance-frequency dispersion relation used here, is based on the characteristics for high-k/III-V interfaces by [22]:

$$C_{tot} = C_{DC} - C_{\omega} \cdot \ln\left(\omega/\omega_0\right) \quad (1)$$

where C_{DC} is a low-frequency (ultimately DC) capacitance, C_{ω} is a frequency-dependent term that models the frequency dispersion – linear capacitance reduction for each frequency decade, $\omega = 2\pi f$ is the angular frequency, while ω_0 is the normalized angular frequency, here set as $\omega_0 = 2\pi \cdot 100\ GHz$ [23]. As seen in Fig. 4a, the fitting successfully predicts the dispersive behavior of the capacitance at both the lowest biasing voltage and at the positive voltage peak biasing voltage up until ~10 GHz. As is indicated in Fig. 4b-d, the fitting captures the characteristics at all measured voltage levels and investigated film thicknesses. The dispersive behavior increases for thinner ferroelectric films which is expected, since the defect-rich high-κ/InAs interface constitutes a larger fraction of the film. Importantly, the fit predicts the coercive voltages accurately, which is interpreted as if domain switching has a negligible contribution to the measured small-signal dynamic properties. This is expected, as domain switching is mainly a transient behavior whereas RF measurements are made in a steady-state, with a small-signal CW excitation, i.e., all transient switching is expected to have already occurred. As a result, the ferroelectric exhibits a behavior similar to a dielectric film for all biasing points, while the domain switching occurs in between each measurement point.

In Fig. 4b-d, the prominence of the positive voltage peak is nearly frequency independent, whereas the negative voltage peak continuously shrinks with increasing frequency. This behavior is explained by the response time of the minority carriers of the narrow bandgap semiconductor. At positive voltages, when semiconductor is in accumulation, the quickly-generated majority carriers dominate the signal response, together with the capacitance of the ferroelectric film. At negative voltage, traps and minority carriers dominate the capacitance response, showing stronger frequency dispersion, than at the positive voltage. This implies that the ferroelectric film is unaffected by the increasing frequency of operation and that the ferroelectric MIM capacitor would show a symmetric

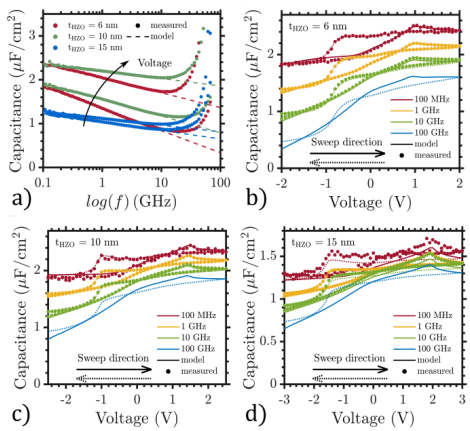

Fig. 4. (a) Model fit of the capacitance frequency dispersion at specific bias points. b-d) CV curve for varying thickness of the ferroelectric film: b) 6 nm, c) 10 nm, and d) 15 nm. The capacitance fit predicts HZO film mm-wave performance, extending the range up to 100 GHz.

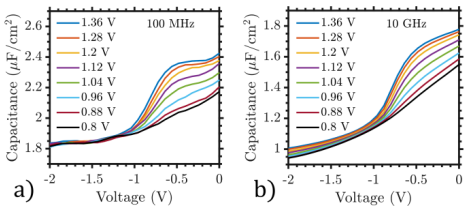

Fig. 5. The 6-nm-thick HZO MOSCAP capacitance at: a) 100 MHz, and b) 10 GHz, depending on how its polarization state has been reconfigured by a previous positive sweep. A 0 to -2V sweeps indicate the increasing capacitance at sub-coercive voltages for increasing peak preset-voltage.

response in which both peaks are equally affected by the frequency dispersion. The capacitance dispersion fit at high frequencies confirms such response, as shown in Fig. 4.

Fig. 5 demonstrates the preset-pulsing scheme, in which a single positive bias measurement is followed by a sweep in the negative direction. The positive bias point is then increased, followed by a negative sweep with an increased capacitance at the sub-coercive voltage. Such hysteresis is used to effectively create a reconfigurable capacitor in which the small-signal capacitance is tuned up to 25%, as modulated by the previous positive voltage state. For a wider bandgap semiconductor, the capacitance modulation increases, as the lowest capacitance value is restricted by the fast generation rate of minority carriers in the narrow bandgap InAs. Lastly, using a p-type semiconductor, the reconfigurable capacitance would be observed at the positive voltage bias.

IV. Conclusion

The ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ MOSCAP devices have been fabricated in an RF-compatible process flow and characterized in a frequency range from 10 kHz to 10 GHz, with the capacitance dispersion relation extending the observable range to 100 GHz. The wide frequency range and the capacitance dispersion reveals the HZO film's dielectric behavior in between domain-switching events. Furthermore, the structures demonstrate reconfigurable capacitance properties, in a preset-pulsing scheme, extending into the mm-wave frequencies. The proposed technology demonstrates potential application in ferroelectric MOS transistors, as well as reconfigurable electronics, such as varactors.

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